PERFECT WIRELESS EXPERIENCE

SC218

Hardware Guide

V1.1

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Safety Instructions

Do not operate wireless communication products in areas where the use of radio is not recommended without proper equipment certification. These areas include environments that may generate radio interference, such as flammable and explosive environments, medical devices, aircraft or any other equipment that may be subject to any form of radio interference.

The driver or operator of any vehicle shall not operate wireless communication products while controlling the vehicle. Doing so will reduce the driver's or operator's control and operation of the vehicle, resulting in safety risks.

Wireless communication devices do not guarantee effective connection under any circumstances, such as when the (U) SIM card is invalid or the device is in arrears. In an emergency, please use the emergency call function when the device is turned on, and ensure that the device is located in an area with sufficient signal strength.

Contents

Applicable Model

No.	Applicable Model	Description
1	SC218-EAU-20	4GB+64GB, applicable in Europe
2	SC218-JP-20	4GB+64GB, applicable in Japan
3	SC218-NA-20	4GB+64GB, applicable in North America
4	SC218-EAU-60	8GB+128GB, applicable in Europe
5	SC218-JP-60	8GB+128GB, applicable in Japan
6	SC218-NA-60	8GB+128GB, applicable in North America

Change History

V1.1 (2023-09-07)	Modify document format
	Add SD_DET description
	Modify RF performance
	Add SC218-EAU/NA/JP project
V1.0 (2023-05-11)	Initial version

1 Foreword

1.1 Description

This document describes the electrical characteristics, RF performance, structure size, application environment, etc. of SC218 series module (hereinafter referred to as module). With the assistance of the document and other instructions, the developers can quickly understand the hardware functions of the module and develop products.

1.2 Reference Standards

This product is designed with reference to the following standards:

- 3GPP TS 51.010-1 V10.5.0: Mobile Station (MS) conformance specification; Part 1: Conformance specification
- 3GPP TS 34.121-1 V10.8.0: User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 1: Conformance specification
- 3GPP TS 21.111 V10.0.0: USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit (USAT)
- 3GPP TS 36.124V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPPTS27.005 V10.0.1: Use of Data Terminal Equipment - Data Circuit terminating

Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)

- IEEE 802.11n WLAN MAC and PHY, October 2009 + IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- IEEE Std 802.11b, IEEE Std 802.11a, IEEE Std 802.11g, IEEE Std 802.11n, IEEE Std 802.11ac
- IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1+ EDR/3.0/3.0 +HS, August 6, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.2.0, November 7, 2014
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/5.0.2, December 07,2017

2 Product Overview

2.1 General Description

The module integrates core components such as Baseband, MCP, PMU, Transceiver, PA; it supports long distance multi-mode communication such as FDD/TDD-LTE, WCDMA, GSM and WIFI/BT short-distance radio transmission technology, as well as GNSS wireless positioning technology. The module is embedded with Android operating system and supports various interfaces such as MIPI/USB/UART/SPI/I2C. It is the optimal solution for the core system of wireless smart products. Its corresponding network modes and frequency bands are as follows:

Table 1.SC218-NA supported bands

Mode	Band
FDD-LTE	Band 2/4/5/7/12/13/17/25/26/66/71
TDD-LTE	Band 41(2496-2690MHz)
WIFI802.11a/b/g/n/ac	2402-2482MHz;5170-5835MHz
BT5.0	2402-2480MHz
GNSS	GPS/GLONASS/BeiDou

Table 2.SC218-EAU supported bands

Mode	Band
GSM	GSM850/EGSM900/DCS1800/PCS1900
WCDMA	Band 1/2/5/8
FDD-LTE	Band 1/2/3/4/5/7/8/20/28

Mode	Band
TDD-LTE	Band 38/40/41 (2535-2655MHz)
WIFI802.11a/b/g/n/ac	2402-2482MHz; 5170-5835MHz
BT5.0	2402-2480MHz
GNSS	GPS/GLONASS/BeiDou

Table 3.SC218-JP supported bands

Mode	Band
WCDMA	Band 1/6/8/9/19
FDD-LTE	Band 1/3/8/18/19/26/28
TDD-LTE	Band 41(2535-2655MHz)
WIFI802.11a/b/g/n/ac	2402-2482MHz;5170-5835MHz
BT5.0	2402-2480MHz
GNSS	GPS/GLONASS/BeiDou

2.2 Main Performance

The module is available in LCC + LGA package with 281 pins, including 148 LCC pins and 133 LGA pins. The dimension is 41 (±0.15) mm × 41 (±0.15) mm × 2.85 (max) mm. It can be embedded in various M2M applications. It is suitable for the development of smart devices such as smart POS, cash registers, robots, UAVs, smart homes, security monitoring, multimedia terminals, ECR, and face payment terminals. The following table describes the detailed performance.

Table 4. Performance specifications

Performance	Description
Power Supply	DC: 3.5-4.35 V, typical voltage: 3.8 V

Performance	Description
Application processor	Customized 64-bit ARM v8-compliant applications processor (Qualcomm®Kryo™ 260 CPU) KryoGold: quad high-performance cores targeting 2.2GHz, L2: 1MB KryoSilver: quad low-power cores targeting 1.843GHz, L2: 1MB
Memory	4 GB + 64GB [1] SC218-EAU/JP/NA-20 8 GB + 128GB SC218-EAU/JP/NA-60
Power class	Class 4 (33 dBm ± 2 dB) for GSM850/EGSM900 Class 1 (30 dBm ± 2 dB) for DCS1800/PCS1900 Class E2 (27 dBm ± 3 dB) for GSM850/EGSM900 8-PSK Class E2 (26 dBm ± 3 dB) for DCS1800/PCS1900 8-PSK Class 3 (24 dBm + 1/-3 dB) for WCDMA bands Class 3 (23 dBm ± 2 dB) for LTE FDD bands Class 3 (23 dBm ± 2 dB) for LTE TDD bands
GSM/GPRS/EDGE features	R99: CSD transmission rate: 9.6 kbps, 14.4 kbps GPRS: Support GPRS multi-slot class 33 Coding formats: CS-1/CS-2/CS-3 and CS-4 Up to 5 Rx time slots per frame EDGE: Support EDGE multi-slot class 33 Support GMSK and 8-PSK Uplink encoding format: CS 1-4 and MCS 1-9

Performance	Description
	Downlink encoding format: CS 1-4 and MCS 1-9
WCDMA features	Support 3GPP R8 DC-HSPA+ Support 16-QAM, 64-QAM and QPSK modulation CAT6 HSUPA: maximum uplink rate 5.76 Mbps CAT24 HSDPA: maximum downlink rate 42 Mbps
LTE features	Support FDD/TDD R10 Support FDD/TDD CAT4 Support 1.4-20 M RF bandwidth Downlink support 2 × 2 MIMO Maximum uplink rate 50 Mbps, maximum downlink rate 150 Mbps
WLAN features	Support 2.4 G and 5 G WLAN wireless communication, support 802.11a, 802.11b, 802.11g, 802.11n and 802.11ac, the maximum rate is up to 433 Mbps
Bluetooth features	BT5.0 (BR/EDR + BLE)
Satellite positioning	GPS/GLONASS/BeiDou
LCD Interface	One 4-Lane MIPI_DSI interface Support for 1080P maximum
Camera interface	Two 4-Lane MIPI_CSI interfaces, which can be configured as 4+4 Lanes or 4+2+1 Lanes Dual ISP (16 +16 MP, or 24MP)
Audio interface	Input: 3 analog MIC inputs, Internal MIC_BIAS pull-up Output: one stereo headset output One differential receiver output

Performance	Description
	One differential speaker driver
USB interface	Two USB interface One USB 3.1 interface that is downward compatible with USB 2.0; USB 3.1 interface supports SS (5 Gbps) mode but does not support software download. USB 2.0 supports HS (480 Mbps) mode and software download, and is downward compatible with FS and LS interface, and supports HUB extensible USB OTG, supports DP over Type C One USB2.0 interface only support host mode
UIM interface	Two UIM card interfaces, support 1.8/2.95V UIM card adaptive Support dual-SIM dual-standby and hot plugging
UART interface	Three UART interfaces, up to 4 MHz; One 4-line UART interface, supports hardware flow control One 2-line UART interface One 2-line debug UART interface
SDIO Interface	One 4-bit SDIO interface; SD card supports hot plugging
I2C interface	Multiple I2C interfaces for TP, camera, sensor, etc.
ADC Interfaces	One ADC
RTC	Support
Antenna Interface	TRX antenna, DRX antenna, GNSS antenna, WIFI/BT antenna
Physical characteristics	Dimensions: 41 (±0.15) mm × 41 (±0.15) mm × 2.85 (max) mm Packaging: 148 LCC pins +133LGA pins Weight: about 9.6g
Temperature range	Operating temperature[2]: -30°C to 75°C

Performance	Description
	Storage temperature: -40°C to -85°C
Software update	USB/OTA/SD
RoHS	RoHS compliant

1. The memory can be adjusted and adapted according to different needs.
2. When the module is operating within this temperature range, the functions of it are normal and the relevant performance meets the 3GPP standard.

2.3 Function Block Diagram

Function block diagram shows the main hardware features of the module, including:

- Baseband
- Wireless transceiver
- Power Management
- Memory
- Peripheral interface
  - Communication expansion interface (USB/UART/I2C/SD)
  - UIM card interface
  - MIPI_DSI interface
  - MIPI_CSI interface
  - Analog audio interface

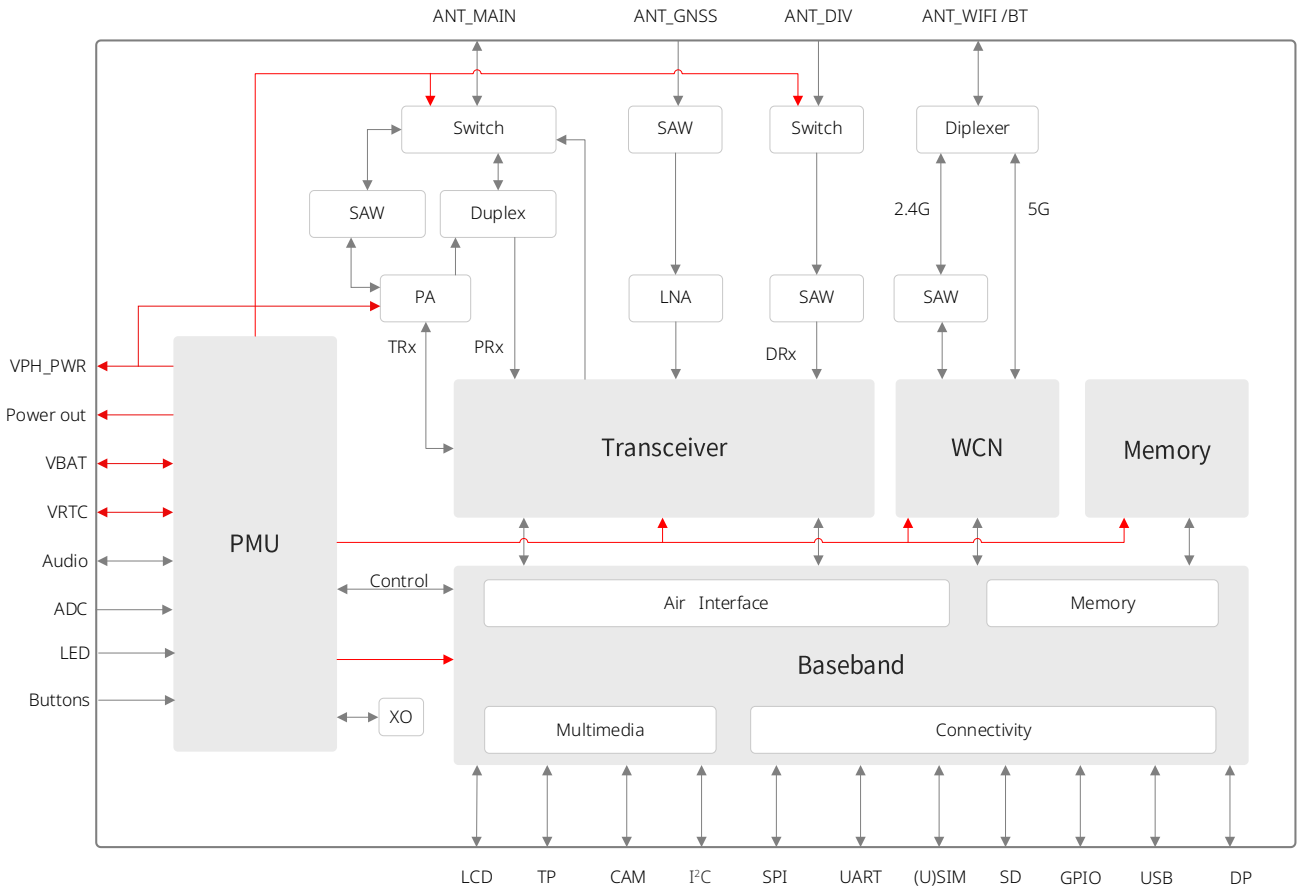

Figure 1. Functional block diagram

2.4 Pin Definition

2.4.1 Pin Assignment

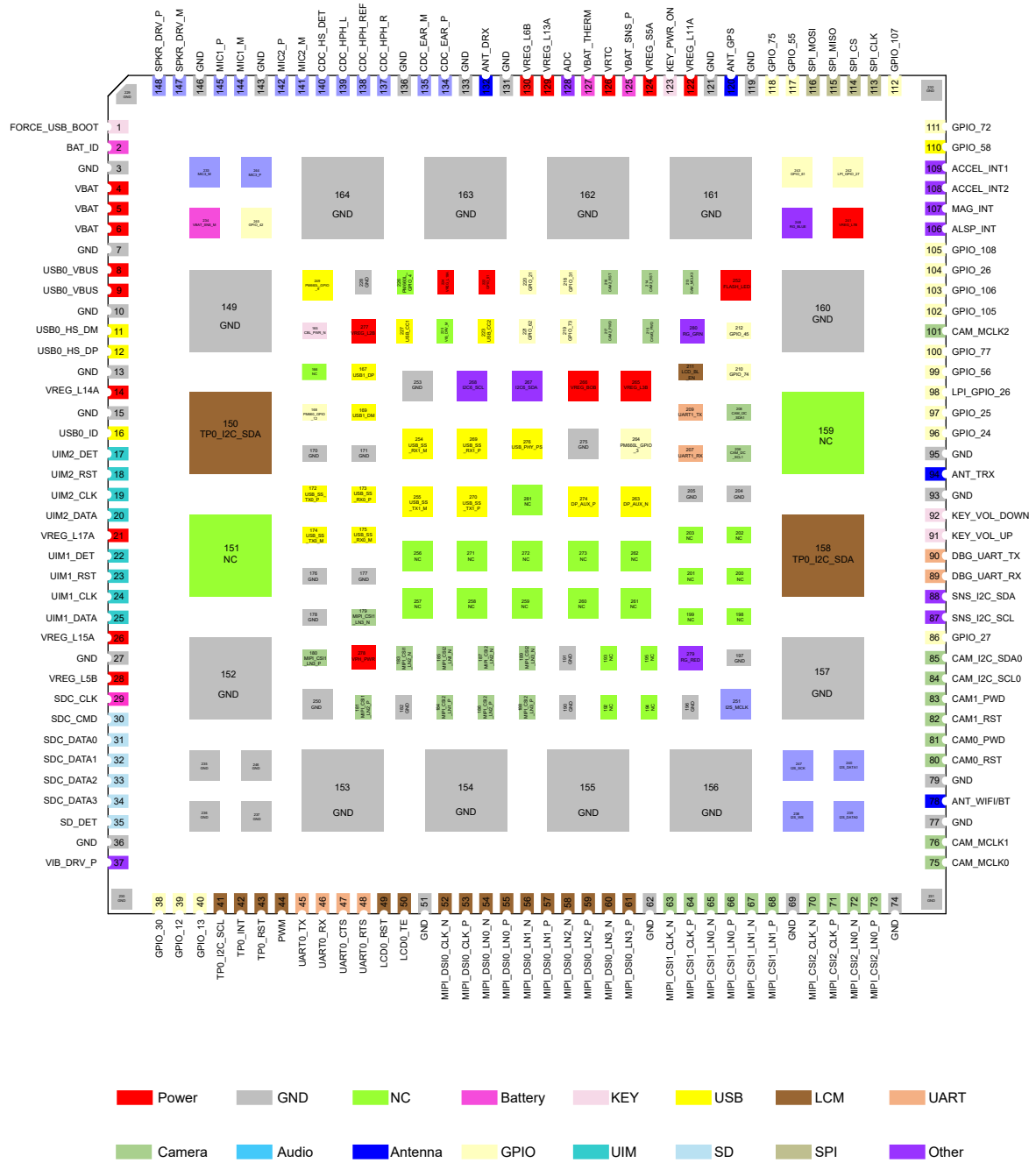

Figure 2. Pin assignment (top view)

"NC" indicates No Connect, and the pin for this position is reserved and does not need to be connected.

2.4.2 Pin Description

Table 5. I/O parameters description

Type	Description
I/O	Input/output
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open drain

Module Pin descriptions as the following table:

Table 6. Pin description

Pin Name	Pin No.	I/O	Pin Description	Remarks
Power interface				
VBAT	4,5,6	PI/PO	Main power supply	--
VRTC	126	PI/PO	RTC power supply	--
VREG_L18A	224	PO	Codec 2.8V power supply	
VREG_L6B	130	PO	LCM, TP 3.3V power supply	--

Pin Name	Pin No.	I/O	Pin Description	Remarks
VREG_L13A	129	PO	I/O 1.8V power supply	--
VPH_PWR	278	PO	General-purpose peripheral power supply	1A Irated
VREG_L17A	21	PO	UIM2 card power supply	--
VREG_L15A	26	PO	UIM1 card power supply	--
VREG_L11A	122	PO	Display touchscreen 1.8V power supply	--
VREG_BOB	266	PO	3.3V power supply	--
VREG_L7B	241	PO	DP 3.1V power supply	--
VREG_S5A	124	PO	1.35V power supply	--
VREG_L2B	277	PO	SDIO power supply	Dedicated for SD card
VREG_L5B	28	PO	SD card power supply	
VREG_L14A	14	PO	Sensors 1.8V power supply	--
VREG_L3B	265	PO	Sensors 3 V power supply	--
Motor interface				
VIB_DRV_P	37	AO	Haptics H-bridge driver output plus	--
VIB_DRV_M	225	AO	Haptics H-bridge driver output minus	--
Ground				
GND	3, 7, 10, 13, 15, 27, 36, 51, 62, 69, 74, 77, 79, 93, 95, 119, 121, 131, 133, 136, 143, 146, 149, 152, 153, 154, 155, 156, 157, 160, 161, 162, 163, 164, 170, 171, 176, 177, 178, 182, 190, 191, 196, 197, 204, 205, 228, 229, 230, 231, 232, 235, 236,	地	58	

Pin Name	Pin No.	I/O	Pin Description	Remarks
	237, 246, 250, 253, 275			
Battery interface				
VBAT_SNS_P	125	AI	Battery voltage sense input plus	connect to battery positive node
VBAT_SNS_M	234	AI	Battery voltage sense input minus	connect to battery negative node. When battery is unused, connected to GND
VBAT_THERM	127	AI	Battery temperature detection	Connect the pin to GND with 10 KΩ resistor, cannot float
BAT_ID	2	AI	Battery ID pin	Keep it float if unused
Button				
FORCE_USB_BOOT	1	DI	Force download button	Active high
KEY_VOL_UP	91	DI	Volume + button	Active low
KEY_VOL_DOWN	92	DI	Volume - button	Active low
KEY_PWR_ON	123	DI	Power on/off button	Active low
CBL_PWR_N	165	DI	Auto power-on trigger	Active low
UIM card interface				
UIM2_DET	17	DI	UIM2 hot plugging detection	Active high
UIM2_RST	18	DO	UIM2 reset signal	--
UIM2_CLK	19	DO	UIM2 clock signal	--
UIM2_DATA	20	DI/DO	UIM2 data signal	--

Pin Name	Pin No.	I/O	Pin Description	Remarks
UIM1_DET	22	DI	UIM1 hot plugging detection	Active high
UIM1_RST	23	DO	UIM1 reset signal	--
UIM1_CLK	24	DO	UIM1 clock signal	--
UIM1_DATA	25	DI/DO	UIM1 data signal	--
SD card interface				
SD_DET	35	DI	SD card detection	Active low by default
SD_DATA3	34	DI/DO	SD card data bit 3	--
SD_DATA2	33	DI/DO	SD card data bit 2	--
SD_DATA1	32	DI/DO	SD card data bit 1	--
SD_DATA0	31	DI/DO	SD card data bit 0	--
SD_CMD	30	DI/DO	SD card command interface	--
SD_CLK	29	DO	SD card clock	--
I2C interface				
TP0_I2C_SCL	41	DO	TP I2C clock signal	Dedicated for TP
TP0_I2C_SDA	150,158	DI/DO	TP I2C data signal	
CAM_I2C_SCL0	84	DO	CAM0 I2C clock signal	Dedicated for camera
CAM_I2C_SDA0	85	DI/DO	CAM0 I2C data signal	
CAM_I2C_SCL1	206	DO	CAM1/2 I2C clock signal	Dedicated for camera
CAM_I2C_SDA1	208	I/O	CAM1 I2C data signal	
I2C6_SCL	268	DO	I2C clock signal	For general peripheral
I2C6_SDA	267	I/O	I2C data signal	

Pin Name	Pin No.	I/O	Pin Description	Remarks
SNS_I2C_SCL	87	DO	Sensor I2C clock	Dedicated for sensors
SNS_I2C_SDA	88	I/O	Sensor I2C data	
USB interface				
USB0_VBUS	8,9	PI/PO	USB 5V power supply	--
GPIO_58	110	DI	Micro USB&Type C select	
PM660L_GPIO_9	249	DI	Micro USB&Type C select	
USB_PHY_PS	276	DI	USB port configure select	
USB0_ID	16	DI	USB 2.0 OTG detection	
USB0_HS_DM	11	AI/AO	USB high-speed 0 data–minus	--
USB0_HS_DP	12	AI/AO	USB high-speed 0 data–plus	--
USB_SS_RX0_M	175	AI	USB super-speed 0 receive – minus	--
USB_SS_RX0_P	173	AI	USB super-speed 0 receive – plus	--
USB_SS_TX0_M	174	AO	USB super-speed 0 transmit – minus	--
USB_SS_TX0_P	172	AO	USB super-speed 0 transmit – minus	--
USB_SS_RX1_M	254	AI	USB super-speed 1 receive – minus	--
USB_SS_RX1_P	269	AI	USB super-speed 1 receive – plus	--
USB_SS_TX1_M	255	AO	USB super-speed 1 transmit – minus	--

Pin Name	Pin No.	I/O	Pin Description	Remarks
USB_SS_TX1_P	270	AO	USB super-speed 1 transmit – minus	--
USB_CC1	227	AI	CC1 pin for the USB Type-C connector	--
USB_CC2	223	AI	CC2 pin for the USB Type-C connector	--
DP_AUX_N	263	AI/AO	DisplayPort auxiliary channel – negative	
DP_AUX_P	274	AI/AO	DisplayPort auxiliary channel – positive	
USB1_DM	169	AI/AO	USB high-speed 1 data – minus	
USB1_DP	167	AI/AO	USB high-speed 1 data –plus	
UART interface				
UART0_TX	45	DO	UART0 transmit	--
UART0_RX	46	DI	UART0 receive	--
UART0_CTS	47	DI	UART0 clear-to-send	--
UART0_RTS	48	DO	UART0 ready-for-receive	--
DBG_UART_RX	89	DI	Debug UART receive	--
DBG_UART_TX	90	DO	Debug UART transmit	--
UART1_RX	207	DI	UART1 transmit	--
UART1_TX	209	DO	UART1 receive	--
SPI Interface				
SPI_CLK	113	DO	SPI clock	--

Pin Name	Pin No.	I/O	Pin Description	Remarks
SPI_CS	114	DO	SPI chip select	--
SPI_MISO	115	DI	SPI master in slave out	--
SPI_MOSI	116	DO	SPI master output slave in	--
LCD interface				
MIPI_DSI0_CLK_N	52	AO	LCD MIPI-DSI signal	--
MIPI_DSI0_CLK_P	53	AO		--
MIPI_DSI0_LN0_N	54	AO		--
MIPI_DSI0_LN0_P	55	AO		--
MIPI_DSI0_LN1_N	56	AO		--
MIPI_DSI0_LN1_P	57	AO		--
MIPI_DSI0_LN2_N	58	AO		--
MIPI_DSI0_LN2_P	59	AO		--
MIPI_DSI0_LN3_N	60	AO		--
MIPI_DSI0_LN3_P	61	AO		--
PWM	44	DO	LCD backlight brightness PWM control	--
LCD_RST	49	DO	LCD reset signal	Boot configuration
LCD_TE	50	DI	LCD vertical synchronization	--
LCD_BL_EN	211	DO	Blacklight enable	
TP interface				
TP0_INT	42	DI	TP interrupt	--

Pin Name	Pin No.	I/O	Pin Description	Remarks
TP0_RST	43	DO	TP reset signal	--
Camera interface				
MIPI_CSI1_CLK_N	63	AI	Camera MIPI-CSI1cinterface. Keep the unused pins floating	--
MIPI_CSI1_CLK_P	64	AI		--
MIPI_CSI1_LN0_N	65	AI		--
MIPI_CSI1_LN0_P	66	AI		--
MIPI_CSI1_LN1_N	67	AI		--
MIPI_CSI1_LN1_P	68	AI		--
MIPI_CSI1_LN2_N	183	AI		--
MIPI_CSI1_LN2_P	181	AI		--
MIPI_CSI1_LN3_N	179	AI		--
MIPI_CSI1_LN3_P	180	AI		--
MIPI_CSI2_CLK_N	70	AI	Camera MIPI-CSI2 interface. Keep the unused pins floating	--
MIPI_CSI2_CLK_P	71	AI		--
MIPI_CSI2_LN0_N	72	AI		--
MIPI_CSI2_LN0_P	73	AI		--
MIPI_CSI2_LN1_N	185	AI		--
MIPI_CSI2_LN1_P	184	AI		--
MIPI_CSI2_LN2_N	187	AI		--
MIPI_CSI2_LN2_P	186	AI		--
MIPI_CSI2_LN3_N	189	AI		--
MIPI_CSI2_LN3_P	188	AI		--

Pin Name	Pin No.	I/O	Pin Description	Remarks
CAM_MCLK0	75	DO	Camera 0 clock signal	--
CAM0_RST	80	DO	Camera 0 reset signal	--
CAM0_PWD	81	DO	Camera 0 shutdown signal	--
CAM_MCLK1	76	DO	Camera 1 clock signal	--
CAM1_RST	82	DO	Camera 1 reset signal	--
CAM1_PWD	83	DO	Camera 1 shutdown signal	--
CAM_MCLK2	101	DO	Camera 2 clock signal	--
CAM2_RST	216	DO	Camera 2 reset signal	--
CAM2_PWD	217	DO	Camera 2 shutdown signal	--
CAM_MCLK3	213	DO	Camera 3 clock signal	--
CAM3_RST	214	DO	Camera 3 reset signal	--
CAM3_PWD	215	DO	Camera 3 shutdown signal	--
FLASH_LED	252	AO	Flash high-side current source for LED	Up to1.5 A
Audio interface				
MIC1_P	145	AI	Main MIC input+	Internal MIC_BIAS pull-up
MIC1_M	144	AI	Main MIC input-	Differential input
MIC2_P	142	AI	Headset MIC input+	Internal MIC_BIAS pull-up
MIC2_M	141	AI	Headset MIC input+	Single-ended

Pin Name	Pin No.	I/O	Pin Description	Remarks
				input
MIC3_P	244	AI	Secondary MIC input+	Internal MIC_BIAS pull-up
MIC3_M	233	AI	Secondary MIC input-	Single-ended input
CDC_EAR_P	134	AO	Receiver output+	--
CDC_EAR_M	135	AO	Receiver output-	--
SPKR_DRV_P	148	AO	Differential speaker driver output+	
SPKR_DRV_M	147	AO	Differential speaker driver output-	
CDC_HPH_R	137	AO	Headset right channel output	--
CDC_HPH_REF	138	/	Headset reference ground	Connect to ground
CDC_HPH_L	139	AO	Headset left channel output	--
CDC_HS_DET	140	AI	Headset plug detection	--
I2S interface				
I2S_MCLK	251	DO	MI2S master clock	
I2S_SCK	247	DI/DO	MI2S bit clock	
I2S_WS	238	DI/DO	MI2S word select (L/R)	
I2S_DATA0	239	DI/DO	MI2S serial data channel 0	
I2S_DATA1	240	DI/DO	MI2S serial data channel 1	
Antenna interface				

Pin Name	Pin No.	I/O	Pin Description	Remarks
ANT_TRX	94	AI/AO	Main antenna	--
ANT_DRX	132	AI	Diversity antenna	--
ANT_WIFI/BT	78	AI/AO	WIFI/BT antenna	--
ANT_GNSS	120	AI	GNSS antenna	--
GPIO Interface				
GPIO_30	38	DI/DO	General purpose input and Output,1.8V power	--
GPIO_31	218	DI/DO		--
GPIO_12	39	DI/DO		--
GPIO_13	40	DI/DO		--
GPIO_24	96	DI/DO		--
GPIO_25	97	DI/DO		--
GPIO_26	104	DI/DO		--
GPIO_27	86	DI/DO		--
LPI_GPIO_26	98	DI/DO		--
GPIO_56	99	DI/DO		--
GPIO_77	100	DI/DO		--
GPIO_105	102	DI/DO		--
GPIO_106	103	DI/DO		--
GPIO_108	105	DI/DO		--
GPIO_72	111	DI/DO		--
GPIO_107	112	DI/DO		--
GPIO_55	117	DI/DO		--

Pin Name	Pin No.	I/O	Pin Description	Remarks
GPIO_75	118	DI/DO		--
GPIO_42	245	DI/DO		--
PM660L_GPIO_3	264	DI/DO		--
LPI_GPIO_27	242	DI/DO		--
GPIO_61	243	DI/DO		--
GPIO_74	210	DI/DO		--
GPIO_45	212	DI/DO		--
GPIO_73	219	DI/DO		--
GPIO_21	220	DI/DO		--
GPIO_62	221	DI/DO		--
GPIO_51	222	DI/DO		--
PM660_GPIO_12	168	DI/DO		--
PM660L_GPIO_4	226	DI/DO		--
LED interface				
RG_BLUE	248	AO	RGB LED high-side current source for the red LED	Up to 8mA
RG_GRN	280	AO	RGB LED high-side current source for the green LED	Up to 8mA
RG_RED	279	AO	RGB LED high-side current source for the red LED	Up to 8mA
Sensor interface				
ALSP_INT	106	DI	Ambient light and Proximity sensor interrupt	--

Pin Name	Pin No.	I/O	Pin Description	Remarks
MAG_INT	107	DI	Magnetic sensor interrupt	--
ACCEL_INT1	109	DI	G-Sensor interrupt 1	--
ACCEL_INT2	108	DI	G-Sensor interrupt 2	--
Other Interfaces				
ADC	128	AI	ADC input	--
NC	166,192,193,194,195,200,201,202,203,256,257,258,259,260,261,262,271,272,273			--

3 Application Interfaces

3.1 Power Supply

The module provides three VBAT pins for connecting to external power supply source. The input range of power is 3.5 V to 4.35V and the recommended value is 3.8 V. The performance of the power supply such as its load capacity, ripple etc. will directly affect the operating performance and stability of the module. The peak current of the module can reach 3 A. If the power supply capacity is insufficient, the power supply transient voltage drops below 3.5 V, which may cause the module power-off or restart. The power supply voltage drop is shown in the following figure:

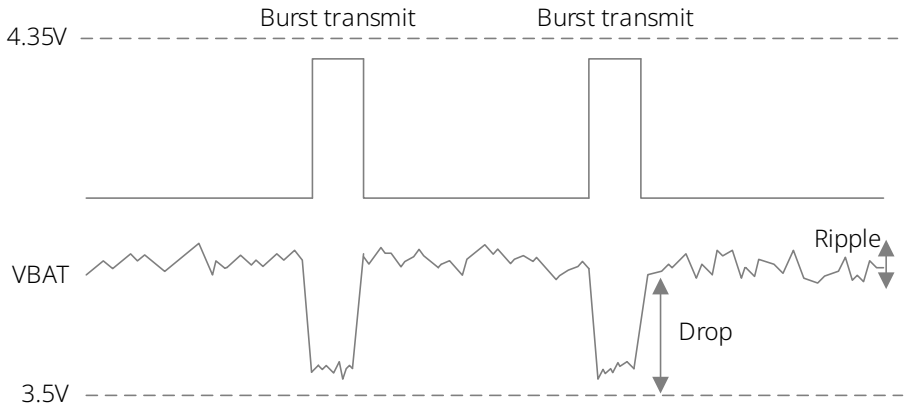

Figure 3.Voltage drop

3.1.1 Power Input

External power source supplies the module by VBAT pins. To ensure the power transient voltage is no less than 3.5 V, it is recommended to connect two 220μF tantalum capacitors with low ESR and filter capacitors of 1μF, 100nF, 39pF and 33pF in parallel to the VBAT input of the module. Besides, the PCB route of VBAT should be as short and wide as possible (no less than 3 mm) and the ground plane of the power section should be flat to reduce the equivalent impedance of the VBAT route and avoid significant voltage drop at high currents at maximum transmit power.

Table 7. Power supply

Parameter	Minimum	Typical	Maximum	Unit
VBAT input voltage	3.5	3.8	4.4	V
VBAT operating current	--	--	3	A

The voltage range of VBAT power supply must be between 3.5 V and 4.35V, including the superimposed value of ripple, drop, instantaneous overshoot and other voltages.

The following figure shows the reference design of power circuit.

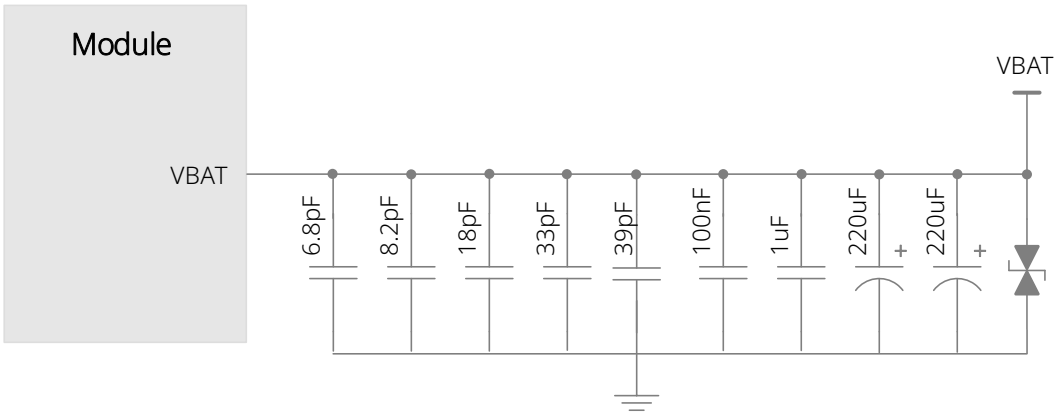

Figure 4. Power supply reference design

The following table describes the filter capacitor design of power supply.

Table 8. Filter capacitor design of power supply

Recommended Capacitor	Application	Description
220 μF×2	Regulating capacitor	To reduce power fluctuations during module operation, low ESR capacitors are required. LDO or DCDC power supply requires capacitor with a capacitance of no less

Recommended Capacitor	Application	Description
		than 440μF. Battery power supply requires capacitors with a capacitance of 100-220μF.
1μF, 100nF	Low frequency filter capacitors	Filter out interference caused by clock and digital signals.
39 pF, 33 pF, 18 pF, 8.2 pF, 6.8 pF	Decoupling capacitor	Filter high frequency interference.

3.1.2 VRTC

VRTC is the power supply of the internal RTC clock of the module. When powered on VBAT pin, the VRTC pin will output voltage. When VBAT is disconnected, if the real-time clock needs to be maintained, it needs to be powered by an external power source (such as a coin battery). The VRTC parameters are as follows:

Table 9. VRTC parameters

Parameter	Minimum	Typical	Maximum	Unit
VRTC output voltage	2.5	3.0	3.2	V
VRTC input voltage (clock works well)	2.5	3.0	3.2	V
VRTC input current (clock works well)	5	7	8	uA

The VRTC power supply uses the following reference circuit when powered by an external power source:

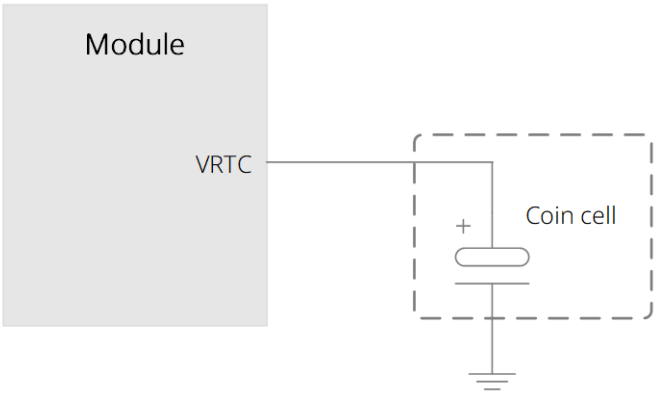

Figure 5. VRTC reference design

3.1.3 VPH_PWR

The module supports the output of VPH_PWR as the peripheral power supply, the voltage is the same as that of VBAT and the maximum output current is 1A. If the module internal fuel gauge function is used, VPH_PWR needs to be used as the LCD, backlight, camera and other peripheral power supply to obtain higher power calculation accuracy.

3.1.4 Power Output

The module provides multiple power outputs for peripheral circuits. 33 pF and 10 pF capacitors can be connected in parallel to avoid high frequency interference effectively. When multiple peripherals share one LDO power output, please make sure the total capacitance is no more than 1uF.

Table 10. Power output

Pin Name	Pin No.	Description	Nominal voltage(V)	Irated (mA)	Sleep state
VPH_PWR	278	Primary system supply	VBAT	1000	On
VREG_L18A	224	Codec 2.8V	2.864	50	Off
VREG_L6B	130	LCM, TP	3.312	50	Off

Pin Name	Pin No.	Description	Nominal voltage(V)	Irated (mA)	Sleep state
VREG_L13A	129	Primary IOVDD	1.8	500	On
VREG_L17A	21	UICC2 dedicated	1.808	150	Off
VREG_L15A	26	UICC1. NFC dedicated	1.808	150	Off
VREG_L11A	122	Display touchscreen	1.8	150	Off
VREG_BOB	266	External LDO input	1.8	3000 (Varies based on Vin)	Bypass
VREG_L7B	241	USB (EUD)	3.316	100	Lowered
VREG_S5A	124	Camera LDO	1.35	3000	Lowered
VREG_L2B	277	SD Card_IO	2.96	50	Off
VREG_L5B	28	SD/MMC card	2.96	600	Off
VREG_L14A	14	Sensors (1.8 V)	1.8	150	Off
VREG_L3B	265	Sensors 3 V	3.008	600	Off

When use the LDO, the total capacitance of the power supply must less than 1uF.

3.2 Control Signal

3.2.1 Power On/Off

The module provides two-way power-on/off control signals to control module's power-on/off, restart and sleep/wakeup.

Table 11. Power-on/off control

Pin Name	Pin No.	I/O	Description	Remarks
KEY_PWR_ON	123	DI	Active low, used to power on/off and restart the module, make the module to sleep and wake up the module	--
CBL_PWR_N	165	DI	Active low, used to power on the module only	--

3.2.1.1 Power-on

After the module's VBAT pin is powered on, pull down KEY_PWR_ON pin for 2s–6s to trigger module to start. The keystroke and OC driver power-on reference circuit are designed as follows:

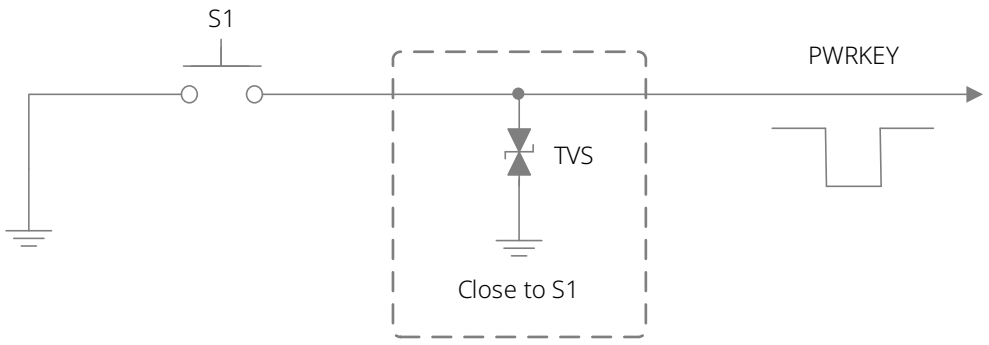

Figure 6. Buttons power-on reference design

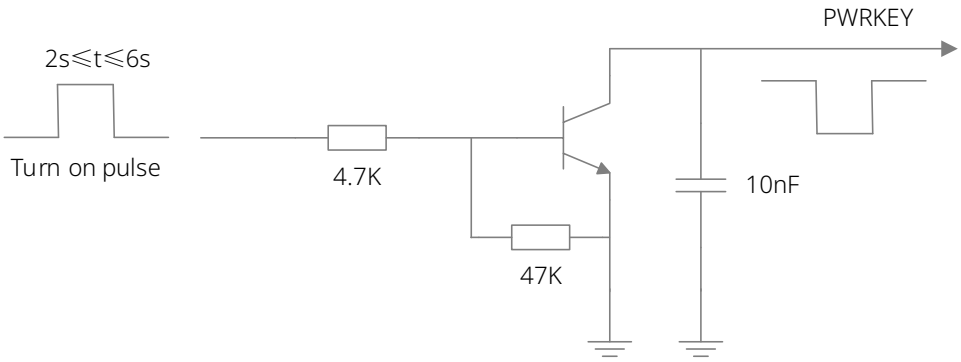

Figure 7. OC driver power-on reference design

The CBL_PWR_N pin is connected to the ground through a 1K resistor, and the module can be started up automatically after power-on. The following figure shows the reference circuit for automatic startup upon power-on.

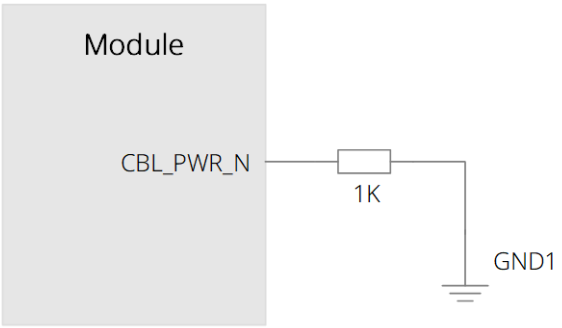

Figure 8. CBL power-on reference design

Power on sequence is shown as follows:

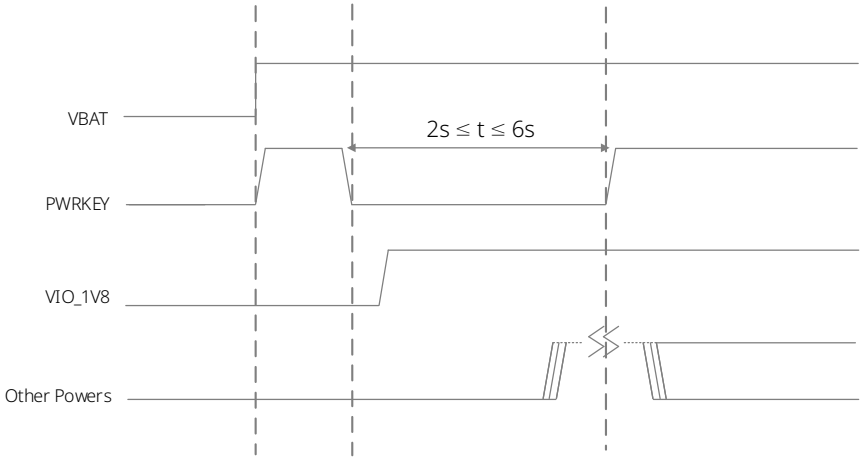

Figure 9. Power on sequence

3.2.1.2 Power-off and Reset

Normal power off: When the module is in operating mode, pull down KEY_PWR_ON pin for more than 2-6s. A dialog box is displayed, prompting you to power off or restart the module.

Forced power off: Pull down KEY_PWR_ON pin for 8s to 15s, and the module will be forcibly powered off. The forced power off timing is as follows:

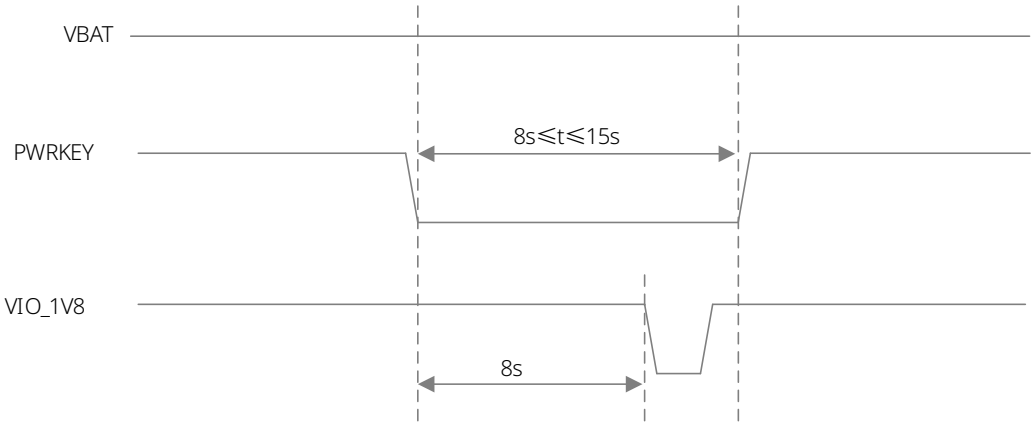

Figure 10. Power-off sequence

When the system is abnormal or crashes, you can forcibly reset the module. The normal power-off method is recommended in normal cases, because

forced reset may cause data loss and other anomalies.

3.2.1.3 Sleep/Wakeup

When module is in standby mode, pull down KEY_PWR_ON pin for 0.5s and the module will enter sleep mode. The system supports automatic sleep. The time from standby to sleep can be configured through software.

When module is in sleep mode, pull down KEY_PWR_ON pin for 0.5s and the module can be woken up.

3.2.1.4 Volume Control

KEY_VOL_UP and KEY_VOL_DOWN pins are used as the volume down key and volume up key; the volume key circuit design can be referred to the power-on circuit design.

3.3 USB

The module supports one USB 3.1 interface that is downward compatible with USB 2.0 interface. USB 3.1 interface supports SS (5 Gbps) mode, but does not support software download. USB 2.0 interface supports the HS (480 Mbps) mode and software download, and is downward compatible with FS and LS interface. USB supports OTG function and HUB expansion interface. The pin definition of the USB interface is as follows:

Table 12. USB 3.1 pin definition

Pin name	Pin NO.	I/O	Description	Remarks
USB0_VBUS	8,9	PI/PO	USB 5V power supply	--
GPIO_58	110	DI	Micro USB&Type C select	--
PM660L_GPIO_9	249	DI	Micro USB&Type C select	--
USB_PHY_PS	276	DI	USB port configure select	--

USB0_ID	16	DI	USB 2.0 OTG detection	--
USB0_HS_DM	11	AI/AO	USB high-speed 0 data–minus	--
USB0_HS_DP	12	AI/AO	USB high-speed 0 data–plus	--
USB_SS_RX0_M	175	AI	USB super-speed 0 receive –minus	--
USB_SS_RX0_P	173	AI	USB super-speed 0 receive – plus	--
USB_SS_TX0_M	174	AO	USB super-speed 0 transmit – minus	--
USB_SS_TX0_P	172	AO	USB super-speed 0 transmit – minus	--
USB_SS_RX1_M	254	AI	USB super-speed 1 receive –minus	--
USB_SS_RX1_P	269	AI	USB super-speed 1 receive – plus	--
USB_SS_TX1_M	255	AO	USB super-speed 1 transmit – minus	--
USB_SS_TX1_P	270	AO	USB super-speed 1 transmit – minus	--
USB_CC1	227	AI	CC1 pin for the USB Type-C connector	--
USB_CC2	223	AI	CC2 pin for the USB Type-C connector	--
DP_AUX_N	263	AI/AO	DisplayPort auxiliary channel – negative	--
DP_AUX_P	274	AI/AO	DisplayPort auxiliary channel – positive	--

The reference circuit design of the USB 3.1 (Type-C) interface is as follows:

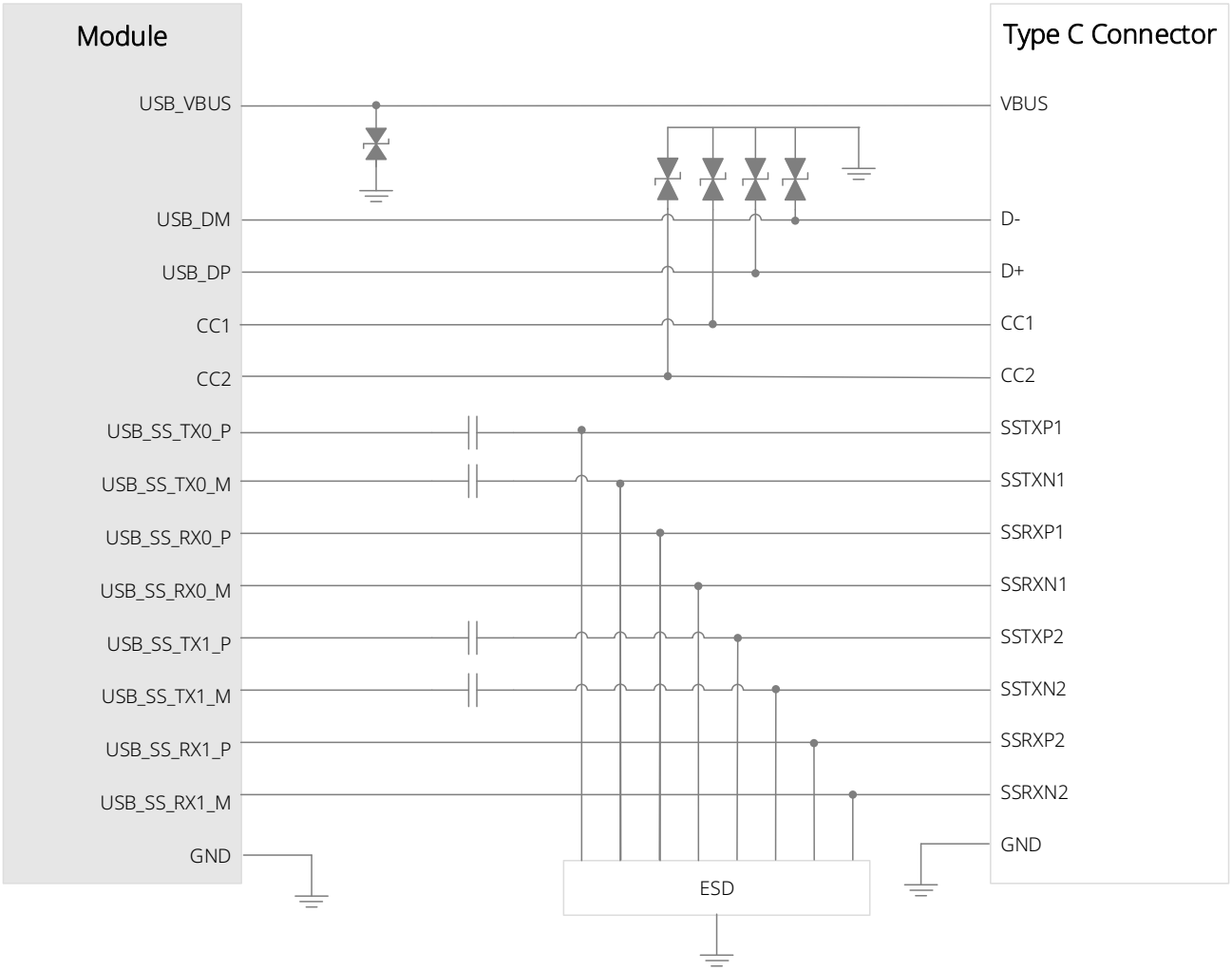

Figure 11. USB 3.1 reference design

The reference design of DP Over Type C is as follows:

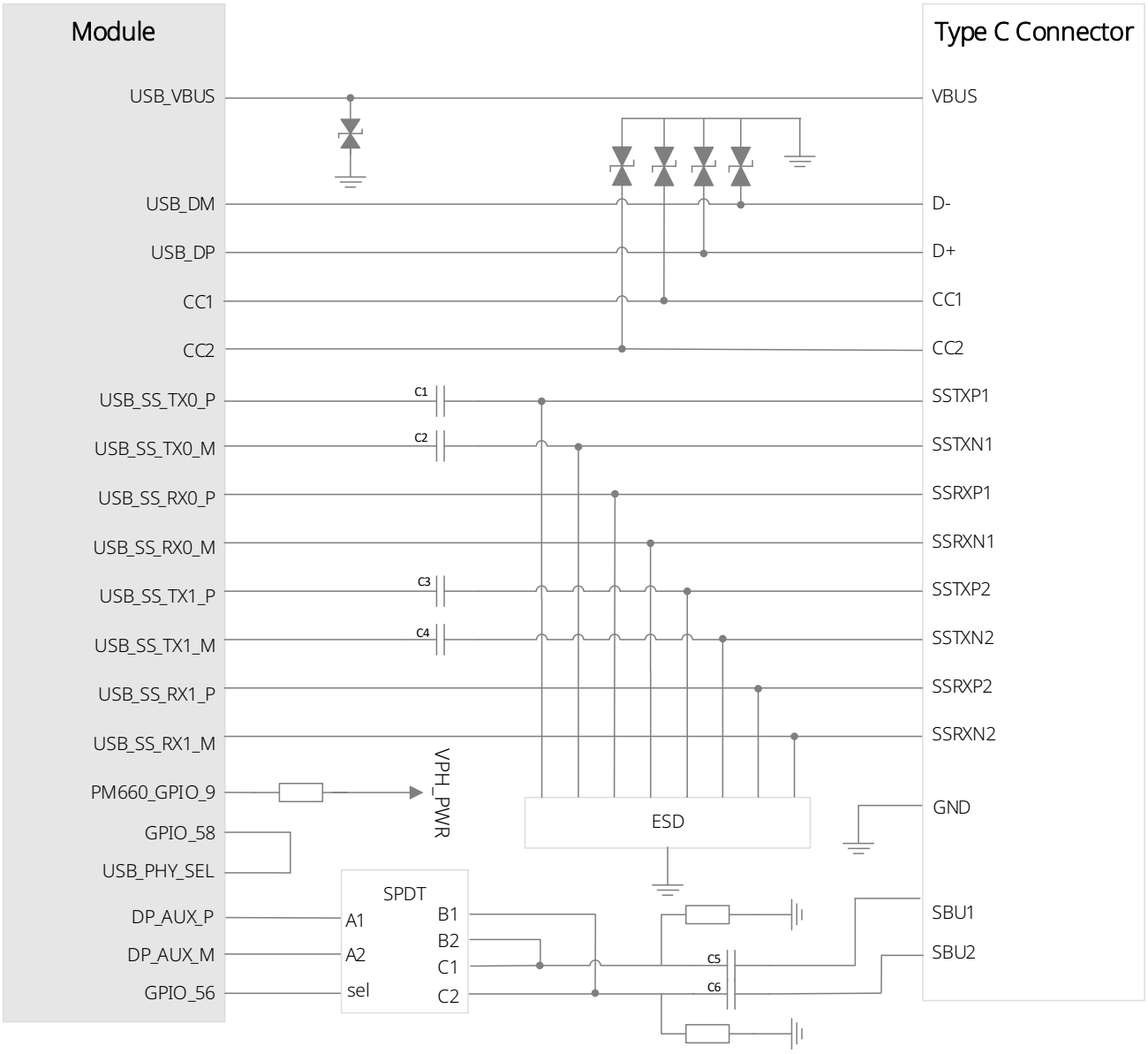

Figure 12. DP over type C reference design

DP reference design:

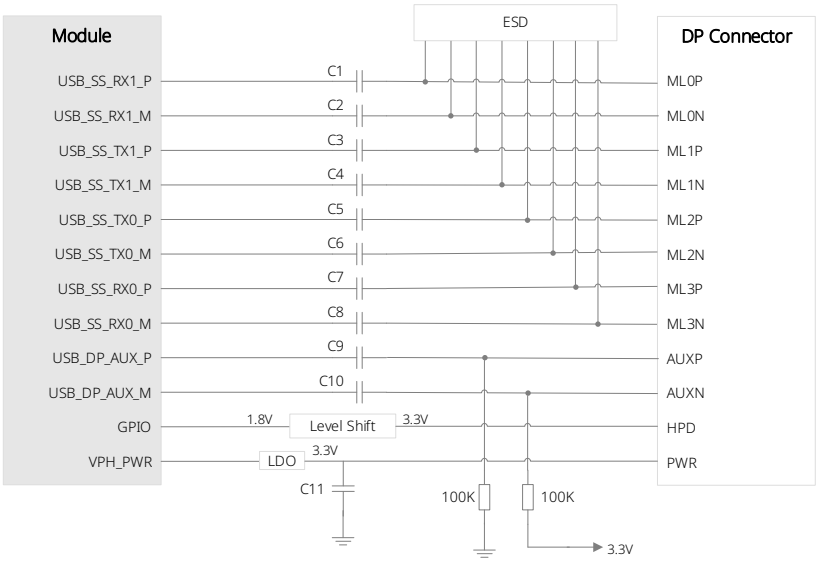

Figure 13.DP reference design

Table 13. USB 2.0 pin definition

Pin Name	Pin No.	I/O	Description	Remarks
USB1_DM	169	AI/AO	USB high-speed 0 data–minus	Only support host mode
USB1_DP	167	AI/AO	USB high-speed 0 data–plus	Only support host mode

The reference design of USB2.0 is as follows:

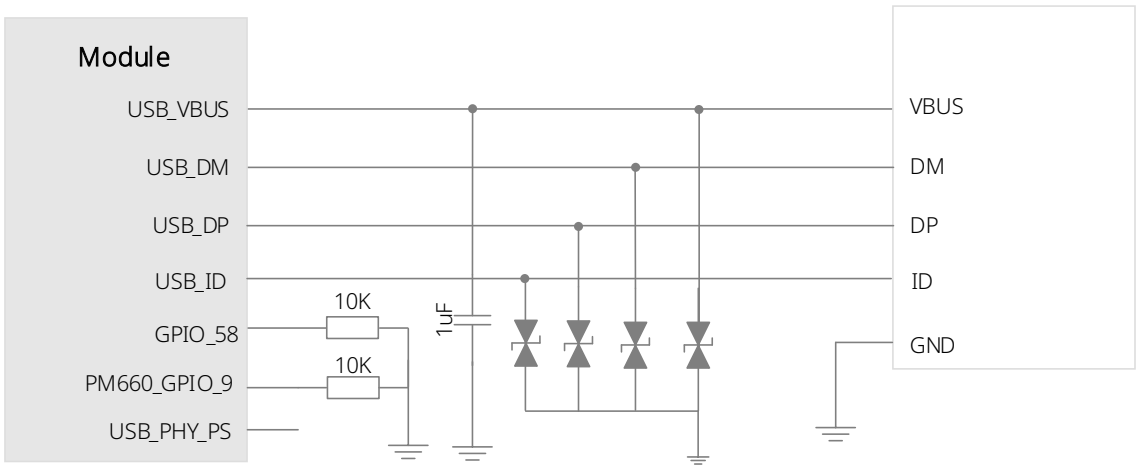

Figure 14.USB 2.0 reference design

Precautions for USB design:

- The junction capacitor for ESD protection device of USB_DP/DM must be less than 2pF.
- USB_DP and USB_DM are high-speed differential signal lines. The highest transmission rate is 480Mbps. Please pay attention to the following requirements during PCB layout:
  - USB_DP and USB_DM signal cables should be parallel and equal in length (differential cable length differences should be controlled within 2 mm), while the right-angle route shall be avoided, and differential 90Ω impedance shall be controlled.
  - USB2.0 differential signal cables should be fully grounded.
- Support OTG function: The VBUS interface of the module provides 5 V output as OTG power supply.
- USB1only support host mode, and need 5V power supply externally.

Precautions for USB 3.1 design:

- USB 3.1 is a high-speed signal cable and needs to be well-shielded (differential cable surrounded by grounding lines should be fully grounded), and follows the principle of high-speed differential cable routing.

- Control the differential impedance, make it 90 Ω ± 10% and ensure that the differential cable length differences are within 0.7 mm.
- The parasitic capacitance of ESD device must be less than 0.5 pF.

3.4 UART

The module defines three sets of UART ports, which are all in 1.8 V voltage domain. The pin definition please refer to Pin description.

The voltage domain of each serial port is 1.8 V; when communicating with other voltage domain serial ports, it is necessary to add a level-shifting chip with the following reference circuit design:

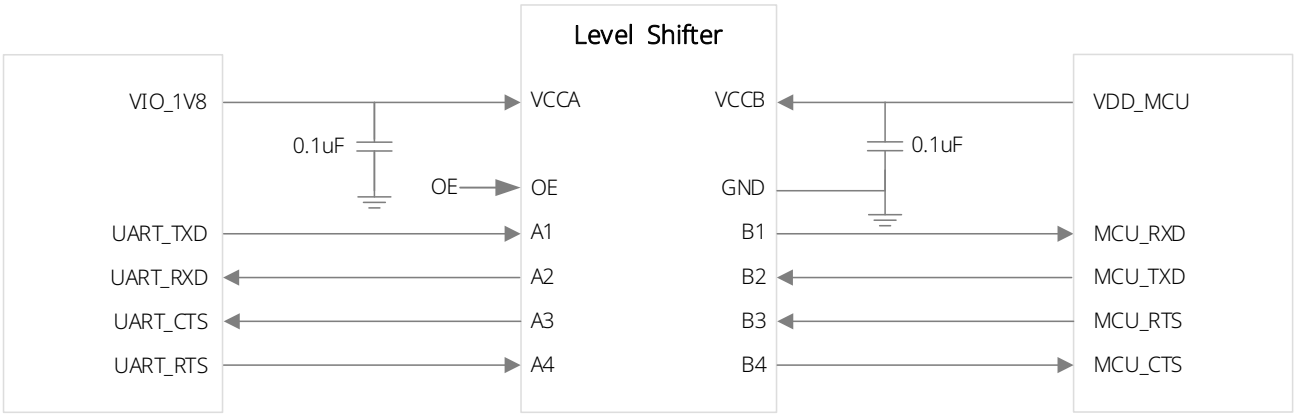

Figure 15.Level shift reference design

3.5 SPI

The module provides one set of SPI interfaces that support master and slave mode. The pin definition please refer to Pin description.

3.6 SD card

The module supports one SD card interface. The pin definition please refer to Pin description.

SD card reference design is as follows:

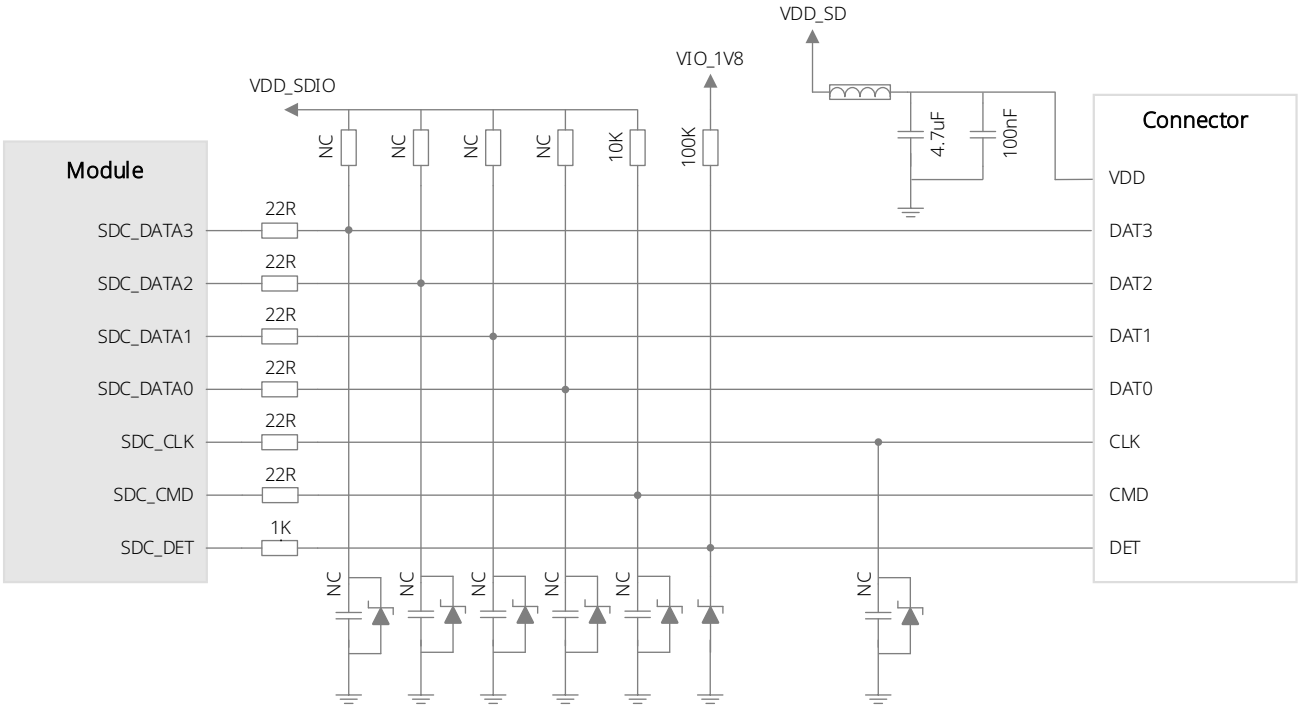

Figure 16. SD card reference design

- VREG_L3B is the SD card peripheral driving power and can provide about 600mA current. Pay attention to control the width of cable, which should be larger than 0.6 mm.
- SD_DET pin cannot floating, pull up or pull down according to active type, if don't use SD card, corresponding driver must be delete by software. Pull up SD_DET with VREG_L13A power supply
- SD is a high-speed digital signal line and must be shielded. Their length must be equal during layout.
- Note that the length of the SD card clock and signal cables should not exceed 50 mm, and the TVS tube should be a device with a parasitic capacitance less than 0.5 pF.

3.7 UIM

The module provides two UIM card interfaces that support dual card dual standby. The pin

definition please refer to Pin description.

UIM reference circuit design is as follows:

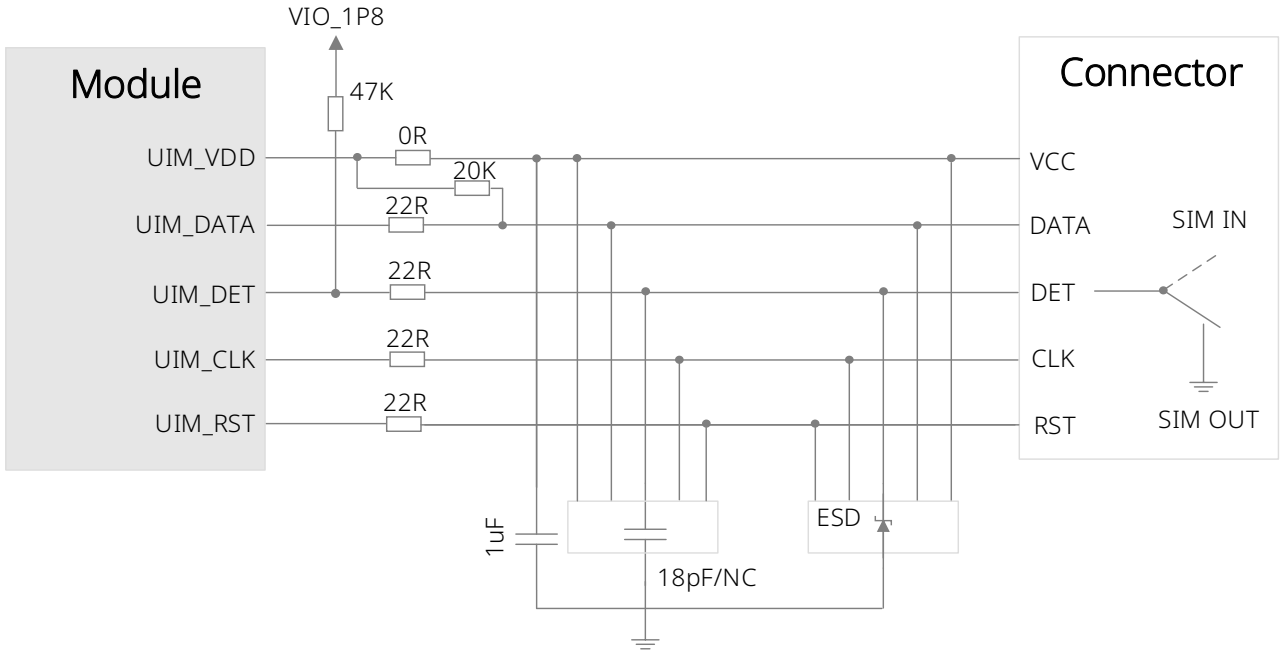

Figure 17. UIM reference design

3.8 GPIO

The module has rich GPIO resources and the interface level is 1.8 V. The pin definition is as follows:

Table 14. GPIO list

Pin Name	Pin No.	Reset state	Function	Interrupt	Note
GPIO_30	38	B-PD:nppukpB	Configurable I/O BLSP 8 bit 1: I2C_SDA	YES	--
GPIO_31	218	B-PD:nppukpB	Configurable I/O BLSP 8 bit 0: I2C_SCL	YES	--
GPIO_12	39	B-PD:nppukp	Configurable I/O	NO	--

Pin Name	Pin No.	Reset state	Function	Interrupt	Note
GPIO_13	40	B-PD:nppukp	Configurable I/O	YES	--
GPIO_24	96	B-PD:nppukp DO DO B DO	Configurable I/O BLSP 7 bit 3: SPI_ MOSI UART_TXD MI2S 2-bit clock SoundWire clock	NO	--
GPIO_25	97	B-PD:nppukp DI DI B B	Configurable I/O BLSP 7 bit 2: SPI_MISO UART_RXD MI2S 2 word select (L/R) SoundWire data	YES	--
GPIO_26	104	B-PD:nppukp DO DI B B	Configurable I/O BLSP 7 bit 1: SPI_ CS_N UART_ CTS_N I2C_ SDA MI2S2 serial data channel0	NO	--
GPIO_27	86	B-PD:nppukp DO DO B B	Configurable I/O BLSP 7 bit 0: SPI_ CLK UART_RFR_N I2C_SCL MI2S 2 serial data channel 1	NO	--
LPI_GPIO_26	98	DO B-PD:nppukp	LPI DMIC 1 clock Configurable I/O	NO	--

Pin Name	Pin No.	Reset state	Function	Interrupt	Note
GPIO_56	99	B-PD:nppukp	Configurable I/O	YES	
GPIO_77	100	B-PD:nppukp	Configurable I/O	YES	
GPIO_105	102	B-PD:nppukp DO	Configurable I/O GRFC_11	YES	--
GPIO_106	103	B-PD:nppukp DO	Configurable I/O GRFC_10	NO	--
GPIO_108	105	B-PD:nppukp DO	Configurable I/O GRFC_12	NO	--
GPIO_72	111	B-PD:nppukp	Configurable I/O	YES	--
GPIO_107	112	B-PD:nppukp	Configurable I/O	YES	--
GPIO_55	117	B-PD:nppukp	Configurable I/O	YES	--
GPIO_75	118	B-PD:nppukp	Configurable I/O	YES	--
GPIO_42	245	B-PD:nppukp	Configurable I/O	YES	--
PM660L_GPIO_3	264	PD:nppu	Configurable I/O	NO	--
LPI_GPIO_27	242	B-PD:nppukp	Configurable I/O	YES	--
GPIO_61	243	B-PD:nppukp	Configurable I/O	NO	--
GPIO_74	210	B-PD:nppukp	Configurable I/O	YES	--
GPIO_45	212	PD:nppukp	Configurable I/O	YES	--
GPIO_73	219	PD:nppukp	Configurable I/O	YES	--
GPIO_21	220	PD:nppukp	Configurable I/O	YES	--
GPIO_62	221	PD:nppukp	Configurable I/O	NO	--
GPIO_51	222	PD:nppukp	Configurable I/O	YES	--

Pin Name	Pin No.	Reset state	Function	Interrupt	Note
PM660_GPIO_12	168	PD:nppu	Configurable I/O	NO	--
PM660L_GPIO_4	226	PD:nppu	Configurable I/O	NO	--

GPIOS with Boot configuration note cannot be pulled up externally, otherwise may cause module abnormal.

Table 15.Parameter description

Parameter	Description
B	Bidirectional digital with CMOS input
NP	pdpukp: defaulted to no-pull with programmable options following the colon (:).
PD	nppukp: defaulted to pull-down with programmable options following the colon (:).
PU	nppdkp: defaulted to pull-up with programmable options following the colon (:).
KP	nppdpu: defaulted to keeper with programmable options following the colon (:).

3.9 I2C

The module provides 4 sets of I2C interfaces for TP, camera, sensor and peripheral. The pin definition please refer to Pin description.

When I2C has more than one peripheral, please ensure the uniqueness of every peripheral address. If one of the peripherals has high requirement for timeliness, do not set the peripherals to share one set of I2C interfaces.

3.10 ADC

The module provides one ADC interface. The pin definition please refer to Pin description.

3.11 Battery Supply Interface

The module support battery of 10K thermal resistor by default, for other type thermal battery are software configuration.

The reference design of battery is as follows:

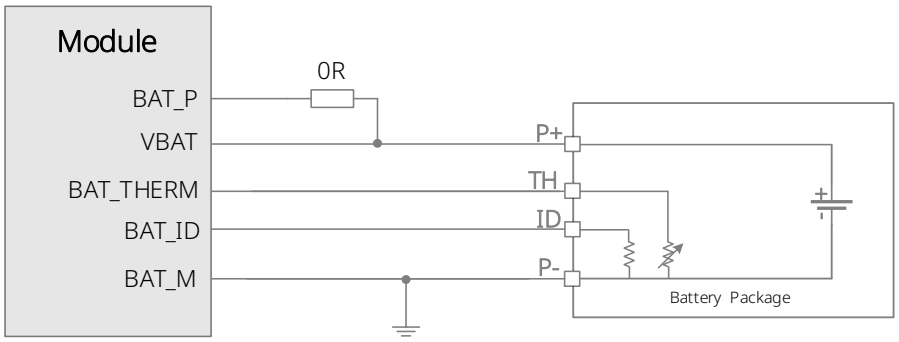

Figure 18.Battery circuit reference design

3.12 Haptics Driver Interface

Software selectable linear resonant actuator (LRA)/eccentric rotating mass (ERM), The reference design of haptics is as follows.

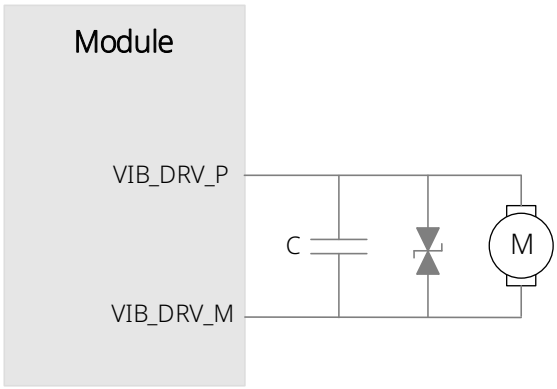

Figure 19.Haptics reference design

3.13 LCD

The screen interface is based on MIPI_DSI standard and supports one set of 4-Lane high-speed differential data transmission. It supports 1080P resolution，The pin definition please refer to Pin description.

The reference design of LCD interface is as follows:

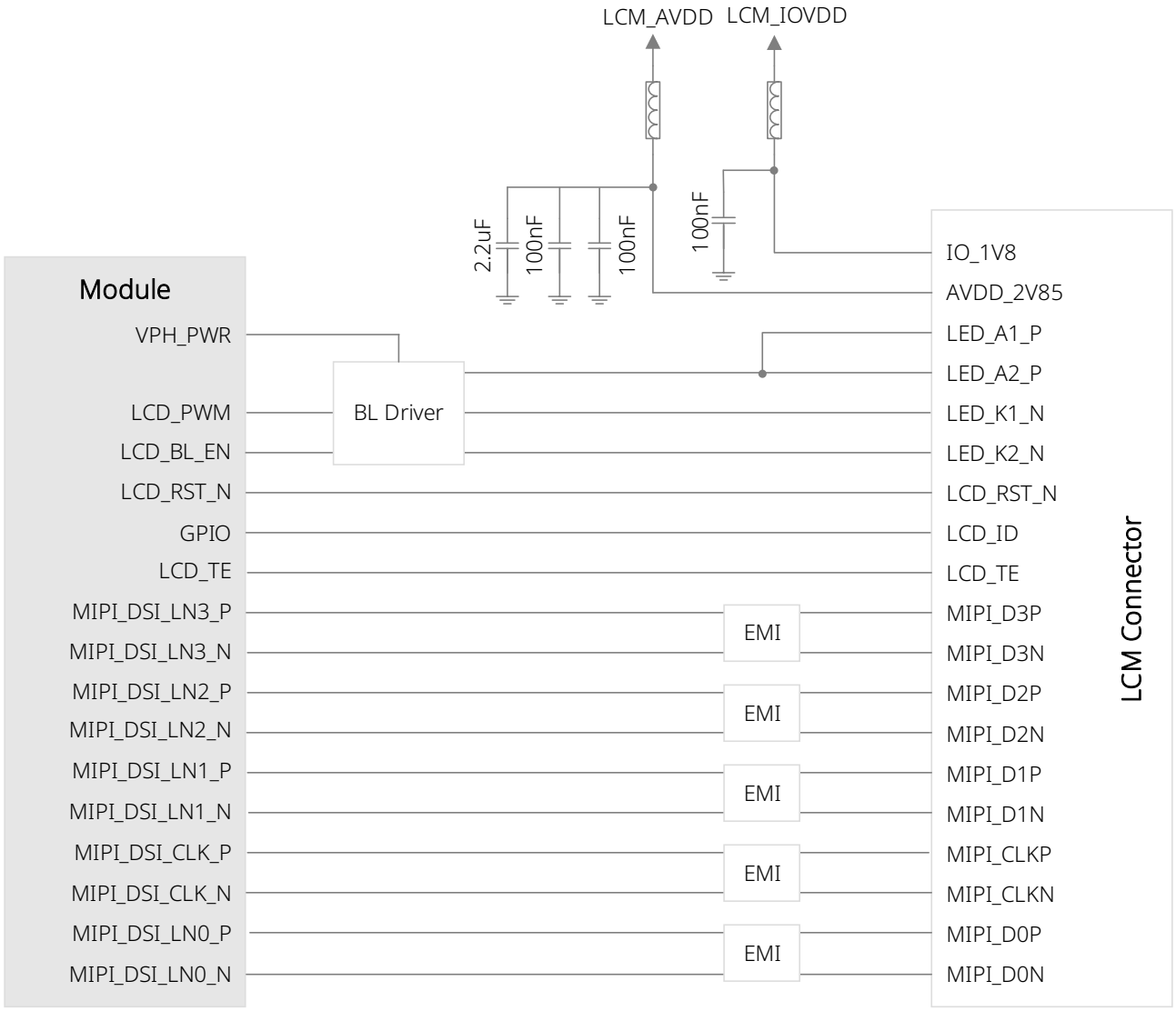

Figure 20. LCD reference design

Precautions for LCD design:

- MIPI is a high-speed signal line. It is recommended to connect the common mode inductor in series near the LCD connector to reduce the EMI (electromagnetic interference) of the circuit;
- MIPI routing is recommended to be designed in the inner layer, and connected using GND in three dimensions;
- The MIPI signal line needs to be controlled with a 100 Ω differential impedance with tolerance ±10%;

- The total length of the cable shall not exceed 300 mm;
- The intra lane match of MIPI signal cable must be controlled within 0.67 mm;
- The inter lane match of MIPI signal cable must be controlled within 1.3 mm;
- EMI components are optional, and the whole routing stray capacitance should be controlled under 1pF;
- It is recommended that the space of intra-lane differential line should be 1 times of the route width and the space between differential line and other routes should be controlled 2.5 times of the route width.

3.14 TP

The module provides one set of I2C interfaces that can be used to connect to the TP and the module provides power, interrupt, reset pins required for the TP. The pin definition please refer to Pin description.

TP reference circuit design is as follows:

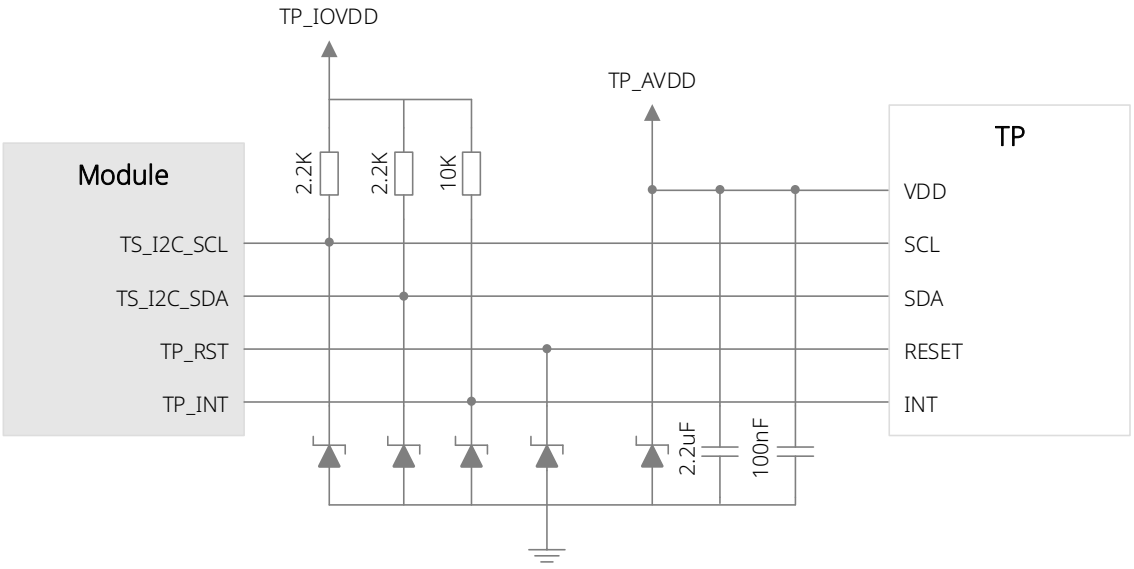

Figure 21. TP reference design

3.15 Camera

The camera interface of module is based on the MIPI_CSI standard, and can support two (4 Lane + 4 Lane) or three (4 Lane + 2 Lane + 1 Lane) cameras. The maximum resolution is 24 MP. The module doesn't have dedicate camera power supply, and external LDO is needed. The pin definition please refer to Pin description.

3.15.1 4 lane camera

The reference circuit design of 4 lane camera is as follows:

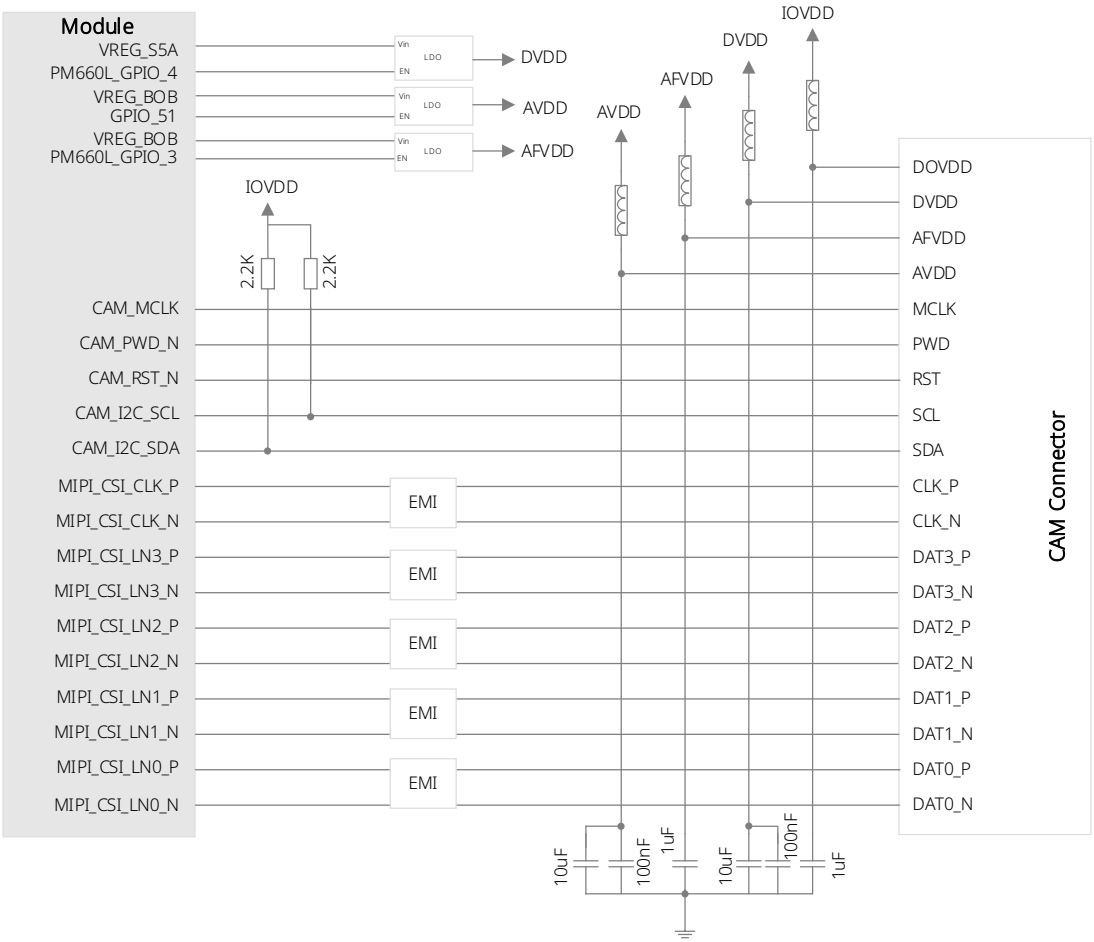

Figure 22. 4 lane camera reference design

3.15.2 2 lane camera

The reference circuit design of 2 lane camera is as follows:

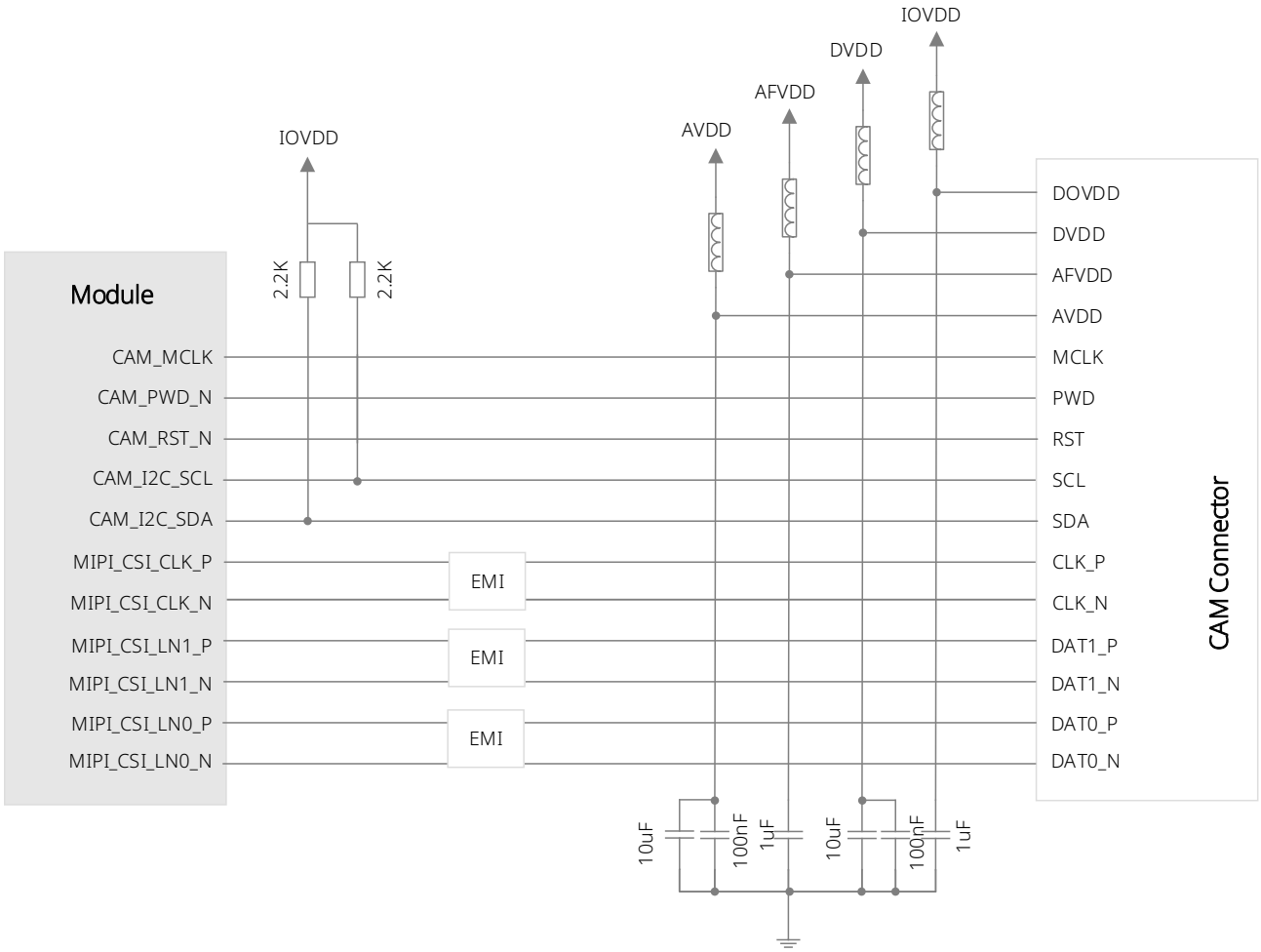

Figure 23. 2 lane camera reference design

3.15.3 1 lane camera

The reference circuit design of 1 lane camera is as follows:

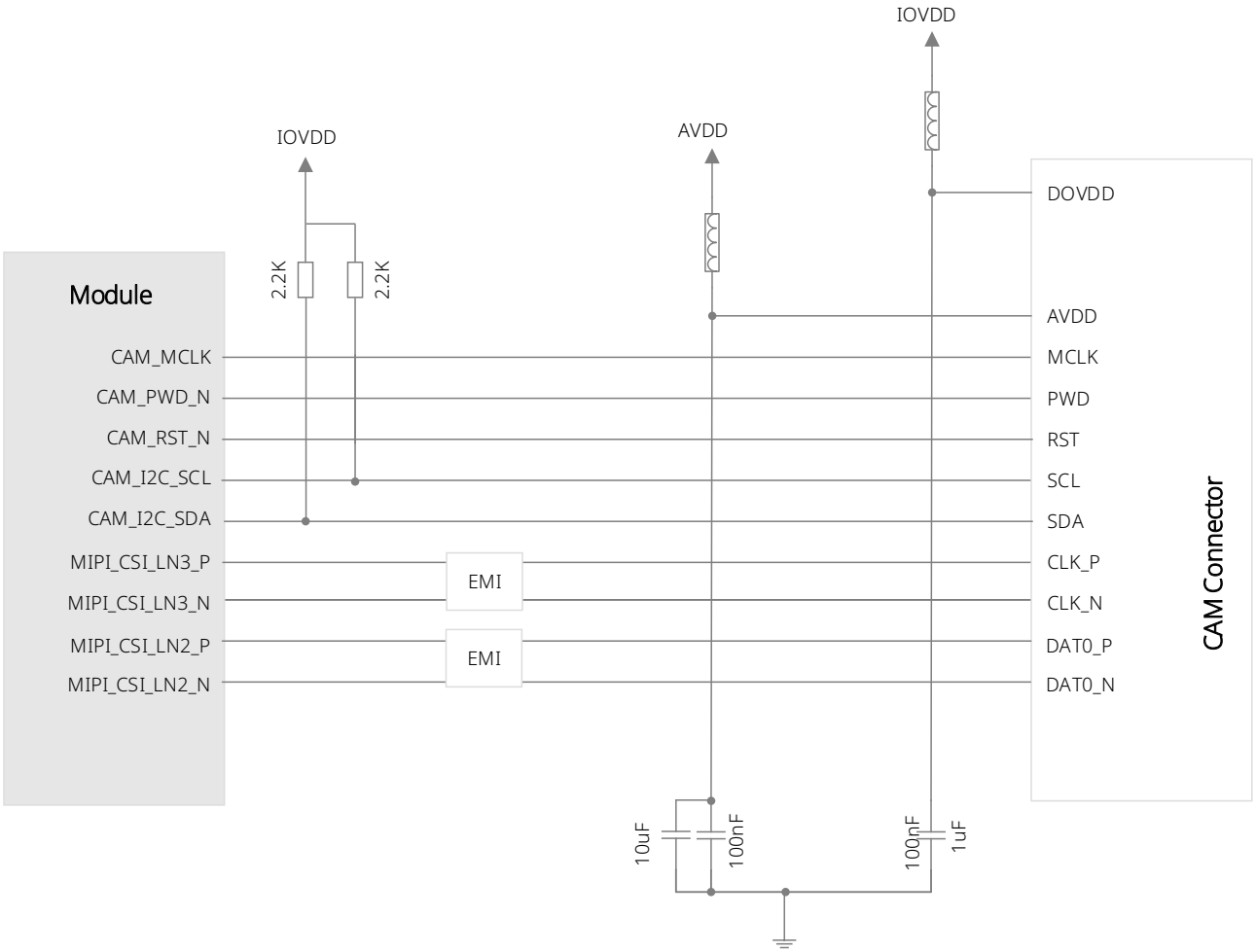

Figure 24. 1 lane camera reference design

3.15.4 Design Considerations

MIPI_CSI is a high-speed signal line. Pay attention to the following points during PCB layout.

- MIPI is a high-speed signal line. It is recommended to connect the common mode inductor in series near the camera connector to reduce the EMI (electromagnetic interference) of the circuit;
- MIPI routing is recommended to be designed in the inner layer, and connected using GND in three dimensions;
- The MIPI signal line needs to be controlled with a 100 Ω differential impedance with

tolerance ±10%;

- The total length of the cable shall not exceed 300 mm;
- The intra lane match of MIPI signal cable must be controlled within 0.67 mm;
- The inter lane match of MIPI signal cable must be controlled within 1.3 mm;
- It is recommended that the space of intra-lane differential line should be 1 times of the route width and the space between differential line and other routes should be controlled 2.5 times of the route width ;
- When one 4 lane CSI are divided to 2 lane+1 lane, only MIPI_CSI 3_DP/M can be used as MIPI_CLK_P/M;

Design considerations for other signal cable:

- CAM_MCLK is a high-speed clock signal cable and requires fully grounded.
- The camera AVDD power supply routing should be away from interference sources to avoid interference of power noise;
- It is recommended to add LDO with high PSRR ability to the camera AVDD power supply;
- VDD_1V2 should be provided by external high-power noise reduction ratio LDO.
- If you need both two cameras to work at the same time, don't choose to share I2C. If you need to share I2C, confirm that the I2C addresses of the two cameras are unique.

3.16 Audio

3.16.1 Definition of Audio Interface

The module supports analog audio interface, and has 3 inputs and 3 outputs. The pin definition please refer to Pin description:

Audio interface design consideration:

- Internal MIC_BIAS pull-up, so that you do not need to add it;

- The reference ground of the headphone should be grounded near the connector;
- Differential speaker interface cannot connect to external PA. If necessary, use the headphone interface;
- It is recommended to use receiver with 32 Ω impedance;
- Reduce noise and improve audio quality, the following approaches are recommended:
  - Keep audio PCB routing away from the antenna and high-frequency digital signal;
  - Reserve LC filter circuit in audio circuit to reduce EMI;
  - Shield the audio routing.

3.16.2 Speaker

One class-D mono differential loud speaker driver. The reference design is as follows:

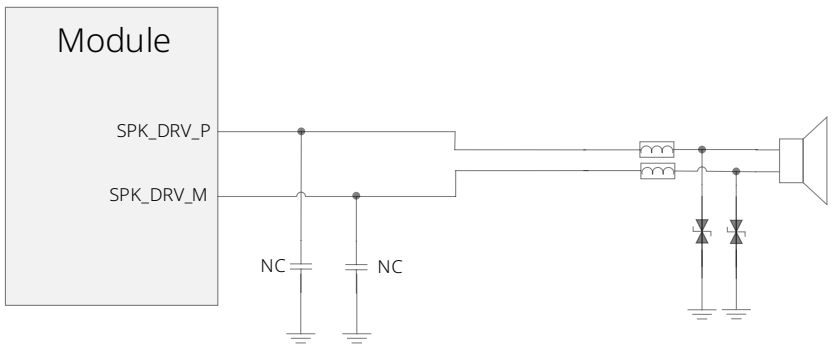

Figure 25. Speaker reference design

3.16.3 MIC

Three MIC input, Internal MIC_BIAS pull-up. It is recommended to use a silicon MIC, and the reference design is as follows:

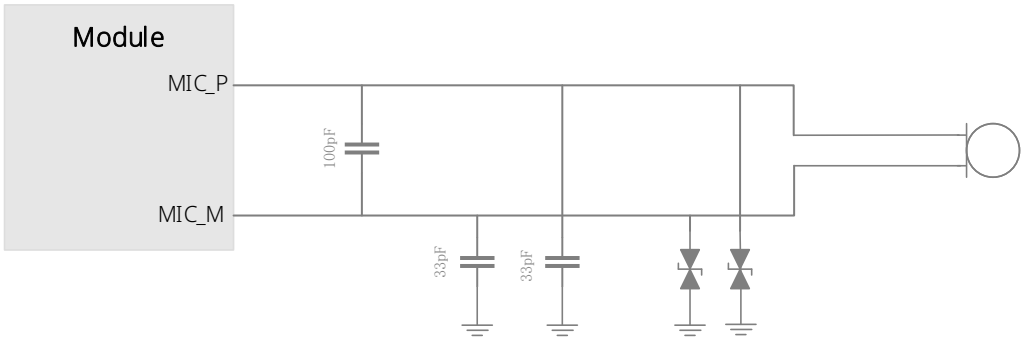

Figure 26. Microphone reference design

3.16.4 Receiver

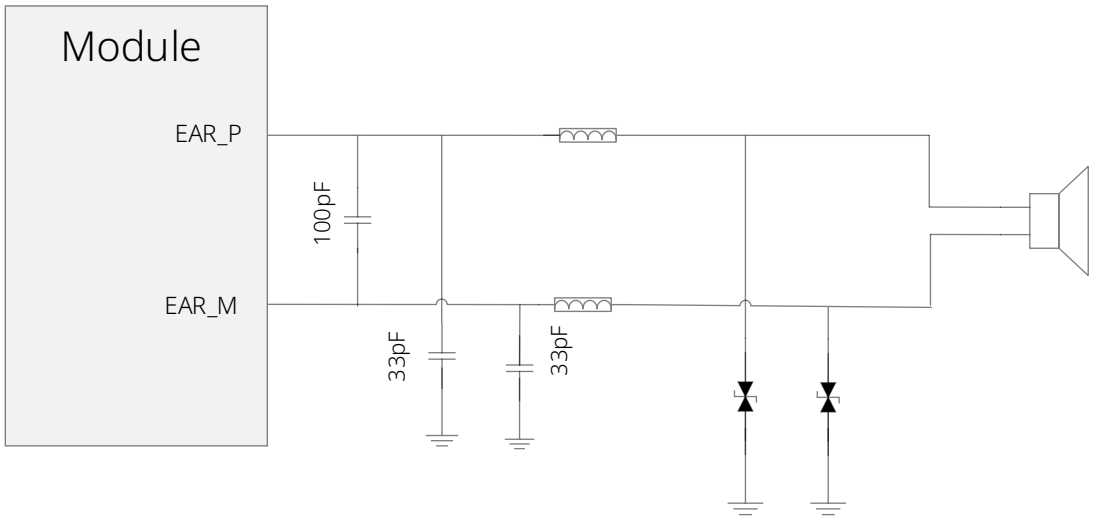

Figure 27. Receiver reference design

3.16.5 Headset

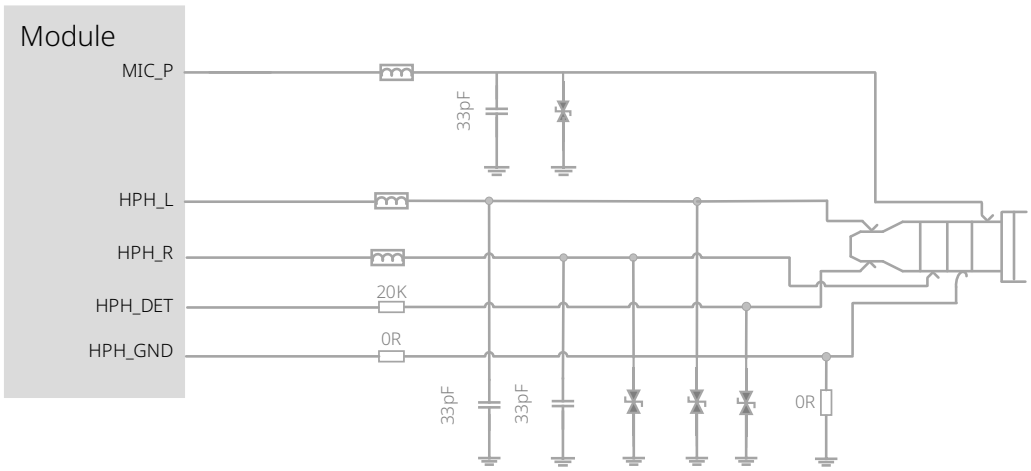

Figure 28. Headset reference design

Use a bi-directional TVS tube for the ESD protection device of the headphone interface.

3.17 Forced Download Interface

The module provides an emergency download interface. Connect the FORCE_USB_BOOT pin with VREG_L13A pin when powering on, and the module can enter the emergency download mode, which is used for the final processing mode when the product fails to power on or run normally. To facilitate the subsequent software upgrade and product debugging, please reserve this pin. The reference design is as follows:

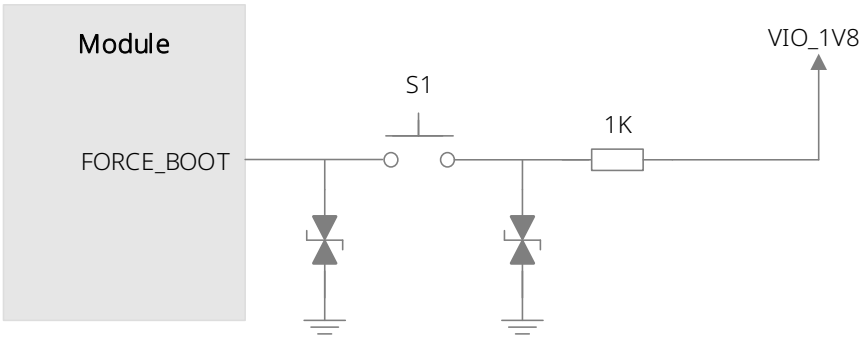

Figure 29. forced download reference design

3.18 RGB Interface

Three brightness control of red, green, and blue channels 8 mA max per channel. The reference design is as follows.

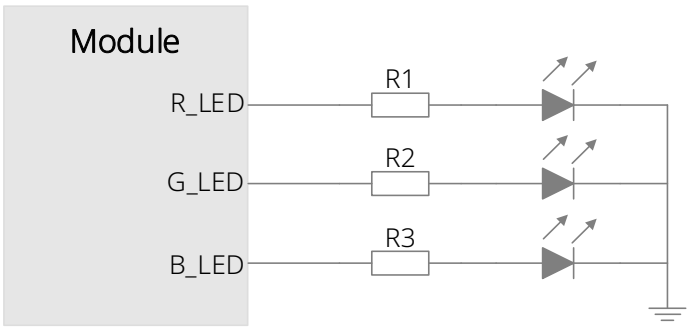

Figure 30. RGB reference design

4 Antenna Interface

The module supports 2G/3G/4G main antenna/diversity reception antenna, WIFI/BT antenna and GNSS antenna.

4.1 MAIN/DRX Antenna

The module provides two 2G/3G/4G antenna interfaces. The ANT_MAIN is used to receive and transmit RF signal, and the ANT_DRX is used for diversity reception.

4.1.1 Operating Bands

Table 2.SC218-NA operating band

Mode	Band	TX（MHz）	RX（MHz）
LTE FDD	Band 2	1850-1910	1930-1990
	Band 4	1710-1754	2110-2155
	Band 5	824-849	869-894
	Band 7	2500-2570	2620-2699
	Band 12	698-716	728-746
	Band 13	777-787	746-756
	Band 17	704-716	734-746
	Band 25	1850-1915	1930-1995
	Band 26	814-850	859-894
	Band 66	1710-1780	2110-2180
	Band 71	663-698	617-652

Mode	Band	TX（MHz）	RX（MHz）
LTE TDD	Band 41	2496-2690	2496-2690

Table 17.SC218-EAU operating band

Mode	Band	TX (MHz)	RX (MHz)
GSM	850	824-849	869-894
	900	880-915	925-960
	1800	1710-1785	1805-1880
	1900	850-1910	1930-1990
WCDMA	Band 1	1920-1980	2110-2170
	Band 2	1850-1910	1930-1990
	Band 5	824-849	869-894
	Band 8	880-915	925-960
LTE FDD	Band 1	1920-1980	2110-2170
	Band 2	1850-1910	1930-1990
	Band 3	1710-1785	1805-1880
	Band 4	1710-1755	2110-2155
	Band 5	824-849	869-894
	Band 7	2500-2570	2620-2690
	Band 8	880-915	925-960
	Band 20	832-862	791-821
	Band 28	703-748	758-803

Mode	Band	TX (MHz)	RX (MHz)
LTE TDD	Band 38	2570-2620	2570-2620
	Band 40	2300-2400	2300-2400
	Band 41	2535-2655	2535-2655

Table 18.SC218-JP operating band

Mode	Band	TX（MHz）	RX（MHz）
WCDMA	Band 1	1920-1980	2110-2170
	Band 6	832-838	877-883
	Band 8	880-915	925-960
	Band 9	1752-1783	1847-1875
	Band 19	832-843	877-888
LTE FDD	Band 1	1920-1980	2110-2170
	Band 3	1710-1785	1805-1880
	Band 8	880-915	925-960
	Band 18	815-830	860-875
	Band 19	830-845	875-890
	Band 26	814-850	859-894
	Band 28	703-748	758-803
LTE TDD	Band 41	2535-2655	2525-2655

4.1.2 Circuit Reference Design

For use of the module, the antenna pin and the RF connector or antenna feed point on the main board should be connected via an RF route. A microstrip is recommended as the RF cable, the insertion loss must be within 0.2 dB, and the impedance must be 50 Ω. A π-type circuit is reserved between the module and the antenna connector (or feed point) for antenna debugging. Two parallel devices are directly connected across the RF route without branch pulled out. It is recommended to reserve the TVS device welding position at the antenna interface. The reference circuit is shown below:

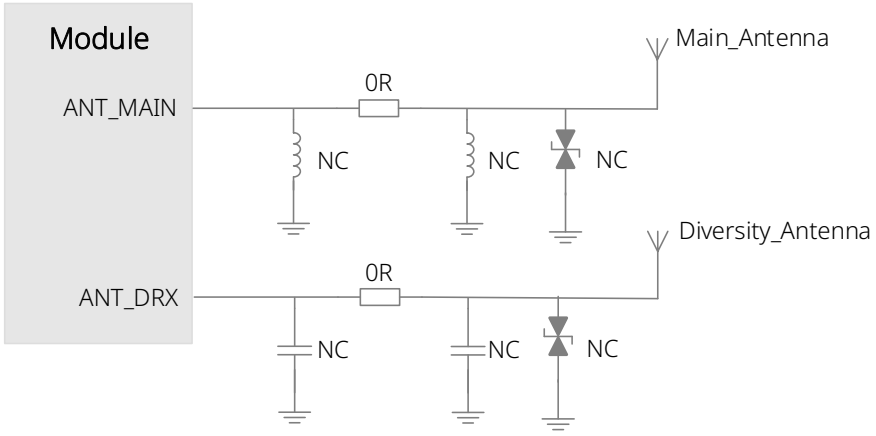

Figure 31. Antenna reference circuit

4.2 WIFI/BT Antenna

Microstrip route is recommended for the WIFI/BT RF route, with insertion loss within 0.2dB and impedance at 50Ω.

4.2.1 Operating Bands

Table 19.Operating band

Mode	Frequency	Unit
WIFI	2402 - 2482	MHz

Mode	Frequency	Unit
	5170 - 5835	MHz
BT	2402 - 2480	MHz

4.2.2 Circuit Reference Design

The reference circuit of WIFI/BT antenna is shown as follows:

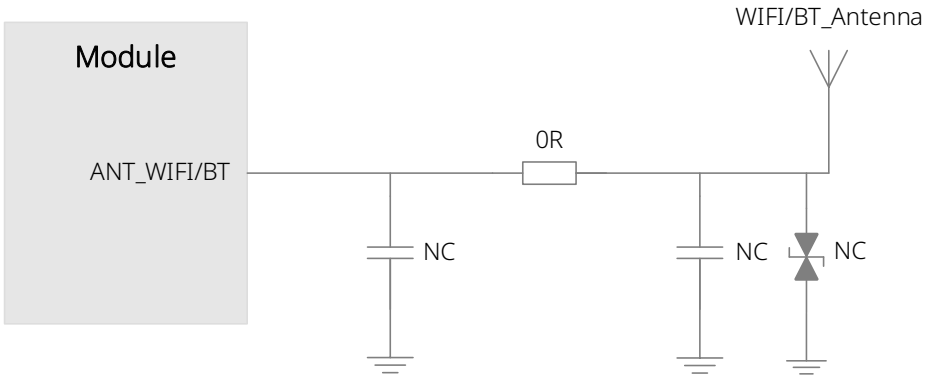

Figure 32. Antenna reference design

4.3 GNSS Antenna

GNSS supports GPS, GLONASS, and BeiDou.

4.3.1 GNSS Operating Frequency

Table 20.GNSS operating frequency

Mode	Frequency	Unit
GPS	1575.42±1.023	MHz
GLONASS	1597.42 - 1605.8	MHz
BeiDou	1561.098±2.046	MHz

4.3.2 Antenna Reference Design

The module has a built-in LNA. The passive antenna is used in the design of the device. Microstrip route is recommended for the GNSS RF route, with insertion loss within 0.2dB and impedance at 50Ω. The GNSS antenna reference design is shown as follows:

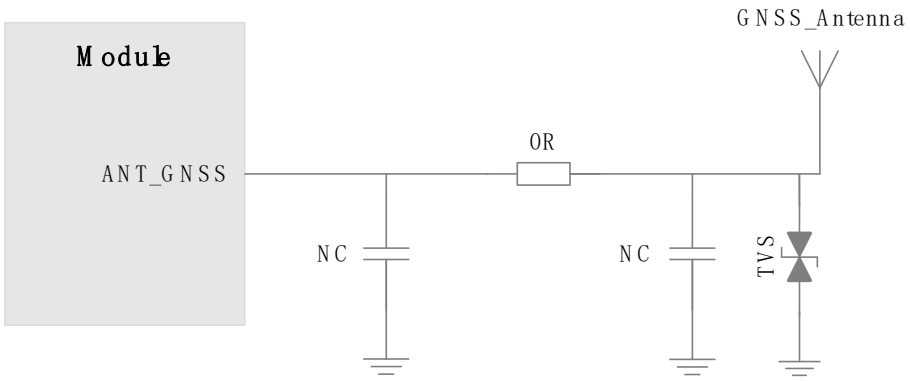

Figure 33. GNSS passive antenna reference design

For passive antenna, it is recommended to add a TVS with a junction capacitance of no more than 0.5 pF; CJ: 0.5 pF; clamping voltage: 5.0 V. Recommended unit: ESD9D5U.

The active antenna reference circuit is shown in the following figure:

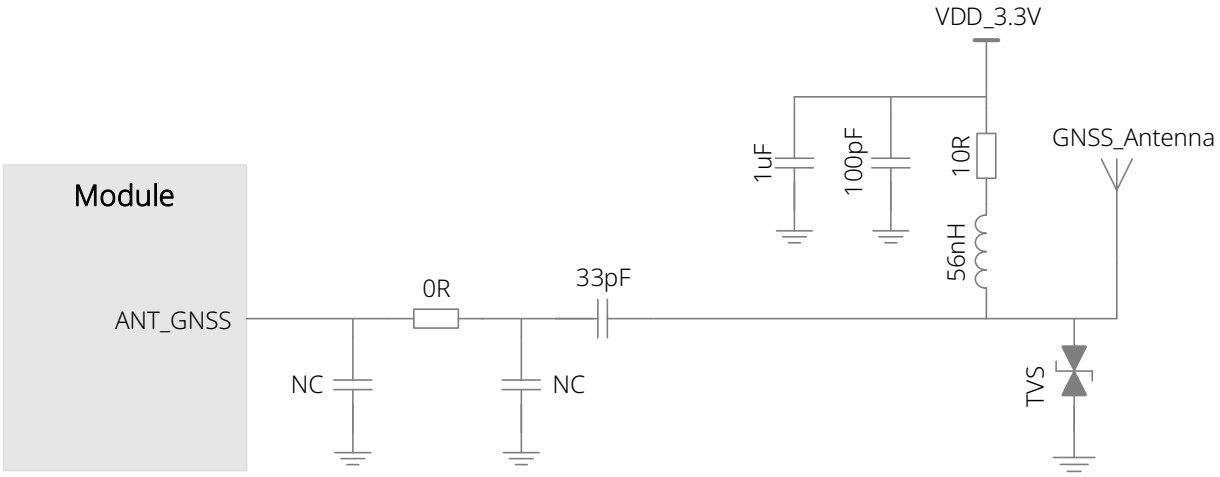

Figure 34. GNSS active antenna connection

The power of the active antenna is fed from the antenna's signal line through a 56 nH inductor. Common active antennas supply power is from 3.3-5.0 V. The active antenna itself consumes very little power, but requires a stable and clean power supply. It is recommended that a high-PSRR LDO be used to power the antenna. The gain of the active antenna is required to be <17db. If the gain is >17db, the reserved π-type matching must be used to increase the attenuation network.

4.4 Antenna Requirements

The module provides four antenna interfaces: main, diversity, WIFI/BT and GNSS. The antenna requirements are as follows:

Table 21. Antenna requirements

Module Antenna Requirement	
Standard	Antenna Requirement
LTE	VSWR: <2 (typical) Gain (dBi): 1 Max input power (W): 5 Input impedance (Ω): 50 Polarization type: vertical direction Insertion loss: <1dB (0.7-1 GHz) Insertion loss: <1.5dB (1.4-2.2 GHz) Insertion loss: <2dB (2.3-2.7 GHz)
WIFI/BT	VSWR: ≤ 2 Gain (dBi): 1 Max input power (W): 5 Input impedance (Ω): 50

Module Antenna Requirement	
	Polarization type: vertical direction Insertion loss: < 1 dB
GNSS	Frequency range: 1559 MHz to 1607 MHz Polarization type: right-circular or linear polarization VSWR: < 2 (typical) Passive antenna gain: > 0 dBi Active antenna NF: < 1.5 dB (typical) Active antenna gain: > -2 dBi
Isolation between GPS and main antenna	> 20 dB
Isolation between WIFI and LTE antenna	> 20 dB

5 RF PCB Layout Design Guide

For user PCB, the characteristic impedance of all RF signal routes should be controlled at 50 Ω. In general, the impedance of the RF signal route is determined by the dielectric constant of the material, the route width (W), the ground clearance (S) and the height of the reference ground plane (H). The control of the characteristic impedance of the PCB usually is implemented in two ways: microstrip route and coplanar waveguide. To illustrate the design principles, the following figures show the structural designs of microstrip route and coplanar waveguide when the impedance line is at 50 Ω.

- Microstrip cable complete structure

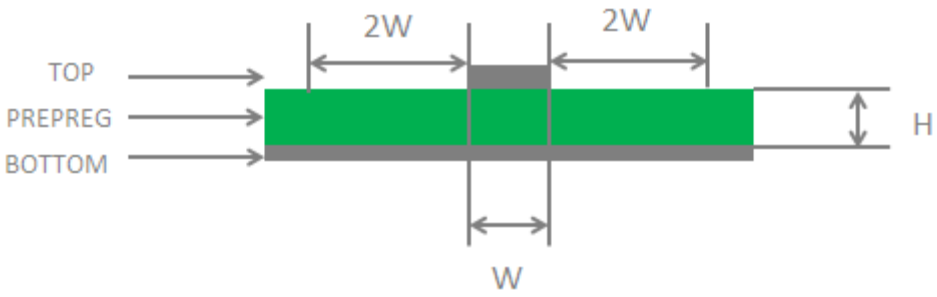

Figure 35.Two-layer PCB microstrip line structure

- Coplanar waveguide complete structure

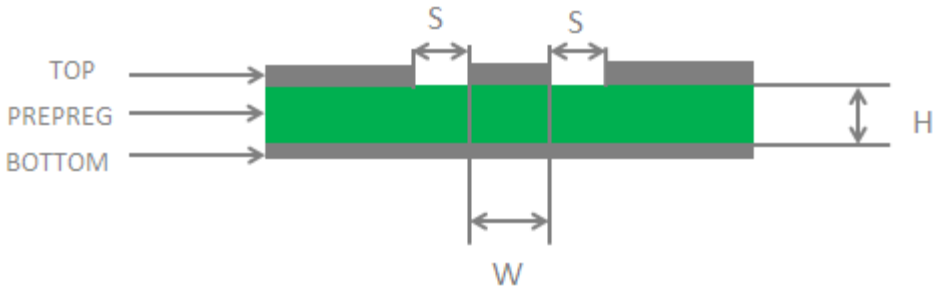

Figure 36.Two-layer PCB coplanar waveguide structure

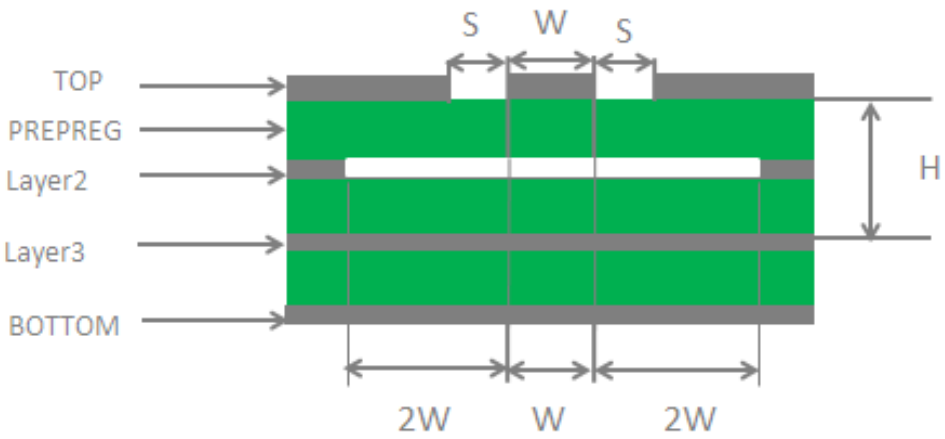

Figure 37. Four-layer PCB coplanar waveguide structure (reference ground layer 3)

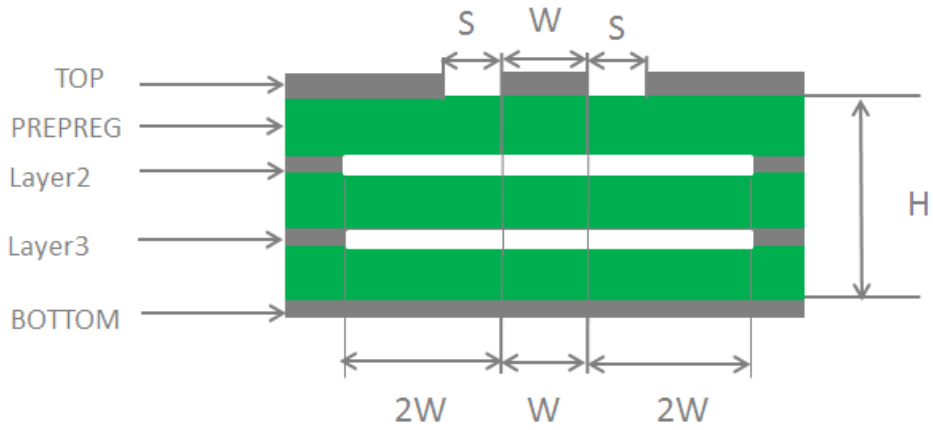

Figure 38. Four-layer PCB coplanar waveguide structure (reference ground layer 4)

In the design of RF antenna interface circuit, in order to ensure good performance and reliability of the RF signal, it is recommended to observe the following principles:

Design principles:

- The impedance simulation tool should be used to accurately control the RF signal line at 50 Ω impedance.
- The GND pin adjacent to the RF pin should not have thermal welding plate and should be in full contact with the ground.

- The distance between the RF pin and the RF connector should be as short as possible. At the same time, avoid the right-angle route. The recommended route angle is 135 degrees.
- When building connector package, keep the signal pin away from the ground.
- The reference ground plane of the RF signal line should be complete; a certain number of ground holes are added around the signal line and the reference ground to help improve the RF performance;
- and the distance between the ground holes and the signal line should be at least 2 times of the line width (2*W).

6 WIFI and Bluetooth

6.1 WIFI Overview

The module supports 2.4 G and 5 G WLAN wireless communications and 802.11a, 802.11b, 802.11g, 802.11n, 802.11ac standards, with a maximum rate up to 433 Mbps. Its characteristics are as follows:

- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode
- Support WAPI
- Support AP mode
- Support Wi-Fi Direct
- Support MCS 0-7 for HT20 and HT40 (If you need to open 2.4 G WIFI 40 M, you need to configure INI file, but it is not recommended)
- Support MCS 0-8 for VHT20
- Support MCS 0-9 for VHT40 and VHT80

6.2 WIFI Performance

Test condition: 3.8V power supply, environment temperature 25°C.

Table 3. WIFI transmitting power

Frequency	Mode	Data Rate	Bandwidth	TX Power (dBm)
2.4G	802.11b	1Mbps	20	16±3
		11Mbps	20	16±3
	802.11g	6Mbps	20	17±3

Frequency	Mode	Data Rate	Bandwidth	TX Power (dBm)
5G		54Mbps	20	13±3
	802.11n	MCS0	20	16±3
		MCS7	20	13±3
		MCS0	40	15±3
		MCS7	40	13±3
	802.11a	6Mbps	20	18±3
		54Mbps	20	15±3
	802.11n	MCS0	20	15±3
		MCS7	20	15±3
		MCS0	40	17±3
		MCS7	40	15±3
	802.11ac	MCS0	20	17±3
		MCS8	20	13±3
		MCS0	40	15±3
		MCS9	40	12±3
		MCS0	80	16±3
		MCS9	80	11±3

Table 23. WIFI receiving sensitivity

Frequency	Mode	Data Rate	Bandwidth (MHz)	Sensitivity (dBm)*
2.4G	802.11b	1 Mbps	20	-91
		11 Mbps	20	-87
		6 Mbps	20	-87

Frequency	Mode	Data Rate	Bandwidth (MHz)	Sensitivity (dBm)*
5G	802.11g	54 Mbps	20	-72
	802.11n	MCS0	20	-88
		MCS7	20	-68
		MCS0	40	-84
		MCS7	40	-64
	802.11a	6 Mbps	20	-90
		54 Mbps	20	-74
	802.11n	MCS0	20	-89
		MCS7	20	-70
		MCS0	40	-84
		MCS7	40	-65
	802.11ac	MCS0	20	-90
		MCS8	20	-67
		MCS0	40	-87
		MCS9	40	-60
		MCS0	80	-83
		MCS9	80	-58

The sensitivity here is a typical value.

6.3 Bluetooth Overview

The module supports BT5.0 (BR/EDR + BLE) standards. The modulation method supports

GFSK, 8-DPSK and π/4-DQPSK.BR/EDR. Channel bandwidth is 1 MHz and can accommodate 79 channels. The BLE channel bandwidth is 2 MHz and can accommodate 40 channels. Its main features are as follows:

- BT 5.0 + BR/EDR + BLE
- Support for ANT protocol
- Support for BT-WLAN coexistence operation, including optional concurrent receive
- Up to 3.5 piconets (master, slave and page scanning)

Table 4. BT rate and version information

Version	Data Rate	Throughput	Note
BT1.2	1 Mbit/s	> 80 Kbit/s	--
BT2.0 + EDR	3 Mbit/s	> 80 Kbit/s	--
BT3.0 + HS	24 Mbit/s	Refer to 3.0+HS	--
BT4.2 LE	24 Mbit/s	Refer to 4.2 LE	--
BT5.0	24 Mbit/s	Refer to 5.0	--

6.4 Bluetooth Performance

Test condition: 3.8 V power supply, environment temperature 25°C.

Table 25. BT performance indicators

Type	DH-5	2-DH5	3-DH5	BLE	Unit
Transmitting power	10±2.5	10±2.5	10±2.5	1±2.5	dBm
Receiving sensitivity	-88	-86	-84	-92	dBm

7 GNSS

7.1 Overview

The module supports multiple positioning systems including GPS, GLONASS and BeiDou. The module is embedded with LNA which can effectively improve the sensitivity of GNSS.

7.2 GNSS Performance

Test condition: 3.8 V power supply, environment temperature 25°C.

Table 5. GNSS positioning performance

Parameter	Description	Typical Result	Unit
Sensitivity	Acquisition	-145	dBm
	Tracking	-157	dBm
C/No	-130 dBm	39	dB-Hz
TTFF	Cold start	44	s
	Warm start	40	s
	Hot start	2.5	s
CEP	Static accuracy (95% @-130dbm)	5	m

8 Electricity, Reliability and RF Performance

8.1 Recommended Parameters

Table 27.Recommended parameters

Parameter	Min	Normal	Max	Unit
Battery voltage	3.5	3.8	4.4	V
USB_VBUS	4.75	5	5.25	V
RTC voltage	2.45	3.0	3.35	V
Operating temperature	-30	25	75	°C
Storage temperature	-40	25	85	°C

8.2 Power Consumption

Test condition: 3.8 V power supply, environment temperature 25°C.

Table 6. SC218-NA Power consumption

Parameter	Description	Condition	Typical	Unit
I_{off}	Static leakage current	Leakage current before power on	60	uA
	Normal power-off	Power off leakage current	100	
I_{sleep}	Radio off	AT+CFUN=4 airplane Mode	4	mA
	TDD LTE	DPC (Default Paging Cycle)=#256	8	
	FDD LTE	DPC (Default Paging Cycle)=#256	8	
$I_{LTE-RMS}$		Band2@ max power(10MHz,1RB)	700	mA

Parameter	Description	Condition	Typical	Unit
	FDD data RMS current	Band4@ max power(10MHz,1RB)	700	
		Band5@ max power(10MHz,1RB)	720	
		Band7@ max power(10MHz,1RB)	720	
		Band12@ max power(10MHz,1RB)	700	
		Band13@ max power(10MHz,1RB)	700	
		Band17@ max power(10MHz,1RB)	700	
		Band25@ max power(10MHz,1RB)	700	
		Band26@ max power(10MHz,1RB)	700	
		Band66@ max power(10MHz,1RB)	700	
		Band71@ max power(10MHz,1RB)	700	
	TDD data RMS current	Band41@ max power(10MHz,1RB)	430	mA

Table 29. SC218-EAU Power consumption

Parameter	Description	Condition	Typical	Unit
I_{off}	Static leakage current	Leakage current before power on	60	uA
	Normal power-off	Power off leakage current	100	
I_{sleep}	Radio off	AT+CFUN=4 airplane Mode	4	mA
	GSM	MFRMS = 5	7	
	WCDMA	DRX = 8	8	

Parameter	Description	Condition	Typical	Unit
	TDD LTE	DPC (Default Paging Cycle) = #256	8	
	FDD LTE	DPC (Default Paging Cycle) = #256	8	
$I_{GSM-RMS}$	GSM voice RMS current	GSM850 @ PCL=5	270	mA
		GSM850 @ PCL=19	97	
		EGSM900 @ PCL=5	270	
		EGSM900 @ PCL=19	97	
		DCS1800 @ PCL=0	210	
		DCS1800 @ PCL=15	90	
		PCS1900 @ PCL=0	210	
		PCS1900 @ PCL=15	90	
$I_{GSM-MAX}$	GSM voice peak current	GSM850 @ PCL=5	270	mA
		EGSM900 @ PCL=5	270	
		DCS1800 @ PCL=0	210	
		DCS1900 @ PCL=0	210	
$I_{GPRS-RMS}$	GPRS data RMS current	GSM850@ Gamma=3 (1UL/4DL)	246	
		GSM850@ Gamma=3 (4UL/1DL)	640	
		EGSM900@ Gamma=3 (1UL/4DL)	245	
		EGSM900@ Gamma=3 (4UL/1DL)	631	

Parameter	Description	Condition	Typical	Unit
		DCS1800@ Gamma=3 (1UL/4DL)	190	
		DCS1800@ Gamma=3 (4UL/1DL)	500	
		PCS1900@ Gamma=3 (1UL/4DL)	170	
		PCS1900@ Gamma=3 (4UL/1DL)	500	
$I_{EGPRS-RMS}$	EGPRS data RMS current	GSM850@ Gamma=6 (1UL/4DL)	180	mA
		GSM850@ Gamma=6 (4UL/1DL)	446	
		EGSM900@ Gamma=6 (1UL/4DL)	180	
		EGSM900@ Gamma=6 (4UL/1DL)	430	
		DCS1800@ Gamma=5 (1UL/4DL)	170	
		DCS1800@ Gamma=5 (4UL/1DL)	500	
		PCS1900@ Gamma=5 (1UL/4DL)	200	
		PCS1900@ Gamma=5 (4UL/1DL)	510	
$I_{WCDMA-RMS}$	WCDMA	Band1@ max power	700	mA

Parameter	Description	Condition	Typical	Unit
$I_{LTE-RMS}$	RMS current	Band2@ max power	700	mA
		Band5@ max power	700	
		Band8@ max power	700	
	FDD data RMS current	Band1@max power (10MHz, 1RB)	700	
		Band2@max power (10MHz, 1RB)	700	
		Band3@max power (10MHz, 1RB)	700	
		Band4@max power (10MHz, 1RB)	725	
		Band5@max power (10MHz, 1RB)	700	
		Band7@max power (10MHz, 1RB)	770	
		Band8@ max power (10MHz,1RB)	720	
		Band20@max power (10MHz, 1RB)	700	
		Band28@max power (10MHz, 1RB)	700	
	TDD data RMS current	Band38@ max power (10MHz,1RB)	430	
		Band40@max power (10MHz, 1RB)	430	

Parameter	Description	Condition	Typical	Unit
		Band4@max power (10MHz, 1RB)	430	

Table 30.SC218-JP Power consumption

Parameter	Description	Condition	Typical	Unit
I_{off}	Static leakage current	Leakage current before power on	60	uA
	Normal power-off	Power off leakage current	100	
I_{sleep}	Radio off	AT+CFUN=4 airplane Mode	4	mA
	GSM	MFRMS=5	7	
	WCDMA	DRX=8	8	
	TDD LTE	DPC (Default Paging Cycle)=#256	8	
	FDD LTE	DPC (Default Paging Cycle)=#256	8	
$I_{WCDMA-RMS}$	WCDMA RMS current	Band1@ max power	700	mA
		Band6@ max power	700	
		Band8@ max power	700	
		Band9@ max power	700	
		Band19@ max power	700	
$I_{LTE-RMS}$	FDD data RMS current	Band1@ max power(10MHz,1RB)	700	mA
		Band3@ max power(10MHz,1RB)	700	

Parameter	Description	Condition		Typical	Unit
		Band8@ power(10MHz,1RB)	max	720	
		Band18@ power(10MHz,1RB)	max	720	
		Band19@ power(10MHz,1RB)	max	700	
		Band26@ power(10MHz,1RB)	max	700	
		Band28@ power(10MHz,1RB)	max	720	
	TDD data RMS current	Band41@ power(10MHz,1RB)	max	430	mA

8.3 RF Transmitting Power

The transmit power of each band of the module is shown in the following table:

Test condition: 3.8 V power supply, environment temperature 25°C, LTE power test performed with 12 MHz bandwidth.

Table 31.SC218-NA RF transmitting power

Mode	Band	Max Power(dBm)	Min Power(dBm)
LTE FDD	Band 2	23.0±2	<-39
	Band 4	23.0±2	<-39
	Band 5	23.0±2	<-39
	Band 7	23.0±2	<-39

	Band 12	23.0±2	<-39
	Band 13	23.0±2	<-39
	Band 17	23.0±2	<-39
	Band 25	23.0±2	<-39
	Band 26	23.0±2	<-39
	Band 66	23.0±2	<-39
	Band 71	23.0±2	<-39
LTE TDD	Band 41	23.0±2	<-39

Table 32.SC218-EAU RF transmitting power

Mode	Band	Max Power (dBm)	Min Power (dBm)
GSM	850 (GMSK)	33±2	5±5
	900 (GMSK)	33±2	5±5
	1800 (GMSK)	30±2	0±5
	1900 (GMSK)	30±2	0±5
	850 (8PSK)	27.0±3	5±5
	900 (8PSK)	27.0±3	5±5
	1800 (8PSK)	26.0±3	0±5
	1900 (8PSK)	26.0±3	0±5
WCDMA	Band 1	24+1/-3	<-49
	Band 2	24+1/-3	<-49
	Band 5	24+1/-3	<-49
	Band 8	24+1/-3	<-49

Mode	Band	Max Power (dBm)	Min Power (dBm)
LTE FDD	Band 1	23.0±2	<-39
	Band 2	23.0±2	<-39
	Band 3	23.0±2	<-39
	Band 4	23.0±2	<-39
	Band 5	23.0±2	<-39
	Band 7	23.0±2	<-39
	Band 8	23.0±2	<-39
	Band 20	23.0±2	<-39
	Band 28	23.0±2	<-39
LTE TDD	Band 38	23.0±2	<-39
	Band 40	23.0±2	<-39
	Band 41	23.0±2	<-39

Table 33.SC218-JP RF transmitting power

Mode	Band	Max Power(dBm)	Min Power(dBm)
WCDMA	Band 1	24+1/-3	<-49
	Band 6	24+1/-3	<-49
	Band 8	24+1/-3	<-49
	Band 9	24+1/-3	<-49
	Band 19	24+1/-3	<-49
LTE FDD	Band 1	23.0±2	<-39
	Band 3	23.0±2	<-39
	Band 8	23.0±2	<-39
	Band 18	23.0±2	<-39

Mode	Band	Max Power(dBm)	Min Power(dBm)
	Band 19	23.0±2	<-39
	Band 26	23.0±2	<-39
	Band 28	23.0±2	<-39
LTE TDD	Band 41	23.0±2	<-39

8.4 RF Receiver Sensitivity

The sensitivity of each frequency band of the module is shown in the following table:

Test condition: 3.8 V power supply, environment temperature 25°C, LTE power test performed with 10 MHz bandwidth. For RB configuration, see 3GPP standard.

Table 34.SC218-NA RF receiving sensitivity

Mode	Band	Primary	Diversity	PRX+Div	3GPP Requirement	Unit
LTE FDD	Band 2	-98	-98.5	-101.9	-94.3	dBm
	Band 4	-97	-98	-101.1	-96.3	dBm
	Band 5	-98.5	-99	-102.1	-94.3	dBm
	Band 7	-96	-97	-100.5	-94.3	dBm
	Band 12	-98.5	-99	-101.5	-93.3	dBm
	Band 13	-98.5	-99	-99.4	-93.3	dBm
	Band 17	-98.5	-99	-101.7	-93.3	dBm
	Band 25	-98	-98.5	-101.9	-92.8	dBm
	Band 26	-98.5	-99	-103.3	-93.8	dBm
	Band 66	-97	-98	-100.3	-95.8	dBm
	Band 71	-99	-98.8	-101.3	-93.5	dBm

LTE TDD	Band 41	-96.5	-97	-98.6	-94.3	dBm

Table 35.SC218-EAU RF receiving sensitivity

Mode	Band	Primary	Diversity	PRX + Div	3GPP Requirement	Unit
GSM	850	-109	-	-	-102	dBm
	900	-110	-	-	-102	dBm
	1800	-109	-	-	-102	dBm
	1900	-108	-	-	-102	dBm
WCDMA	Band 1	-109.5	-	-	-106.7	dBm
	Band 2	-109.5	-	-	-104.7	dBm
	Band 3	-109.5	-	-	-103.7	dBm
	Band 5	-110	-	-	-104.7	dBm
	Band 8	-110	-	-	-103.7	dBm
LTE FDD	Band 1	-97.3	-98.3	-100.3	-96.3	dBm
	Band 2	-97	-98.5	-100	-94.3	dBm
	Band 3	-97.5	-98	-100	-93.3	dBm
	Band 4	-97	-98	-100	-96.3	dBm
	Band 5	-98	-99	-100.5	-94.3	dBm
	Band 7	-96	-97	-100	-94.3	dBm
	Band 8	-99.3	-99.5	-102.3	-93.3	dBm
	Band 20	-97.5	-98	-100	-93.3	dBm
	Band 28A	-97	-98	-100	-94.8	dBm

Mode	Band	Primary	Diversity	PRX + Div	3GPP Requirement	Unit
	Band 28B	-97	-97	-99.5	-94.8	dBm
LTE TDD	Band 38	-96.3	-96.3	-98	-96.3	dBm
	Band 40	-96.3	-96.3	-99	-96.3	dBm
	Band 41	-94.5	-95	-97.5	-94.3	dBm

Table 36. SC218-JP RF receiving sensitivity

Mode	Band	Primary	Diversity	PRX + Div	3GPP Requirement	Unit
WCDMA	Band 1	-109.5	-	-	-106.7	dBm
	Band 6	-109.5	-	-	-104.7	dBm
	Band 8	-108.5	-	-	-103.7	dBm
	Band 9	-109.5	-	-	-104.7	dBm
	Band 19	-109.5	-	-	-106.7	dBm
LTE FDD	Band 1	-97.3	-98.3	-100.3	-96.3	dBm
	Band 3	-97.5	-98	-100	-93.3	dBm
	Band 8	-99.3	-99.5	-102.3	-93.3	dBm
	Band 18	-97.5	-98.5	-100	-93.3	dBm
	Band 19	-97.5	-98.5	-100	-93.3	dBm
	Band 16	-97.5	-98.5	-100	-93.3	dBm
	Band 28A	-97	-98	-100	-94.8	dBm
	Band 28B	-97	-97	-99.5	-94.8	dBm
LTE TDD	Band 41	-94.5	-95	-97.5	-94.3	dBm

8.5 Electrostatic Protection

In the application of the module, static electricity generated by human body and static electricity generated by friction between micro-electronics are discharged to the module through various channels and may cause damage to the module. Therefore, ESD protection should be taken seriously. In the process of R&D, production assembly and testing, especially in product design, ESD protection measures should be taken. For example, ESD protection should be added at the designed circuit interfaces and at the points susceptible to electrostatic discharge or impact. Anti-static gloves should be worn during production.

The following table lists ESD performance parameters (Temperature: 25°C, Humidity: 30%–60%):

Table 37.ESD performance

Test Point	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna Interface	±5	±10	kV
Other interfaces	±0.5	±1	kV

9 Structure Specifications

9.1 Product Appearance

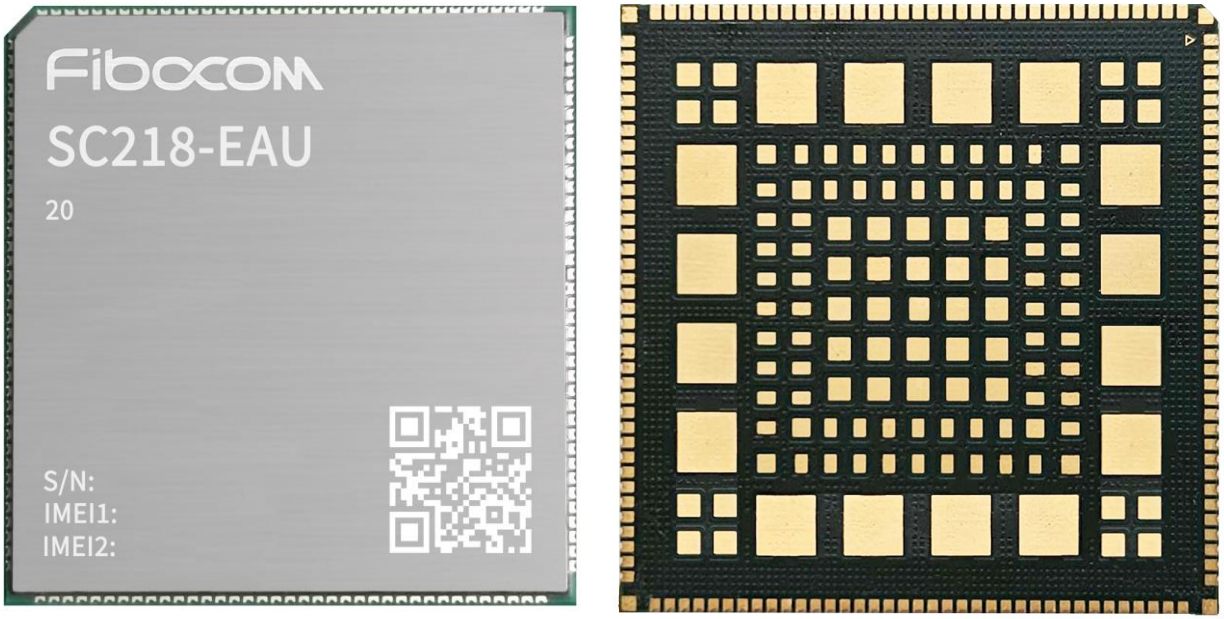

Figure 39.Product appearance

9.2 Structural Dimensions

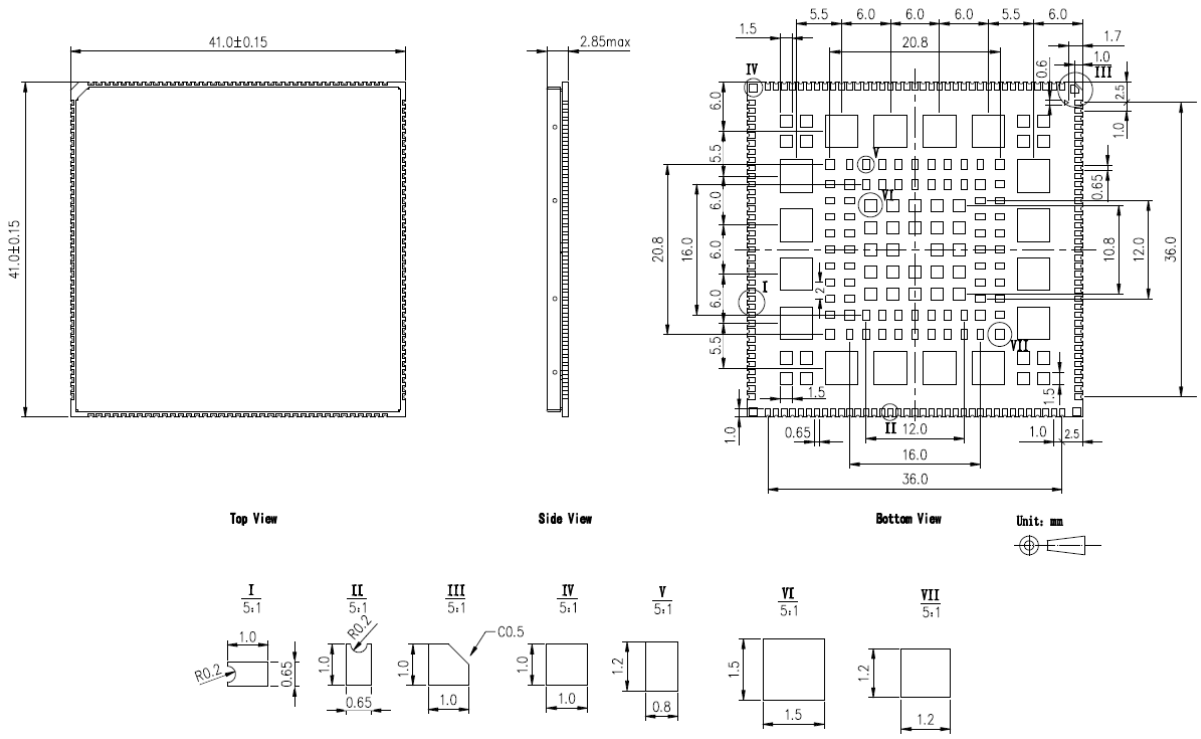

Figure 40.Structural dimensions

9.3 Recommended PCB Soldering Pad Design

For PCB soldering pad and stencil design, please refer to *Fibocom_SC218_SMT Design Guide*.

9.4 Recommended Thermal Design

For recommended module and peripheral thermal design, see *Fibocom_SC218_Thermal Design Guide*.

10 Production and Storage

10.1 SMT

Refer to *Fibocom_SC218_SMT Design Guide_V1.0*.

10.2 Packaging and Storage

Refer to *Fibocom_SC218_SMT Design Guide_V1.0*.

Appendix A Acronyms and Abbreviations

Table 38.Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
bps	Bits Per Second
CS	Coding Scheme
DRX	Discontinuous Reception
FDD	Frequency Division Duplexing
GMSK	Gaussian Minimum Shift Keying
HSDPA	High Speed Down Link Packet Access
IMEI	International Mobile Equipment Identity
Imax	Maximum Load Current
LED	Light Emitting Diode
LSB	Least Significant Bit
LTE	Long Term Evolution
ME	Mobile Equipment
MS	Mobile Station
MT	Mobile Terminated
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation

Abbreviation	Description
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
RMS	Root Mean Square
RTC	Real Time Clock
Rx	Receive
SMS	Short Message Service
TDMA	Time Division Multiple Access
TE	Terminal Equipment
TX	Transmitting Direction
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
USSD	Unstructured Supplementary Service Data
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
VIHmax	Maximum Input High Level Voltage Value
VIHmin	Minimum Input High Level Voltage Value
VILmax	Maximum Input Low Level Voltage Value

Abbreviation	Description
VILmin	Minimum Input Low Level Voltage Value
VImax	Absolute Maximum Input Voltage Value
VImin	Absolute Minimum Input Voltage Value
VOHmax	Maximum Output High Level Voltage Value
VOHmin	Minimum Output High Level Voltage Value
VOLmax	Maximum Output Low Level Voltage Value
VOLmin	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

Appendix B GPRS Encoding Scheme

Table 39. GPRS encoding scheme

Encoding Method	CS-1	CS-2	CS-3	CS-4
Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl. USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

Appendix C GPRS Multi-timeslot

In the GPRS standard, 29 types of GPRS multi-timeslot modes are defined for mobile stations. The multi-timeslot class defines the maximum uplink and downlink rates, represented by 3+1 or 2+2. The first number represents the number of downlink timeslots and the second number represents the number of uplink timeslots. Active timeslot represents the total number of timeslots that the GPRS device can use for both uplink and downlink communications at the same time.

Table 40. Multislot allocation of different classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
33	5	4	6

Appendix D EDGE Modulation and Encoding Method

Table 7. EDGE modulation and encoding method.

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1	GMSK	/	9.05kbit/s	18.1kbit/s	36.2kbit/s
CS-2	GMSK	/	13.4kbit/s	26.8kbit/s	53.6kbit/s
CS-3	GMSK	/	15.6kbit/s	31.2kbit/s	62.4kbit/s
CS-4	GMSK	/	21.4kbit/s	42.8kbit/s	85.6kbit/s
MCS-1	GMSK	C	8.80kbit/s	17.6kbit/s	35.2kbit/s
MCS-2	GMSK	B	11.2kbit/s	22.4kbit/s	44.8kbit/s
MCS-3	GMSK	A	14.8kbit/s	29.6kbit/s	59.2kbit/s
MCS-4	GMSK	C	17.6kbit/s	35.2kbit/s	70.4kbit/s
MCS-5	8-PSK	B	22.4kbit/s	44.8kbit/s	89.6kbit/s
MCS-6	8-PSK	A	29.6kbit/s	59.2kbit/s	118.4kbit/s
MCS-7	8-PSK	B	44.8kbit/s	89.6kbit/s	179.2kbit/s
MCS-8	8-PSK	A	54.4kbit/s	108.8kbit/s	217.6kbit/s
MCS-9	8-PSK	A	59.2kbit/s	118.4kbit/s	236.8kbit/s

OEM/Integrators Installation Manual

Important Notice to OEM integrators 1. This module is limited to OEM installation ONLY. 2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b). 3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations 4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting, and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Fibocom that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: ZMOSC218NA” “Contains IC: 21374-SC218NA”. The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90, part 96 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Industry Canada Statement

This device complies with Industry Canada’s licence-exempt RSSs. Operation is subject to the following two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body

Déclaration d'exposition aux radiations:
Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna. As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed
3) Note: When B48 using these max tune up power, the host manufacturer should reduce the antenna gain to meet the FCC maximum EIRP limit.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions cannot be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 21374-SC218NA”.

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 21374-SC218NA ".

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.