PERFECT WIRELESS EXPERIENCE

SC208-GL Hardware Guide

V1.1

Contents

Applicable Models

No.	Applicable Model	Description
1	SC208-GL-20	4GB+64GB memory, suitable for Global
2	SC208-GL-50	6GB+128GB memory, suitable for Global

Change History

V1.1 (2024-07-02)	Fixed some network names to be consistent with the hardware resource list; Change PIN221 PM4250 GPIO 1 to NC, Cannot be used, RESERVED; Added support for SC208-GL-50 models; WCDMA B3 is no longer supported; Adjust WIFI/BT power, WCDMA/LTE power consumption, sensitivity;
V1.0 (2024-05-31)	Initial version.

1 Foreword

1.1 Description

This document describes the electrical characteristics, RF performance, structure size, application environment, etc. of the SC208-GL module. With the assistance of the document and other instructions, the developers can quickly understand the hardware functions of the module and develop products.

1.2 Reference Standards

This product is designed with reference to the following standards:

- 3GPP TS 51.010-1 V10.5.0：Mobile Station（MS）conformance specification; Part 1： Conformance specification
- 3GPP TS 34.121-1 V10.8.0：User Equipment（UE）conformance specification; Radio transmission and reception（FDD）;Part 1：Conformance specification
- 3GPP TS 34.122 V10.1.0：Technical Specification Group Radio Access Network; Radio transmission and reception（TDD）
- 3GPP TS 36.521-1 V15.0.0：User Equipment（UE） conformance specification; Radio transmission and reception; Part 1：Conformance testing
- 3GPP TS 38.300 V15.5.0 ：3rd Generation Partnership Project; Technical Specification Group Radio Access Network; NR; NR and NG-RAN Overall Description; Stage 2
- 3GPP TS 38.521-1 V15.2.0 ： User Equipment（UE） conformance specification; Radio transmission and reception; Part 1： Range 1 Standalone;
- 3GPP TS 38.521-3 V15.2.0：User Equipment（UE） conformance specification; Radio transmission and reception; Part 3：Range 1 and Range 2 Interworking operation with other radios;
- IEEE 802.11n WLAN MAC and PHY, October 2009+ IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- IEEE Std 802.11b, IEEE Std 802.11a, IEEE Std 802.11g, IEEE Std 802.11n, IEEE Std 802.11ac, IEEE Std 802.11ax；
- IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0+EDR/2.1/2.1+EDR/3.0/3.0+HS, August 6, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.2.0, November 7, 2014
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/5.0.2, December 07,2017
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/5.1.1, August 07,2019
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/5.2
- 3GPP TS 36.124V10.3.0：Electro Magnetic Compatibility（EMC）requirements for mobile terminals and ancillary equipment
- 3GPP TS 21.111 V10.0.0：USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0：Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V10.11.0：Characteristics of the Universal Subscriber Identity Module (USIM) application

- 3GPP TS 31.11 V10.16.0：Universal Subscriber Identity Module (USIM) Application Toolkit (USAT)
- 3GPP TS 27.007 V10.0.8：AT command set for User Equipment (UE)
- 3GPPTS27.005 V10.0.1：Use of Data Terminal Equipment -Data Circuit terminating Equipment (DTE – DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
- PCI_Express_M.2_Specification_Rev1.1_TS_12092016_NCB
- Universal Serial Bus Specification 2.0
- Universal Serial Bus Specification 3.0

2 Product Overview

2.1 Product Introduction

The module integrates core components such as Baseband, Memory, PMU, Transceiver, PA; it supports long distance multi-mode communication such as FDD/TDD-LTE, WCDMA, GSM and WIFI/BT short-distance radio transmission technology, as well as GNSS wireless positioning technology. The module is embedded with Android operating system and support various interfaces such as MIPI/USB/UART/SPI/I2C. It is theoptimal solution for the core system of wireless smart products. Its correspondingnetwork modes and frequency bands are as follows:

Table 1. Introduction to bands of SC208-GL

Mode	Band
GSM/GPRS/EDGE	GSM850/EGSM900/PCS1900/DCS1800
WCDMA	Band 1/2/4/5/6/8/9/19
FDD-LTE	Band 1/2/3/4/5/7/8/12/13/17/18/19/20/25/26/28/66/71
TDD-LTE	Band 34/38/39/40/41
WIFI802.11a/b/g/n/ac	2402MHz~2482MHz 5170MHz~5835MHz
BT5.0	2402MHz~2480MHz
GNSS	GPS/Beidou/GLONASS/Galileo/QZSS

2.2 Key Features

Table 2. Key features

Feature	Description
Product Marketing Name	LTE Module
Power Supply	DC: 3.5–4.35V, typical: 3.8 V
Application processor	A customized 64□bit Arm v-8.0 compliant applications processor Kryo Gold: quad high-performance cores Kryo Silver: quad low-power cores
Memory	4GB + 64GB 6GB + 128GB
Power class	Class 4 (33dBm±2dB) for GSM850/900

	Class 1 (30dBm±2dB) for DCS1800/1900 Class E2 (27dBm±3dB) for GSM850/900 8-PSK Class E2 (26dBm+3/-4dB) for DCS1800/1900 8-PSK Class 3 (24dBm+1/-3dB) for WCDMA bands Class 3 (23dBm±2dB) for LTE FDD bands Class 3 (23dBm±2dB) for LTE TDD bands
WCDMA features	Support 3GPP R8 DC-HSPA+ Support 16-QAM, 64-QAM and QPSK modulation CAT6 HSUPA: Maximum uplink rate 5.76Mbps CAT24 HSDPA: Maximum downlink rate 42Mbps
LTE features	Supports FDD/TDD R10 Supports FDD/TDD cat4 16 QAM for UL, 64 QAM for DL Supports DL 2x2 MIMO FDD maximum uplink speed 50Mbps, maximum downlink speed 150Mbps TDD maximum uplink speed 30Mbps, maximum downlink speed 130Mbps
WLAN features	Support 2.4G and 5G WLAN wireless communication. Support 802.11a, 802.11b, 802.11g, 802.11n, 802.11ac. Maximum rate up to 433Mbps
Bluetooth features	BT5.0
Satellite positioning	GPS/GLONASS/BeiDou/Galileo/QZSS
SMS	Text and PDU modes Point-to-Point MO and MT SMS cell broadcast SMS storage: stored in the module by default
LCD interface	One 4-Lane MIPI_DSI D-PHY 1.2 interface Maximum rate 1.5Gbps/lane
Camera interface	Three 4-Lane MIPI_CSI D-PHY 1.2 interfaces Maximum rate 2.5Gbps/lane, configurable as 4+4+2+1 or 4+4+4

Audio interface	Analog audio input: 3 sets of analog microphone inputs with internal bias integration. Analog audio output: a set of differential earpiece outputs A set of stereo headphone outputs A set of differential Lineout outputs that require external audio PA
USB interface	One USB interface USB conforms to the 3.1 Gen 1 specification and is downward compatible with USB2.0. It can be used for data transmission and software debugging.
(U)SIM interface	Two (U)SIM card interfaces supporting 1.8V or 2.95V (U)SIM card adaptation Support dual (U)SIM dual standby single pass, support hot plug
UART interface	Two UART serial interfaces, with the maximum rate up to 4Mbps. A set of debugging UART serial ports A set of four-wire serial ports supporting RTS and CTS hardware flow control
SD interface	Support 4-bit SD3.0, 1.8V/2.95V SD cards and hot plug
I2C interface	Multiple I2C interfaces can be used for peripherals such as TP, camera, sensor etc.
ADC interface	One channel universal ADC
RTC	Supported
Antenna interface	TRX, DRX, GNSS, WIFI/BT antenna interfaces.
Physical characteristics	Dimensions: 41.0(±0.15)*41.0(±0.15)*2.8 (max) mm Package: 148 LCC+128 LGA Weight: About 10.6 g
Temperature range	Operating temperature[1]: -30°C~75°C[1)] Storage temperature: -40°C~85°C
Software update	USB/OTA/SD
RoHS	Comply with RoHS standard

When the module is operating within this temperature range, the functions of it are normal and the relevant performance meets the 3GPP standard.

2.3 Description of Development Kit

Fibocom configures a complete development board kit for the module, which makes it convenient for users to quickly understand the module performance. For the usage of development board, refer to Fibocom_SC208-GL_ADP User Guide and Fibocom_EVB-SOC_User Guide.

3 Pin Definition

3.1 Pin Distribution

The top surface view of module pin distribution is as follows:

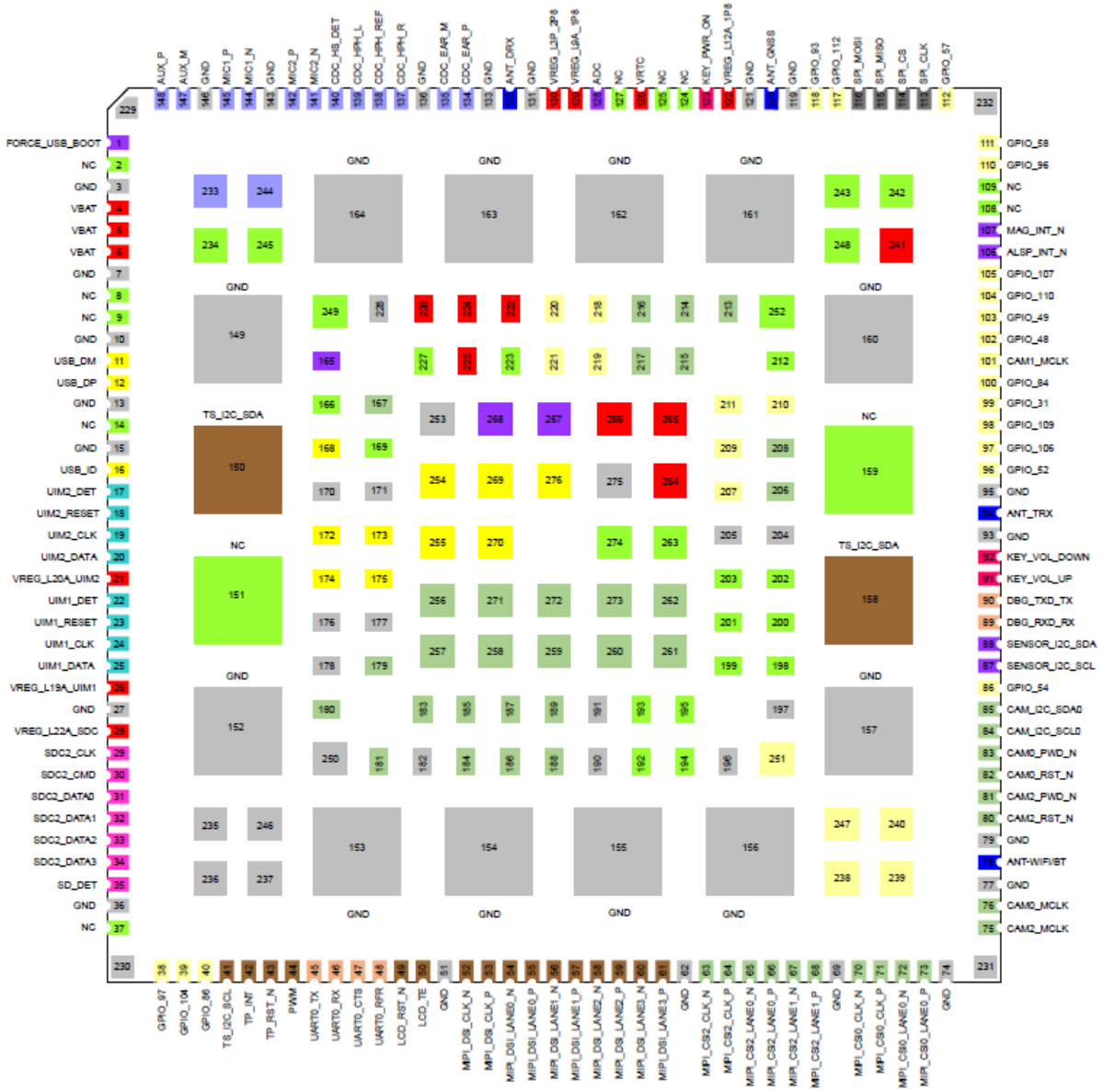

Figure 1. Pin distribution

3.2 Pin Description

Table 3. I/O type definition

Type	Description	Type	Description
PI	Power input	AIO	Analog input and output
PO	Power output	OD	Open drain
DI	Digital input	PU	Pull-up high level
DO	Digital output	PD	Pull-down low level
DIO	Digital input and output	T	Tristate, that is, high resistance state, which is determined by the peripheral circuit
AI	Analog input	G	Ground
AO	Analog output	- -	- -

Table 4. Power interfaces

Pin No.	Pin Name	I/O	Reset Value[1]	Pin Description	DC Feature
4,5,6	VBAT	PI	- -	Module power supply	- -
126	VRTC	PI/PO	- -	RTC clock power supply pin	- -
129	VREG_L9A_1P8	PO	- -	IO1.8V voltage output, can pull up the IO belonging to the local voltage domain output by the module, external chips cannot be used	1.8V
122	VREG_L12A_1P8	PO	- -	1.8V voltage output, CPU for self use, cannot be used externally	1.8V
26	VREG_L19A_UIM1	PO	- -	Limited to SIM card 1 power supply only	1.8V/3.0V
21	VREG_L20A_UIM2	PO	- -	Limited to SIM card 2 power supply only	1.8V/3.0V
28	VREG_L22A_SDC	PO	- -	Limited to SD card power supply only	1.8V/2.96V
225	VREG_L5A_SDIO	PO		SDIO pull-up power supply only	1.8V/2.96V

Pin No.	Pin Name	I/O	Reset Value[1]	Pin Description	DC Feature
241	VREG_L15A_3P0	PO	- -	3.128V voltage, CPU for self use, cannot be used externally	3.0V
264	VREG_L1P_1P1	PO	- -	Camera DVDD power supply 1	1.1V
226	VREG_L2P_1P2	PO	- -	Camera DVDD power supply 2	1.2V
130	VREG_L3P_2P8	PO	- -	Camera AVDD power supply 1	2.8V
222	VREG_L4P_2P9	PO	- -	Camera AVDD power supply 2	2.9V
224	VREG_L5P_2P8	PO	- -	Camera AFVDD power supply	2.8V
265	VREG_L6P_2P8	PO	- -	Camera AVDD power supply 3	2.8V
266	VREG_L7P_1P8	PO	- -	Camera DOVDD power supply	1.8V
3, 7, 10, 13, 15, 27, 36, 51, 62, 69, 74, 77, 79, 93, 95, 119, 121, 131, 133, 136, 143, 146, 149, 152, 153, 154, 155, 156, 157, 160, 161, 162, 163, 164, 170, 171, 176, 177, 178, 182, 190, 191, 196, 197, 204, 205, 228, 229, 230, 231, 232, 235, 236, 237, 246, 250, 253, 275					58 GND

Table 5. Control interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
123	KEY_PWR_N	DI	- -	Power-on key	- -
91	KEY_VOL_UP	DI	- -	Volume + key	- -
92	KEY_VOL_DOWN	DI	- -	Volume - key	- -
165	CBL_PWR_N	DI	- -	Auto power on	- -

Table 6. USIM interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
17	UIM2_DETECT	DI	- -	UIM2 presence detection	1.8V
18	UIM2_RESET	DO	- -	UIM2 reset	- -
19	UIM2_CLK	DO	- -	UIM2 clock	- -
20	UIM2_DATA	DI/DO	- -	UIM2 data	- -
22	UIM1_DETECT	DI	- -	UIM1 presence detection	1.8V

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
23	UIM1_RESET	DO	- -	UIM1 reset	- -
24	UIM1_CLK	DO	- -	UIM1 clock	- -
25	UIM1_DATA	DI/DO	- -	UIM1 data	- -

Table 7. SD interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
29	SDC2_CLK	DO	- -	SD card clock	- -
30	SDC2_CMD	DI/DO	- -	SD card command	- -
31	SDC2_DATA0	DI/DO	- -	SD card data bit 0	- -
32	SDC2_DATA1	DI/DO	- -	SD card data bit 1	- -
33	SDC2_DATA2	DI/DO	- -	SD card data bit 2	- -
34	SDC2_DATA3	DI/DO	- -	SD card data bit 3	- -
35	SD_CARD_DET_N	DI	- -	SD presence detection	---

Table 8. USB interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
168	USB_IN_DET	AI	- -	VBUS input detection	- -
11	USB_ DM	AIO	- -	USB 2.0 differential data signal-	- -
12	USB_DP	AIO	- -	USB 2.0 differential data signal+	- -
16	USB_ID	DI	- -	USB ID pin	- -
172	USB_SS_TX0_P	AO	- -	USB 3.1 channel 0 sending (+)	- -
173	USB_SS_RX0_P	AI	- -	USB 3.1 channel 0 reception (+)	- -
174	USB_SS_TX0_M	AO	- -	USB 3.1 channel 0 sending (-)	- -
175	USB_SS_RX0_M	AI	- -	USB 3.1 channel 0 reception (-)	- -
254	USB_SS_RX1_M	AI	- -	USB 3.1 channel 1 reception (-)	- -

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
255	USB_SS_TX1_M	AO	- -	USB 3.1 Channel 1 sending (-)	- -
269	USB_SS_RX1_P	AI	- -	USB 3.1 channel 1 reception (+)	- -
270	USB_SS_TX1_P	AO	- -	USB 3.1 Channel 1 sending (+)	- -
276	USB_PHY_PS	DI	- -	USB front and back insertion flag	- -

Table 9. SPI interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
113	SPI_CLK	DO	- -	SPI clock	1.8V
114	SPI_CS	DO	- -	SPI chip selection	1.8V
115	SPI_MISO	DI	- -	SPI master input slave output	1.8V
116	SPI_MOSI	DO	- -	SPI master output slave input	1.8V

Table 10. UART interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
90	DBG_UART_TX	DO	- -	Debug UART sending	1.8V
89	DBG_UART_RX	DI	- -	Debug UART reception	1.8V
45	UART_TX	DO	- -	UART sending	1.8V
46	UART_RX	DI	- -	UART reception	1.8V
47	UART_CTS	DI	- -	UART clear to send	1.8V
48	UART_RFR	DO	- -	UART requests to send	1.8V

Table 11. I2C interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
87	SENSOR_I2C_SCL	DO	- -	Sensor I2C clock	1.8V
88	SENSOR_I2C_SDA	DI/DO	- -	Sensor I2C data	1.8V
41	TS_I2C_SCL	DO	- -	TP I2C clock	1.8V

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
150,158	TS_I2C_SDA	DI/DO	- -	TP I2C data	1.8V
84	CAM_I2C_SCL0	DO	- -	Camera0 I2C clock	1.8V
85	CAM_I2C_SDA0	DI/DO	- -	Camera0 I2C data	1.8V
206	CAM_I2C_SCL1	DO	- -	Camera1 I2C clock	1.8V
208	CAM_I2C_SDA1	DI/DO	- -	Camera1 I2C data	1.8V
268	APPS_I2C_SCL	DO	- -	I2C clock	1.8V
267	APPS_I2C_SDA	DI/DO	- -	I2C data	1.8V

Table 12. LPI_I2S interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
247	LPI_MI2S1_CLK	DO	- -	LPI_I2S clock	- -
238	LPI_MI2S1_WS	DO	- -	LPI_I2S data word select	- -
239	LPI_MI2S1_DATA0	DI/DO	- -	LPI_I2S data channel 0	- -
240	LPI_MI2S1_DATA1	DI/DO	- -	LPI_I2S data channel 1	- -
251	MI2S_MCLK1_A	DO	- -	I2S system master clock	- -

Table 13. Display interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
53	MIPI_DSI_CLK_P	AO	- -	MIPI DSI differential CLK +	- -
52	MIPI_DSI_CLK_N	AO	- -	MIPI DSI differential CLK -	- -
55	MIPI_DSI_LANE0_P	AO	- -	MIPI DSI differential lane 0 +	- -
54	MIPI_DSI_LANE0_N	AO	- -	MIPI DSI differential lane 0 -	- -
57	MIPI_DSI_LANE1_P	AO	- -	MIPI DSI differential lane 1 +	- -
56	MIPI_DSI_LANE1_N	AO	- -	MIPI DSI differential lane 1 -	- -
59	MIPI_DSI_LANE2_P	AO	- -	MIPI DSI differential lane 2 +	- -
58	MIPI_DSI_LANE2_N	AO	- -	MIPI DSI differential lane 2 -	- -

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
61	MIPI_DSI_LANE3_P	AO	- -	MIPI DSI differential lane 3 +	- -
60	MIPI_DSI_LANE3_N	AO	- -	MIPI DSI differential lane 3 -	- -
49	LCD_RST_N	DO	- -	LCD reset signal	- -
44	PWM	DO	- -	LCD PWM modulation	- -
50	LCD_TE	DI	- -	LCD screen synchronization signal	- -

Table 14. TP interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
42	TS0_INT_N	DI	- -	TP interrupt	1.8V
43	TS_RST_N	DO	- -	TP reset	1.8V

Table 15. Camera interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
70	MIPI_CSI0_CLK_N	AI	- -	Camera 0 MIPI clock-	- -
71	MIPI_CSI0_CLK_P	AI	- -	Camera 0 MIPI clock+	- -
72	MIPI_CSI0_LANE0_N	AI	- -	Camera 0 MIPI Lane0-	- -
73	MIPI_CSI0_LANE0_P	AI	- -	Camera 0 MIPI Lane0+	- -
185	MIPI_CSI0_LANE1_N	AI	- -	Camera 0 MIPI Lane1-	- -
184	MIPI_CSI0_LANE1_P	AI	- -	Camera 0 MIPI Lane1+	- -
76	CAM0_MCLK	DO	- -	Camera 0 MCLK signal	- -
82	CAM0_RST_N	DO	- -	Camera 0 reset	1.8V
83	CAM0_PWD_N	DO	- -	Camera 0 PWD signal	1.8V
189	MIPI_CSI0_LANE3_N	AI	- -	Camera 3 MIPI clock-	- -
188	MIPI_CSI0_LANE3_P	AI	- -	Camera 3 MIPI clock+	- -
187	MIPI_CSI0_LANE2_N	AI	- -	Camera 3 MIPI Lane0-	- -

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
186	MIPI_CSI0_LANE2_P	AI	- -	Camera 3 MIPI Lane0+	- -
213	CAM3_MCLK	DO	- -	Camera 3 MCLK signal	- -
214	CAM3_RST_N	DO	- -	Camera 3 reset	1.8V
215	CAM3_PWD_N	DO	- -	Camera 3 PWD signal	1.8V
256	MIPI_CSI1_CLK_N	AI	- -	Camera 1 MIPI clock-	- -
257	MIPI_CSI1_CLK_P	AI	- -	Camera 1 MIPI clock+	- -
258	MIPI_CSI1_LANE0_N	AI	- -	Camera 1 MIPI Lane0-	- -
259	MIPI_CSI1_LANE1_N	AI	- -	Camera 1 MIPI Lane1-	- -
260	MIPI_CSI1_LANE2_N	AI	- -	Camera 1 MIPI Lane2-	- -
261	MIPI_CSI1_LANE3_N	AI	- -	Camera 1 MIPI Lane3-	- -
271	MIPI_CSI1_LANE0_P	AI	- -	Camera 1 MIPI Lane0+	- -
272	MIPI_CSI1_LANE1_P	AI	- -	Camera 1 MIPI Lane1+	- -
273	MIPI_CSI1_LANE2_P	AI	- -	Camera 1 MIPI Lane2+	- -
262	MIPI_CSI1_LANE3_P	AI	- -	Camera 1 MIPI Lane3+	- -
101	CAM1_MCLK	DO	- -	Camera 1 MCLK signal	- -
216	CAM1_RST_N	DO	- -	Camera 1 reset	1.8V
217	CAM1_PWD_N	DO	- -	Camera 1 PWD signal	1.8V
63	MIPI_CSI2_CLK_N	AI	- -	Camera 2 MIPI clock-	- -
64	MIPI_CSI2_CLK_P	AI	- -	Camera 2 MIPI clock+	- -
65	MIPI_CSI2_LANE0_N	AI	- -	Camera 2 MIPI Lane 0-	- -
66	MIPI_CSI2_LANE0_P	AI	- -	Camera 2 MIPI Lane 0+	- -
67	MIPI_CSI2_LANE1_N	AI	- -	Camera 2 MIPI Lane 1-	- -
68	MIPI_CSI2_LANE1_P	AI	- -	Camera 2 MIPI Lane 1+	- -
183	MIPI_CSI2_LANE2_N	AI	- -	Camera 2 MIPI Lane 2-	- -
181	MIPI_CSI2_LANE2_P	AI	- -	Camera 2 MIPI Lane 2+	- -

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
179	MIPI_CSI2_LANE3_N	AI	- -	Camera 2 MIPI Lane 3-	- -
180	MIPI_CSI2_LANE3_P	AI	- -	Camera 2 MIPI Lane 3+	- -
75	CAM2_MCLK	DO	- -	Camera 2 MCLK signal	- -
80	CAM2_RST_N	DO	- -	Camera 2 reset	1.8V
81	CAM2_PWD_N	DO	- -	Camera 2 PWD signal	1.8V

Table 16. Audio interfaces

Pin No.	Pin Name	I/O	Reset State	Pin Description	DC Feature
141	MIC2_IN_N	AI	- -	Headphone MIC input -	- -
142	MIC2_IN_P	AI	- -	Headphone MIC input +	- -
144	MIC1_IN_N	AI	- -	Main MIC differential input-	- -
145	MIC1_IN_P	AI	- -	Main MIC differential input+	- -
233	MIC3_IN_N	AI	- -	Sub MIC differential input-	- -
244	MIC3_IN_P	AI	- -	Sub MIC differential input+	- -
147	AUX_M	AO	- -	LINOUT differential output-	- -
148	AUX_P	AO	- -	LINOUT differential output+	- -
135	CDC_EAR_M	AO	- -	Receiver output -	- -
134	CDC_EAR_P	AO	- -	Receiver output +	- -
139	CDC_HPH_L	AO	- -	Headphone left channel output	- -
138	CDC_HPH_REF	/	- -	Headphone ground reference	- -
137	CDC_HPH_R	AO	- -	Headphone right channel output	- -
140	CDC_HS_DET	AI	- -	Headphone plug detection	- -

Table 17. Sensor interrupt interfaces

Pin No.	Pin Name	I/O	Reset Value	Pin Description	DC Feature
106	ALSP_INT_N	DI	- -	Interruption of ambient light	1.8V

Pin No.	Pin Name	I/O	Reset Value	Pin Description	DC Feature
				sensor	
107	MAG_INT_N	DI	- -	Geomagnetic sensor interruption	1.8V
108	ACCL_INT_N	DI	- -	Acceleration sensor interruption	1.8V
109	GYRO_INT_N	DI	- -	Gyroscope interruption	1.8V

Table 18. ADC interfaces

Pin No.	Pin Name	I/O	Reset Value	Pin Description	DC Feature
128	ADC	AI	- -	Universal ADC interface	- -

Table 19. GPIO interfaces

Pin No.	Pin Name	I/O	Reset Value	Pin Description	DC Feature
38	GPIO_97	DI/DO	PD	Regular GPIO	1.8V
39	GPIO_104	DI/DO	PD	Regular GPIO	1.8V
40	GPIO_86	DI/DO	PD	Regular GPIO	1.8V
86	GPIO_54	DI/DO	PD	Regular GPIO	1.8V
96	GPIO_52	DI/DO	PD	Regular GPIO	1.8V
97	GPIO_106	DI/DO	PD	Regular GPIO	1.8V
98	GPIO_109	DI/DO	PD	Regular GPIO	1.8V
99	GPIO_31	DI/DO	PD	Regular GPIO	1.8V
100	GPIO_84	DI/DO	PD	Regular GPIO	1.8V
102	GPIO_48	DI/DO	PD	Regular GPIO	1.8V , BOOT_CONFIG
103	GPIO_49	DI/DO	PD	Regular GPIO	1.8V
104	GPIO_110	DI/DO	PD	Regular GPIO	1.8V
105	GPIO_107	DI/DO	PD	Regular GPIO	1.8V
110	GPIO_96	DI/DO	PD	Regular GPIO	1.8V

Pin No.	Pin Name	I/O	Reset Value	Pin Description	DC Feature
111	GPIO_58	DI/DO	PD	Regular GPIO	1.8V
112	GPIO_57	DI/DO	PD	Regular GPIO	1.8V , BOOT_CONFIG
117	GPIO_112	DI/DO	PD	Regular GPIO	1.8V
118	GPIO_93	DI/DO	PD	Regular GPIO	1.8V
210	GPIO_85	DI/DO	PD	Regular GPIO	1.8V
211	GPIO_83	DI/DO	PD	Regular GPIO	1.8V
218	PM4250_GPIO_6	DI/DO	PD	Regular GPIO	1.8V/VPH
219	GPIO_111	DI/DO	PD	Regular GPIO	1.8V
207	GPIO_70	DI/DO	PD	Regular GPIO	1.8V
209	GPIO_69	DI/DO	PU	Regular GPIO	1.8V
220	PM4250_GPIO_2	DI/DO	PD	Regular GPIO	1.8V

- The GPIO of BOOT.CONFIG cannot be pulled up externally, otherwise it may cause power failure.
- All GPIOs are not allowed to have any level state changes during the system startup process;
- GPIO marked with "PU" is not recommended for use as an enable control for default high efficiency devices, such as backlight enable for screens and audio amplifier enable.
- The default power domain of PM4250_GPIO_6 is VPH. Pay attention to the peripheral voltage when using the PM4250_GPIO_6. If you have any questions, you can contact Fibocom.

Table 20. Antenna interfaces

Pin No.	Pin Name	I/O	Reset Value	Pin Description	DC Feature
94	ANT_TRX	AI/AO	- -	2G/3G/4G main antenna	- -
132	ANT_DRX	AI	- -	Diversity reception antenna	- -
78	ANT_WIFI/BT	AI/AO	- -	WIFI/BT antenna	- -
120	ANT_GNSS	AI	- -	GNSS antenna	- -

Table 21. Forced download interfaces

Pin No.	Pin Name	I/O	Reset Value	Pin Description	DC Feature
1	FORCE_USB_BOOT	DI	PD	Forced USB download	- -

Table 22. Reserved interfaces

Pin No.	DC Feature
2, 8, 9, 14, 37, 108, 109, 124, 125, 127, 151, 159, 166, 167, 169, 192, 193, 194, 195, 198, 199, 200, 201, 202, 203, 221,223, 225, 227, 234, 242, 243, 245, 248, 249, 252, 263, 274	36 suspended

4 Application Interfaces

4.1 Power Interfaces

4.1.1 Power Supply Circuit

The module provides 3 VBAT pins, VBAT is used to connect external power sources to power modules.

To ensure that the instantaneous voltage of the VBAT input power supply is not less than 3.5V, it is recommended to parallel two low ESR 220uF tantalum capacitors such as 1uF, 100nF, 39pF, 33pF, etc. near the input end of the module VBAT. It is also recommended that the PCB wiring of the VBAT be as short and wide as possible (not less than 3mm), and the ground plane of the power supply be as complete as possible to reduce the equivalent impedance of the VBAT wiring, ensuring that there is no significant voltage drop under high current conditions such as maximum power emission.

In order to improve the surge resistance of the module, high-power surge tubes should be added near the VBAT end of the module. The reference design of the power supply circuit is shown in the following figure:

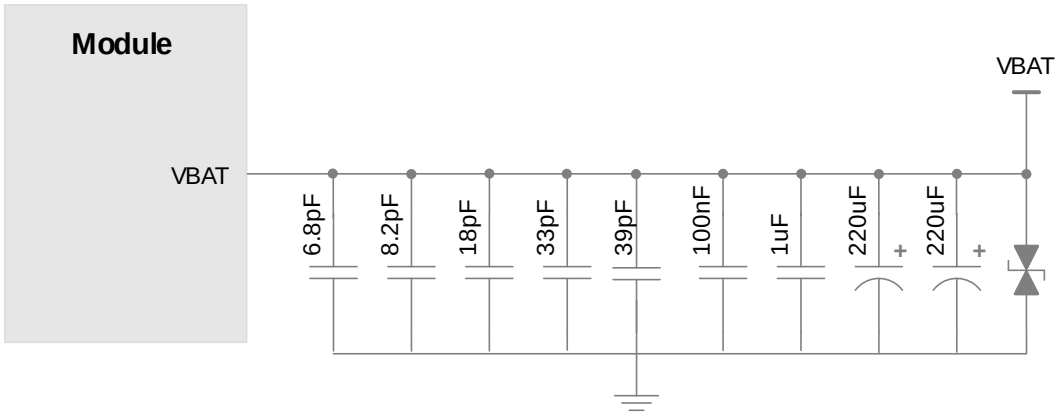

Figure 2. Power supply reference circuit

Filter capacitors should be placed close to the power supply pin, and the capacitance value should be smaller to be closer to the corresponding power supply pin. The filter capacitor is placed on the same side as the module, and must not cross the layer, otherwise there will be the risk of TIS interference, and the trace is as short and wide as possible.

Table 23. Filter capacitor introduction

Recommended Capacitor	Description
ESD	ESD devices are required to protect ESD and EOS. It is recommended to use ESDH5V0FD1.
220uF x 2	For the stabilizing capacitor, select a low ESR (0.7Ω) capacitor with a capacitance value of not less than 220uF x 2. The recommended model is TAJC227K010RNJ. This capacitor must not be omitted, as it

	may lead to random system reboots.
1uF, 100nF	Filter out interference caused by clock and digital signals.
220pF, 150pF, 39pF, 33pF	Filter out low-frequency interference in 700MHz to 900MHz.
18pF, 10pF, 8.2pF	Filter out mid/high-frequency interference in the 1700MHz to 2700MHz.
6.8pF, 3.3pF	Filter out interference in the 3.5GHz to 5GHz frequency range.

Table 24. Power supply

Parameter	I/O	Minimum Value	Typical Value	Maximum Value	Unit
VBAT(DC)	PI	3.5	3.8	4.35	V

- The recommended filter capacitor can be adjusted by the customer based on specific circumstances. It is not a fixed value.

4.1.2 Voltage Drop

The input range of the VBAT power is 3.5 V to 4.35 V and the recommended value is 3.8 V. The performance of the power supply such as its load capacity and ripple will directly affect the operating performance and stability of the module. In extreme cases, the peak current of the module can reach 3A. If the power supply capacity is insufficient, the power supply transient voltage drops below 3.5 V, which may cause the module power off or restart. The power supply voltage drop is shown in the following figure:

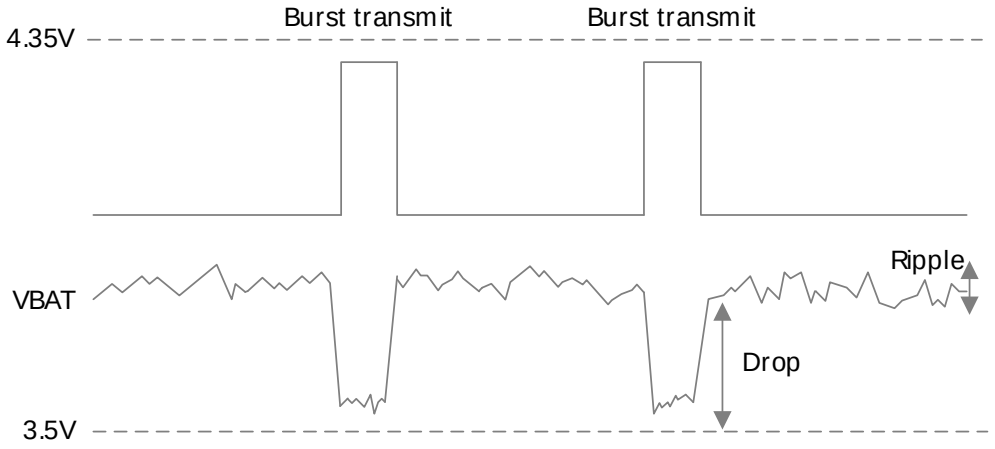

Figure 3. Power supply requirements

The voltage range of the VBAT power supply must be guaranteed between 3.5V and 4.35V, including the superposition value of voltage such as ripple, sag and transient overshoot.

4.1.3 VRTC Interfaces

The VRTC supplies power to the RTC clock in the module. After the module VBAT power supply is powered on, the VRTC outputs voltage. To maintain the real-time clock when the VBAT is off, use an external power supply (such as a button battery). The VRTC parameters are as follows:

Table 25. VRTC parameters

Parameter	Minimum	Typical	Maximum	Unit
VRTC output voltage	2.0	3.0	3.25	V
VRTC input current (clock normal)	TBD	TBD	TBD	uA

4.1.4 Power Output

The module has multiple power outputs, used for peripheral circuit power supply. In application, 33pF and 10pF capacitors can be connected in parallel to effectively filter high-frequency interference.

Table 26. Power output

Pin No.	Pin Name	Function	Default Voltage (V)	Drive Current (mA)	Sleep Status
129	VREG_L9A_1P8	System 1.8V voltage output	1.8V	300	ON
26	VREG_L19A_UIM1	(U) SIM card 1 power supply	1.8V/2.96V	150	- -
21	VREG_L20A_UIM2	(U) SIM card 2 power supply	1.8V/2.96V	150	- -
28	VREG_L22A_SDC	SD card power supply	1.8V/2.96V	600	- -
225	VREG_L5A_SDIO	SDIO pull-up power supply	2.96V	50	- -
264	VREG_L1P_1P1	Camera DVDD power supply 1	1.1V	500	OFF
226	VREG_L2P_1P2	Camera DVDD power supply 2	1.2V	500	OFF
130	VREG_L3P_2P8	Camera AVDD power supply 1	2.8V	300	OFF
222	VREG_L4P_2P9	Camera AVDD power supply 2	2.9V	300	OFF
224	VREG_L5P_2P8	Camera AFVDD power supply	2.8V	300	OFF
265	VREG_L6P_2P8	Camera AVDD power supply 3	2.8V	300	OFF
266	VREG_L7P_1P8	Camera DOVDD power supply	1.8V	300	OFF

Pin No.	Pin Name	Function	Default Voltage (V)	Drive Current (mA)	Sleep Status

VREG_L9A_1P8 is the 1.8V voltage output of IO, which can pull up the IO belonging to the local voltage domain output by the module. External chips cannot be used.

VREG_L12A_1P8 and VREG_L15A_3P0 are for CPU use and cannot be used externally. They cannot be grounded and remain suspended.

4.2 Control Interfaces

4.2.1 Power-on/off

4.2.1.1 Power-on

The module has one power on control signal to control the module to power on/off, restart, sleep/wake up.

After VBAT is powered, pull down the PWRKEY pin for 2s to 6s can triggermodule power on. The button control and OC drive power on reference design is shownas follows:

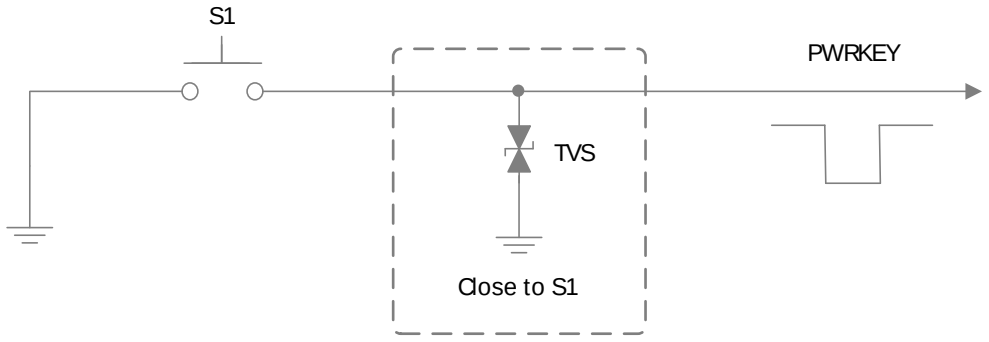

Figure 4. Reference design of key power-on circuit

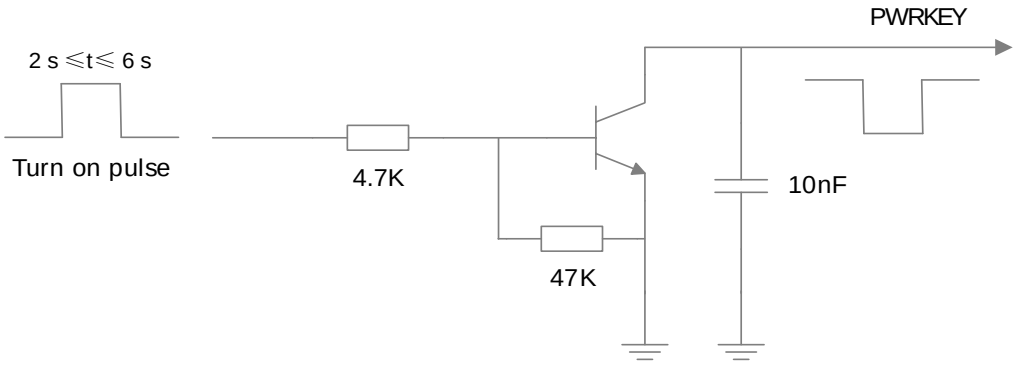

Figure 5. Reference design of OC drive power-on circuit

The power on sequence is shown in the following figure.

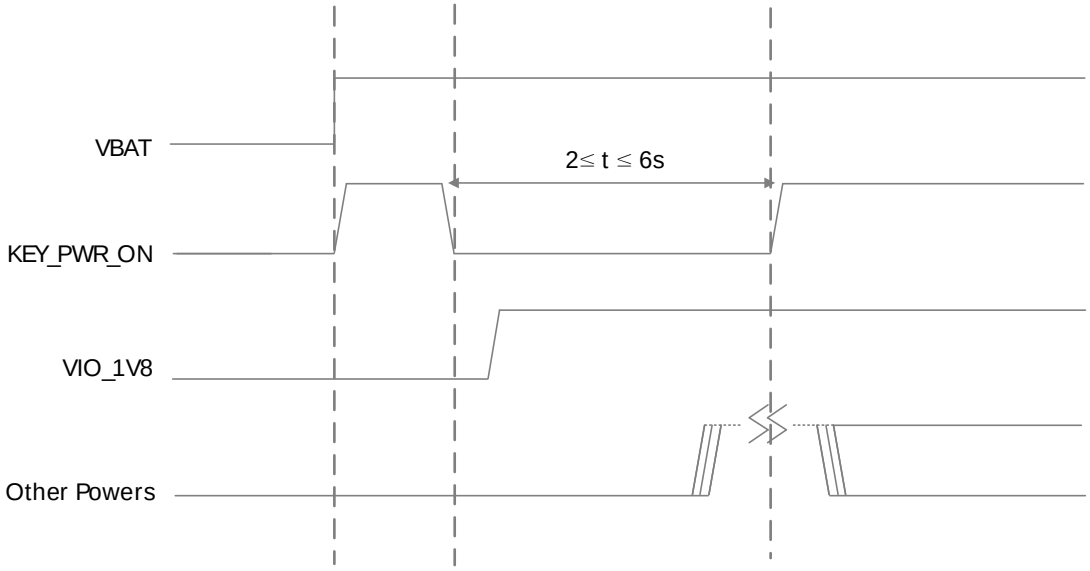

Figure 6. Startup timing sequence

4.2.1.2 Power-off

Normal power off: When turned on, if the PWRKEY pin is pulled down for more than 2 seconds, a selection box will pop up on the display interface (select shutdown or restart).

When the system is abnormal or shutdown, you can use force power off method to reset the module, please use normal method generally, otherwise may cause data loss and other anomalies.

4.2.2 Sleep and Wakeup

Sleep: When the module is in standby mode, pull down the PWRKEY pin 0.5s, and the module will enter the sleep mode. The system supports automatic sleep. The time from standby to sleep can be configured through software.

Wakeup: When the module is in sleep mode, pull down the PWRKEY pin 0.5s, and the module can be woken up.

4.2.3 Volume Control

VOL_UP and VOL_DOWN are the volume up and volume down control button. For its circuit design, refer to the power on circuit design.

4.2.4 Forced Download

The module provides the USB_BOOT pin as the emergency download trigger interface. Pulling the USB_BOOT pin to VREG_L9A_1P8 during the booting phase triggers the module to enter the emergency download mode. This is used for final processing when the product fails to start or run properly due to a fault. Reserve test sites for the convenience of subsequent software upgrades and commissioning.

USB_BOOT reference circuit design is shown as follows:

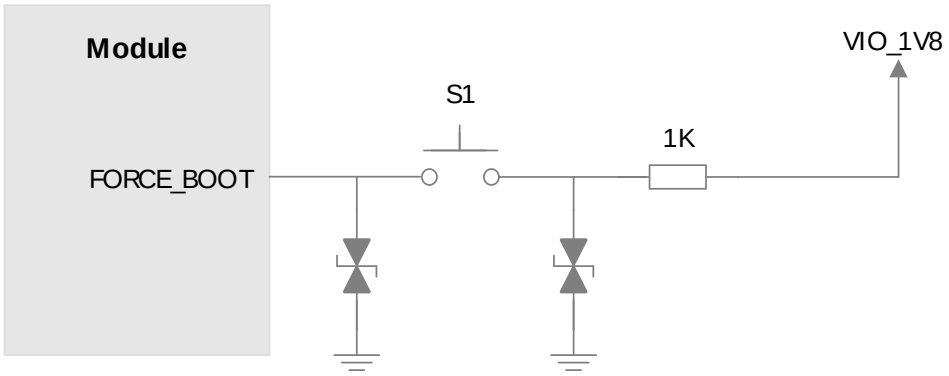

Figure 7. Reference circuit design of forced download

4.3 USB

4.3.1 USB Pin Definition

The module supports a set of USB 3.1 interface that is downward compatible with USB 2.0 (supports software download). USB 3.1 supports the SS (5Gbps) mode and cannot support software download. USB supports OTG and HUB expansion. Please refer to pin description section for pin definition.

USB 3.1 (TYPE-C) circuit reference design is shown in the following figure.

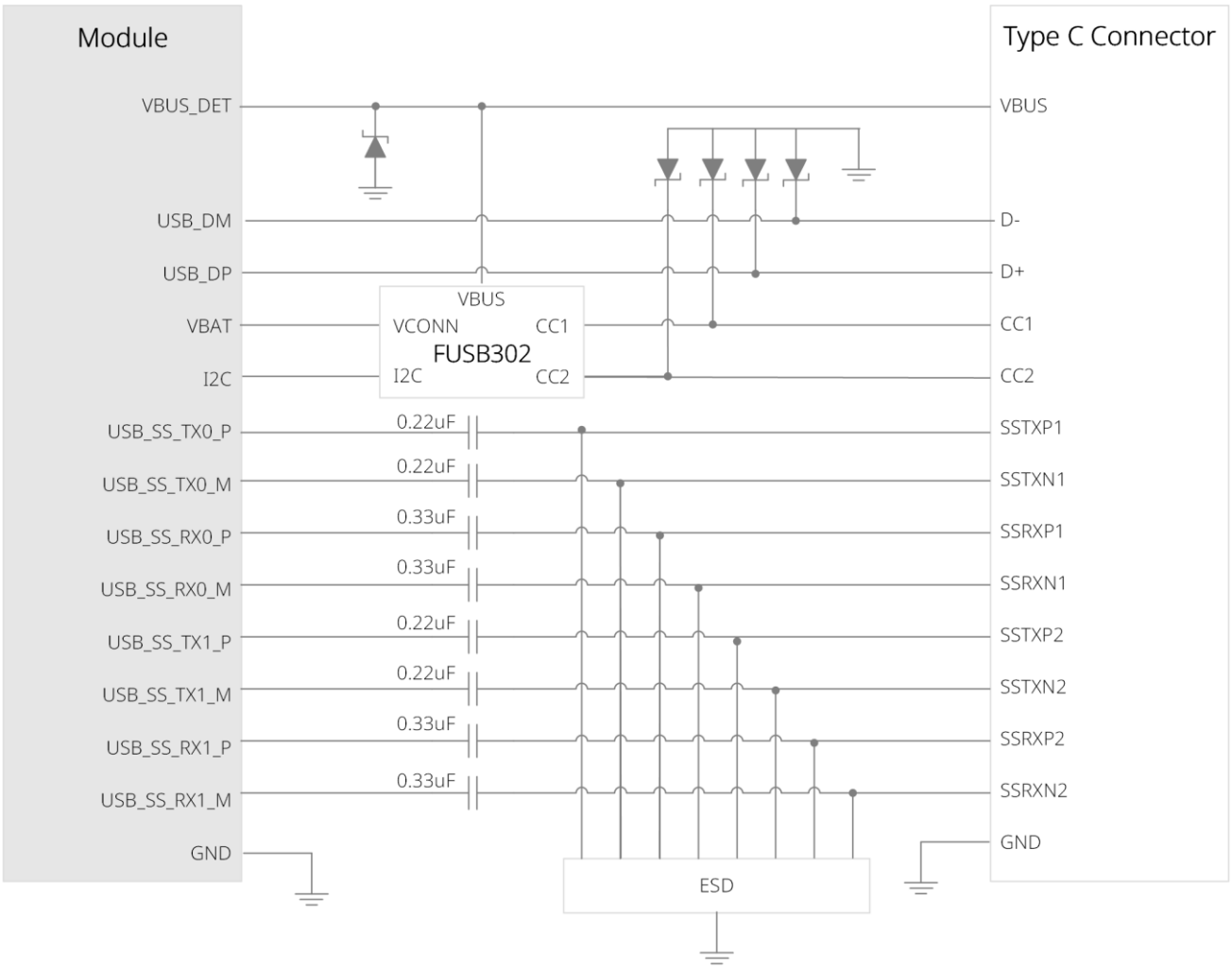

Figure 8. Reference circuit of USB 3.1

The reference circuit of USB 2.0 interface is designed as follows.

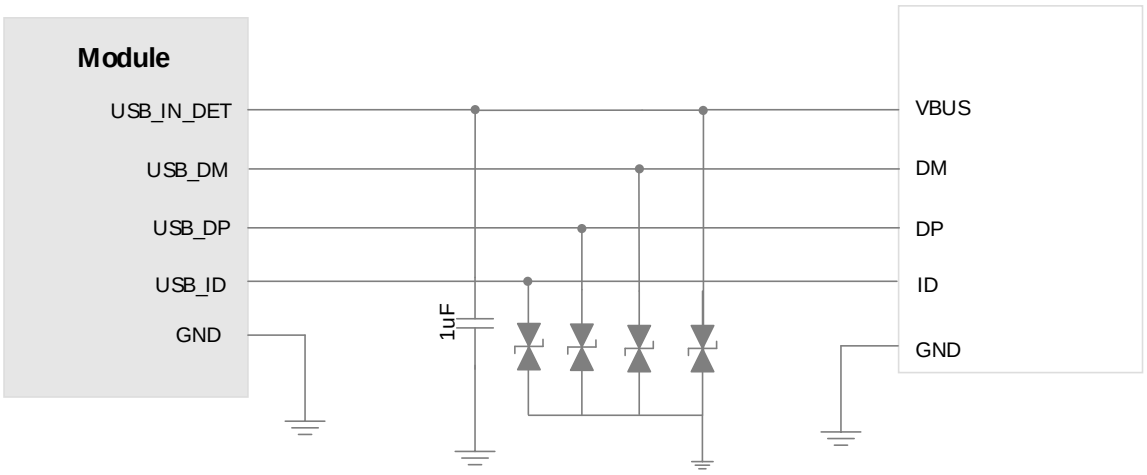

Figure 9. Reference circuit of USB 2.0

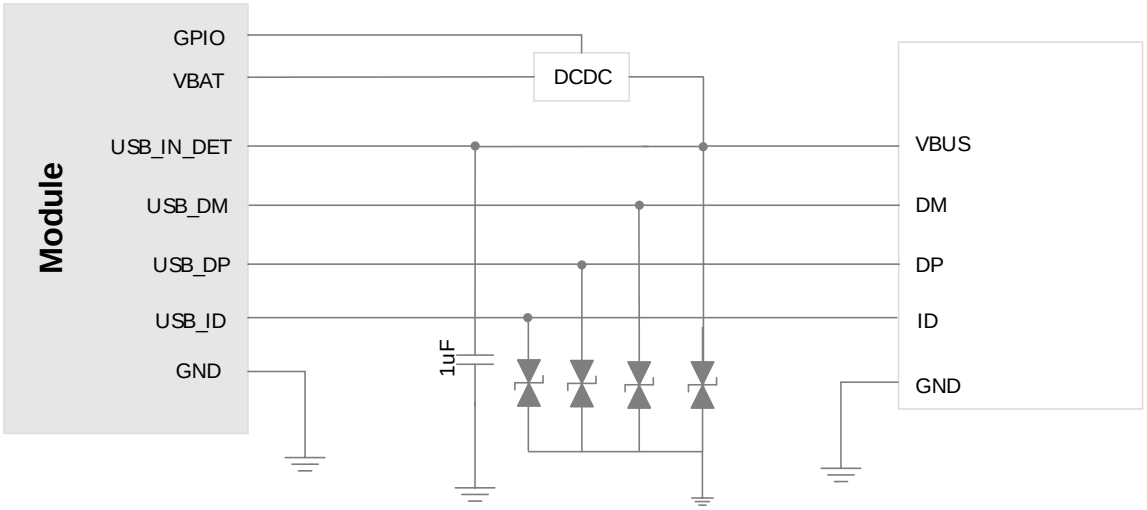

Figure 10. Reference circuit of USB 2.0 (with the OTG function)

4.3.2 USB Design Considerations

USB is a high-speed signal line. It is important to pay special attention to follow guidelines in PCB layout:

- The USB signal line needs to be controlled with a 90Ω differential impedance with tolerance ±10%.
- The USB signal lines are treated with equal length, and the length difference of differential lines in the USB 2.0 signal group is controlled within 2 mm; The length difference of differential line in the USB 3.0 signal group is controlled within 0.7 mm, and the length difference between groups is controlled within 10 mm.
- The recommended spacing between USB3.0 signal Rx and Tx is 3 times line width and the spacing between differential lines and other routing lines is 4 times line width.

- ESD protection devices shall be added near the USB interface: The parasitic capacitance of ESD protection devices for USB 2.0 signals shall not exceed 2pF. The parasitic capacitance of the ESD protection device for USB 3.0 signals shall not exceed 0.2pF.

4.4 UART

The module defines two UART interfaces, all of which are in 1.8V voltage domain. Please refer to pin description section for pin definition.

The voltage domain of each serial port is 1.8V. When communicating with other voltage domain serial ports, it is necessary to add a level-shifting chip. The reference circuit design is as follows.

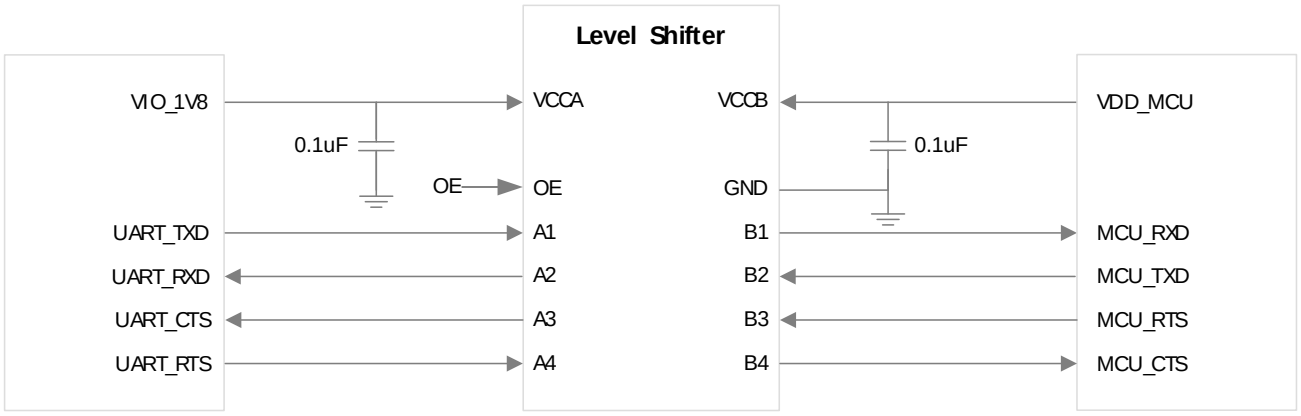

Figure 11. Reference design of level-shifting circuit

4.5 SPI

The module provides one set of SPI default interfaces that support master/slave mode. Please refer to pin description section for pin definition.

The reference schematic of SPI circuit is shown in the following figure.

Figure 12. SPI interface reference circuit

4.6 I2C

The module has multiple sets of general I2C interfaces, which can be used to connect peripherals respectively. Please refer to pin description section for pin definition.

When I2C has more than one peripheral, ensure the uniqueness of every peripheral address. If one of the peripherals has high requirement for timeliness, do not set the peripherals to share one set of I2C interfaces.

The APPS_I2C interface has a mounted I2C device inside the module at address 0x02. Since the module already has a 2.2KΩ pull-up resistor inside, the APPS_I2C interface can't be connected to a pull-up externally and can only be used as an I2C interface and can't be configured as any other type such as GPIO.

4.7 SD

The module supports one set of SD card interface. Please refer to the pin description section for pin definition.

The SD card reference circuit is designed as follows:

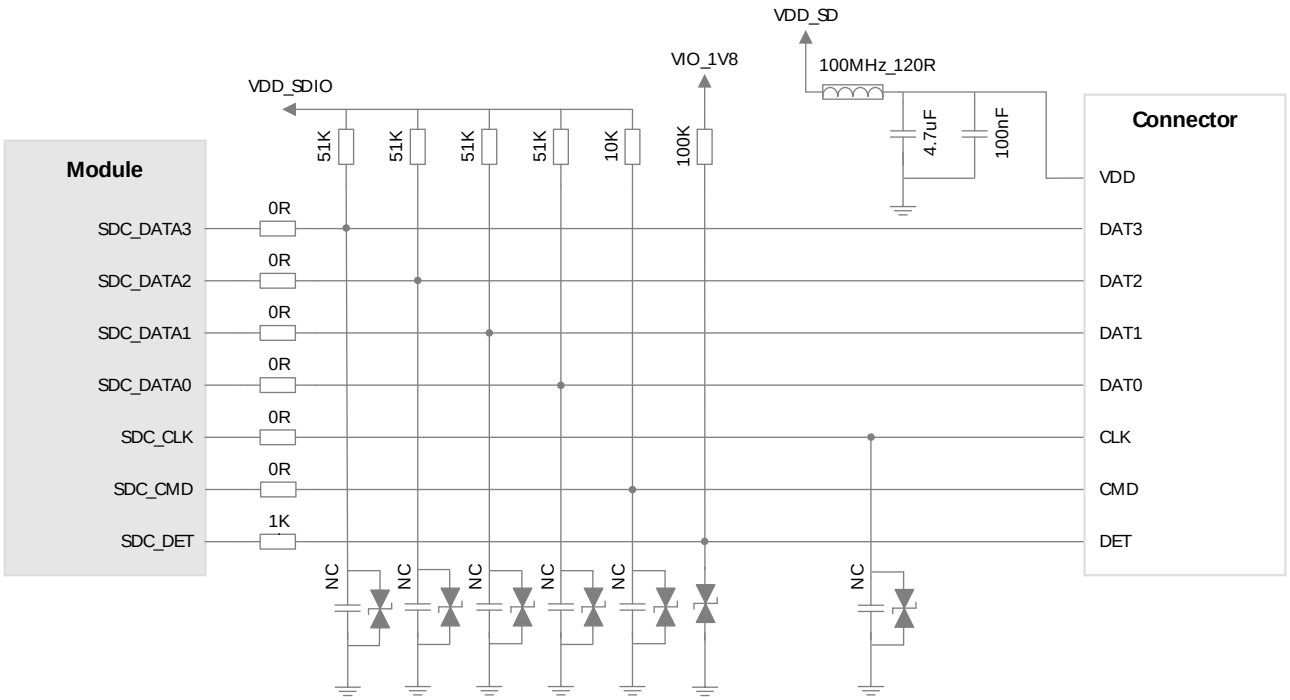

Figure 13. SD card reference circuit

EMC and ESD protection should be considered in the design of SDIO circuit, and the anti-interference ability should be improved to ensure the stable operation of SD card. The following rules should be strictly followed in the design:

- The length of the SDIO trace is ≤ 50 mm and the length difference between the clock signal and data signal traces is ≤ 2 mm.
- SDIO signal should be three-dimensional, and away from strong interference sources such as RF

antennas, DCDC power supplies, and clock signal lines.

- The SDIO signals should have a complete reference ground and the impedance of the data lines should be controlled at 50Ω (±10%).
- The total capacitance of the load on the SDIO signal lines should be less than 1pF.

- VDD_SD is the power supply for the SD card peripheral drive, capable of providing approximately 600mA of current. Pay attention to control the trace width to be at least 0.6mm.
- The pull-up for SD_DET, please use the VREG_L9A_1P8 power source.
- The pull-up for SDIO, please use the VREG_L5A power source.
- SD is a high-speed digital signal line that requires three-dimensional shielding, and should be kept away from strong sources of interference such as RF antennas, DC-DC power supplies, and clock signal lines.
- The SDIO signal must have a complete reference ground, and the data line impedance should be controlled at 50Ω (±10%).
- For the SD card clock and signal lines, pay attention to not exceed a trace length of 50mm, and select TVS devices with parasitic capacitance less than 0.5pF.

4.8 (U)SIM

The module has two sets of (U)SIM interfaces, supports dual card dual standby, and supports hot plug. Please refer to pin description section for pin definition.

The (U)SIM reference circuit is designed as follows:

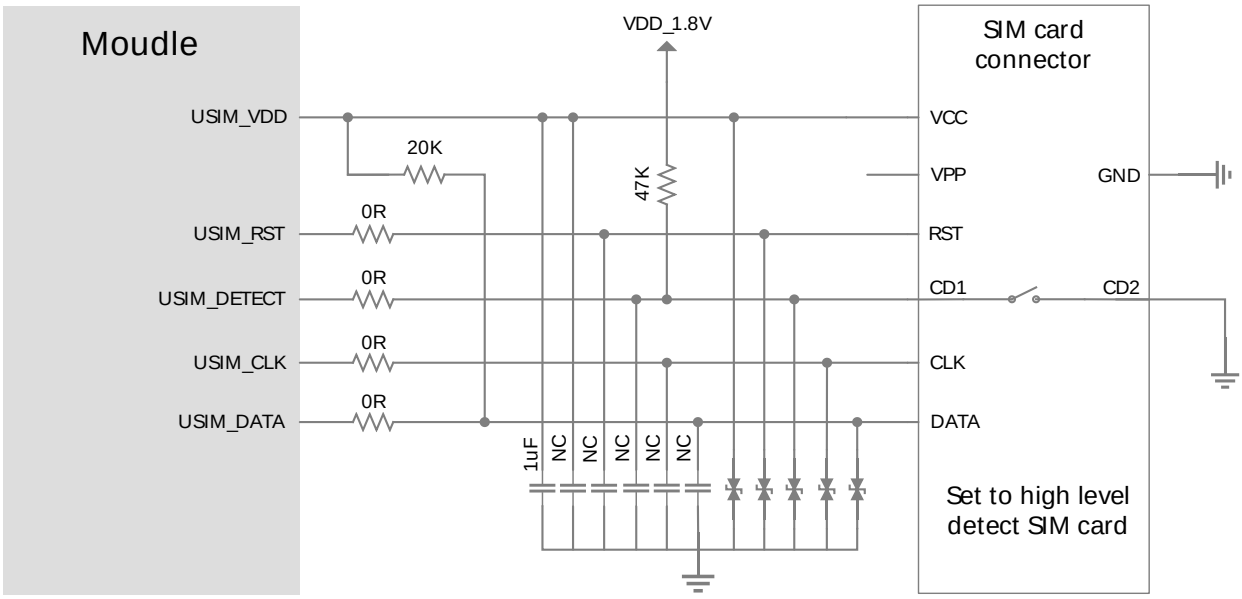

Figure 14. (U)SIM reference schematic

4.9 GPIO

The module has rich GPIO resources and the power domain is 1.8V. The pin definition is as follows:

Table 27. GPIO list

Pin No.	Pin Name	I/O	Function Description	Wake-up	Note
38	GPIO_97	PD:nppukp	Configurable I/O	YES	- -
39	GPIO_104	PD:nppukp	Configurable I/O	YES	- -
40	GPIO_86	PD:nppukp	Configurable I/O	YES	- -
86	GPIO_54	PD:nppukp	Configurable I/O	NO	- -
96	GPIO_52	PD:nppukp	Configurable I/O	NO	
97	GPIO_106	PD:nppukp	Configurable I/O	YES	- -
98	GPIO_109	PD:nppukp	Configurable I/O	NO	- -
99	GPIO_31	PD:nppukp	Configurable I/O	YES	- -
100	GPIO_84	PD:nppukp	Configurable I/O	YES	- -
102	GPIO_48	PD:nppukp	Configurable I/O	NO	BOOT_CONFIG
103	GPIO_49	PD:nppukp	Configurable I/O	NO	- -
104	GPIO_110	PD:nppukp	Configurable I/O	NO	- -
105	GPIO_107	PD:nppukp	Configurable I/O	YES	- -
110	GPIO_96	PD:nppukp	Configurable I/O	YES	- -
111	GPIO_58	PD:nppukp	Configurable I/O	NO	- -
112	GPIO_57	PD:nppukp	Configurable I/O	NO	BOOT_CONFIG
117	GPIO_112	PD:nppukp	Configurable I/O	YES	- -
118	GPIO_93	PD:nppukp	Configurable I/O	YES	- -
210	GPIO_85	PD:nppukp	Configurable I/O	YES	- -
211	GPIO_83	PD:nppukp	Configurable I/O	YES	- -
218	PM4250_GPIO_6	PD:nppukp	Configurable I/O	YES	- -
219	GPIO_111	PD:nppukp	Configurable I/O	NO	- -
207	GPIO_70	PD:nppukp	Configurable I/O	YES	- -

Pin No.	Pin Name	I/O	Function Description	Wake-up	Note
209	GPIO_69	PU:nppukp	Configurable I/O	YES	- -
220	PM4250_GPIO_2	PD:nppukp	Configurable I/O	YES	- -

Table 28. Parameter description

Parameter	Description
B	Bidirectional digital with CMOS input
NP	pdpukp = default no-pull with programmable options following the colon (:)
PD	nppukp = default pull-down with programmable options following the colon (:)
PU	nppdkp = default pull-up with programmable options following the colon (:)
KP:	nppdpu = default keeper with programmable options following the colon (:)

4.10 ADC

The module has one universal ADC interface, and the voltage input range is 0~VBAT. Please refer to the pin description section for pin definition.

4.11 LCD

The screen interface is based on the MIPI_DSI standard and supports one group of 4-Lane high-speed differential data transmission with a maximum FHD+ resolution. Please refer to the pin description section for pin definition.

The LCD reference design is shown in the following figure.

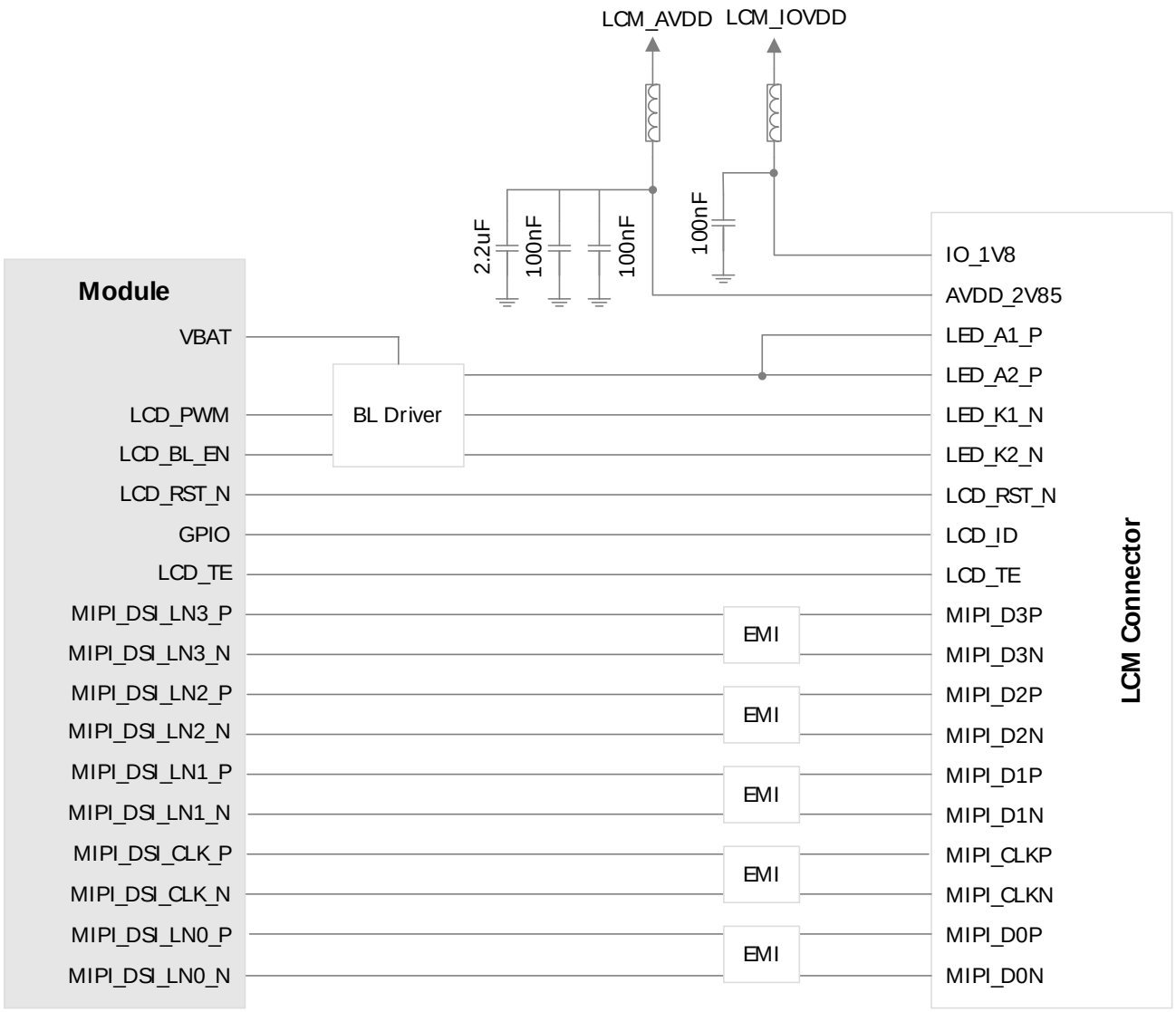

Figure 15. Reference schematic of LCD interface circuit

Precautions for LCD design are as follows:

- It is recommended to connect the common mode inductor in series near the LCD connector to reduce EMI.
- The MIPI signal line needs to be controlled with a 100Ω differential impedance with tolerance ±10%.
- The length difference of the differential line within the group is controlled within 0.7 mm, and the length difference between the groups is controlled within 1.4 mm.
- It is recommended that the space of intra-lane differential line should be 1 times of the route width and the space between differential line and other routes should be controlled 2.5 times of the route width.

4.12 Touch Panel

Module provides one set of I2C interfaces that can be used to connectthe TP and it provides power supply, interrupt and reset pins required by the TP. Please refer to the pin description section for pin definition.

The TP circuit reference design is shown as follows:

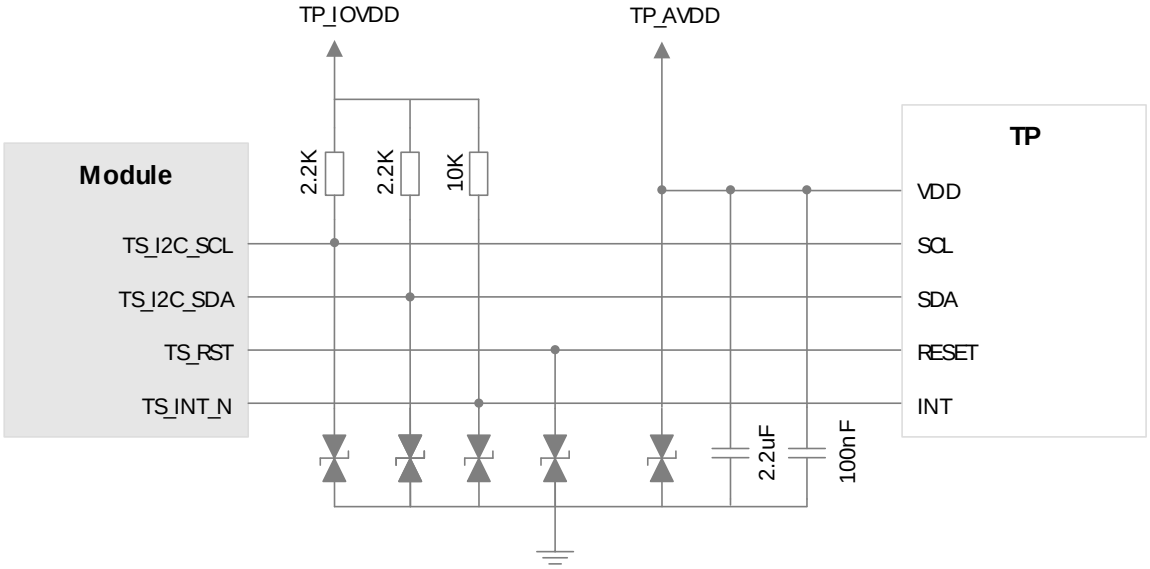

Figure 16. Reference schematic of TP circuit

4.13 Camera

The camera interface of the module is based on the MIPI_CSI standard and can support four camera combinations (4 lane+4 lane+2 lane+1 lane).

Please refer to the pin description section for pin definition.

The camera circuit reference design is shown in the following figure.

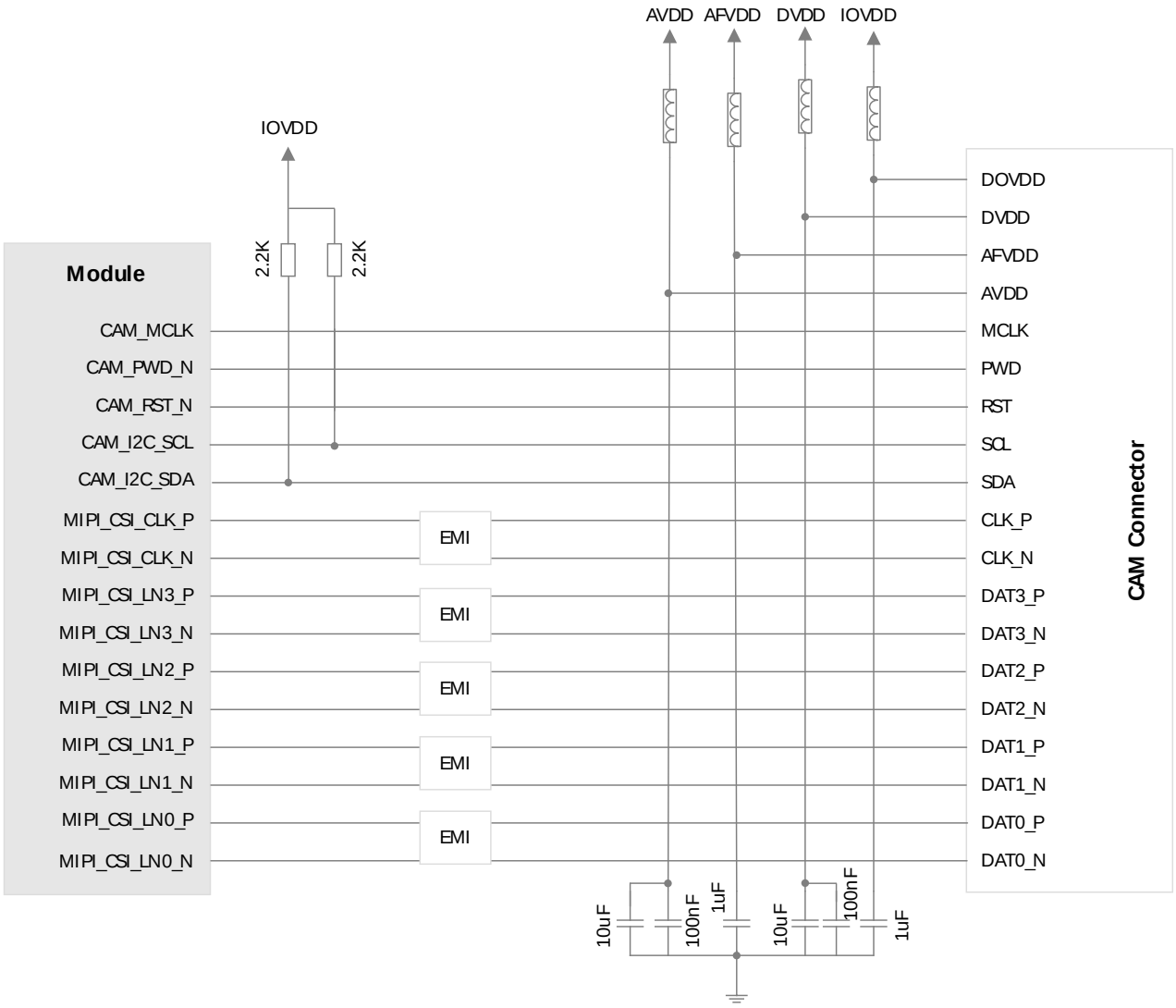

Figure 17. Reference schematic of camera circuit

Design Guidelines of Camera

MIPI_CSI is a high-speed signal. Pay attention to the following points during PCB layout:

- It is recommended to connect a common-mode inductor in series on the MIPI high-speed signal line near the camera connector end to reduce EMI.
- MIPI routing is recommended to be designed in the inner layer, and connected using GND in three dimensions.
- The MIPI signal line needs to be controlled with a 100Ω differential impedance with tolerance ±10%.
- The length difference of differential lines in MIPI signal line groups shall be controlled within 0.7 mm, and the length difference between groups shall be controlled within 1.4 mm.
- It is recommended that the space of intra-lane differential line should be 1 times of the route width and the space between differential line and other routes should be controlled 2.5 times of the route width.

Precautions for design of other signal lines:

- CAM_MCLK is a high-speed clock signal and requires three-dimensional grounding.
- AVDD and DVDD of camera power supply shall be routed away from interference sources to avoid

introducing power supply noise. It is recommended to add LDO with high power supply noise rejection ratio.

- If the cameras are to share I2C, select two cameras that do not work at the same time, and make sure that the two cameras have different addresses.

4.14 Audio

The module supports three analog input interfaces and three analog output interfaces. Please refer to the pin description section for pin definition.

The reference design of ECM type microphone differential input is as follows:

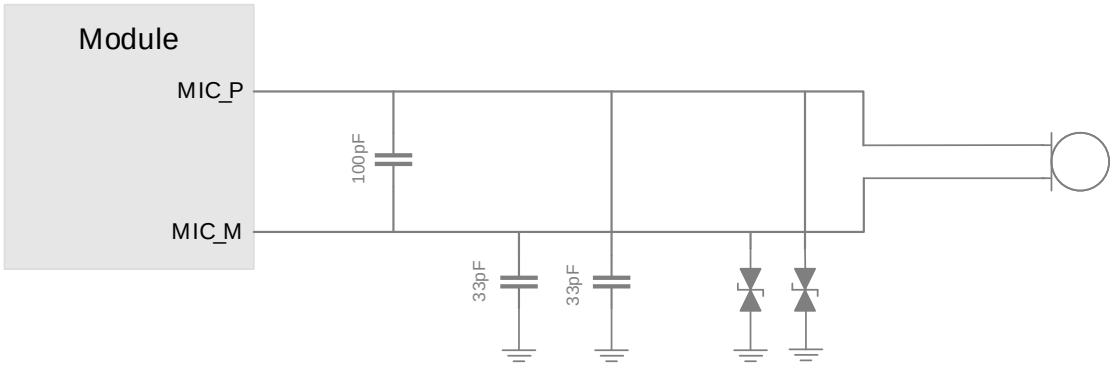

Figure 18. Reference schematic of MIC circuit

The reference design of the earphone is as follows:

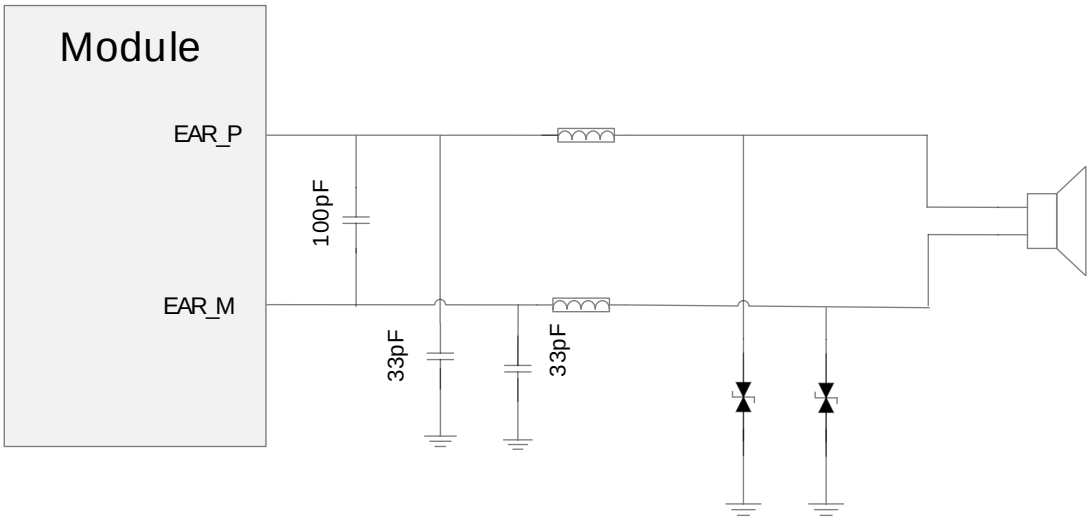

Figure 19. Reference schematic of receiver circuit

The reference circuit of speaker is as follows:

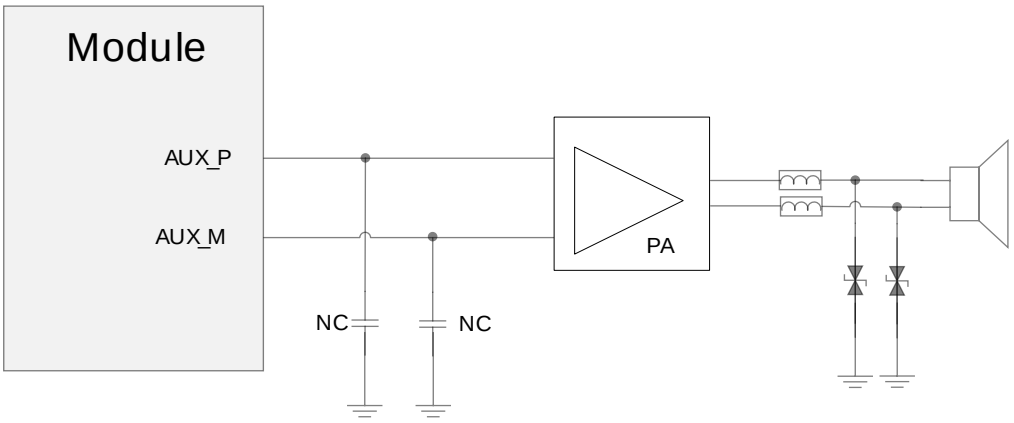

Figure 20. Reference schematic of speaker circuit

The reference design of the headphone is as follows:

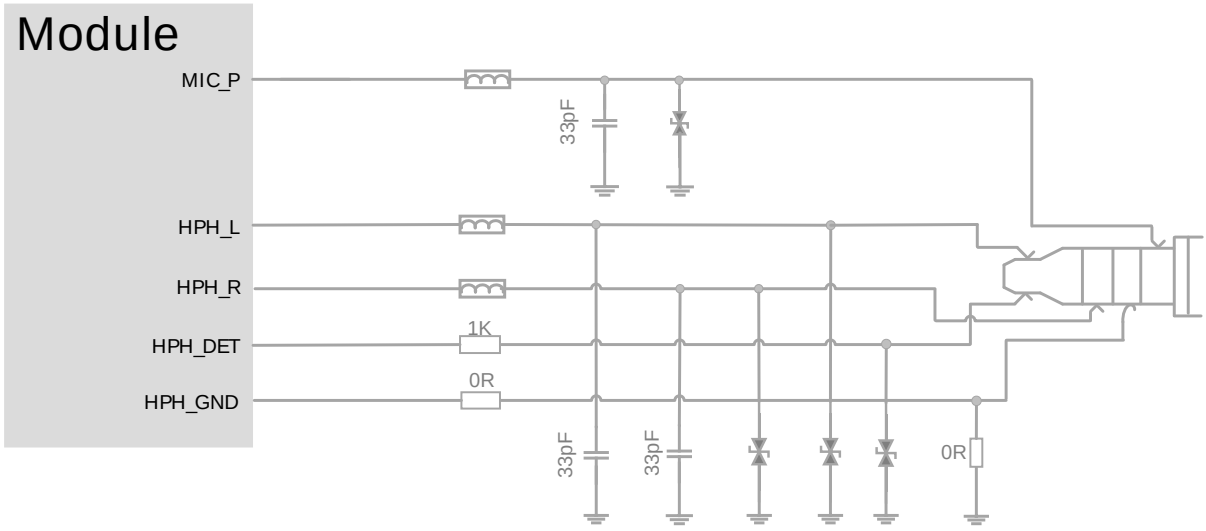

Figure 21. Reference schematic of headphone circuit

Design guidelines of audio interface:

- Module has MIC bias circuit internally, and no external circuit is required. Only supports ECM microphones.
- A set of Class-AB differential AUX PA output cannot directly drive the speaker, and audio power amplifier is required when in use.
- Both the receiver and AUX PA output are of differential type and must follow the differential routing principles.
- Keep audio routes away from radiation and interference sources, such as antennas or power supplies.

5 Antenna Interfaces

5.1 Definition of Antenna Interfaces

Table 29. Definition of antenna interfaces

Pin No.	Pin Name	Function Description	TX	RX	Frequency Range
94	ANT_MAIN	GSM&WCDMA&LTE(LB/MB/HB TRX)	GSM: 850/900/1800/1900 WCDMA: B1/B2/B4/B5/B6/B8/B9/B19 LTE-FDD: B1/B2/B3/B4/B5/B7/B8/B12/B13/B17/B18/B19/B20/B25/B26/B28/B66/B71 LTE-TDD: B34/B38/B39/B40/B41	GSM: 850/900/1800/1900 WCDMA: B1/B2/B4/B5/B6/B8/B9/B19 LTE-FDD: B1/B2/B3/B4/B5/B7/B8/B12/B13/B17/B18/B19/B20/B25/B26/B28/B66/B71 LTE-TDD: B34/B38/B39/B40/B41	617MHz-2689.9MHz
132	ANT_DRX	LTE(LB/MB/HB DRX)	--	LTE-FDD: B1/B2/B3/B4/B5/B7/B8/B12/B13/B17/B18/B19/B20/B25/B26/B28/B66/B71 LTE-TDD: B34/B38/B39/B40/B41	617MHz-2689.9MHz
120	ANT_GNSS	GNSS antenna interface	--	L1	--
78	ANT_WIFI/BT	WI-FI/BT antenna interface	2.4G/5G/BT	2.4G/5G/BT	--

5.2 Operating Frequency

5.2.1 Cellular

Table 30. Reference table of cellular frequency

Mode	Band	TX（MHz）	RX（MHz）
GSM	850	824.2-848.8	869.2-893.8
	900	880.2-914.8	925.2-959.8
	1800	1710.2-1784.8	1805.2-1879.8
	1900	1850.2-1909.8	1930.2-1989.8
WCDMA	Band 1	1922.4-1977.6	2112.4-2167.6
	Band 2	1852.4-1907.6	1932.4-1987.6
	Band 4	1712.4-1752.6	2112.4-2152.6
	Band 5	826.4-846.6	871.4-891.6
	Band 6	832.4-837.6	877.4-882.6
	Band 8	882.4-912.6	927.4-957.6
	Band 9	1752.4-1782.4	1847.4-1877.4
	Band 19	832.4-842.6	877.4-887.6
LTE FDD	Band 1	1920-1979.9	2110-2169.9
	Band 2	1850-1909.9	1930-1989.9
	Band 3	1710-1784.9	1805-1879.9
	Band 4	1710-1754.9	2110-2154.9
	Band 5	824-848.9	869-893.9
	Band 7	2500-2569.9	2620-2689.9
	Band 8	880-914.9	925-959.9
	Band 12	699-715.9	729-745.9
	Band 13	777-786.9	746-755.9
	Band 17	704-715.9	734-745.9

Mode	Band	TX (MHz)	RX (MHz)
	Band 18	815-829.9	860-874.9
	Band 19	830-844.9	875-889.9
	Band 20	832-861.9	791-820.9
	Band 25	1850-1914.9	1930-1994.9
	Band 26	814-848.9	859-893.9
	Band 28	703-747.9	758-802.9
	Band 66	1710-1779.9	2110-2179.9
	Band 71	663-697.9	617-651.9
LTE TDD	Band 34	2010-2024.9	2010-2024.9
	Band 38	2570-2619.9	2570-2619.9
	Band 39	1880-1919.9	1880-1919.9
	Band 40	2300-2399.9	2300-2399.9
	Band 41	2496-2689.9	2496-2689.9

5.2.2 WIFI

The module supports 2.4G/5G WLAN wireless communication, and supports 802.11a, 802.11b, 802.11g, 802.11n and 802.11ac. The maximum throughput is 433Mbps with the following characteristics:

- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode
- Support WAPI
- Support AP mode
- Support Wi-Fi Direct
- 2.4G band supports CCK, OFDM, HT20 and HT40
- 5G band supports OFDM, VHT20, VHT40, VHT80.
- Test condition: 3.8V power supply, environment temperature of 25°C

Table 31. WIFI transmitting power

Frequency	Mode	Date Rate	Bandwidth (MHz)	TX Power (dBm)
2.4G	802.11b	1Mbps	20	17 ±3
		11Mbps	20	17 ±3

Frequency	Mode	Date Rate	Bandwidth (MHz)	TX Power (dBm)
5G	802.11g	6Mbps	20	17 ±3
		54Mbps	20	15 ±3
	802.11n	MCS0	20	15 ±3
		MCS7	20	12 ±3
		MCS0	40	15 ±3
		MCS7	40	12 ±3
	802.11a	6Mbps	20	15 ±3
		54Mbps	20	13 ±3
	802.11n	MCS0	20	14 ±3
		MCS7	20	12 ±3
		MCS0	40	13 ±3
		MCS7	40	12 ±3
	802.11ac	MCS0	20	13 ±3
		MCS8	20	12 ±3
		MCS0	40	13 ±3
		MCS9	40	11±3
		MCS0	80	13 ±3
		MCS9	80	9±3

Table 32. WIFI receiving sensitivity

Frequency	Mode	Date Rate	Bandwidth (MHz)	Sensitivity (dBm)
2.4G	802.11b	1Mbps	20	-90
		11Mbps	20	-86
	802.11g	6Mbps	20	-87
		54Mbps	20	-72
	802.11n	MCS0	20	-86
		MCS7	20	-68

Frequency	Mode	Date Rate	Bandwidth (MHz)	Sensitivity (dBm)
		MCS0	40	TBD
		MCS7	40	TBD
5G	802.11a	6Mbps	20	-88
		54Mbps	20	-72
	802.11n	MCS0	20	-87
		MCS7	20	-68
		MCS0	40	-84
		MCS7	40	-65
	802.11ac	MCS0	20	-88
		MCS8	20	-65
		MCS0	40	-85
		MCS9	40	-62
		MCS0	80	-82
		MCS9	80	-58

Microstrip line is recommended for RF routing of WIFI antenna. The insertion loss of 2.4G band is controlled within 0.2dB, the insertion loss of 5G band is controlled within 0.8dB, and the impedance is controlled within 50Ω.

Table 33. WIFI operating frequency

Mode	Frequency	Unit
2.4G	2402 to 2482	MHz
5G	5170 to 5835	MHz

5.2.3 Bluetooth

The module supports BT5.0 (BR/EDR+BLE) standard. The modulation method supports GFSK, 8-DPSK and π/4-DQPSK. The BR/EDR channel bandwidth is 1MHz and can accommodate 79 channels. The BLE bandwidth is 2MHz and can accommodate 40 channels. Its main features are as follows:

- BT 4.2+BR/EDR+BLE
- Support for ANT protocol
- Support for BT-WLAN coexistence operation, including optional concurrent receive

- Up to 3.5 piconets (master, slave and page scanning)

Table 34. BT rate and version information

Version	Date Rate	Throughput	Note
BT1.2	1Mbit/s	> 80Kbit/s	- -
BT2.0+EDR	3Mbit/s	> 80Kbit/s	- -
BT3.0+HS	24Mbit/s	Refer to 3.0+HS	- -
BT4.2 LE	24Mbit/s	Refer to 4.2 LE	- -
BT5.0 LE	24Mbit/s	Refer to 5.0 LE	- -

Test condition: 3.8V power supply, environment temperature of 25°C

Table 35. BT performance indicator

Type	DH-5	2-DH5	3-DH5	BLE	Unit
Transmitter	10 ±2.5	9 ±2.5	9 ±2.5	6 ±2.5	dBm
Sensitivity	-86	-84	-82	-90	dBm

- The sensitivity here is a typical value. Microstrip line is recommended for the RF routing of Bluetooth antenna, with insertion loss within 0.2dB and impedance at 50Ω.

Table 36. BT operating frequency

Mode	Frequency	Unit
Bluetooth	2402 to 2480	MHz

5.2.4 GNSS

The module supports multiple positioning systems including GPS/Beidou/GLONASS. The module is embedded with LNA, which can effectively improve the sensitivity of GNSS. LNA is embedded in the module, which can effectively improve the sensitivity of GNSS. Test condition: 3.8V power supply, environment temperature of 25°C

Table 37. GNSS positioning performance

Parameter	Description	Typical Result	Unit
Sensitivity	Acquisition	-157	dBm

Parameter	Description	Typical Result	Unit
	Tracking	-146	dBm
C/N	-130dBm	39	dB-Hz
TTFF	Cold Start	44	s
	Warm Start	44	s
	Hot Start	3	s
CEP	Static accuracy (95% @-130dBm)	5	m

Table 38. GNSS operating frequency

Mode	**Frequency**	**Unit**
GPS	1575.42±1.023	MHz
GLONASS	1597.5-1605.9	MHz
BeiDou	1561.098±2.046	MHz
Galileo	1575.42±2.02	MHz
QZSS	1575.42±1.023	MHz

5.3 Antenna Design Circuit

The following figure shows an antenna circuit for a cellular network:

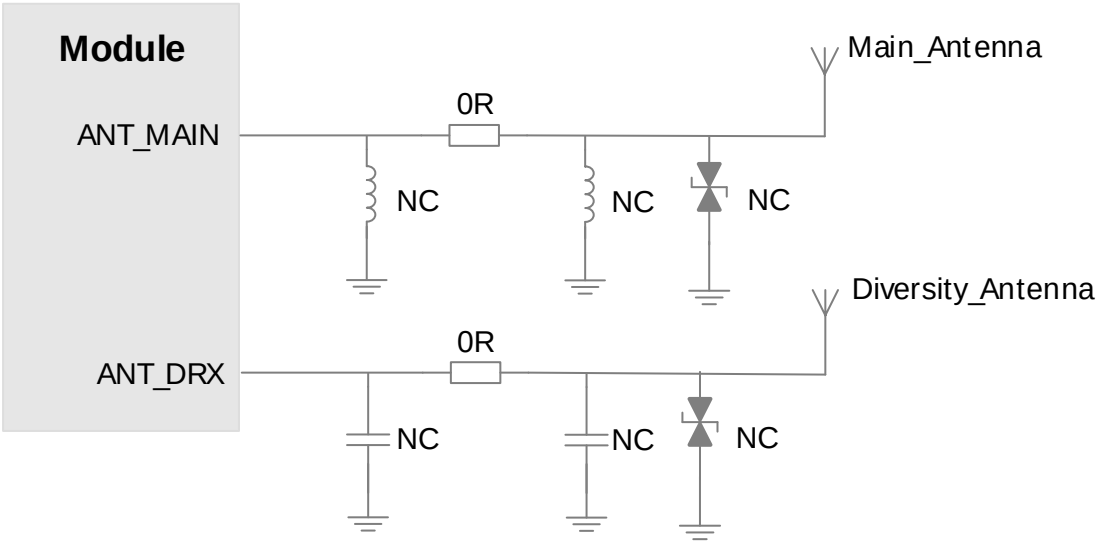

Figure 22. Reference circuit of cellular network antenna

The module has a built-in LNA. The passive antenna is used in the design of the device. Microstrip line is recommended for the GNSS RF routing, with insertion loss within 0.2dB and impedance at 50Ω.

The power supply of the active antenna is fed from the signal line of the antenna through the 56nH inductor. The common active antenna is powered by 3.3V to 5.0V. The power consumption of the active antenna is very small, but the power supply is required to be stable and clean. It is recommended to use LDO with high performance to supply power to the antenna. The active antenna gain is required to be less than 17dB. If the gain is greater than 17dB, the reserved π-type matching needs to be used to increase the attenuation network.

The following figures show the reference circuits of GNSS antenna.

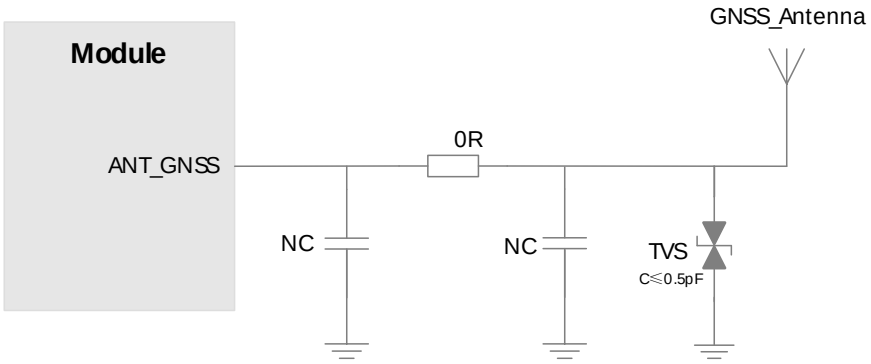

Figure 23. Reference circuit of GNSS passive antenna

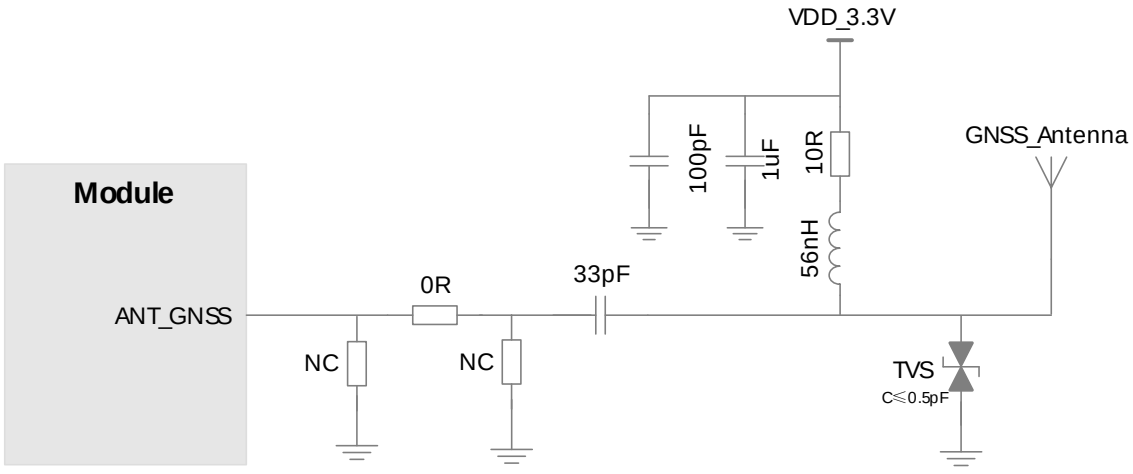

Figure 24. Reference circuit of GNSS active antenna

5.4 Antenna Performance Requirements

Table 39. Antenna performance requirements

Standard	Antenna Performance Requirement
WCDMA/LTE/NR	VSWR: ≤ 2 Gain (dBi): 1 Max input power (W): 5 Input impedance (Ω): 50 Polarization type: vertical direction Insertion loss: < 1dB (0.7GHz to 1GHz) Insertion loss: < 1.5dB (1.4GHz to 2.2GHz) Insertion loss: < 2dB (2.3GHz to 5GHz)
WIFI/BT	VSWR: ≤ 2 Gain (dBi): 1 Max input power (W): 5 Input impedance (Ω): 50 Polarization type: vertical direction Insertion loss: < 2dB
GNSS	Frequency range: 1559MHz to 1607MHz Polarization type: right-circular or linear polarization VSWR: < 2 (typical value) Passive antenna gain: > 0dBi Active antenna NF: < 1.5dB (typical value) Active antenna gain: > -2dBi
Isolation between GPS and MAIN antennas:	> 20dB
Isolation between WIFI and MAIN antennas:	> 20dB

5.5 PCB Layout Reference Design

In practical applications, the shorter the RF microstrip trace, the better. Impedance is usually closely related to the width (W) and thickness of the trace, the height (H) of the reference layer, the spacing (S) between the trace and the left and right sides of the ground, and the dielectric constant of the material. The impedance control model of RF microstrip line is divided into planar reference model and coplanar impedance model. Generally, if the planar reference model can meet the requirements, the coplanar impedance model should not be used.

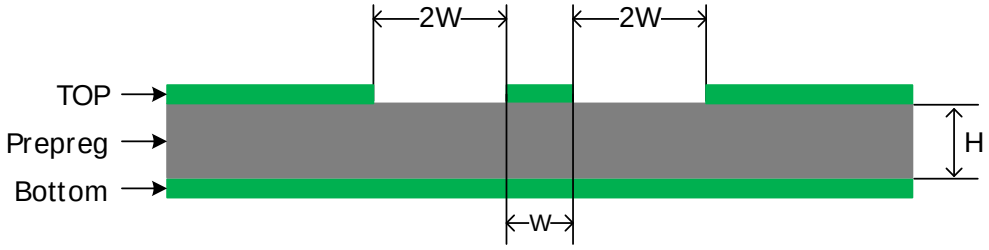

Figure 25. Planar reference model for a two-layer board

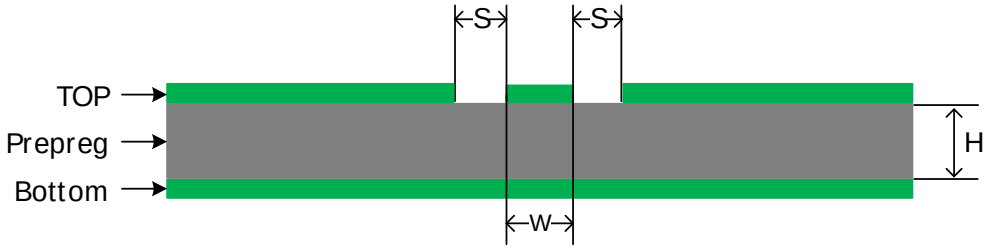

Figure 26. Coplanar impedance model for a two-layer board

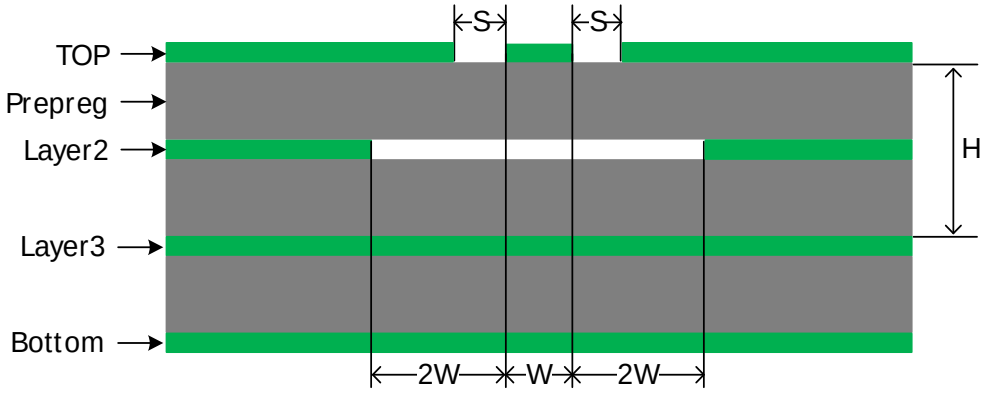

Figure 27. Coplanar impedance model for a four-layer board

The design rules are as follows:

- The RF trace impedance is controlled to 50Ω, and the reference ground must be kept intact.
- The RF routing should be curved as far as possible, and both sides of the routing should be protected by vias. The distance between vias and traces should be greater than 2 times the line width.
- There should be clearance below the RF connector, and the RF routing should be far away from the interference source to avoid crossing and paralleling with the interference source.

6 Electrical Features

6.1 Normal Operating Voltage

The following table shows the normal operating voltage range of the module, and all the performance indicators of the module are guaranteed within this operating voltage range.

Table 40. Operating voltage

Parameter	Min	Normal	Max	Unit
VBAT	3.5	3.8	4.35	V
VRTC	2.0	3.0	3.25	V
USB_IN_DET	3	5	18	V

6.2 Absolute Maximum Voltage

The following table shows the absolute maximum rated parameters of the module, which can cause permanent damage to the device if it exceeds the absolute maximum parameter range.

Table 41. Absolute maximum parameters

Parameter	Min	Max	Unit
VBAT	-0.3	6	V

6.3 Operating Temperature and Storage Temperature

Table 42. Operating temperature and storage temperature

Parameter	Min	Max	Unit
Operating ambient temperature	-30	75	°C
Storage temperature	-40	85	°C

6.4 Power Consumption

The power consumption measurement is closely related to the operating state of the module, and the test conditions are as follows:

The ambient temperature is 25°C and the power supply voltage is 3.8V.

Table 43. Operating current[2)]

Parameter	Description	Condition	Typical Result	Unit
I_{off}	Quiescent leakage current	Power on and won't turn on	50	uA
	Soft shutdown leakage current	When the module is powered on, the AT command is turned off or the pop-up box option is selected to shut down	40	
I_{sleep}	Radio Off	Airplane mode standby	4.5	mA
	GSM	MFRMS=5	8	
	WCDMA	DRX=8	8	
	LTE FDD	DPC (Default Paging Cycle)=#256	8	
	LTE TDD	DPC (Default Paging Cycle)=#256	8	
$I_{GSM-RMS}$	GSM voice RMS Current	GSM850@ PCL=5	350	mA
		GSM850@ PCL=19	150	
		EGSM900@ PCL=5	350	
		EGSM900@ PCL=19	150	
		DCS1800@ PCL=0	200	
		DCS1800@ PCL=15	150	
		PCS1900@ PCL=0	200	
		PCS1900@ PCL=15	150	
$I_{GSM-MAX}$	GSM voice Peak Current	GSM850@ PCL=5	2500	mA
		EGSM900@ PCL=5	2700	
		DCS1800@ PCL=0	1400	
		PCS1900@ PCL=0	1600	
$I_{GPRS-RMS}$	GPRS data RMS Current	GSM850@Gamma=3(1UL/1DL)	300	mA
		GSM850@Gamma=3(4UL/1DL)	700	
		EGSM900@Gamma=3(1UL/1DL)	300	
		EGSM900@Gamma=3(4UL/1DL)	800	

Parameter	Description	Condition	Typical Result	Unit
		DCS1800@Gamma=3(1UL/1DL)	200	
		DCS1800@Gamma=3(4UL/1DL)	400	
		PCS1900@Gamma=3(1UL/1DL)	200	
		PCS1900@Gamma=3(4UL/1DL)	400	
$I_{EGPRS-RMS}$	EGPRS data RMS Current	GSM850@Gamma=6(1UL/1DL)	200	mA
		GSM850@Gamma=6(4UL/1DL)	500	
		EGSM900@Gamma=6(1UL/1DL)	250	
		EGSM900@Gamma=6(4UL/1DL)	500	
		DCS1800@Gamma=5(1UL/1DL)	200	
		DCS1800@Gamma=5(4UL/1DL)	400	
		PCS1900@Gamma=5(1UL/1DL)	200	
		PCS1900@Gamma=5(4UL/1DL)	400	
$I_{WCDMA-RMS}$	WCDMA RMS Current	Band 1 @ max power	600	mA
		Band 2 @ max power	600	
		Band 4 @ max power	600	
		Band 5 @ max power	600	
		Band 6 @ max power	650	
		Band 8 @ max power	600	
		Band 9 @ max power	700	
		Band 19 @ max power	650	
$I_{LTE-RMS}$	LTE FDD RMS Current	Band 1 @max power(10MHz,1RB)	700	mA
		Band 2 @max power(10MHz,1RB)	650	
		Band 3 @max power(10MHz,1RB)	650	
		Band 4 @max power(10MHz,1RB)	700	
		Band 5 @max power(10MHz,1RB)	700	
		Band 7 @max power(10MHz,1RB)	800	

Parameter	Description	Condition	Typical Result	Unit
		Band 8 @max power(10MHz,1RB)	700	
		Band 12 @max power(10MHz,1RB)	700	
		Band 13 @max power(10MHz,1RB)	700	
		Band 17 @max power(10MHz,1RB)	700	
		Band 18 @max power(10MHz,1RB)	700	
		Band 19 @max power(10MHz,1RB)	700	
		Band 20 @max power(10MHz,1RB)	700	
		Band 25 @max power(10MHz,1RB)	700	
		Band 26 @max power(10MHz,1RB)	700	
		Band 28 @max power(10MHz,1RB)	700	
		Band 66 @max power(10MHz,1RB)	700	
		Band 71 @max power(10MHz,1RB)	700	
	LTE TDD RMS Current	Band 34 @max power(10MHz,1RB)	450	
		Band 38 @max power(10MHz,1RB)	500	
		Band 39 @max power(10MHz,1RB)	450	
		Band 40 @max power(10MHz,1RB)	450	
		Band 41 @max power(10MHz,1RB)	500	

The above power consumption data is the test result of SC208-GL-20. On this basis, the power consumption of memory increases by 1mA for each additional specification.

6.5 Maximum Transmitting Power

The maximum transmitting power is the transmitting power measured at the antenna pin at an ambient temperature of 25°C. Users should fully consider the insertion loss on the RF path when designing, so as to avoid excessive insertion loss affecting TRP indicators. The maximum transmitting power of the module is as follows:

Test conditions: power supply voltage of 3.8V, ambient temperature of 25□, LTE maximum power test 10M bandwidth 12RB.

Table 44. RF transmitting power

Mode	Band	Max Power(dBm)	Min Power(dBm)
GSM	850(GMSK)	33±2	5±5
	900(GMSK)	33±2	5±5
	1800(GMSK)	30±2	0±5
	1900(GMSK)	30±2	0±5
GSM	850(8PSK)	27.0±3	5±5
	900(8PSK)	27.0±3	5±5
	1800(8PSK)	26.0±3	0±5
	1900(8PSK)	26.0±3	0±5
WCDMA	Band 1	24+1/-3	<-49
	Band 2	24+1/-3	<-49
	Band 4	24+1/-3	<-49
	Band 5	24+1/-3	<-49
	Band 6	24+1/-3	<-49
	Band 8	24+1/-3	<-49
	Band 9	24+1/-3	<-49
	Band 19	24+1/-3	<-49
LTE FDD	Band 1	23.0±2	<-39
	Band 2	23.0±2	<-39
	Band 3	23.0±2	<-39
	Band 4	23.0±2	<-39
	Band 5	23.0±2	<-39
	Band 7	23.0±2	<-39
	Band 8	23.0±2	<-39
	Band 12	23.0±2	<-39
	Band 13	23.0±2	<-39

Mode	Band	Max Power(dBm)	Min Power(dBm)
	Band 17	23.0±2	<-39
	Band 18	23.0±2	<-39
	Band 19	23.0±2	<-39
	Band 20	23.0±2	<-39
	Band 25	23.0±2	<-39
	Band 26	23.0±2	<-39
	Band 28	23.0±2	<-39
	Band 66	23.0±2	<-39
	Band 71	23.0±2	<-39
LTE TDD	Band 34	23.0±2	<-39
	Band 38	23.0±2	<-39
	Band 39	23.0±2	<-39
	Band 40	23.0±2	<-39
	Band 41	23.0±2	<-39

6.6 Receiving Sensitivity

Receiving sensitivity is the receiving sensitivity of the module measured at the antenna pin at an ambient temperature of 25°C. Users should fully consider the insertion loss on the RF path when designing, so as to avoid excessive insertion loss affecting TIS indicators. The receiving sensitivity of the module is as follows:

Test conditions: power supply of 3.8V and environment temperature of 25°C

Table 45. RF Receiving Sensitivity (typical)

Mode	Band	Primary	Diversity	PRX+Div	3GPP Requirement	Unit
GSM	850	-108	N/A	N/A	-102.0	dBm
	900	-108	N/A	N/A	-102.0	dBm
	1800	-108	N/A	N/A	-100.0	dBm
	1900	-108	N/A	N/A	-100.0	dBm

WCDMA	Band 1	-108	N/A	N/A	-106.7	dBm
	Band 2	-109	N/A	N/A	-104.7	dBm
	Band 4	-108	N/A	N/A	-106.7	dBm
	Band 5	-108	N/A	N/A	-104.7	dBm
	Band 6	-108	N/A	N/A	-106.7	dBm
	Band 8	-109	N/A	N/A	-103.7	dBm
	Band 9	-108	N/A	N/A	-105.7	dBm
	Band 19	-108	N/A	N/A	-106.7	dBm
LTE-FDD (10M)	Band 1	-97.5	-99	-100	-96.3	dBm
	Band 2	-98	-99	-100.5	-94.3	dBm
	Band 3	-96.5	-98.5	-99	-93.3	dBm
	Band 4	-97	-99	-99.5	-96.3	dBm
	Band 5	-98	-99	-100.5	-94.3	dBm
	Band 7	-96.5	-97.5	-99	-94.3	dBm
	Band 8	-98	-99	-100	-93.3	dBm
	Band 12	-98	-99	-100	-93.3	dBm
	Band 13	-97.5	-99	-100	-93.3	dBm
	Band 17	-98	-99	-100	-93.3	dBm
	Band 18	-98	-98	-100	-96.3	dBm
	Band 19	-98	-98.5	-100	-96.3	dBm
	Band 20	-98	-98	-100	-93.3	dBm
	Band 25	-98	-99	-100	-92.8	dBm
	Band 26	-98	-98	-100	-93.8	dBm
	Band 28	-98	-98	-100	-94.8	dBm
	Band 66	-97	-99	-99.5	-95.8	dBm
	Band 71	-98	-98.5	-100	-93.5	dBm
LTE-TDD (10M)	Band 34	-97	-98.5	-100	-96.3	dBm

	Band 38	-97	-97.5	-100	-96.3	dBm
	Band 39	-97	-99	-99.5	-96.3	dBm
	Band 40	-97	-98	-99	-96.3	dBm
	Band 41	-97	-97.5	-99	-94.3	dBm

The LTE sensitivity test bandwidth is 10M. Refer to 3GPP for the RB configuration.

6.7 Electrostatic Features

In the application of the module, static electricity generated by human body and static electricity generated by friction between micro-electronics are discharged to the module through various channels and may cause damage to the module. In the process of R&D, production assembly and testing, especially in product design, ESD protection measures should be taken. For example, ESD protection should added at the designed circuit interfaces and at the points susceptible to damage or impact from electrostatic discharge. Anti-static gloves should be worn during production. The ESD protection level at 25□ ambient temperature and 45% humidity is described in the following table.

Table 46. ESD protection level

Test Point	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna interface	±4	±8	kV
Other interface	±0.5	±1	kV

- The data is tested based on the development board of Fibocom.
- ESD performance is strongly related to PCB design, and key control signals should be protected.
- When designing the whole machine, pay attention to maintain the integrity and connectivity of GND.

6.8 Reliability

The reliability test of Fibocom is conducted according to the industrial level. For the reliability test results, refer to *Fibocom_SC208-GL_Industry Standard Reliability Test Report*

6.9 Thermal Design

For more thermal design guidance, refer to *Fibocom_General Thermal Design Guide for Modules.*

7 Structure Specifications

7.1 Product Appearance

Figure 28. Product appearance

7.2 Structure Dimensions

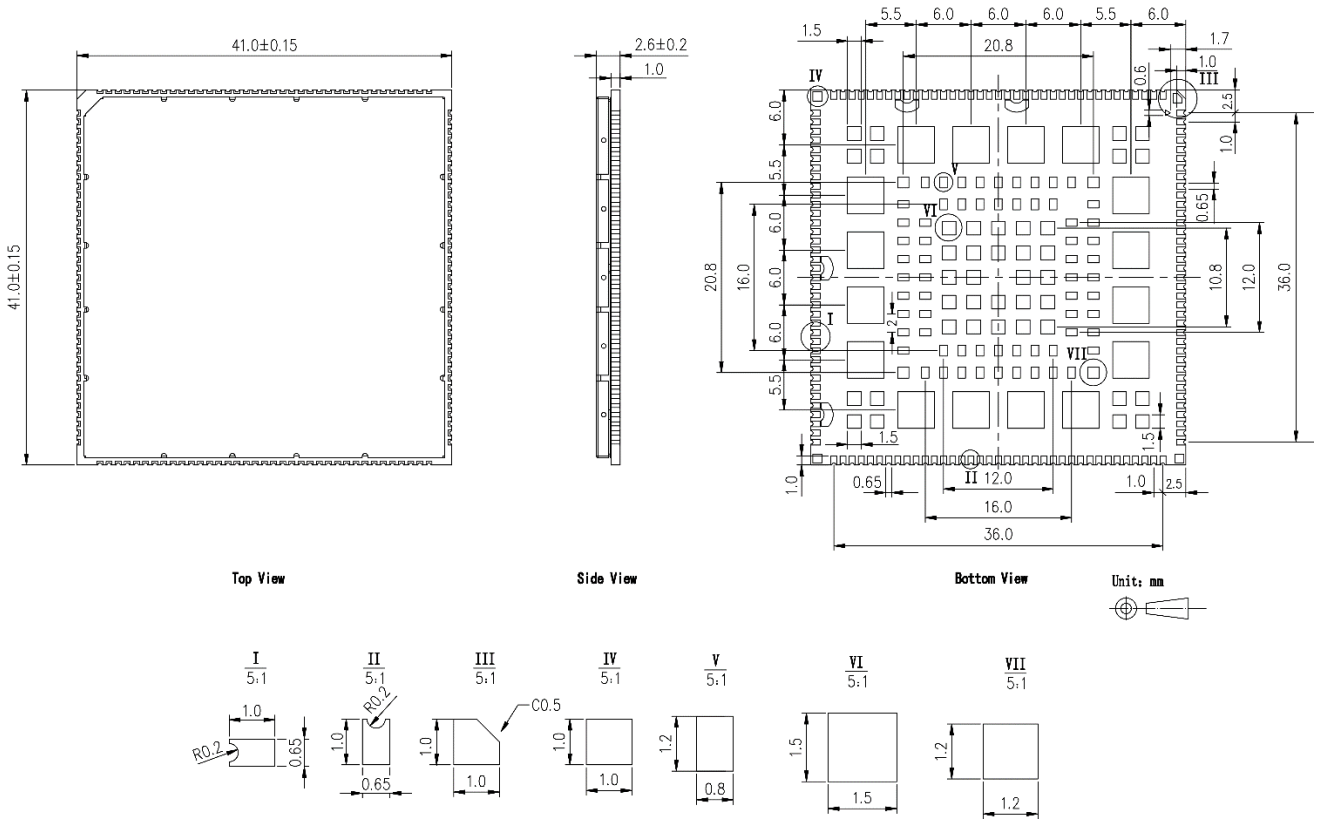

Figure 29. Structure dimensions (unit: mm)

7.3 PCB Package

The following figure shows the PCB package size of the module, and users can design the PCB package by themselves. Fibocom also provides users with a designed document *Fibocom_SC208_ Package*, which can be found in the package.

8 Storage, Production and Packaging

8.1 Storage, Production and Packaging

Refer to the *Fibocom_SC208-GL_SMT Design Guide* for storage, production, and packaging.

Appendix A. Reference Documents

Category	Document Name
Hardware	Fibocom_SC208_CA_ENDC_List
Reference design	Fibocom_SC208_Package
	Fibocom_SC208_Reference Design
Development kit	Fibocom_SC208_ADP User Guide
	Fibocom_EVKB-SOC User Guide
User Guide	Fibocom_Design Guide_RF Antenna
	Fibocom_SC208_SMT Design Guide
	Fibocom_General Thermal Design Guide for Modules

Appendix B. Acronyms and Abbreviations

Acronym and Abbreviation	Description
AMR	Adaptive Multi-rate
bps	Bits Per Second
CS	Coding Scheme
DRX	Discontinuous Reception
FDD	Frequency Division Duplexing
GMSK	Gaussian Minimum Shift Keying
HSDPA	High Speed Down Link Packet Access
IMEI	International Mobile Equipment Identity
Imax	Maximum Load Current
LED	Light Emitting Diode
LSB	Least Significant Bit
LTE	Long Term Evolution
CA	Carrier Aggregation
DLCA	Downlink Carrier Aggregation
SCell	Secondary Cell for CA
ME	Mobile Equipment
MS	Mobile Station
MT	Mobile Terminated
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PSK	Phase Shift Keying

QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized RMS
RMS	Root Mean Square
RTC	Real Time Clock
Rx	Receive
SMS	Short Message Service
TDMA	Time Division Multiple Access
TE	Terminal Equipment
TX	Transmitting Direction
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
USSD	Unstructured Supplementary Service Data
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
VIHmax	Maximum Input High Level Voltage Value
VIHmin	Minimum Input High Level Voltage Valu
VILmax	Maximum Input Low Level Voltage Value
VILmin	Minimum Input Low Level Voltage Value

VImax	Absolute Maximum Input Voltage Value
VImin	Absolute Minimum Input Voltage Value
VOHmax	Maximum Output High Level Voltage Value
VOHmin	Minimum Output High Level Voltage Value
VOLmax	Maximum Output Low Level Voltage Value
VOLmin	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

Hereby, Fibocom Wireless Inc. declares that the radio equipment type [designation of type of radio equipment] is in compliance with Directive 2014/53/EU as well as UK Radio Equipment Regulations SI 2017 No.1206. The full text of the EU/UK declaration of conformity is available at the following internet address: Download Center (fibocom.com) for CE.

Frequency band: 5150 - 5250 MHz:

Indoor use: Inside buildings only. Installations and use inside road vehicles and train carriages are not permitted. Limited outdoor use: If used outdoors, equipment shall not be attached to a fixed installation or to the external body of road vehicles, a fixed infrastructure or a fixed outdoor antenna. Use by unmanned aircraft systems (UAS) is limited to within the 5170 - 5250 MHz band.

Frequency band: 5250 - 5350 MHz:

Indoor use: Inside buildings only. Installations and use in road vehicles, trains and aircraft are not permitted. Outdoor use is not permitted.

Frequency band: 5470 - 5725 MHz:

Installations and use in road vehicles, trains and aircraft and use for unmanned aircraft systems (UAS) are not permitted.

FCC Conformance information

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.

2.This module is limited to installation in mobile applications, according to Part 2.1091(b).

3. The separate approval is required for all other operating configurations, including portable

configurations with respect to Part 2.1093 and different antenna configurations

4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify

compliance as a composite system. When testing the host device for compliance with Part 15

Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while

the transmitter module(s) are installed and operating. The modules should be transmitting and

the evaluation should confirm that the module's intentional emissions are compliant (i.e.

fundamental and out of band emissions). The host manufacturer must verify that there are no

additional unintentional emissions other than what is permitted in Part 15 Subpart B or

emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the

host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described

by the instructions, require that the host product manufacturer must notify to Fibocom Wireless

Inc. that they wish to change the antenna trace design. In this case, a Class II permissive change

application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: ZMOSC208GL” “Contains IC: 21374-SC208GL “ The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,

(2) The transmitter module may not be co-located with any other transmitter or antenna. Part 15 antenna must meet the requirements of FCC Rule §15.203, which requires the use of a permanently attached antenna or of an antenna that uses a unique coupling.

(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

	Antenna Type	Gain (dBi)
BT EDR/BT LE/WLAN 2.4G	Dipole	3.02
RLAN 5G	Dipole	6.30
GSM 850	Dipole	1.32
PCS 1900	Dipole	2.85
WCDMA Band II	Dipole	2.85
WCDMA Band IV	Dipole	2.98
WCDMA Band V	Dipole	1.32
LTE Band 2	Dipole	2.85
LTE Band 4	Dipole	2.98
LTE Band 7	Dipole	2.21
LTE Band 12	Dipole	1.61
LTE Band 13	Dipole	1.83
LTE Band 17	Dipole	1.58
LTE Band 25	Dipole	2.77

LTE Band 26	Dipole	0.7
LTE Band 38	Dipole	1.71
LTE Band 41	Dipole	2.21
LTE Band 66	Dipole	2.98
LTE Band 71	Dipole	1.61

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for

compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90 , part 15B requirements for Modular Approval. The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and 2) The transmitter module may not be co-located with any other transmitter or antenna. As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

11. ISED Conformance information

Industry Canada Statement This device complies with Industry Canada's licence-exempt RSSs.

Operation is subject to the following two conditions:

(1) This device may not cause interference; and

(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

(1) l'appareil ne doit pas produire de brouillage, et

(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled

environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and

2) The transmitter module may not be co-located with any other transmitter or antenna. As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et

2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for reevaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be

installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 21374-SC208GL”.

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 21374-SC208GL ".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module. Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.