FCC ID: YNIJAZWARES15295

Technical Description :

The brief circuit description is listed as follows :
- U1 and associated circuit act as optical mouse sensor.
- U2 and associated circuit act as 2.4GHz RF transceiver module.
- U3 and associated circuit act as MCU.
- U4 and associated circuit act as EEPROM.
- Y2 and associated circuit act as Clock Oscillator of U2.
- Y1 and associated circuit act as Clock Oscillator of U3.

Antenna Used :

A patch antenna has been used.

SGN6210
RF Transceiver/Framer

Production Data Sheet

Product Description:

The Signia SGN6210 IC is a low-cost, fully integrated CMOS radio frequency (RF) transceiver block, combined with a 64-byte buffered framer block. In normal applications, the SGN6210 is connected to a low-cost microcomputer (MCU). The on-chip framer processes and stores the RF data in the background, unloading this critical timing function from the MCU. This lowers MCU speed requirements, expedites product development time, and frees the MCU for implementing additional product features.

The RF transceiver block is a self-contained, fast-hopping GFSK data modem, optimized for use in the widely available 2.4 GHz ISM band. It contains transmit, receive, VCO and PLL functions, including an on-chip channel filter and resonator, thus minimizing the need for external components. The receiver utilizes extensive digital processing for excellent overall performance, even in the presence of interference and transmitter impairments. Transmit power is digitally controlled. The low-IF receiver architecture results in sensitivity to -80 dBm or better, with impressive selectivity.

The framer register settings determine the over-the-air formatting characteristics. Transmit data is easily sent over-the-air as a complete frame of data, with preamble, address, payload, and CRC. Receiving data is just the opposite, using the preamble to train the receiver clock recovery, then the address is checked, then the data is reverse formatted for receive, followed by CRC. All of this is done in hardware to ease the programming and overhead requirements of the baseband MCU.

For longer battery life, power consumption is minimized by automatic enabling of the various transmit, receive, PLL, and PA sections, depending on the instantaneous state of the chip. A sleep mode is also provided for ultra low current consumption.

This product is supplied in lead-free, RoHS compliant, 32-lead 5x5 mm JEDEC standard QFN package, featuring an exposed pad on the bottom for best RF characteristics.

Ordering Information

SGN6210 RF Transceiver/Framer

Signia Technologies, Inc.
500 Yosemite Dr., Suite 100
Milpitas, CA 95035 USA

Phone: (408) 945-9988
FAX: (408) 945-9119
sales@signiatech.com

Key Features:

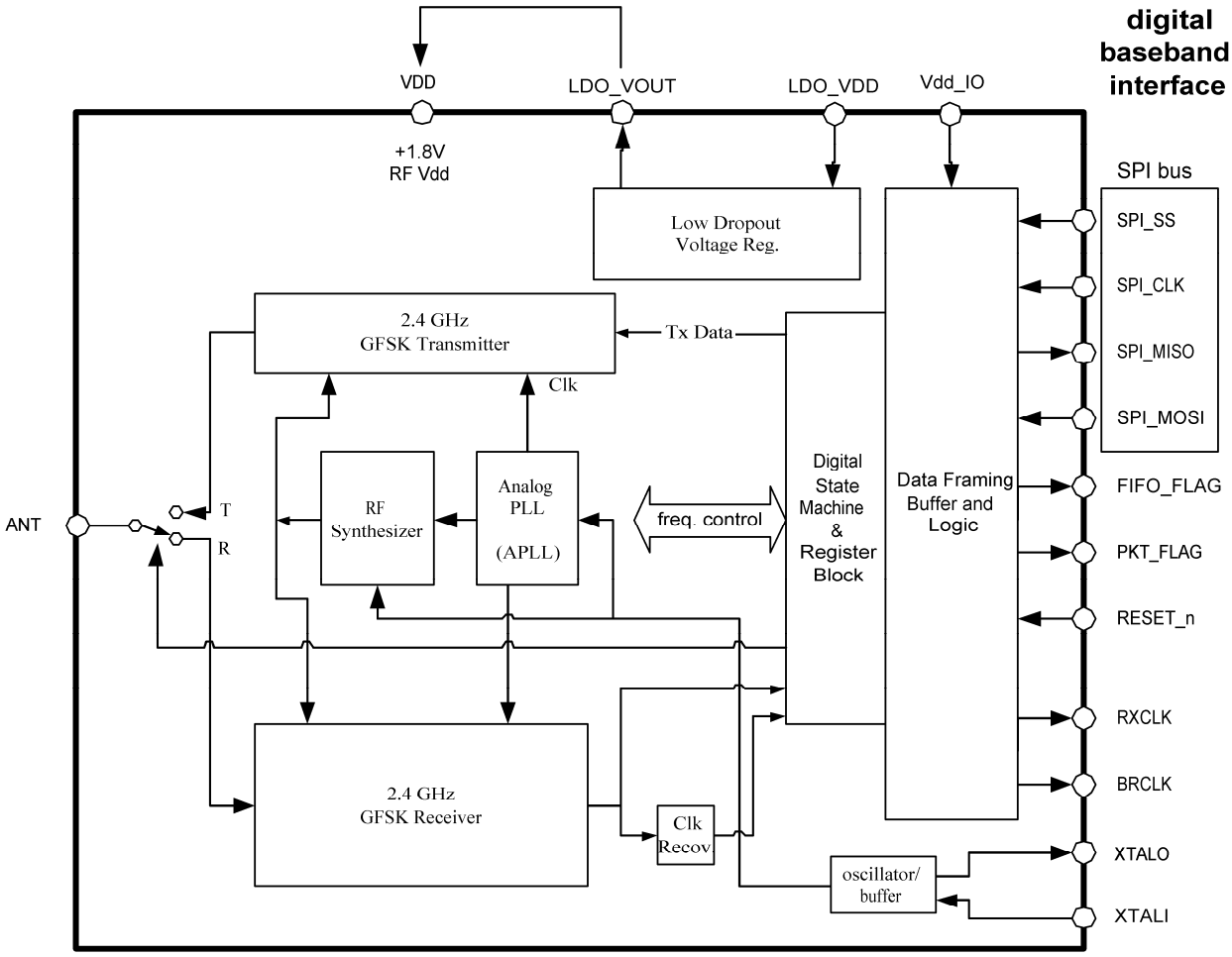
- Combines 2.4 GHz GFSK RF transceiver with 8-bit data framer function
- Eliminates need for external software or hardware FIFO; offloads MCU for other tasks
- Simple microprocessor interface – 4 wires for SPI, plus 3 wires for RST/buffer control
- Each transmit, receive buffer is 64 bytes deep
- Long packets are possible if buffers are read/written before overflow/underflow occurs
- Always 1 Mbps over-the-air symbol rate, regardless of MCU speed or architecture
- Preamble can be 1 to 8 bytes
- Supports 1, 2, 3, or 4 word address (up to 64 bits)
- Various Payload data formats to eliminate DC offset, enhance receive clock recovery and BER
- Programmable data whitening
- Supports Forward Error Correction (FEC): none, 1/3, or 2/3
- Supports 16-bit CRC
- Power management for minimizing current consumption
- Lead-free 5x5mm QFN package with minimum RF parasitics

RoHS Lead Free

Applications:

- Wireless devices that need quick time-to-market
- Battery Powered wireless devices
- Wireless streaming audio
- Home and factory automation
- Simple and fast wireless data networks
- Cordless headsets and Cellular Phones
- Wireless voice and VOIP
- Wireless security and access control

Block Diagram



Ratings

Absolute Maximum Ratings					
Parameter	**Symbol**	**Rating**			**Unit**
		MIN	**TYP**	**MAX**	
Operating Temp.	T_{OP}	-40		+85	°C
Storage Temp.	$T_{STORAGE}$	-55		+125	°C
V_{DD_IO} Supply Volt.	V_{DDIO_MAX}			+3.7	VDC
V_{DD} Supply Volt.	V_{DD_MAX}			+2.5	
Applied Voltages to Other Pins	V_{OTHER}	-0.3		+3.7	VDC
Input RF Level	P_{IN}			+10	dBm
Output Load mismatch (Z_0=50Ω)	$VSWR_{OUT}$			10:1	VSWR

Notes:

1. Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics section below.
2. These devices are electro-static sensitive. Devices should be transported and stored in anti-static containers. Equipment and personnel contacting the devices need to be properly grounded. Cover workbenches with grounded conductive mats.

Electrical Characteristics

The following specifications are guaranteed for T_A = 25 °C, V_{DD} = 1.80 ± 0.18 VDC, unless otherwise noted:

Parameter	Symbol	Specification			Units	Test Condition and Notes
		MIN	TYP	MAX		
Current Consumption						
Current Consumption - TX	I_{DD_TX}		26		mA	P_{OUT} = nominal output power
Current Consumption - RX	I_{DD_RX}		25		mA	
Current Consumption – DEEP IDLE	$I_{DD\_D\_IDLE}$		1.9		mA	RF Synthesizer and VCO: OFF (see Reg. 21)
Current Consumption - SLEEP	I_{DD_SLP}		3.5		uA	
Digital Inputs						
Logic input high	V_{IH}	0.8 V_{DD_io}		V_{DD_io}	V	
Logic input low	V_{IL}	0		0.8	V	
Input Capacitance	$C_{\_IN}$			10	pF	
Input Leakage Current	$I_{\_LEAK\_IN}$			10	uA	
Digital Outputs						
Logic output high	V_{OH}	0.8 V_{DD_io}		V_{DD_io}	V	
Logic output low	V_{OL}			0.4	V	
Output Capacitance	$C_{\_OUT}$			10	pF	
Output Leakage Current	$I_{\_LEAK\_OUT}$			10	uA	
Rise/Fall Time	$T_{\_RISE\_OUT}$			5	nS	
Clock Signals						
BRCLK output frequency	F_{BRCLK}		1, 12, or xtal Freq.		MHz	Depends on Register settings. Always either: 1 MHz Tx clock, 12 MHz APLL clock (Tx, Rx, and Idle), or the buffered 12 MHz crystal oscillator frequency.
SPI_CLK rise, fall time	T_{r_spi}			200	nS	Requirement for error-free register reading, writing.
SPI_CLK frequency range	F_{SPI}	0	12		MHz	
Overall Transceiver						
Operating Frequency Range	$F_{\_OP}$	2400		2482	MHz	
Antenna port mismatch (Z_0=50Ω)	$VSWR_{\_I}$		<2:1		VSWR	Receive mode. Meas. using 50 Ohm balun.
	$VSWR_{\_O}$		<2:1		VSWR	Transmit mode. Meas. using 50 Ohm balun.

Parameter	Symbol	Specification			Units	Test Condition and Notes	
		MIN	TYP	MAX			
Receive Section						**For BER ≤ 0.1%:**	
Receiver sensitivity			-85	-80	dBm	Meas. at ANT pin.	
Maximum useable signal		-20			dBm		
Input 3rd order intercept point	IIP_3	-14	-11		dBm		
Data (Symbol) rate	Ts		1		us		
Min. Carrier/Interference ratio						For BER ≤ 0.1%	
Co-Channel Interference	$CI_{\_cochannel}$		9	11	dB	-60 dBm desired signal.	
Adjacent Ch. Interference, 1MHz offset	$CI_{\_1}$		-1.5	0	dB	-60 dBm desired signal.	
Adjacent Ch. Interference, 2MHz offset	$CI_{\_2}$		-30		dB	-60 dBm desired signal. Interference at 2 MHz below desired signal.	
Adjacent Ch. Interference, ≥ 3MHz offset	$CI_{\_3}$		-40		dB	-67 dBm desired signal.	
Image Frequency Interference	$CI_{\_Image}$		-23	-9	dB	-60 dBm desired signal. Image freq. is always 2 MHz higher than desired signal.	
Adjacent (1MHz) interference to image	$CI_{\_Image\_11}$		-34	-20	dB	-67 dBm desired signal. Always 3 MHz higher than desired signal.	
Out-of-Band Blocking	$OBB_{\_1}$	-10			dBm	30 MHz to 2000 MHz	Meas. with ACX BF2520 ceramic filter on ant. pin. Desired sig. -70 dBm, BER ≤ 0.1%.
	$OBB_{\_2}$	-27			dBm	2000 MHz to 2400 MHz	
	$OBB_{\_3}$	-27			dBm	2500 MHz to 3000 MHz	
	$OBB_{\_4}$	-10			dBm	3000 MHz to 12.75 GHz	
Transmit Section						**Reg. 9, bits 15-8 set to 00000000**	
RF Output Power	P_{AV}		+2		dBm	Power Level 0. Meas. using ACX BL2012 50 Ohm balun.	
Modulation Characteristics							
Peak FM Deviation, 00001111 pattern	$\Delta f1_{avg}$	280	314	350	kHz		
Peak FM Deviation, 01010101 pattern	$\Delta f2_{max}$	230			kHz	For at least 99.9% of all $\Delta f2_{max}$ meas.	
ISI, % Eye Open	$\Delta f2_{avg} / \Delta f1_{avg}$	80			%	1010 data sequence referenced to 00001111 data sequence	
Zero Crossing Error	ZCERR	-125		125	ns	+/- 1/8 of Symbol Period	
In-Band Spurious Emission							
(+/- 550kHz)	IBS_1			-20	dBc		
2MHz offset	IBS_2			-40	dBm		
>3MHz offset	IBS_3			-60	dBm		
Out-of-Band Spurious Emission, Operation	OBS_O_1		< -60	-36	dBm	30 MHz ~ 1 GHz	
	OBS_O_2		-45	-30	dBm	1 GHz ~ 12.75 GHz, excludes desired signal.	
	OBS_O_3		< -60	-47	dBm	1.8 GHz ~ 1.9 GHz	
	OBS_O_4		< -65	-47	dBm	5.15 GHz ~ 5.3 GHz	

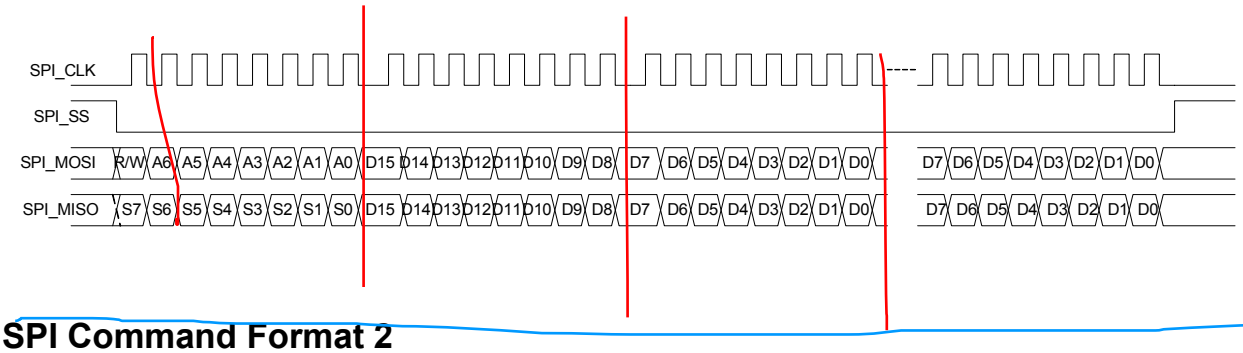
Parameter	Symbol	Specification			Units	Test Condition and Notes	
		MIN	TYP	MAX			
RF VCO and PLL Section							
Typical PLL lock range	F_{LOCK}	2340		2560	MHz		
Tx, Rx Frequency Tolerance			--		ppm	Same as XTAL pins frequency tolerance	
Channel (Step) Size			1		MHz		
SSB Phase Noise			-95		dBc/Hz	550kHz offset	
			-115		dBc/Hz	2MHz offset	
Crystal oscillator freq. range (Reference Frequency)			12		MHz	Designed for 12 MHz crystal reference freq.	
Crystal oscillator digital trim range, typ.		-12		+12	ppm		
RF PLL Settling Time	T_{HOP}		75	150	uS		
Out-of-Band Spur. Emissions	$OBS_{\_1}$		< -75	-57	dBm	30 MHz ~ 1 GHz	IDLE state, Synthesizer and VCO ON.
	$OBS_{\_2}$		-68	-47	dBm	1 GHz ~ 12.75 GHz	
LDO Voltage Regulator Section							
Dropout Voltage	V_{do}			(tbd)	V	Measured during Receive state	
Quiescent current	I_q			6	uA	No-load current consumed by LDO reg.	

Pin Description

Pin No.	Pin Name	Type	Description
1, 2	VDD	PWR	Power supply voltage.
3	NC	--	DO NOT CONNECT. Reserved for factory test.
4	GND	GND	Ground connection.
5	ANT	50Ω RF	RF input/output.
6	VDD	PWR	Power supply voltage.
7, 8	NC	--	DO NOT CONNECT. Reserved for factory test.
9, 10	VDD	PWR	Power supply voltage.
11, 12, 13	NC	--	DO NOT CONNECT. Reserved for factory test.
14	BRCLK	O	Outputs 1MHz Tx symbol clock, 12 MHz APLL, or crystal clock. See register definitions for details.
15	PKT_FLAG	O	Transmit/Receive packet process flag.
16	RXCLK	O	Receiver symbol timing clock recovery output. Fixed at 1 MHz fundamental rate.
17	FIFO_FLAG	O	FIFO full/empty flag.
18	VDD	PWR	Power supply voltage.
19	GND	GND	Ground connection.
20	SPI_SS	I	Enable line for the SPI bus. Active low.
21	SPI_MOSI	I	Data input for the SPI bus.
22	SPI_CLK	I	Clock line for the SPI bus.
23	RESET_n	I	When RESET_n is low, most of the chip shuts down to conserve power. When raised high, RESET_n is used to turn on the chip, restoring all registers to their default value.
24	SPI_MISO	O	Data output for the SPI bus.
25	VDD_IO	PWR	Vdd for the digital i/o pins. Nominally +3.3 VDC.
26	LDO_VDD	PWR	Unregulated input to the on-chip LDO volt. regulator.
27	LDO_VOUT	PWR	+1.8V output of the on-chip LDO voltage regulator.
28	CKPHA	D I	SPI Clock phase. When 0, SPI_MOSI data clocked in on rising edge of SPI_CLK. When 1, SPI_MOSI data clocked in on falling edge of SPI_CLK.
29	GND	GND	Ground connection.
30	VDD	PWR	Power supply voltage.
31	XTALO	A O	Output of the crystal oscillator gain block.
32	XTALI	A I	Input to the crystal oscillator gain block.
Exposed pad	GND	GND	Ground connection.

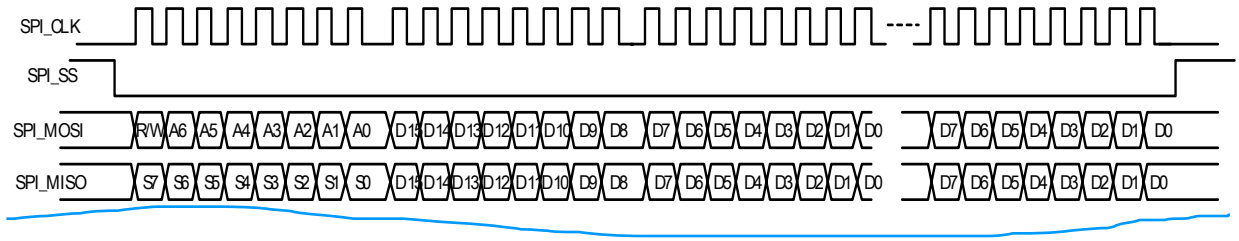
SPI Command Format 1

CKPHA = 0:



SPI Command Format 2

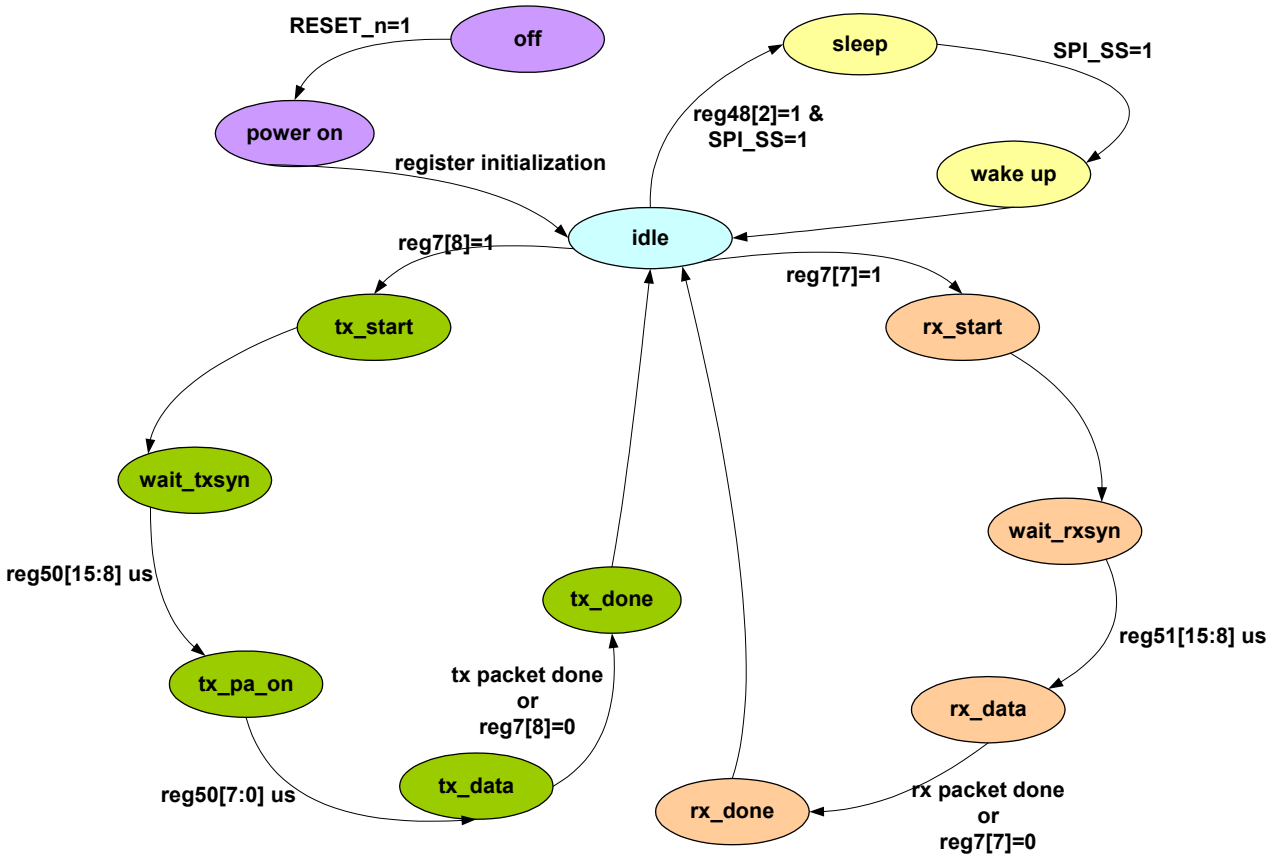
CKPHA = 1:



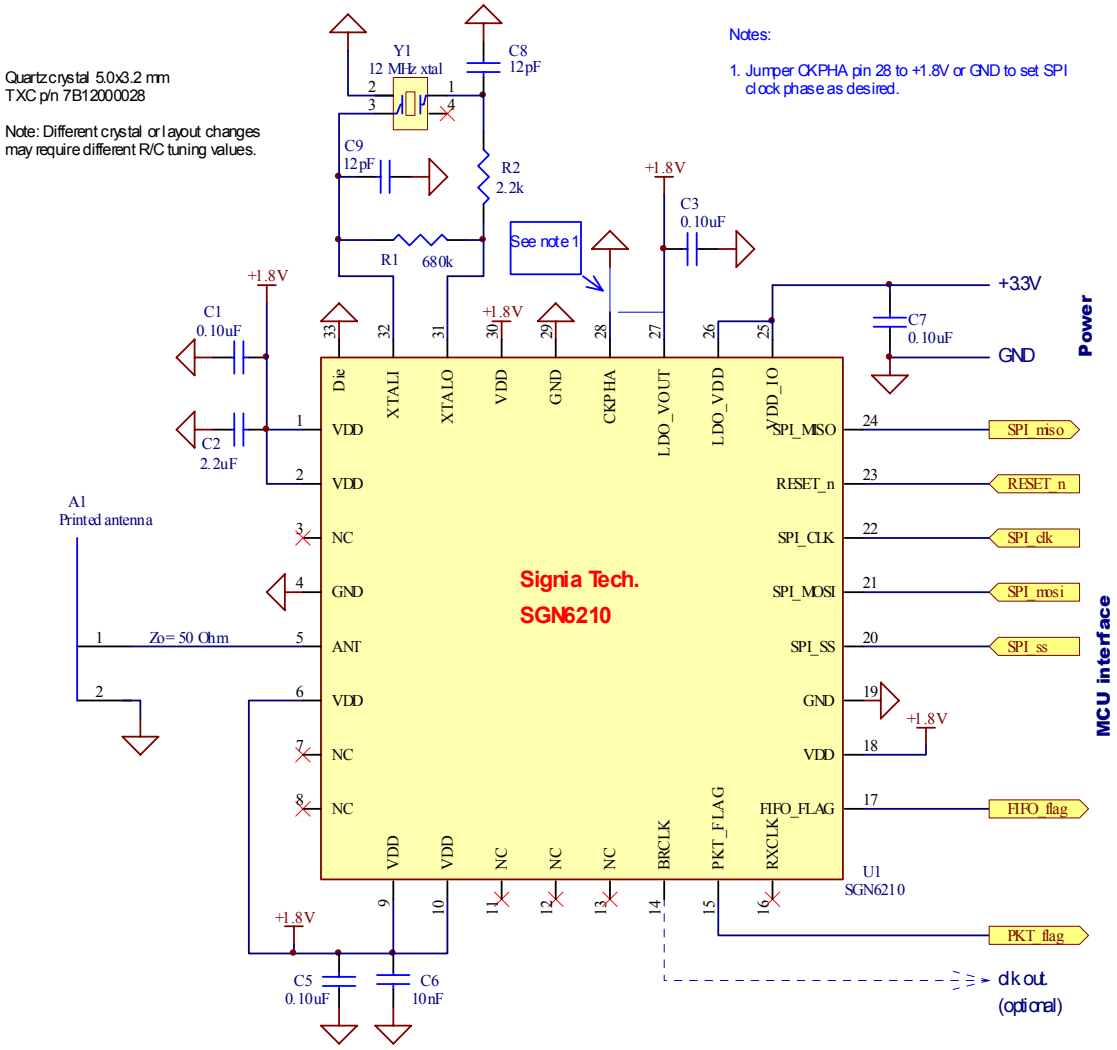
Register Information

For the latest register value recommendations, please contact your Signia technical representative.

State Diagram



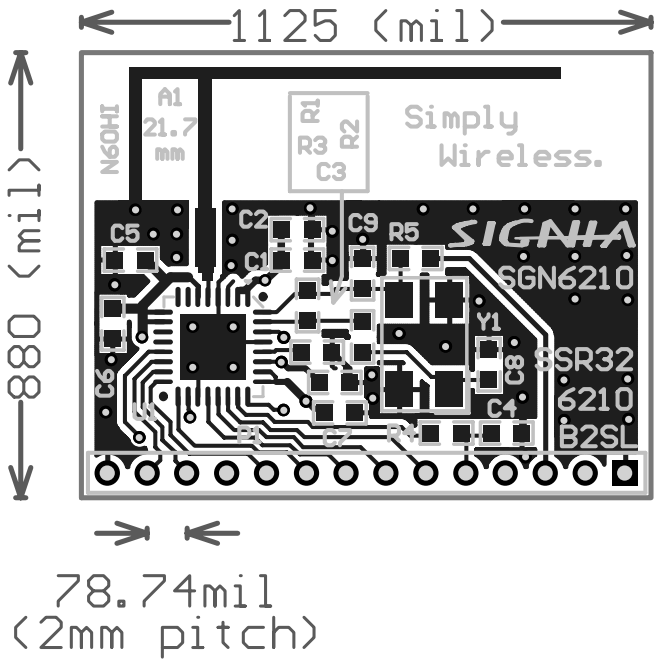
Typical Application



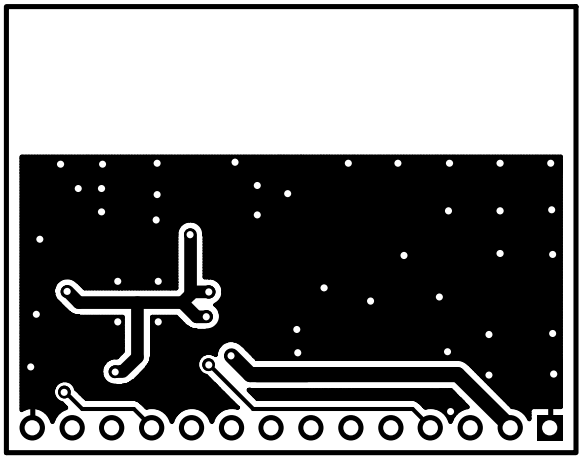
Simple, low-power (0 dBm)
2.4 GHz RF Transceiver
with Framing and data buffers

Typical 2-Layer PCB Layout

Top Layer:

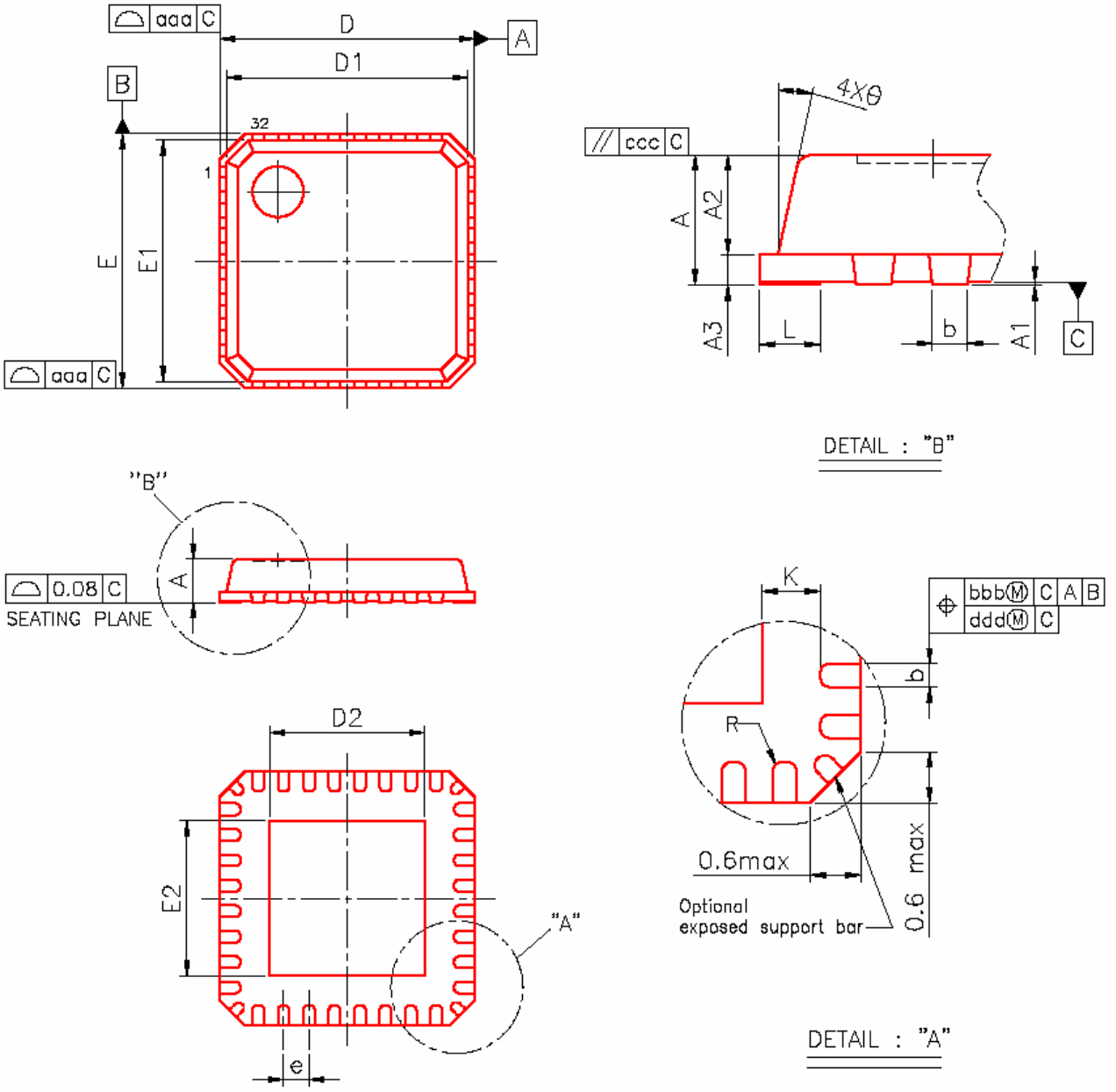


Bottom Layer, as viewed through the top layer:



Package Outline

QFN 32 Lead Exposed Pad Package, 5x5 mm Pkg. 0.5mm Pitch (JEDEC) MO-220-A



Dim.	Min.	Nom.	Max.	Dim.	Min.	Nom.	Max.
A	0.80	0.85	1.00	L	0.30	0.40	0.50
A1	0.00	0.02	0.05	θ	0°	--	12°
A2	0.60	0.65	0.80	R	0.09	--	--
A3		0.20 REF		K	0.20	--	--
b	0.18	0.25	0.30	aaa	--	--	0.15
D/E		5.00 BSC		bbb	--	--	0.10
D1/E1		4.75 BSC		ccc	--	--	0.10
D2/E2	3.15	3.30	3.45	ddd	--	--	0.05
e		0.50 BSC					

IR Reflow Standard

Follow : IPC/JEDEC J-STD-020 B

Condition : Average ramp-up rate (183ºC to peak): 3 ºC/sec. max.

Preheat: 100~150ºC 60~120sec

Temperature maintained above 183ºC: 60~150 seconds

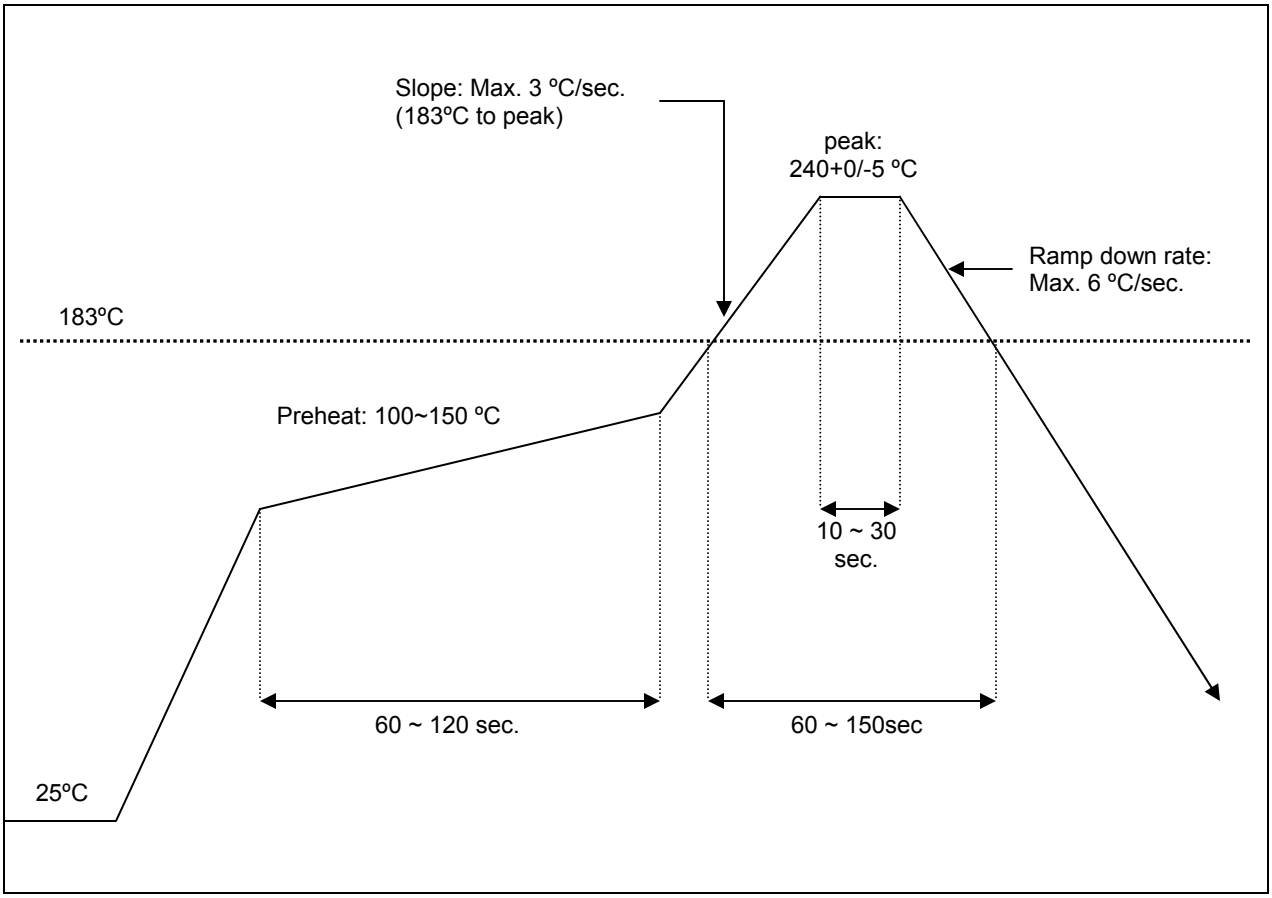
Time within 5ºC of actual peak temperature: 10 ~ 30 sec.

Peak temperature: 240+0/-5 ºC

Ramp-down rate: 6 ºC/sec. max.

Time 25ºC to peak temperature: 6 minutes max.

Cycle interval: 5 minutes



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