DZ-ZB-SP IEEE 802.15.4/ZigBee RF Module

Quickly add wireless communication with these high performances modules

The DiZiC DZ-ZB-SP 802.15.4 Module allows you to quickly add wireless networking capabilities to your products. These ZigBee-compliant modules are ready-to-use, simple to operate, and available in a wide range of configurations. They are ideal for industrial sensors, consumer remote controls, home appliances, and more.

Compact Form Factor – With 30 mm by 19 mm, this module can be shielded for enhanced EMI protection.

DZ-ZB-SP Module with Shield

Complete System-on-Module
- 2.4 GHz CSS transceiver
- 32-bit ARM® Cortex-M3 processor
- 128 kB flash, 8kB RAM memory
- AES128 encryption accelerator
- Flexible ADC, UART serial communication, and general purpose timers
- Highly configurable GPIO with Schmitt trigger inputs

Industry-leading ARM Cortex-M3 processor
- Leading 32-bit processing performance
- Highly efficient Thumb-2 instruction set
- Operation at 6, 12 or 24 MHz
- Flexible Nested Vectored Interrupt Controller

Innovative network and processor debug
- Serial Wire Debug interface
- Standard ARM debug capabilities:
  Flash Patch &Breakpoint; Data Watch-point & Trace

RF Performances
- Rx sensitivity (- 100 dBm)
- Tx output power level (+8 dBm)

Low power consumption, advanced management
- RX Current (w/ CPU): 27 mA
- TX Current (w/ CPU, +3dBm) 31 mA
- Low deep sleep current, less than 400nA
- Low-frequency internal RC oscillator for low-power sleep timing
- High-frequency internal RC oscillator for fast (100 usec) processor start-up from sleep

Target Applications
- Smart Energy
- Building automation and control (HVAC)
- Home automation and control
- Security and monitoring
- AMR/AMI
- Medical
- General ZigBee wireless sensor networking
- Wireless hand-held terminals
- Industry telemetry /automatic data collection
- Temperature and humidity control systems

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1. Product Approvals

The DZ-ZB-SP has been designed to meet all national regulations for world-wide use.
The transmitter module may not be co-located with any other transmitter or antenna.
Please be advised that DiZiC Co., Ltd. declares that the DZ-ZB-G module will be used exclusively by OEM's or ODM's and will therefore not be directly accessible by end users.

1.1. FCC Approvals

The DZ-ZB-SP with PCB Antenna has been tested to comply with FCC CFR Part 15 (USA) The devices meet the requirements for modular transmitter approval as detailed in the FCC public notice DA00.1407.transmitter.

FCC statement:

This device complies with Part 15 of the FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC ID: YCMDZZBSP

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by the manufacturer may void the user's authority to operate the equipment.

FCC Labeling Requirements

When integrating the DZ-ZB-SP into a product it must be ensured that the FCC labeling requirements are met. This includes a clearly visible label on the outside of the finished product specifying the DiZiC FCC identifier (FCC ID: YCMDZZBSP) as well as the FCC notice shown on the previous page. This exterior label can use wording such as "Contains Transmitter Module FCC ID: YCMDZZBSP " or "Contains FCC ID: YCMDZZBSP " although any similar wording that expresses the same meaning may be used.

1.2. IC (Industry Canada) Approvals

The DZ-ZB-SP with integrated Antenna has been tested to comply with IC.

IC-ID: 9022A- DZZBSP

The labeling requirements for Industry Canada are similar to those of the FCC. Again, a clearly visibly label must be placed on the outside of the finished product stating something like "Contains Transmitter Module, IC: 9022A- DZZBSP ", although any similar wording that expresses the same meaning may be used.

IC (Industry Canada) statement:

This module complies with Industry Canada RF radiation exposure limits set forth for general population/uncontrolled environment. This device complies with Industry Canada licence-exempt RSS standard(s).Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

The integrator is responsible for the final product to comply to IC ICES-003 and FCC Part 15, Sub. B - Unintentional Radiators.

1.3. European Certification (ETSI)

The DZ-ZB-SP has been certified to the following standards:

- Radio: EN 300 328:V1.7.1
- EMC: EN 301 489-17:V2.1.1
- Safety: EN 60950-1:2005 (Ed. 2.0)

If the DZ-ZB-SP module is incorporated into an OEM product, the OEM product manufacturer must ensure compliance of the final product to the European Harmonized EMC, and low voltage/ safety standards. A Declaration of Conformity must be issued for each of these standards and kept on file as described in Annex II of the R&TTE Directive. The final product must not exceed the specified power ratings, antenna specifications and installation requirements as specified in this user manual. If any of these specifications are exceeded in the final product then a submission must be made to a notified body for compliance testing to all of the required standards.

The 'CE' marking must be applied to a visible location on any OEM product. For more information please refer to http://ec.europa.eu/enterprise/faq/ce-mark.htm. Customers assume full responsibility for learning and meeting the required guidelines for each country in their distribution market.

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2. Configuration

The module comes with different configuration options. RF Output Options, Protocol Stack Options, and EMI Protection Options.

2.1. Power Level Option [S]

The module DZ-ZB-S has the power option S preselected.

Selector	Options	Description
[S]	Standard +8dBm	STM32W chip: System on Chip - where radio, microcontroller, program/user memory, RAM, ZigBee protocols stack are integrated in one chi

Table 1: Power level option

2.2. RF Output Options: Codes [P], [I] or [E]

Three RF output options are available, including an onboard PCB antenna or a U.FL connector.

Selector	Options	Description
[P]	Embedded PCB Antenna	
[I]	I-PEX / U.FL connector	
[E]	External +2dBi dipole Antenna	

Table 2: Output options

2.3. Protocol Stack Options: Codes [F], [X] or [Z]

Three protocol stack options are available, including an RF4CE stack, a Zigbee Pro stack from Ember, and a proprietary MAC/Phy stack

Selector	Options	Description
[F]	RF4CE stack	
[X]	Proprietary stack	
[Z]	EmberZnet PRO stack	

Table 3: Protocol stack options

2.4. EMI Protection Options: Codes [M] or []

A metal shield cap can be added to the module for EMI protection.

Selector	Options	Description
[M]	Metal shield cap	Enables enhanced level of electromagnetic immunity (EMI) protection.
[ ]	Standard module	RF Module without metal shielding

Table 4: EMI protection options

3. Block Diagram

The DZ-ZB Module is low-power, highly sensitivity IEEE 802.15.4 / ZigBee-compliant module. This multi-functional device is based on the STMicroelectronics STM32W108 fully integrated System-on-Chip [1] (STM32W108CBU6x version).

This STM32W108 SoC integrates a 2.4 GHz IEEE 802.15.4-compliant transceiver, a 32-bit ARM® Cortex™- M3 microprocessor, Flash and RAM memory, as well as peripherals for use by designers of ZigBee-based systems [2]

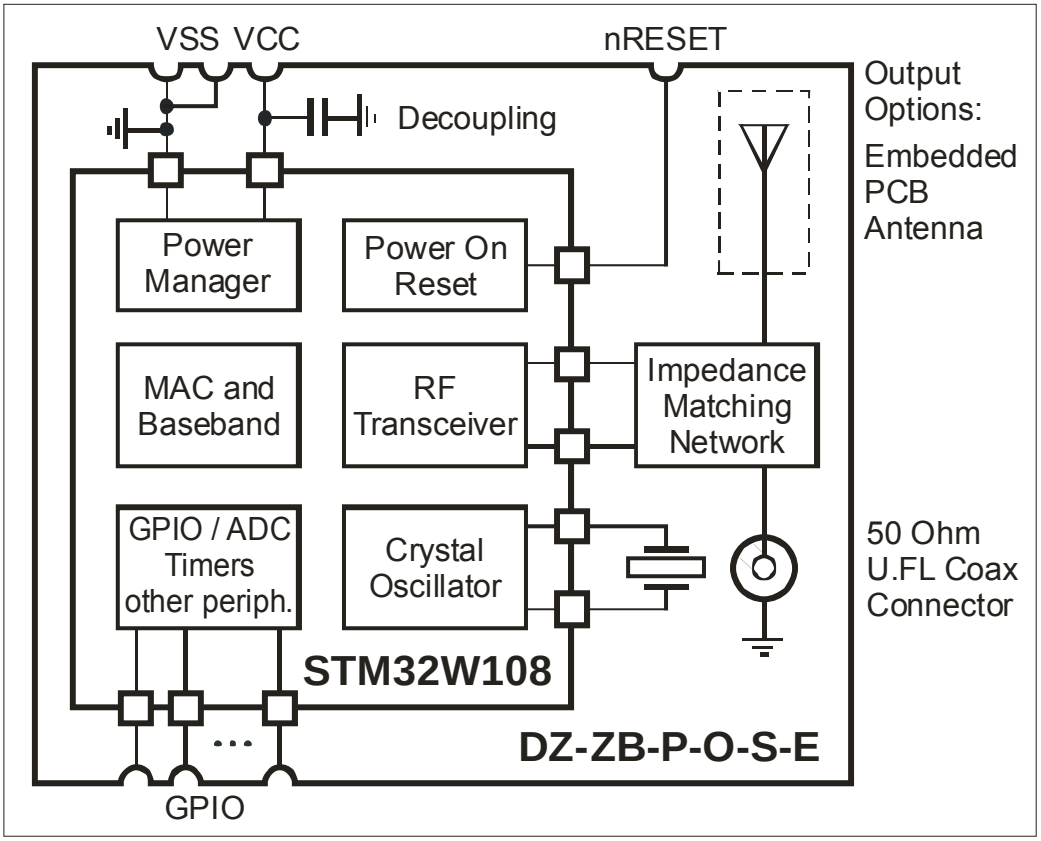

Fig. 1 *Simplified Block Diagram of the Module*

4. Absolute Maximum Rating

Stresses above the absolute maximum ratings listed in this section may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability

4.1. Voltage Characteristics

Ratings	Min.	Max.	Unit
VCC input voltage (VDD_PADS)	-0.3	+3.6	V
RF Input Power (for max level for correct packet reception Receive characteristics) RX signal input		15	dBm
Voltage on any GPIO (PA[7:0], PB[7:0], PC[7:0]), SWCLK, nRESET	-0.3	VDD_PADS +0.3	V

Table 5: Voltage characteristics

4.2. Current Characteristics

Symbol	Ratings	Max.	Unit
IVDD	Total current into VDD/VDDA power lines (source)	150	mA
IVSS	Total current out of VSS ground lines (sink)	150	mA
IIO	Output current sunk by any I/O and control pin	25	mA

Table 6: Current characteristics

4.3. Thermal Characteristics

Symbol	Ratings	Value	Unit
TSTG	Storage temperature range	-40 to +85	°C
TJ	Maximum junction temperature	150	°C

Table 7: Thermal characteristics

5. Components

This section describes the key components of the *DZ-ZB Module* including the STM32W108 SoC, the RF Front End, and the protocol stacks.

5.1. STM32W108 –System-on-Chip Transceiver

The STM32W108 is a fully integrated System-on-Chip that includes:

- 2.4 GHz, IEEE 802.15.4 compliant transceiver
- 32-bit ARM® Cortex™ -M3 microprocessor
- Flash and RAM memory
- Peripherals for use of designers of ZigBee-based systems

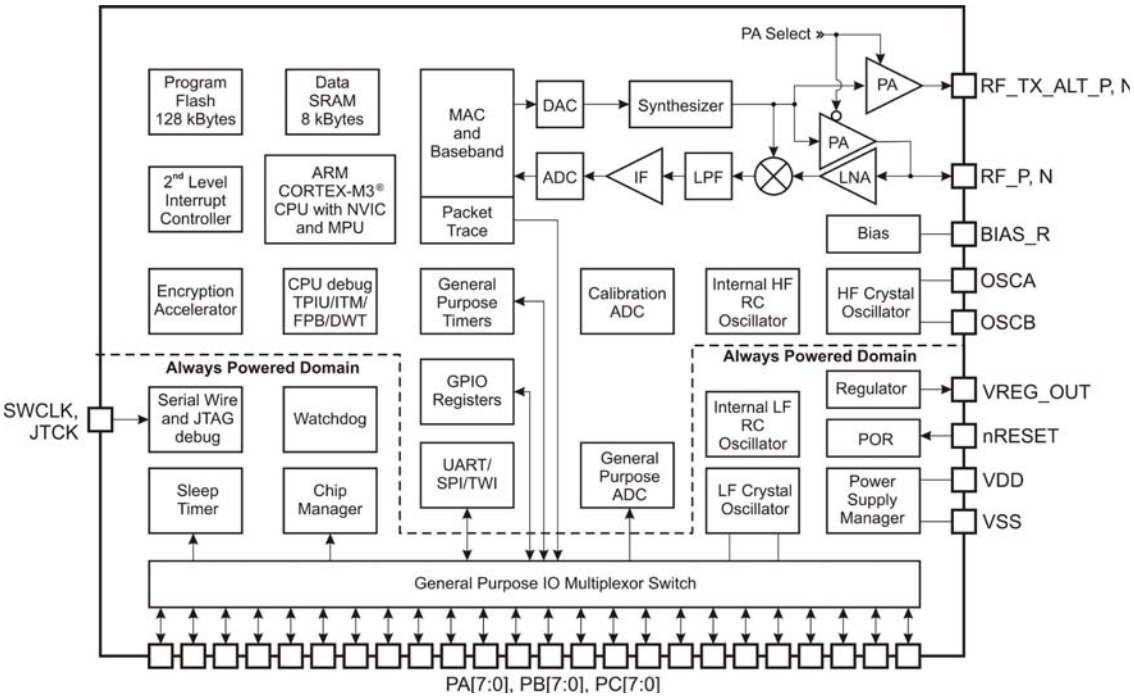

Fig. 2 *Block diagram of System-on-Chip STM32W108*

5.1.1. IEEE802.15.4 Compliant Transceiver

This SoC transceiver utilizes an efficient architecture that exceeds the dynamic range requirements imposed by the IEEE 802.15.4-2003 standard by over 15 dB. The integrated receive channel filtering allows for robust co-existence with other communication standards in the 2.4 GHz spectrum such as IEEE 802.11 and Bluetooth. The integrated regulator, VCO, loop filter, and power amplifier keep the external component count low. An optional high performance radio mode (boost mode) is software-selectable to boost dynamic range.

5.1.2. Operation Modes

The integrated 32-bit ARM® Cortex™-M3 microprocessor is highly optimized for high performance, low power consumption, and efficient memory utilization. With its integrated MPU, the STM32W108 supports two different modes of operation: System mode and Application mode.

The networking stack software runs in System Mode with full access to all areas of the chip. Application code, however, runs in Application Mode with limited access to STM32W108 resources. This allows for the scheduling of events by the application developer while preventing modification of restricted areas of memory and registers. This architecture results in increased stability and reliability of deployed solutions.

5.1.3. Flash and RAM Memory

The STM32W108 has 128 Kbytes of embedded Flash memory and 8 Kbytes of integrated RAM for data and program storage. The STM32W108 HAL software employs an effective wear-leveling algorithm that optimizes the lifetime of the embedded Flash.

5.1.4. Integrated MAC Functions

To maintain the strict timing requirements imposed by ZigBee and IEEE 802.15.4-2003 standards, the STM32W108 IC integrates a number of MAC functions into the hardware. The MAC hardware handles automatic ACK transmission and reception, automatic back off delay, and clear channel assessment for transmission, as well as automatic filtering of received packets. A packet trace interface is also integrated in the MAC hardware allowing complete, non-intrusive capture of all packets to and from the STM32W108 IC.

5.1.5. Power Management

The STM32W108 IC offers a number of advanced power management features that enables long battery life. A high-frequency internal RC oscillator allows the processor core to begin code execution quickly upon waking. Various deep sleep modes are available with less than 1 µs power consumption while retaining RAM contents.

5.1.6. Peripherals

To support user-defined applications, on-chip peripherals include UART, SPI, TWI, ADC, general-purpose timers, and up to 24 GPIOs. Additionally, an integrated voltage regulator, power-on-reset circuit, and sleep timer are available.

5.1.7. Interfaces

The STM32W108 IC utilizes standard Serial Wire and JTAG interfaces for powerful software debugging and programming of the ARM Cortex-M3 core. The STM32W108 IC integrates the standard ARM system debug components including Flash Patch and Breakpoint (FPB), Data Watch-point and Trace (DWT), and Instrumentation Trace Macrocell (ITM).

5.2. Protocol Stacks

Three protocols stacks are available:

- RF4CE (Radio Frequency for Consumer Electronics) stack, which is used primarily for a wide range of remotely-controlled audio/visual consumer electronics products.32-bit ARM® Cortex™ -M3 microprocessor
- Proprietary ZigBee stack, which is a robust ZigBee protocol software package for wireless control and monitoring applications
- EmberZNet PRO stack, which is a complete ZigBee protocol software package containing all the elements required for robust and reliable mesh networking applications

Figure 4 below shows the a block diagram of the three optional ZigBee stacks

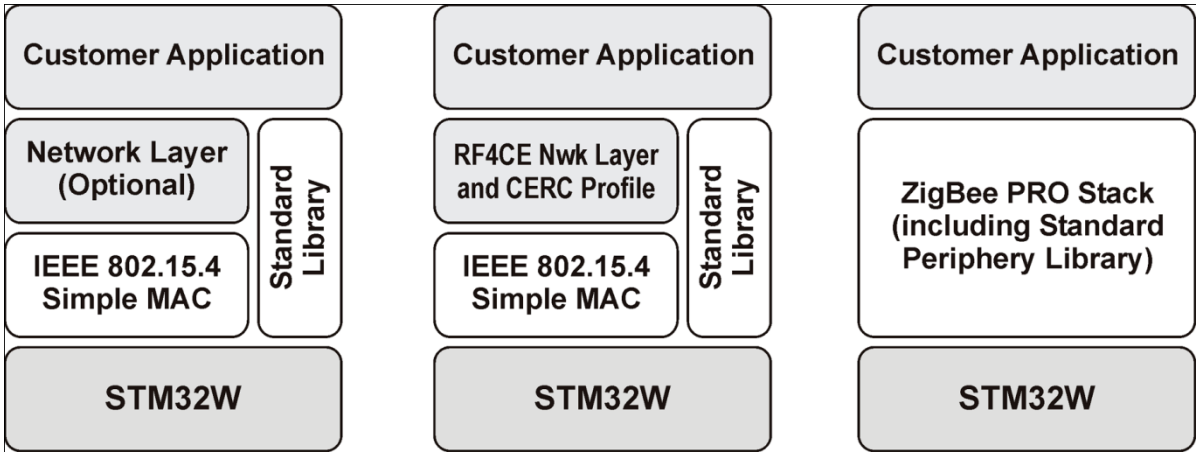

Fig. 3 *Available protocol stacks.*

6. Electrical Characteristics

6.1. Parameter conditions

6.1.1. Minimum and Maximum Values

Note: Unless otherwise specified, all voltages are referenced as VSS.

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = T_A max (given by the selected temperature range).
Data based on characterization results, design simulation, and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3).

6.1.2. Typical values

Unless otherwise specified, typical data are based on T_A = 25°C, VDD = 3.3 V (for the 2V VDD 3.6 V voltage range). They are given only as design guidelines and are not tested. Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

6.2. Operating Conditions

6.2.1. General Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	VCC input voltage (VDD_PADS)	+2.1	-	+3.6	V
TOP	Operating temperature range	-40	-	+85	°C

Table 8: General operating conditions

6.2.2. Electrostatic Discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Symbol	Ratings	Conditions	Class	Maximum value	Unit
VESD (HBM)	Electrostatic discharge voltage (Charge Device Model) for non-RF pins	TA = +25 °C conforming to JESD22-A114	2	±2000	V
VESD (CDM)	Electrostatic discharge voltage (Charge Device Model) for RF pins	TA = +25 °C conforming to JESD22-C101	II	±400	
	Moisture sensitivity level			±225	
MSL	Electrostatic discharge voltage (Human Body Model)			MSL3	–

Table 9: ESD absolute maximum

6.2.3. DC Characteristics

Parameter	Conditions	Typical value	Unit
Regulator input voltage (VDD_PADS)	–	2.0 - 3.6	V
Deep Sleep Current			
Quiescent current, internal RC oscillator disabled	-40°C, VDD_PADS = 3.6 V	0.4	µA
	+25°C, VDD_PADS = 3.6 V	0.4	µA
	+85°C, VDD_PADS = 3.6 V	0.4	µA
Quiescent current, including internal RC oscillator	-40°C, VDD_PADS = 3.6 V	0.7	µA
	+25°C, VDD_PADS = 3.6 V	0.8	µA
	+85°C, VDD_PADS = 3.6 V	1.2	µA
Quiescent current, including 32.768 kHz oscillator	-40°C, VDD_PADS = 3.6 V	1.2	µA
	+25°C, VDD_PADS = 3.6 V	1.3	µA
	+85°C, VDD_PADS = 3.6 V	1.7	µA
Quiescent current, including internal RC oscillator and 32.768 kHz oscillator	-40°C, VDD_PADS = 3.6 V	1.4	µA
	+25°C, VDD_PADS = 3.6 V	1.5	µA
	+85°C, VDD_PADS = 3.6 V	2	µA
Simulated deep sleep (debug mode) current	With no debugger activity	200	µA
Reset Current			
Quiescent current, nRESET asserted	Typical at 25°C/3 V Max at 85°C/3.6 V	1.2	µA
Processor and peripheral Currents			
ARM® Cortex-M3, RAM, and flash memory	25°C, 1.8 V memory and 1.25 V core ARM® Cortex-M3 running at 12 MHz from crystal oscillator Radio and all peripherals off	8.0	mA

Parameter	Conditions	Typical value	Unit
ARM® Cortex-M3, RAM, and flash memory	25°C, 1.8 V memory and 1.25 V core ARM® Cortex- M3 running at 24 MHz from crystal oscillator Radio and all peripherals off	9.0	mA
ARM® Cortex-M3, RAM, and flash memory sleep current	25°C, 1.8 V memory and 1.25 V core ARM® Cortex- M3 clocked at 12 MHz from the crystal oscillator Radio and all peripherals off	4.0	mA
ARM® Cortex-M3, RAM, and flash memory sleep current	25°C, 1.8 V memory and 1.25 V core ARM® Cortex-M3 clocked at 6 MHz from the high frequency RC oscillator Radio and all peripherals off	2.0	mA
Serial controller current	For each controller at maximum data rate	0.2	mA
General purpose timer current	For each timer at maximum clock rate	0.1	mA
General purpose ADC current	At maximum sample rate, DMA enabled	1.1	mA
Rx Current			
Radio receiver, MAC, and baseband	ARM® Cortex-M3 sleeping	20	mA
Total RX current (Radio receiver, MAC and baseband, CPU +IRAM, and Flash memory)	VDD_PADS = 3,0 V, 25°C, ARM® Cortex-M3 running at 12 MHz	27	mA
VDD_PADS = 3,0 V, 25°C, ARM® Cortex-M3 running at 24 MHz	-	28	mA
Boost mode total RX current (Radio receiver, MAC and baseband, CPU+IRAM, and Flash memory)	VDD_PADS = 3,0 V, 25°C, ARM® Cortex-M3 running at 12 MHz	28	mA
VDD_PADS = 3,0 V, 25°C, ARM® Cortex-M3 running at 24 MHz	-	29	mA
Tx Current			
Radio transmitter, MAC, and baseband	25°C and 1.8 V core; max. power out (+3 dBm typical) ARM® Cortex-M3 sleeping	26	mA
Total TX current (Radio transmitter, MAC and baseband, CPU+IRAM, and Flash memory)	VDD_PADS = 3.0 V, 25°C; maximum power setting +7dBm; running at 24 MHz	40	mA
	VDD_PADS = 3.0 V, 25°C; +3 dBm power setting; ARM® Cortex-M3 running at 24 MHz	32	mA
	VDD_PADS = 3.0 V, 25°C; 0dBm power setting; ARM® Cortex-M3 running at 24 MHz	30	mA
	VDD_PADS = 3.0 V, 25°C; minimum power setting; ARM® Cortex-M3 running at 24 MHz	24	mA

Table 10: DC electrical characteristics

6.3. RF Characteristic

6.3.1. Receiver Characteristics

Parameter	Conditions	Typical value	Unit
Frequency range	–	2400 - 2500	MHz
Sensitivity (boost mode)	Sensitivity 1% PER, 20 byte packet defined by IEEE 802.15.4-2003	-100	dBm
Sensitivity (normal mode)	Sensitivity 1% PER, 20 byte packet defined by IEEE 802.15.4-2003	-99	dBm
Co-channel rejection	IEEE 802.15.4 signal at -82dBm	-6	dBc
Relative frequency error (2 x 40 ppm required by IEEE 802.15.4)		-120…+120	ppm
Relative timing error (2 x 40 ppm required by IEEE 802.15.4)		-120…+120	ppm
Linear RSSI range			dBm
RSSI Range		-90 … -30	dBm

Table 11: Receiver characteristics

6.3.2. Transmitter Characteristics

Parameter	Conditions	Typical value	Unit
Maximum output power (boost mode)	At highest power setting	+8	dBm
Maximum output power	At highest power setting	+3	dBm
Minimum output power	At lowest power setting	-32	dBm
Error vector magnitude	As defined by IEEE 802.15.4, which sets a 35% maximum	5 … 15	%
Carrier frequency error	-	-40 … +40	ppm
PSD mask relative	3.5 MHz away	-20	dBm
PSD mask absolute	3.5 MHz away	-30	dBm

Table 12: Transmitter characteristics

7. Mechanical Characteristics

7.1. Module Pad Diagram

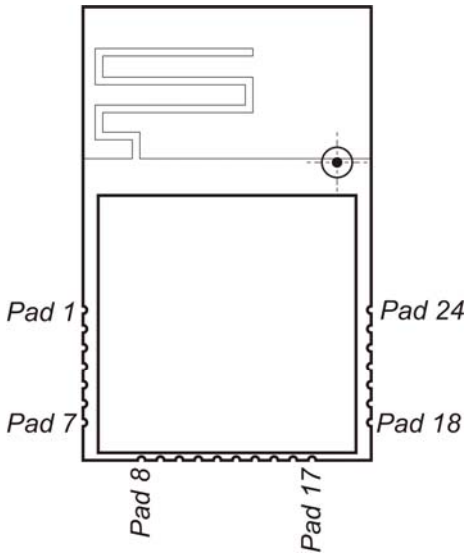

Fig. 4 *Pad connection diagram for modules (top view)*

7.2. Module Pads

Pad	Signal Name	Direction	Description
1	nRESET	I	Active low chip reset (internal pull-up)
2	PA7	I/O High current	Digital I/O Disable REG_EN with GPIO_DBGCFG[4]
	TIM1CH4	O	Timer 1 Channel 4 output. Enable timer output with TIM1_CCER Select alternate output function with GPIO_PACFGH[15:12] Disable REG_EN with GPIO_DBGCFG[4]
		I	Timer 1 Channel 4 input. Cannot be remapped
	REG_EN	O	External regulator open drain output. (Enabled after reset)

Pad	Signal Name	Direction	Description
3	PB3	I/O	Digital I/O
	TIM2_CH3 See also Pad 6	O	Timer 2 channel 3 output. Enable remap with TIM2_OR[6]. Enable timer output in TIM2_CCER. Select alternate output function with GPIO_PBCFGL[15:12].
		I	Timer 2 channel 3 input Enable remap with TIM2_OR[6].
	UART_CTS	I	UART CTS handshake of Serial Controller 1 - Enable with SC1_UARTCFG[5]. - Select UART with SC1_MODE.
	SC1SCLK	O	SPI master clock of Serial Controller 1. - Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[6] Enable master with SC1_SPICFG[4]. - Select SPI with SC1_MODE. - Select alternate output function withGPIO_PBCFGL[15:12].
		I	SPI slave clock of Serial Controller 1. Enable slave with SC1_SPICFG[4]. Select SPI with SC1_MODE.
4	PB4	I/O	Digital I/O
	TIM2_CH4 *See also Pad 7*	O	Timer 2 channel 4 output...Enable remap with TIM2_OR[7]. - Enable timer output in TIM2_CCER. - Select alternate output function with GPIO_PBCFGH[3:0].
		I	Timer 2 channel 4 input. - Enable remap with TIM2_OR[7].
	UART_RTS	O	UART RTS handshake of Serial Controller 1. - Either disable timer output in TIM2_CCER, or disable remap withTIM2_OR[7]. - Enable with SC1_UARTCFG[5] Select UART with SC1_MODE. - Select alternate output function with GPIO_PBCFGH[3:0].
	SC1nSSEL	I	SPI slave select of Serial Controller 1. - Enable slave with SC1_SPICFG[4]. - Select SPI with SC1_MODE.
5	PA0	I/O	Digital I/O
	TIM2_CH1 *See also Pad 12*	O	Timer 2 channel 1 output. - Disable remap with TIM2_OR[4]. - Enable timer output in TIM2_CCER. - Select alternate output function with GPIO_PACFGL[3:0].
		I	Timer 2 channel 1 input Disable remap with TIM2_OR[4].
	SC2MOSI	O	SPI master data out of Serial Controller 2. - Either disable timer output in TIM2_CCER, or enable remap with TIM2_OR[4]. - Enable master with SC2_SPICFG[4]. - Select SPI with SC2_MODE. - Select alternate output function with GPIO_PACFGL[3:0].
		I	SPI slave data in of Serial Controller 2 - Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE

Pad	Signal Name	Direction	Description
6	PA1	I/O	Digital I/O
	TIM2_CH3 *See also Pad 3*	O	Timer 2 channel 3 output. - Disable remap with TIM2_OR[4]. - Enable timer output in TIM2_CCER. - Select alternate output function with GPIO_PACFGL[3:0].
		I	Timer 2 channel 3 input Disable remap with TIM2_OR[4].
	SC2SDA	I/O	TWI data of Serial Controller 2 - Either disable timer output in TIM2_CCER, or enable remap with TIM2_OR[6] Select TWI with SC2_MODE. - Select alternate open-drain output function with GPIO_PACFGL[7:4].
	SC2MISO	O	SPI slave data out of Serial Controller 2. - Either disable timer output in TIM2_CCER, or enable remap with TIM2_OR[6]. - Enable slave with SC2_SPICFG[4]. - Select SPI with SC2_MODE. - Select alternate output function with GPIO_PACFGL[7:4].
		I	SPI master data in of Serial Controller 2. - Enable slave with SC2_SPICFG[4].
7	PA2	I/O	Digital I/O.
	TIM2_CH4 See also Pad 4	O	Timer 2 channel 4 output. - Disable remap with TIM2_OR[7]. - Enable timer output in TIM2_CCER. - Select alternate output function with GPIO_PACFGL[11:8].
		I	Timer 2 channel 4 input - Disable remap with TIM2_OR[7].
	SC2SCL	I/O	TWI clock of Serial Controller 2. - Either disable timer output in TIM2_CCER, or enable remap with TIM2_OR[7]. - Select TWI with SC2_MODE. - Select alternate open-drain output function with GPIO_PACFGL[11:8].
	SC2SCLK	O	SPI master clock of Serial Controller 2. - Either disable timer output in TIM2_CCER, or enable remap with TIM2_OR[7]. - Enable master with SC2_SPICFG[4]. - Select SPI with SC2_MODE. - Select alternate output function with GPIO_PACFGL[11:8].
		I	SPI slave clock of Serial Controller 2. - Enable slave with SC2_SPICFG[4]. - Select SPI with SC2_MODE.
8	PA3	I/O	Digital I/O.
	SC2nSSEL	I	SPI slave select of Serial Controller 2. - Enable slave with SC2_SPICFG[4]. - Select SPI with SC2_MODE.
	TRACECLK See also Pad 18	O	Synchronous CPU trace clock. - Either disable timer output in TIM2_CCER, or enable remap with TIM2_OR[5]. - Enable trace interface in ARM core. - Select alternate output function with GPIO_PACFGL[15:12].
	TIM2_CH2 See also Pad 13	O	Timer 2 channel 2 output. - Disable remap with TIM2_OR[5]. - Enable timer output in TIM2_CCER. - Select alternate output function with GPIO_PACFGL[15:12].
		I	Timer 2 channel 2 input Disable remap with TIM2_OR[5].

Pad	Signal Name	Direction	Description
9	PA4	I/O	Digital I/O.
	ADC4	Analog	ADC Input 4 - Select analogue function with GPIO_PACFGH[3:0].
	PTI_EN	O	Frame signal of Packet Trace Interface (PTI). - Disable trace interface in ARM core. - Select alternate output function with GPIO_PACFGH[3:0].
	TRACEDATA2	O	Synchronous CPU trace data bit 2 Select 4-wire synchronous trace interface in ARM core Enable trace interface in ARM core Select alternate output function with GPIO_PACFGH[3:0].
10	PA5	I/O	Digital I/O.
	ADC5	Analog	ADC Inputs - Select analog function with GPIO_PACFGH[7:4].
	PTI_DATA	O	Data signal of Packet Trace Interface (PTI). - Disable trace interface in ARM core. - Select alternate output function with GPIO_PACFGH[7:4].
	nBOOTMODE	I	Embedded serial boot-loader activation out of reset. - Signal is active during and immediately after a reset on nRESET.
	TRACEDATA3	O	Synchronous CPU trace data bit 3. - Select 4-wire synchronous trace interface in ARM core. - Enable trace interface in ARM core. - Select alternate output function with GPIO_PACFGH[7:4].
11	PA6	I/O High current	Digital I/O.
	TIM1_CH3	O	Timer 1 channel 3 output. - Enable timer output in TIM1_CCER. - Select alternate output function with GPIO_PACFGH[11:8].
		I	Timer 1 channel 3 input - Cannot be remapped.
12	PB1	I/O	Digital I/O.
	SC1MISO	O	SPI slave data out of Serial Controller 1. Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[4]. Select SPI with SC1_MODE. Select slave with SC1_SPICR. Select alternate output function with GPIO_PBCFGL[7:4].
	SC1MOSI	O	SPI master data out of Serial Controller 1. Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[4] Select SPI with SC1_MODE. Select master with SC1_SPICR. Select alternate output function with GPIO_PBCFGL[7:4].
	SC1SDA	I/O	TWI data of Serial Controller 1. - Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[4]. - Select TWI with SC1_MODE. - Select alternate open-drain output function with GPIO_PBCFGL[7:4].
	SC1TXD	O	UART transmit data of Serial Controller 1. - Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[4]. - Select UART with SC1_MODE. - Select alternate output function with GPIO_PBCFGL[7:4].
	TIM2_CH1 See also Pad 5	O	Timer 2 channel 1 output. - Enable remap with TIM2_OR[4]. - Enable timer output in TIM2_CCER. - Select alternate output function with GPIO_PACFGL[7:4].
		I	Timer 2 channel 1 input. - Disable remap with TIM2_OR[4].

Pad	Signal Name	Direction	Description
13	PB2	I/O	Digital I/O.
	SC1MOSI	I	SPI master data in of Serial Controller 1. - Select SPI with SC1_MODE. - Select master with SC1_SPICR.
	SC1MOSI	I	SPI master data in of Serial Controller 1. - Select SPI with SC1_MODE. - Select master with SC1_SPICR.
	SC1SCL	I/O	TWI clock of Serial Controller 1. - Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[5]. - Select TWI with SC1_MODE. - Select alternate open-drain output function with GPIO_PBCFGL[11:8].
	SC1RXD	I	UART receive data of Serial Controller 1. - Select UART with SC1_MODE.
	TIM2_CH2 See also Pad 8	O	Timer 2 channel 2 output. - Enable remap with TIM2_OR[5]. - Enable timer output in TIM2_CCER. - Select alternate output function with GPIO_PBCFGL[11:8].
		I	Timer 2 channel 2 input. - Enable remap with TIM2_OR[5].
14	SWCLK	I/O	Serial Wire clock input/output with debugger. - Selected when in Serial Wire mode (see JTMS description, Pad 17).
	JTCK	I	JTAG clock input from debugger. - Selected when in JTAG mode (default mode, see JTMS description,Pad 17) Internal pull-down is enabled.
15	PC2	I/O	Digital I/O. - Enable with GPIO_DBGCFG[5].
	JTDO	O	JTAG data out to debugger. - Selected when in JTAG mode (default mode, see JTMS description,Pad 17).
	SWO	O	Serial Wire Output asynchronous trace output to debugger. - Select asynchronous trace interface in ARM core. - Enable trace interface in ARM core. - Select alternate output function with GPIO_PCCFGL[11:8]. - Enable Serial Wire mode (see JTMS description, Pad 17). - Internal pull-up is enabled.
16	PC3	I/O	Digital I/O. - Either enable with GPIO_DBGCFG[5], or enable Serial Wire mode (see JTMS description, Pad 17)
	JTDI	I	JTAG data in from debugger. - Selected when in JTAG mode (default mode, see JTMS description, Pad 17). - Internal pull-up is enabled.
17	PC4	I/O	Digital I/O. - Enable with GPIO_DBGCFG[5].
	JTMS	I	JTAG mode select from debugger. - Selected when in JTAG mode (default mode). - JTAG mode is enabled after power-up or by forcing nRESET low. - Select Serial Wire mode using the ARM-defined protocol through a debugger. - Internal pull-up is enabled.
	SWDIO	I/O	Serial Wire bidirectional data to/from debugger. - Enable Serial Wire mode (see JTMS description) - Select Serial Wire mode using the ARM-defined protocol through a debugger - Internal pull-up is enabled.

Pad	Signal Name	Direction	Description
18	PB0	I/O	Digital I/O.
	VREF	Analog O	ADC reference output. - Enable analog function with GPIO_PBCFGL[3:0].
	VREF	Analog I	ADC reference input. - Enable analog function with GPIO_PBCFGL[3:0]. - Enable reference output with an STM system function.
	IRQA	I	External interrupt source A.
	TRACECLK *See also Pad 8*	O	Synchronous CPU trace clock. - Enable trace interface in ARM core. - Select alternate output function with GPIO_PBCFGL[3:0].
	TIM1CLK	I	Timer 1 external clock input.
	TIM2MSK	I	Timer 2 external clock mask input.
19	PC0	I/O High current	Digital I/O. - Either enable with GPIO_DBGCFG[5], or enable Serial Wire mode (see JTMS description, Pad 17) and disable TRACEDATA1.
	JRST	I	JTAG reset input from debugger. - Selected when in JTAG mode (default mode, see JTMS description) and TRACEDATA1 is disabled. - Internal pull-up is enabled.
	IRQD1	I	Default external interrupt source D
	TRACEDATA1	O	Synchronous CPU trace data bit 1. - Select 2- or 4-wire synchronous trace interface in ARM core. - Enable trace interface in ARM core. - Select alternate output function with GPIO_PCCFGL[3:0].
20	PB7	I/O High current	Digital I/O.
	ADC2	Analog	ADC Input 2. - Enable analog function with GPIO_PBCFGH[15:12].
	IRQC1	I	Default external interrupt source C.
	TIM1_CH2	O	Timer 1 channel 2 output. - Enable timer output in TIM1_CCER. - Select alternate output function with GPIO_PBCFGH[15:12].
		I	Timer 1 channel 2 input.(Cannot be remapped).

Pad	Signal Name	Direction	Description
21	PB6	I/O High current	Digital I/O.
	ADC1	Analog	ADC Input 1. - Enable analog function with GPIO_PBCFGH[11:8].
	IRQB	I	External interrupt source B.
	TIM1_CH1	O	Timer 1 channel 1 output. - Enable timer output in TIM1_CCER. - Select alternate output function with GPIO_PBCFGH[11:8].
		I	Timer 1 channel 1 input. (Cannot be remapped).
22	PB5	I/O	Digital I/O.
	ADC0	Analog	ADC Input 0. - Enable analog function with GPIO_PBCFGH[7:4].
	TIM2CLK	I	Timer 2 external clock input.
	TIM1MSK	I	Timer 2 external clock mask input.
23	VCC	Power	Power supply pad
24	GND	Power	Ground supply pad

Table 13: Pad description.

7.3. Module Mechanical Dimensions

Module dimensions are 30 mm x 19 mm x 2 mm. Figures 5 and 6 below shows a detailed drawing of the package dimensions.

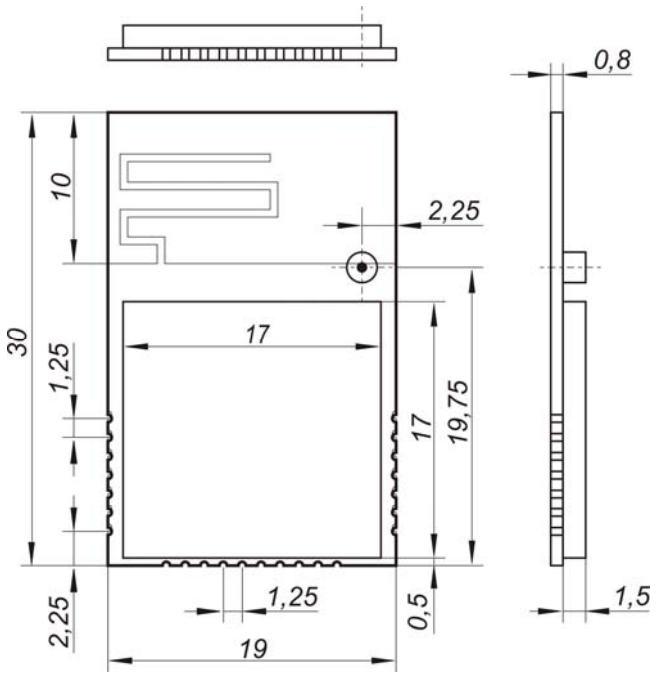

Fig. 5 *Standard module dimensions with metal shielding*

8. Soldering

8.1. Soldering (Reflow) Profile

Figure 6 below shows the solder temperature profile for the DZ-ZB RF Module. This temperature profile is similar for other RoHS compliant packages, but manufacturing lines should be programmed with this profile in order to guarantee proper solder connection to the PCB.

Note: The module can be soldered only once.

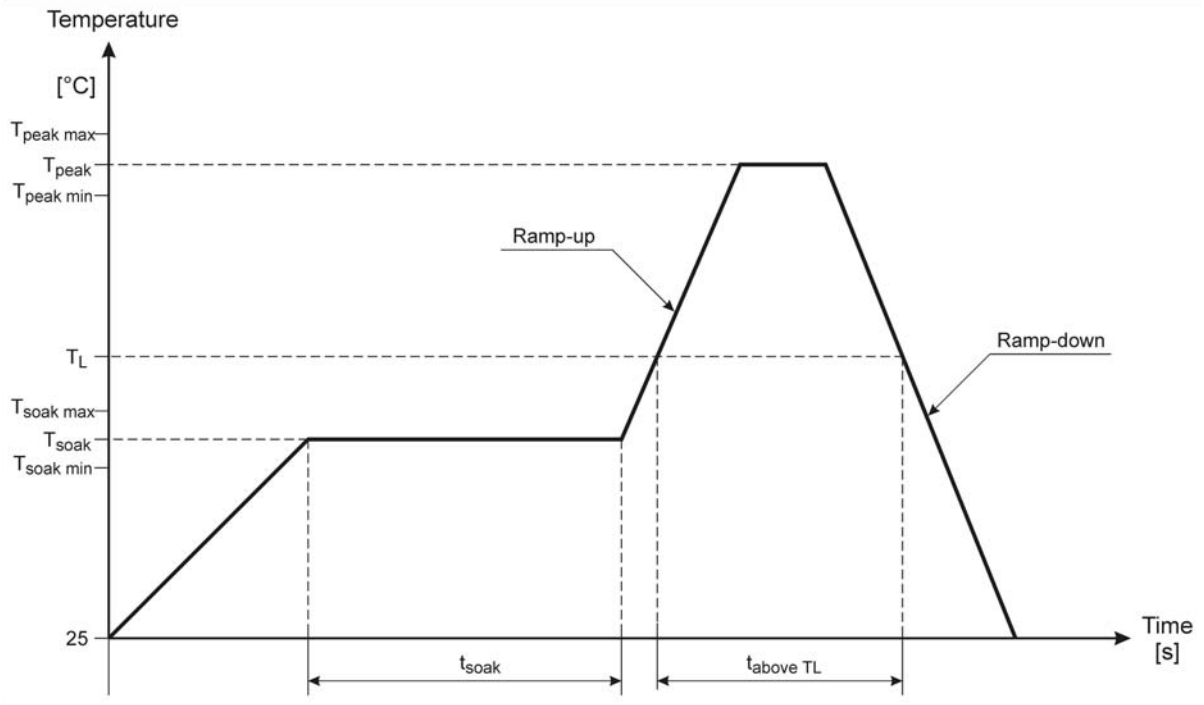

Fig. 6 *Recommended Temperature Profile for Soldering (Reflow)*

8.2. Profile Parameters

Table 14 below describes the temperature profile parameters.
Warning: The module should be processed according to recommended temperature profile only once.

Parameter	Value
Average Ramp Up Rate (from Tsoakmax to Tpeak)	3°C per second max
Average Ramp Up Rate (from 25°C to Tsoakmin)	2°C to 4°C per second max
Minimum Soak Temperature (Tsoakmjn)	150°C
Maximum Soak Temperature (Tsoakmax)	200°C
TL	220°C
Time above TL	30 to 60 seconds
Minimum Peak Temperature Tpeakmin	230°C
Maximum Peak Temperature Tpeakmax	250°C
Ramp Down Rate	6°C per second max

Table 14: Solder Reflow Parameters

8.3. Recommended Footprint

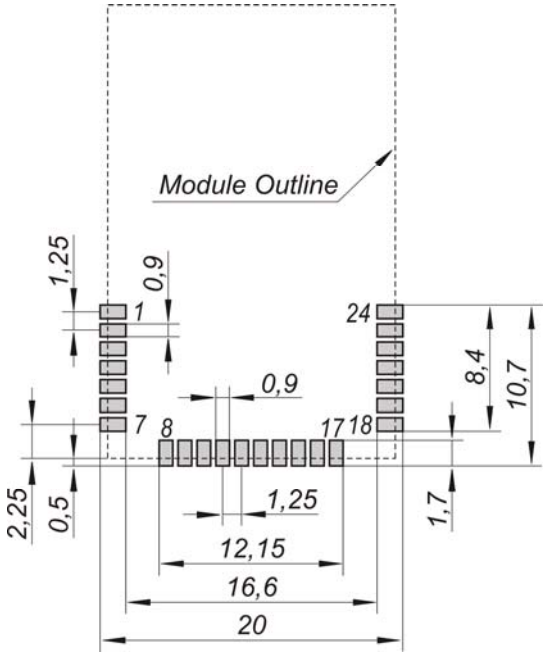

Fig. 7 *Recommended Footprint for Module*

With module configured with output option “P”, that is, with the PCB antenna, the presence of any conductive materials in proximity of the module’s antenna must be prevented. This requirement is valid also for copper traces, ground planes, wires, and connectors.

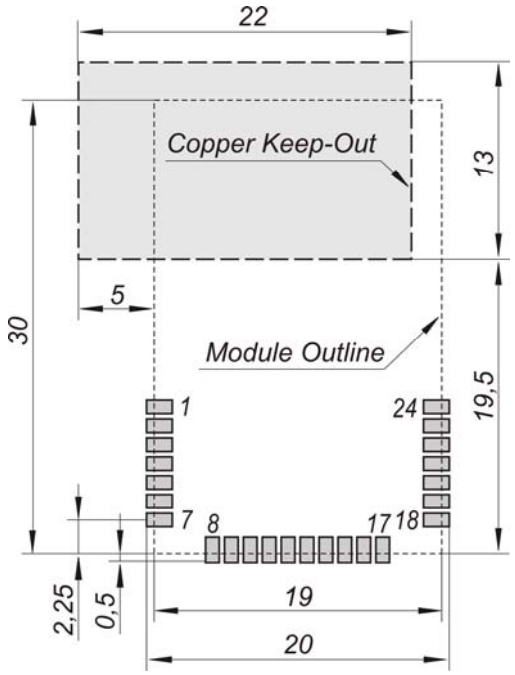

Fig. 8 *Recommended Footprint for Module*

Figure 8 below shows the recommended “Copper-Keep-Out” area where the presence of any copper (and any conductive material as well) should be avoided.

9. References

[1] STM32W108HB, STM32W108CB, High-performance, 802.15.4 wireless system-on-chip, Data brief, 20-Aug-2009, Rev. 1

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[3] RN0034, Release notes, STM32W108xx starter and extension kits EmberZNet 4.0.2 GA, Doc ID 16225, 16-Feb-2010, Rev. 2

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10/30/2012	1.00	Released

About DiZiC

DiZiC develops and manufactures ready-to-use OEM radio modules, PC accessories and gateways targeted for metering, telemetry and security applications with deployments in consumer, commercial or heavy industry devices. Our very talented team of RF experts helps us to offer best in class products. DiZiC delivers quality, reliability and performances at an affordable price.