Hardware Design Guide SPB620 Application Note

1 Preface

This document provides hardware design guidelines for the SPB620 module.

2 Introduction

2.1 Overview

SPB620 is a complete Wi-Fi 6/Bluetooth 5 module with integrated EMC shield, ready for onboard integration in a hosted environment. SPB620 enables a cost efficient ultra-low power, high performance and feature rich client solution. It provides up to 1.658 Gbit/s data rate when operating in concurrent 2x2 MIMO configuration in both the 2.4 GHz and the 5 GHz bands.

SPB620 integrates RF, baseband/MAC, Bluetooth Package Engine, memory, RF filters, oscillator, and EMC shield into a highly integrated and optimized module solution with high quality and reliability to a complete standalone solution with no need for external components.

This highly integrated solution is optimized for customer applications running on a Linux host.
The host interface supports PCIe 2.0, SDIO 3.0 and UART. Internal RAM comprises both code and data memory eliminating the need for external RAM, Flash or ROM memory interfaces. MAC address, trimming values etc. are stored in the on-board memory.

2.2 Key Features

- Support for 802.11 ax/ac/a/b/g/n
- Dual band 2.4/5 GHz
- 2x2 MU-MIMO, 1024 QAM
- Industrial temp -40 to +85°C
- Single supply, 3.3V
- Concurrent WiFi 6 and WiFi 5
- Data Rates:
    - Up to 1.2 Gbps with 802.11ax on 80 MHz channel at 5 GHz and dual spatial streams
    - Up to 458 Mbps using 2.4 GHz PHY simultaneously with 5 GHz and Bluetooth
- Full support for 802.11a/b/g/n/ac/ax
- Supports 802.11d/e/h/i/k/r/u/v/w/z/mc.
- WPA2, WPA3 encryption
- Bluetooth 5.1 including LE long range and 2 Mbps.
- No external components except decoupling on power supply
- Low power consumption including sleep and standby modes.
- Supporting STA, AP and P2P simultaneous operation
- Supports Bluetooth-WLAN coexistence and ISM-LTE coexistence.
- Simultaneous WLAN and Bluetooth operation including BLE.

- Extensive DMA hardware support for data flow to reduce CPU load.
- Advanced power management for optimum power consumption at varying load
- External interface is PCIe or 4-bit SDIO 3.0 for WLAN and UART for Bluetooth
- PCM/I2C audio interface for Bluetooth
- On-board High Frequency High Precision Oscillator 40MHz
- RoHS Compliant

3 Block Diagram

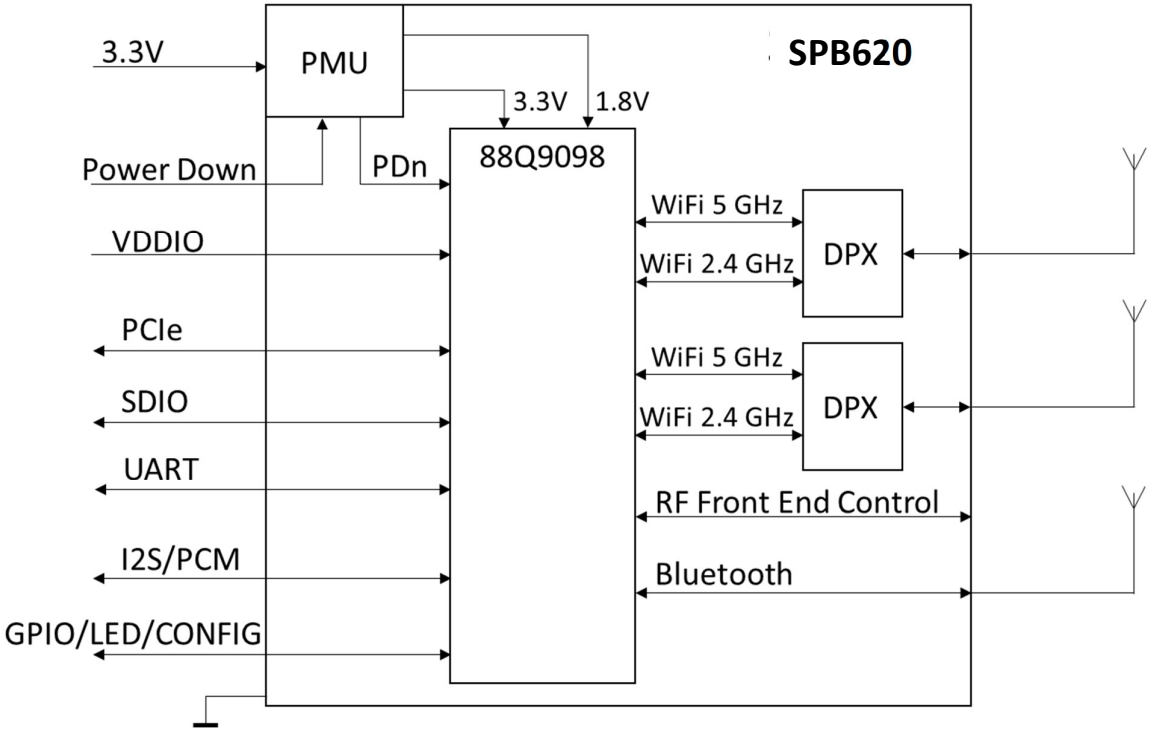

Figure 1. Block diagram.

4 Reference schematic

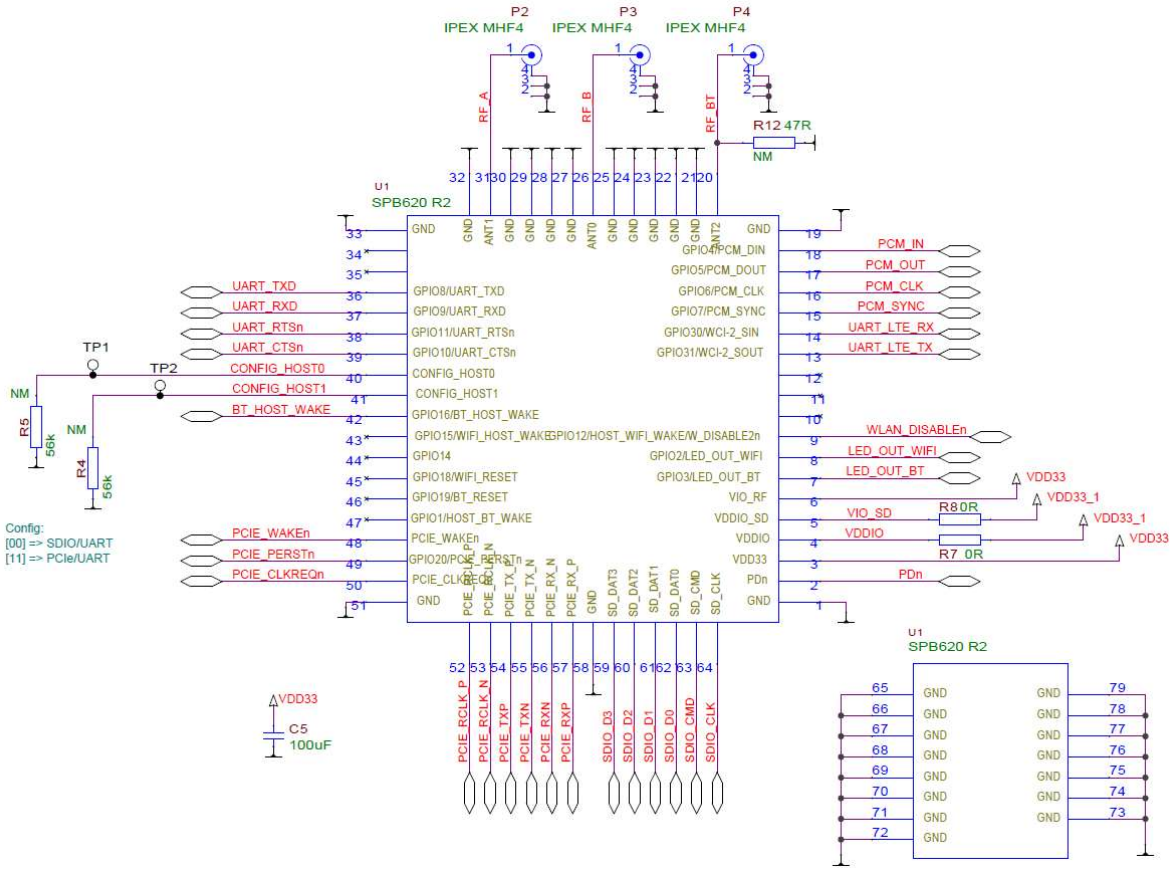

Figure 2. SPB620 reference schematic.

Decouple VDD33 with 100uF to ground.

If the host interface is on 1.8V use a DC-DC converter to create 1.8V for VDDIO and VDDIO_SD. See example shown in Figure 3.

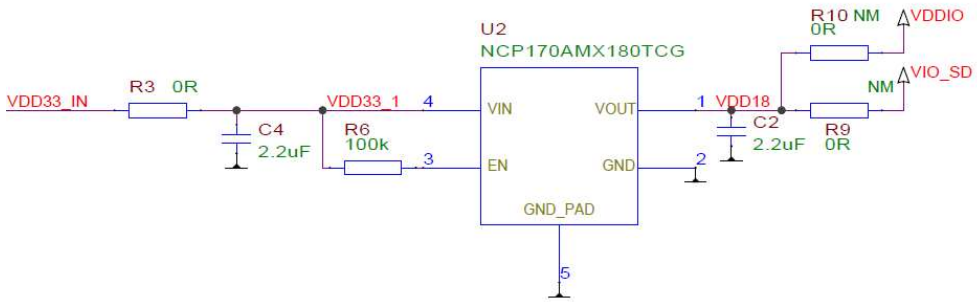

Figure 3. DC-DC for 1.8V IOs

5 Pin Description

The SPB620 module provides several multi-functions IOs that are software configurable.

Table 1. RF Interfaces

Module Pin number	Pin Name	Description
31	RF_A	WLAN RF Port A
26	RF_B	WLAN RF Port B
20	BRF	Bluetooth RF Port

Table 2. PCIe Interface

Module Pin number	Pin Name	Description
52	PCIE_RCLK_P	PCIe differential clock input, positive
53	PCIE_RCLK_N	PCIe differential clock input, negative
54	PCIE_TX_P	PCIe differential data output Place 100nF in series close to the pin
55	PCIE_TX_N	PCIe differential data output Place 100nF in series close to the pin
56	PCIE_RX_N	PCIe differential data input, negative
57	PCIE_RX_P	PCIe differential data input, positive
50	PCIE_CLKREQn	PCIe clock request. External P/U to 3.3V on host side required.
49	PCIE_PERSTn	PCIe host indication to reset device.
48	PCIE_WAKEn	PCIe wake signal. External P/U to 3.3V on host side required.

Table 3. SDIO Host Interface

Module Pin number	Pin Name	Description
64	SD_CLK	Clock input
63	SD_CMD	SDIO 4-bit mode: Command SDIO 1-bit mode: Command
59	SD_DAT3	SDIO 4-bit mode: Data line bit [3] SDIO 1-bit mode: Not used
60	SD_DAT2	SDIO 4-bit mode: Data line bit [2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional)
61	SD_DAT1	SDIO 4-bit mode: Data line bit [1] SDIO 1-bit mode: Interrupt
62	SD_DAT0	SDIO 4-bit mode: Data line bit [0] SDIO 1-bit mode: Data line

The SDIO Interface supports 1-bit and 4-bit SDIO transfer modes up to 208MHz clock frequency.

Table 4. Multi-Purpose Interface [1]

Pin number	Pin Name	No Pad Power State	Reset State	HW[2] State	PD[3] State	PD[4] Prog	Internal PU/PD	PU[5]	PD[5]
7	GPIO3	Tristate	Input	Input	Tristate	Yes	Nominal PU	Yes	Yes
GPIO Mode: GPIO3 (input/output) LED Mode: LED_OUT_BT (output) I2S Mode: I2S_CCLK (output, optional) PCM mode: PCM_MCLK (output, optional)									
8	GPIO2	Tristate	Input	Input	Tristate	Yes	Nominal PU	Yes	Yes
GPIO Mode: GPIO2 (input/output) LED Mode: LED_OUT_WLAN (output)									
9	GPIO12	Tristate	Input	Input	Tristate	Yes	Nominal PD	Yes	Yes
GPIO Mode: GPIO12 (input/output) Default Mode: W_DISABLEn (input) Out-of-band mode: Host to Wi-Fi wake up (input)									
13	GPIO31	Tristate	Input	Input	Tristate	Yes	Nominal PU	Yes	Yes
GPIO Mode: GPIO31 (input/output) JTAG Mode: TDO (JTAG test data, output) WCI-2 Coexistence Mode: WCI-2_SOUT (output)									
14	GPIO30	Tristate	Input	Input	Tristate	Yes	Nominal PU	Yes	Yes
GPIO Mode: GPIO30 (input/output) JTAG Mode: TDI (JTAG test data, input) WCI-2 Coexistence Mode: WCI-2_SIN (input)									
15	GPIO7	Tristate	Input	Input	Tristate	Yes	Nominal PU	Yes	Yes
GPIO Mode: GPIO7 (input/output) I2S Mode: I2S_LRCLK (input/output) PCM Mode: PCM_SYNC (input/output)									
16	GPIO6	Tristate	Input	Input	Tristate	Yes	Weak PU	Yes	Yes
GPIO Mode: GPIO6 (input/output) I2S Mode: I2S_BCLK (input/output) PCM Mode: PCM_CLK (input/output)									
17	GPIO5	Tristate	Input	Input	Tristate	Yes	Weak PU	Yes	Yes
GPIO Mode: GPIO5 (input/output) I2S Mode: I2S_DOUT (output) PCM Mode: PCM_DOUT (output)									
18	GPIO4	Tristate	Input	Input	Tristate	Yes	Weak PU	Yes	Yes
GPIO Mode: GPIO4 (input/output) I2S Mode: I2S_DIN (input) PCM Mode: PCM_DIN (input)									
36	GPIO8	Tristate	Input	Input	Drive low	Yes	Weak PU	No	No
GPIO Mode: GPIO8 (input/output) UART Mode: UART_TXD									
37	GPIO9	Tristate	Input	Input	Tristate	Yes	Nominal PU	Yes	Yes
GPIO Mode: GPIO9 (input/output) UART Mode: UART_RXD									
38	GPIO11	Tristate	Input	Input	Tristate	Yes	Nominal PU	Yes	Yes
GPIO Mode: GPIO11 (input/output) UART Mode: UART_RTSn (output, active low)									
39	GPIO10	Tristate	Input	Input	Tristate	Yes	Weak PU	Yes	Yes
GPIO Mode: GPIO10 (input/output) UART Mode: UART_CTSn (input, active low)									
42	GPIO16	Tristate	Input	Input	Tristate	Yes	Weak PD	Yes	Yes
GPIO Mode: GPIO16 (input/output) Out-of-Band Mode: Bluetooth to host wake up (output)									
43	GPIO15	Tristate	Input	Output	Tristate	Yes	Weak PU	Yes	Yes

Pin number	Pin Name	No Pad Power State	Reset State	HW[2] State	PD[3] State	PD[4] Prog	Internal PU/PD	PU[5]	PD[5]
GPIO Mode: GPIO15 (input/output) Out-of-Band Mode: Wi-Fi to host wake up (output)									
44	GPIO14	Tristate	Input	Output	Tristate	Yes	Weak PU	Yes	Yes
GPIO Mode: GPIO14 (input/output)									
45	GPIO18	Tristate	Input	Input	Tristate	Yes	Weak PU	No	No
GPIO Mode: GPIO18 (input/output) Alternative Mode: Software reset for Wi-Fi subsystem (input)									
46	GPIO19	Tristate	Output	Output	Tristate	Yes	Nominal PU	Yes	No
GPIO Mode: GPIO19 (input/output) Alternative Mode: Software reset for Bluetooth subsystem (input)									
47	GPIO1	Tristate	Output	Output	Tristate	Yes	Weak PU	Yes	No
GPIO Mode: GPIO1 (input/output) Out-of-Band Mode: Host to Bluetooth wakeup (input)									
49	GPIO20	Tristate	Output	Output	Drive high	Yes	Nominal PU	Yes	No
GPIO Mode: GPIO20 (input/output) PCIe Mode: PCIe reset signal from host (input, active low)									
2	PDn	-	-	-	-	-	-	-	-
Full power-down (input, active low) 0 = full power-down 1 = normal mode • Connect to power-down pin of host or VDD33. • External host required to drive this pin high for normal operation. SPB620 has an internal 1M pull-down on this pin.									

[1] Not all GPIO pins can be used for wakeup signals.
[2] Hardware default state after reset.
[3] Power-down state.
[4] Power-down state programmable.
[5] Programmable pull-up/pull-down.

Table 5 Supply Interface

Module Pin number	Pin Name	Description
3	VDD33	Analog 3.3V Supply, decouple with 100uF.
4	VDDIO	GPIO supply. 1.8V or 3.3V
5	VIO_SD	SDIO supply. 1.8V or 3.3V
6	VIO_RF	Digital RF supply, 3.3V
1,19,21,22,23, 24,25,27,28, 29,30,32,33,5 1, 58	GND	Ground
-	GND PAD	All pads in the center of the module shall be connected to GND.

5.1 Host interface

The SPB620 supports three host interfaces:

- SDIO (WLAN only)
- PCIe (WLAN only)
- UART (Bluetooth only)

The interfaces are configured on the CONFIG_HOSTx signals during boot. The pins have internal pull-ups and do not require any external circuitry to be set as “1”. Connect 100 kohm to GND to set the signal to “0”.

CONFIG_HOST[1:0]	WLAN Interface	Bluetooth Interface	Driver Name
00	SDIO	UART	
11	PCIe	UART	

Table 5-6: Host Interface Configuration

6 Bill of Material

Comp	Part name	MFG nr	Description
A1	UWL437		Printed circuit board
C1	100UF 1206 X5R 6.3V 20% GEN		Generic 100uF 1206 X5R 6.3V 20% or better
P2	MHF4 RECEPTACLE MURATA	MM4829-2702	IPEX MHF4 equiv RF-connector
P3	MHF4 RECEPTACLE MURATA	MM4829-2702	IPEX MHF4 equiv RF-connector
P4	MHF4 RECEPTACLE MURATA	MM4829-2702	IPEX MHF4 equiv RF-connector
R7	0R 0201		Generic 0R 0201 resistor
R8	0R 0201		Generic 0R 0201 resistor
U1	SPB620	SPB620-N/L	HDW SPB620 PCB Module

Figure 4. Reference schematic BOM.

7 PCB layout

This section describes the layout of the mother board. A PCIE M2 2230 board is used as an example. It uses MHF4 connectors for RF output. The M2 board also has a 1.8V DCDC for alternative IO voltages. The pcb uses four layers as shown below. VDD33 is colored red, VDDIO is orange and VIO_SD is pink.

7.1 General guidelines

Clear the top layer under the module. Connect the internal ground pads directly to ground using vias, the more the better to improve heat dissipation. In this example, through vias have been used. Use wide copper traces for the 3.3V supply lines to minimize resistive losses. Connect the peripheral ground pads directly to ground using vias. Do not cross RF-signal lines with other lines without a ground plane in between. Use common layout practices.

7.2 PCB stack-up

The following pictures show the layers of the pcb example.

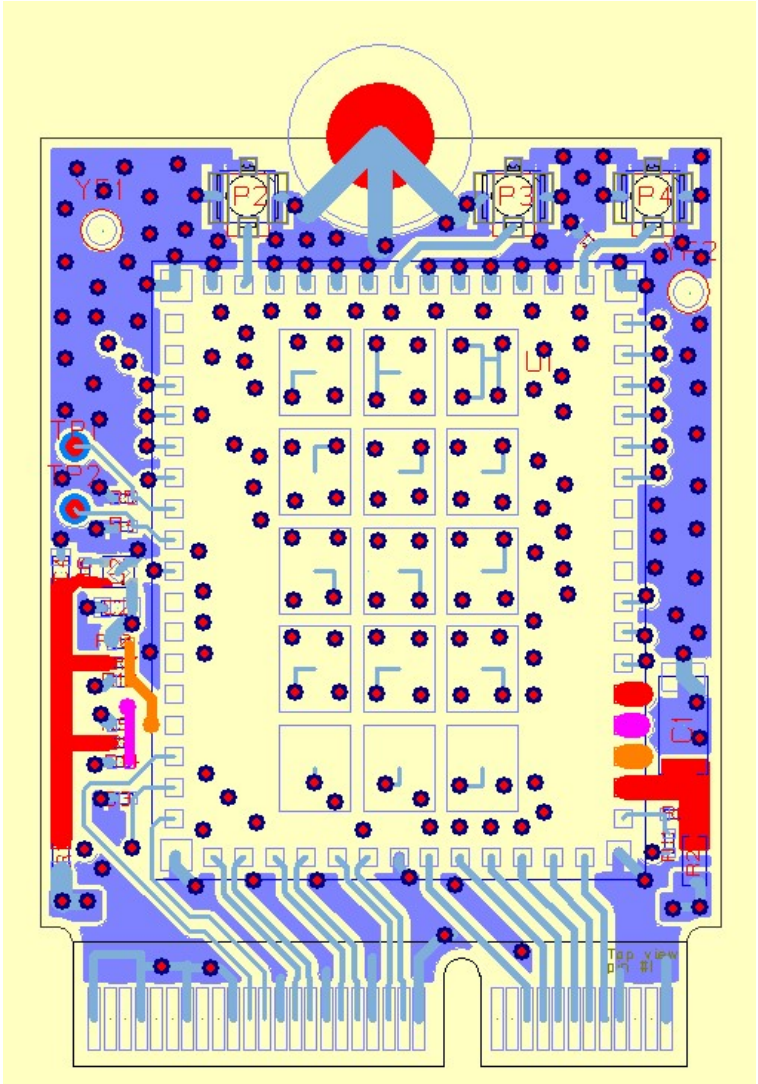

Figure 5. Top layer (signals and ground).

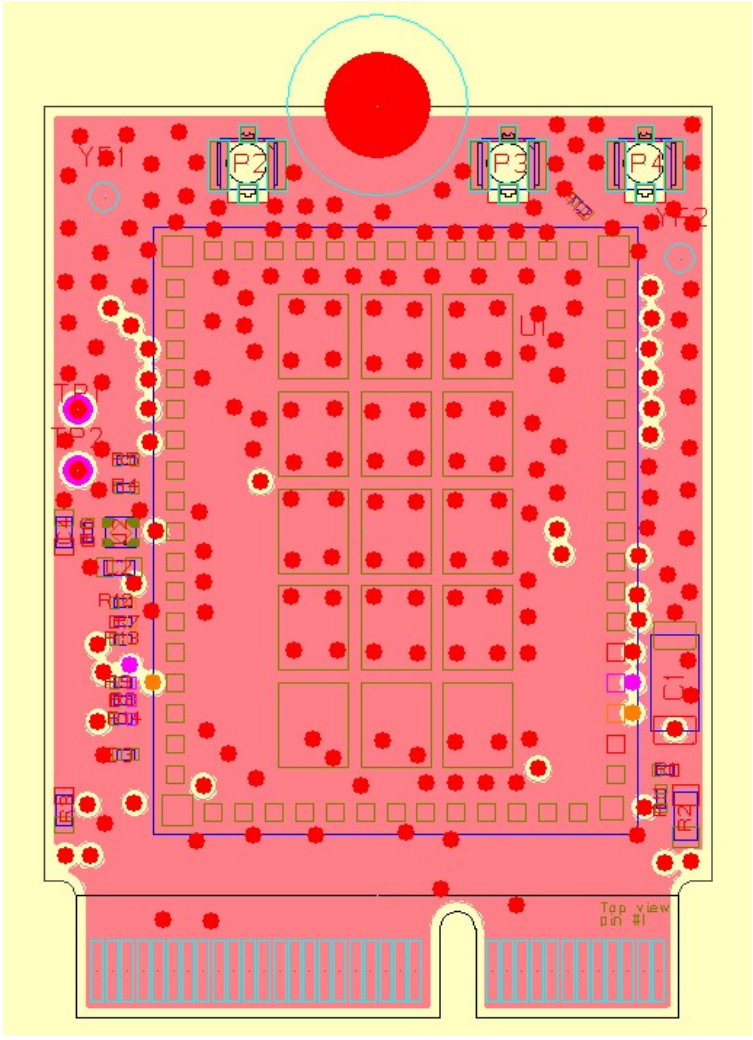

Figure 6. Second layer (RF ground).

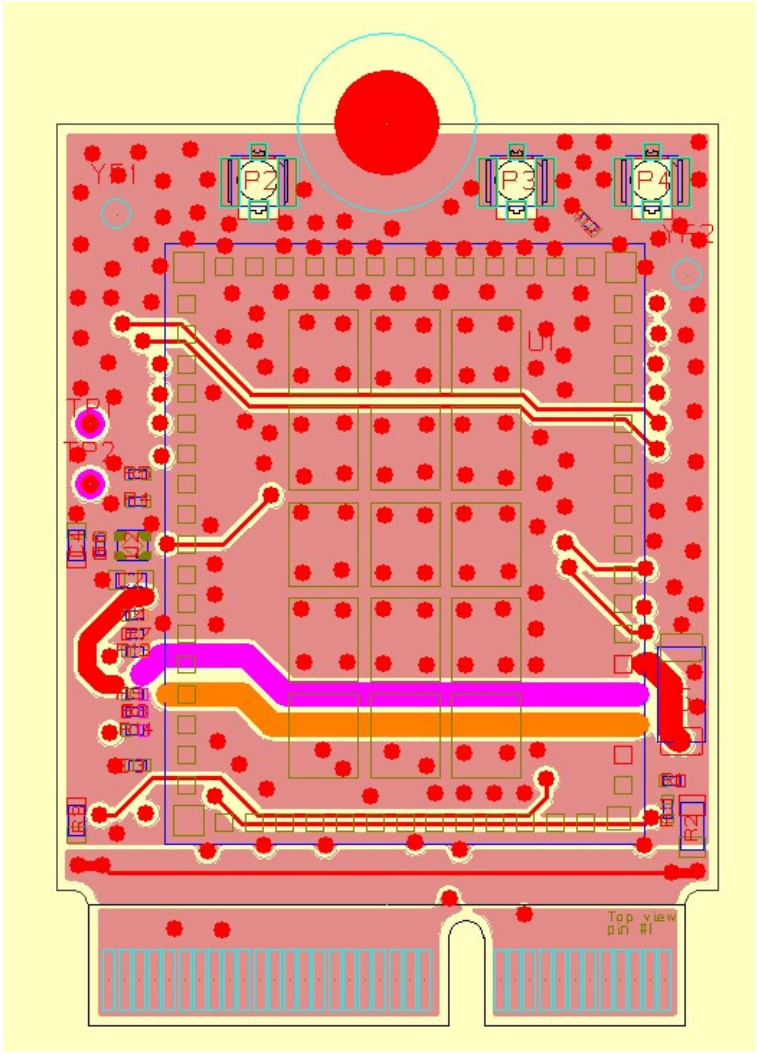

Figure 7. Third layer (ground, signals and supply).

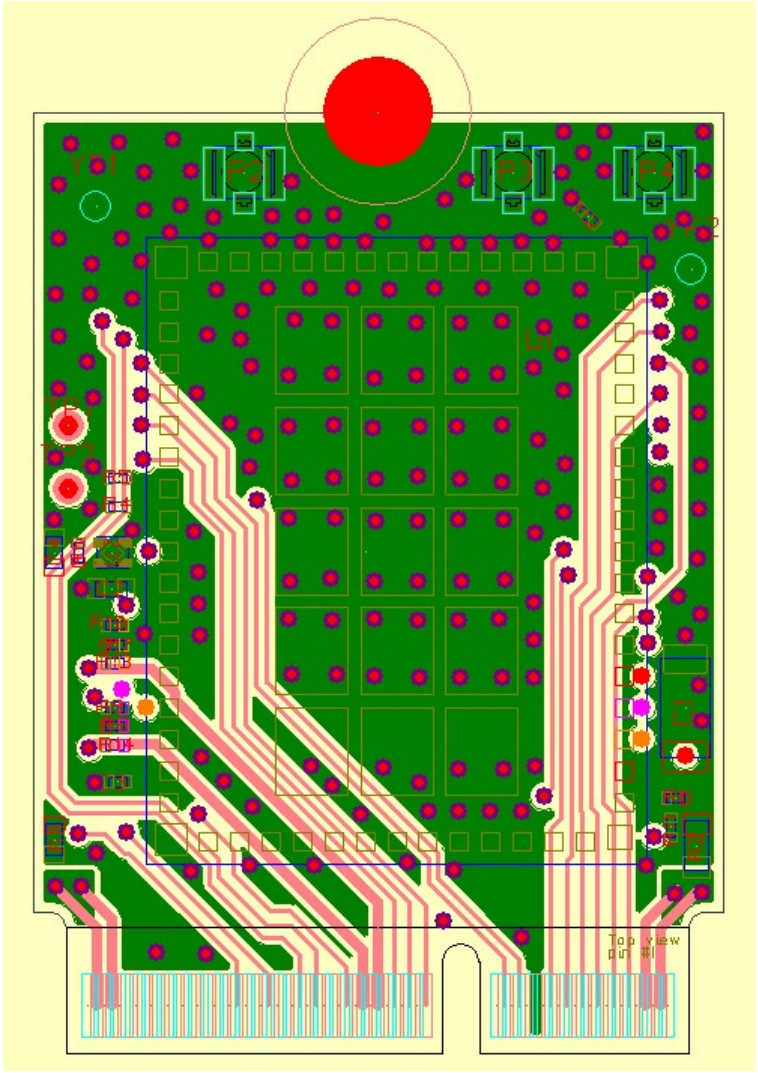

Figure 8. Bottom layer (ground and signals).

8 Options overview

SPB620-N No LTE coexistence filter mounted.
SPB620-L LTE coexistence filter mounted.

Part No.	Description
SPB620-N-2	SPB620 module on Tape&Reel, No LTE co-existence filter
SPB620-L-2	SPB620 module on Tape&Reel, Including LTE co-existence filter
SPB620-N-3	SPB620 module on Tray, No LTE co-existence filter
SPB620-L-3	SPB620 module on Tray, Including LTE co-existence filter
HDA620-SDIO	TBD Development board for SPB620 platform, SD card format
HDA620-PCIE	Development board for SPB620 platform, PCIe card format

Colocation option N has no additional filtering for colocation with LTE units while option L has a bandpass filter on the 2.4GHz paths inside the module to filter out interfering LTE frequencies/reject WLAN TX signals close to LTE frequencies.

9 Antennas

The product is approved with the external antennas in the table below. They are using MHF4 connectors.

SPB620 is approved with the following antennas:

Brand	Model	Type	Cable Length	Gain @ 2.4GHz	Gain @ 5GHz
Molex	204281-1300	Flex Antenna	300 mm	1.3	2.3
Molex	146153-1050	Flex Antenna	50 mm	3.2	4.25
Taoglas	GW.59.3153	Dipole RP-SMA		3.8	5.3
Laird	001-0012	Dipole RP-SMA		2.0	2.0

Table 9. List of FCC approved antennas.

The customer will need to sign a Software Configuration Control Agreement declaring the integration responsibility of the SPB620 WLAN/BT product when it comes to making sure compliance to regulatory domain.

10 Package Specifications

10.1 Mechanical outline

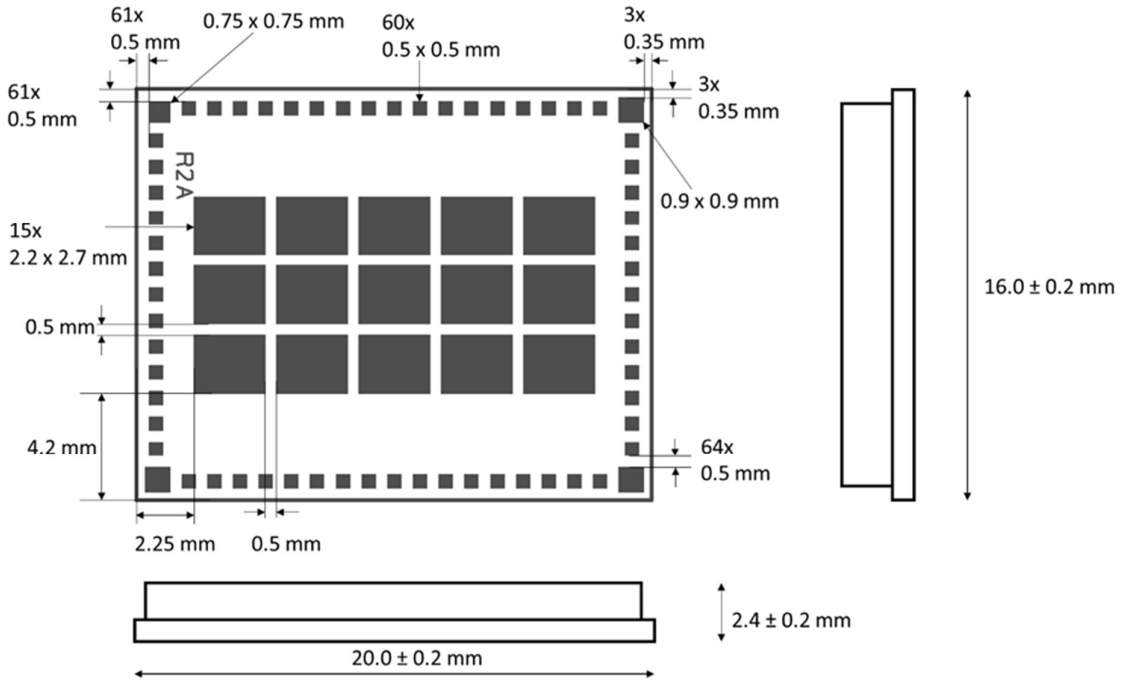

Figure 10. Package dimensions

10.2 Mounting information

Recommended land pattern on the PCB.

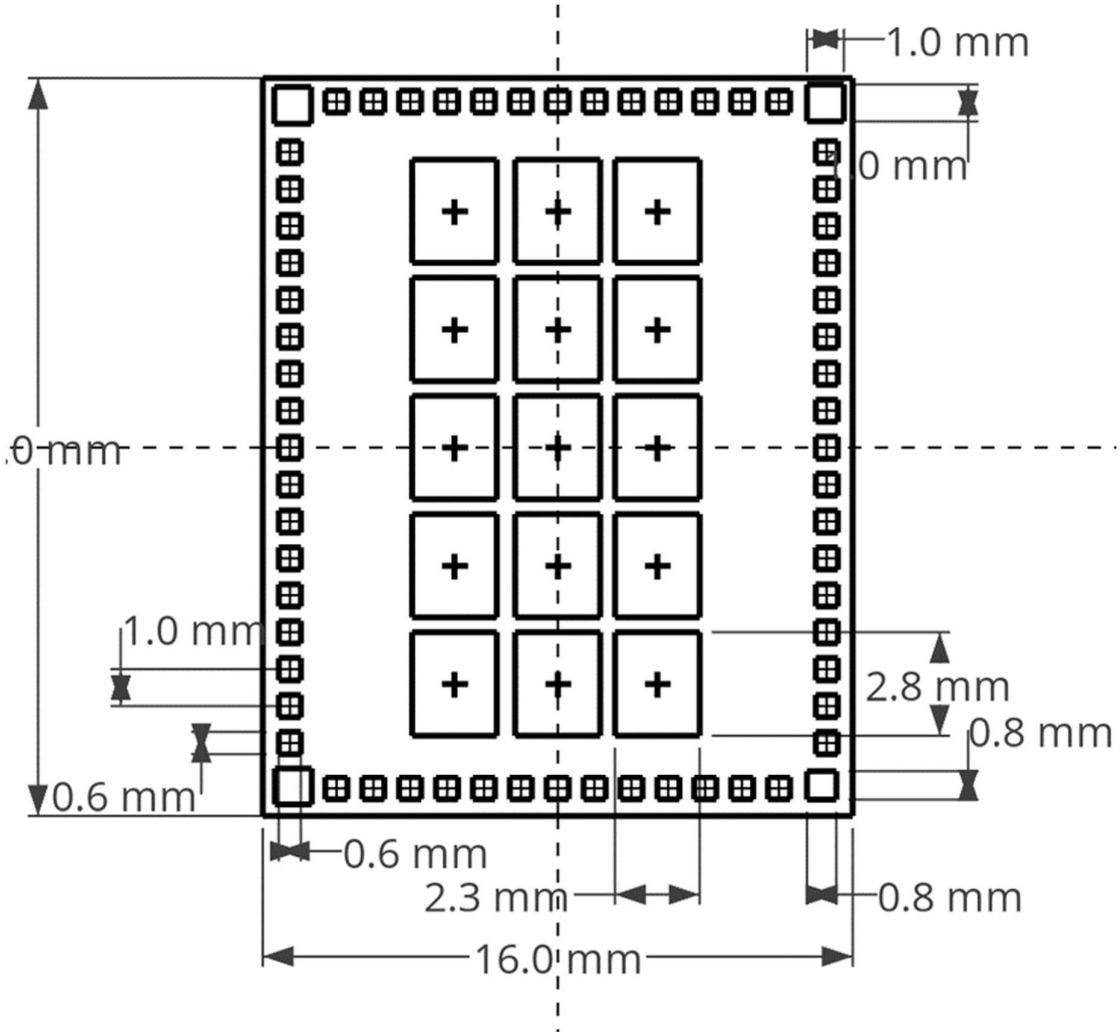

Figure 11. Recommended land pattern on the PCB, top view.

11 Reference PCB Stack-up

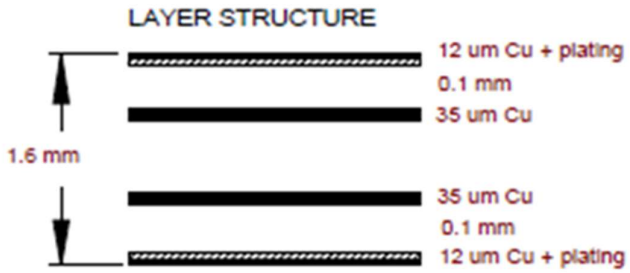

Figure 12. Reference PCB stack-up.