FCM665D

Hardware Design

Short-Range Module Series

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Status: Preliminary

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.

Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.

Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.

Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.

The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.

In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2024-11-21	Devin YU/Casper CHENG	Creation of the document
1.0.0	2024-11-21	Devin YU/Casper CHENG	Preliminary

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1 Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and price-performance ratio

This document defines FCM665D in QuecOpen® solution and describes its hardware interfaces and air interfaces, which are connected with your applications. The document provides a quick insight into interface specifications, RF performance, electrical and mechanical specifications, as well as other related information of the module.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

The module is a cost-effective MCU Wi-Fi 6 and Bluetooth module supporting IEEE 802.11b/g/n/ax and BLE 5.4 standards. It supports Wi-Fi 2.4 GHz and provides multiple interfaces including SPI, QSPI, UART, SDIO, I2C, USB, CAN*, LCM, Camera, PWM, EMAC and I2S for various applications.

The module is an SMD module with compact packaging. The general features of the module are as follow:

- 480 MHz ARMv8-M Star processor
- Built-in 64 KB ROM and 640 KB SRAM memory, 8/16 MB PSRAM and 8/16 MB Flash
- Support for secondary development

Table 2: Basic Information

FCM665D	
Packaging type	LCC + LGA
Pin counts	83
Dimensions	(31.4 ±0.2) mm × (18 ±0.2) mm × (2.15 ±0.2) mm
Weight	approx. 1.96 g

2.1. Key Features

Table 3: Key Features

Basic Information	
Protocols and Standard	● Wi-Fi Protocols: IEEE 802.11b/g/n/ax ● Bluetooth protocol: BLE 5.4 ● All hardware components are fully compliant with EU RoHS directive
Supply Voltage	**VBAT Power Supply:** ● 3.0–3.6 V ● Typ.: 3.3 V
Temperature Ranges	● Normal operating temperature [1]: -40 to +85 °C ● Storage temperature: -45 °C to +95 °C
TE-B Kit	MCU WIFI EVB [2]
Antenna Interface [3]	
Antenna Interfaces	● PCB antenna ● RF coaxial connector ● 50 Ω characteristic impedance
Application Interface [4]	
Application Interfaces	SPI, QSPI, UART, SDIO, I2C, USB, CAN*, LCM, Camera, PWM, I2S, Analog audio, ADC, Touch sensor, EMAC

[1] Within the operating temperature range, the module's related performance meets IEEE and Bluetooth specifications.
[2] Quectel supplies a MCU WIFI EVB with accessories to develop and test the module. For more details, see ***document [1]***.
[3] The module is provided with one of the two antenna/antenna interface designs. For more details, please contact Quectel. Technical Support.
[4] For more details about the interfaces, see ***Chapter 3.3*** and ***Chapter 3.4***.

CE Statement

Hereby, Quectel Wireless Solutions Co., Ltd. declares that the radio equipment type FCM665D is in compliance with Directive 2014/53/EU. This product can be used across EU member states.

The full text of the EU declaration of conformity is available at the following internet address: http://www.quectel.com/support/technical.htm

Disposal of old electrical appliances

The European directive 2012/19/EU on Waste Electrical and Electronic Equipment (WEEE), requires that old household electrical appliances must not be disposed of in the normal unsorted municipal waste stream. Old appliances must be collected separately in order to optimize the recovery and recycling of the materials they contain, and reduce the impact on human health and the environment.

The crossed out “wheeled bin” symbol on the product reminds you of your obligation, that when you dispose of the appliance, it must be separately collected.

Consumers should contact their local authority or retailer for information concerning the correct disposal of their old appliance.

AT	BE	BG	HR	CY	CZ	DK
EE	FI	FR	DE	EL	HU	IE
IT	LV	LT	LU	MT	NL	PL
PT	RO	SK	SI	ES	SE	UK(NI)

This equipment should be installed and operated with minimum distance 20cm between the radiator and your body.

3 Application Interfaces

3.1. Pin Assignment

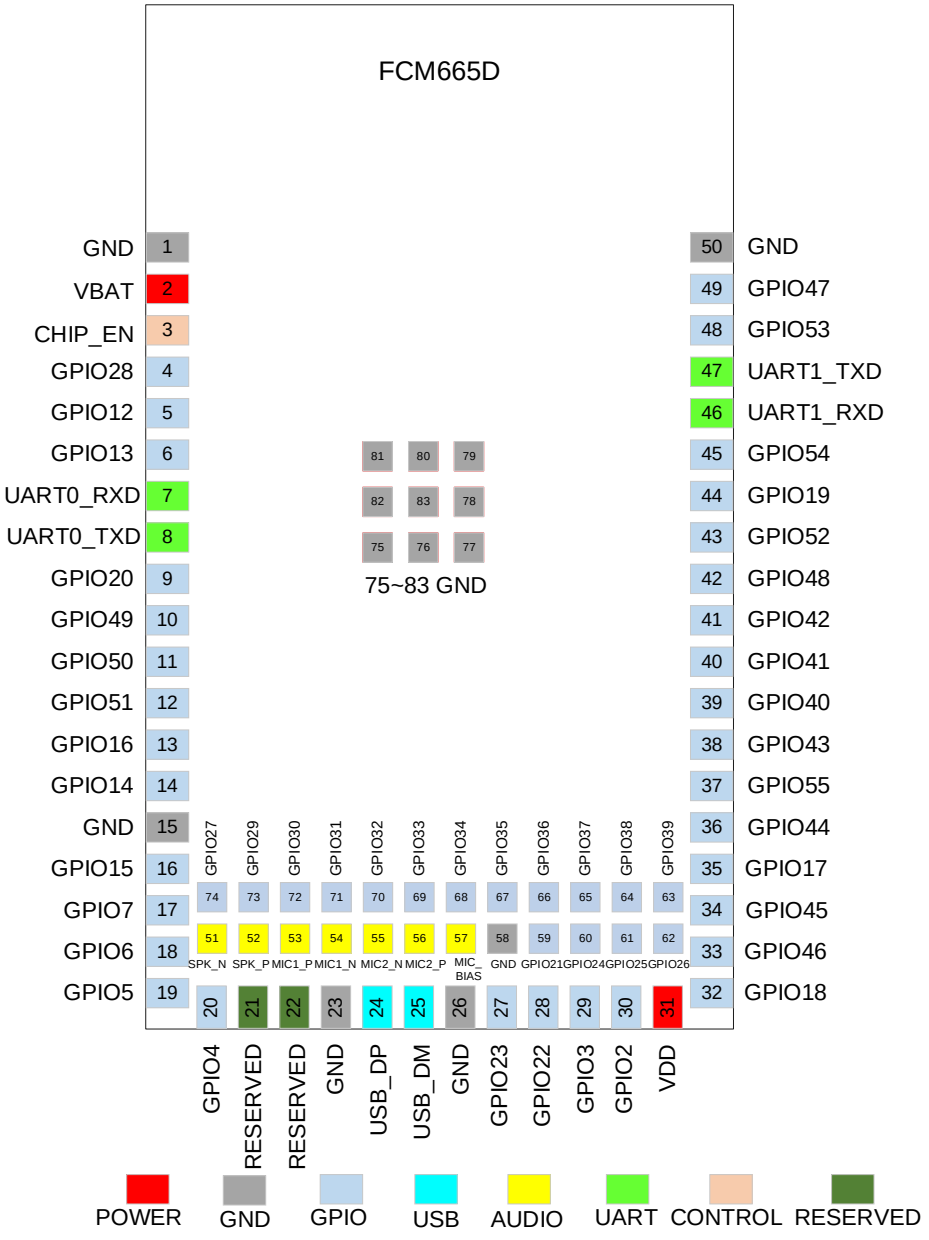


Figure 1: Pin Assignment (Top View)

NOTE

1. Keep all RESERVED and unused pins unconnected.
2. All GND pins should be connected to ground.
3. The module has 50 GPIO interfaces by default. In the case of multiplexing, it supports interfaces including SDIO, UART, SPI, I2C, I2S, PWM and ADC. For more details, see ***Chapter 3.3*** and ***Chapter 3.4***.
4. Ensure that there is no current sink on the module's pins before the module turns on.

3.2. Pin Definitions

Table 4: Parameter Definition

Parameter	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
PI	Power Input
PO	Power Output
PD	Pull-down
PU	Pull-up
Hi-Z	High Impedance

DC characteristics include power domain and rated current.

Table 5: Pin Description

Power Supply						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
VBAT	2	PI	-	Power supply for the module	Vmax = 3.6 V Vmin = 3.0 V Vnom = 3.3 V	It must be provided with sufficient current of at least 0.6 A.
VDD	31	PO	-	Provide 3.3 V for external circuits	3.3 V	The power supply current should not exceed 0.15 A.
GND	1、15、23、26、50、58、75~83					
Control Signal						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
CHIP_EN	3	DI	PU	Module enable (default)	VBAT	Hardware enable. Internally pulled up to VBAT. Active high.
			PD	Module reset		Hardware reset. Internally pulled up to VBAT. Active high.
UART Interfaces						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
UART0_RXD	7	DI	-	UART0 receive	VBAT	
UART0_TXD	8	DO	-	UART0 transmit		
UART1_RXD	46	DI	-	UART1 receive		
UART1_TXD	47	DO	-	UART1 transmit		
USB Interface						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
USB_DP	24	AIO	-	USB 2.0 differential data (+)		USB 2.0 compliant. Require 85–100 Ω differential

USB_DM	25	AIO	-	USB 2.0 differential data (-)		impedance, and 90 Ω is recommended. Test points must be reserved.
GPIO Interfaces						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
GPIO2	30	DIO	Hi-Z	General-purpose input/output	VBAT	Interrupt wakeup.
GPIO3	29	DIO	Hi-Z	General-purpose input/output		
GPIO4	20	DIO	Hi-Z	General-purpose input/output		
GPIO5	19	DIO	Hi-Z	General-purpose input/output		
GPIO6	18	DIO	Hi-Z	General-purpose input/output		
GPIO7	17	DIO	Hi-Z	General-purpose input/output		
GPIO12	5	DIO	Hi-Z	General-purpose input/output		
GPIO13	6	DIO	Hi-Z	General-purpose input/output		
GPIO14	14	DIO	Hi-Z	General-purpose input/output		
GPIO15	16	DIO	Hi-Z	General-purpose input/output		
GPIO16	13	DIO	Hi-Z	General-purpose input/output		
GPIO17	35	DIO	Hi-Z	General-purpose input/output		
GPIO18	32	DIO	Hi-Z	General-purpose input/output		
GPIO19	44	DIO	Hi-Z	General-purpose input/output		
GPIO20	9	DIO	Hi-Z	General-purpose input/output		
GPIO21	59	DIO	Hi-Z	General-purpose input/output		
GPIO22	28	DIO	Hi-Z	General-purpose input/output		

GPIO23	27	DIO	Hi-Z	General-purpose input/output
GPIO24	60	DIO	Hi-Z	General-purpose input/output
GPIO25	61	DIO	Hi-Z	General-purpose input/output
GPIO26	62	DIO	Hi-Z	General-purpose input/output
GPIO27	74	DIO	Hi-Z	General-purpose input/output
GPIO28	4	DIO	Hi-Z	General-purpose input/output
GPIO29	73	DIO	Hi-Z	General-purpose input/output
GPIO30	72	DIO	Hi-Z	General-purpose input/output
GPIO31	71	DIO	Hi-Z	General-purpose input/output
GPIO32	70	DIO	Hi-Z	General-purpose input/output
GPIO33	69	DIO	Hi-Z	General-purpose input/output
GPIO34	68	DIO	Hi-Z	General-purpose input/output
GPIO35	67	DIO	Hi-Z	General-purpose input/output
GPIO36	66	DIO	Hi-Z	General-purpose input/output
GPIO37	65	DIO	Hi-Z	General-purpose input/output
GPIO38	64	DIO	Hi-Z	General-purpose input/output
GPIO39	63	DIO	Hi-Z	General-purpose input/output
GPIO40	39	DIO	Hi-Z	General-purpose input/output
GPIO41	40	DIO	Hi-Z	General-purpose input/output
GPIO42	41	DIO	Hi-Z	General-purpose input/output
GPIO43	38	DIO	Hi-Z	General-purpose input/output

GPIO44	36	DIO	Hi-Z	General-purpose input/output		
GPIO45	34	DIO	Hi-Z	General-purpose input/output		
GPIO46	33	DIO	Hi-Z	General-purpose input/output		
GPIO47	49	DIO	Hi-Z	General-purpose input/output		
GPIO48	42	DIO	Hi-Z	General-purpose input/output		
GPIO49	10	DIO	Hi-Z	General-purpose input/output		
GPIO50	11	DIO	Hi-Z	General-purpose input/output		
GPIO51	12	DIO	Hi-Z	General-purpose input/output		
GPIO52	43	DIO	Hi-Z	General-purpose input/output		
GPIO53	48	DIO	Hi-Z	General-purpose input/output		
GPIO54	45	DIO	Hi-Z	General-purpose input/output		
GPIO55	37	DIO	Hi-Z	General-purpose input/output		
Analog Audio Interfaces						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
SPK_N	51	AO	-	Analog audio differential output (+)		
SPK_P	52	AO	-	Analog audio differential output (-)		
MIC1_P	53	AI	-	Microphone analog input1 (+)		
MIC1_N	54	AI	-	Microphone analog input1 (-)		
MIC2_N	55	AI	-	Microphone analog input2 (-)		
MIC2_P	56	AI	-	Microphone analog input2 (+)		

MIC_BIAS	57	AO	-	Bias voltage output for microphone

RESERVED Pins		
Pin Name	**Pin No.**	**Comment**
RESERVED	21, 22	Keep them unconnected.

3.3. GPIO Multiplexing

The module provides 50 GPIOs by default, and has up to 54 GPIOs in the case of multiplexing. Pins are defined as follows:

Table 6: GPIO Multiplexing

Pin Name	Pin No.	Multiplexing Function 0 (GPIO No.)	Multiplexing Function 1	Multiplexing Function 2	Multiplexing Function 3	Multiplexing Function 4	Multiplexing Function 5	Multiplexing Function 6
UART1_TXD	47	GPIO0	I2C1_SCL	-	SC_IO	ADC12	LIN_TXD	-
UART1_RXD	46	GPIO1	I2C1_SDA	-	SC_CLK	ADC13	LIN_RXD	-
GPIO2	30	GPIO2	SPI1_SCK	SDIO_CLK	SC_RSTN	LIN_SLEEP	QSPI1_SCK	-
GPIO3	29	GPIO3	SPI1_CSN	SDIO_CMD	SC_VCC	-	QSPI1_CS	-
GPIO4	20	GPIO4	SPI1_MOSI	SDIO_DATA0	-	COM6	QSPI1_IO0	SEG30
GPIO5	19	GPIO5	SPI1_MISO	SDIO_DATA1	-	COM7	QSPI1_IO1	SEG31
GPIO6	18	GPIO6	CLK13M	PWMG0_PWM0	-	-	QSPI1_IO2	-
GPIO7	17	GPIO7	WIFI_ACTIVE	PWMG0_PWM1	-	-	QSPI1_IO3	-
UART0_RXD	7	GPIO10	DL_UART_RX	SDIO_DATA2	-	-	-	-
UART0_TXD	8	GPIO11	DL_UART_TX	SDIO_DATA3	-	-	-	-

GPIO12	5	GPIO12	UART0_RTS	ADC14	TOUCH0	-	-	-
GPIO13	6	GPIO13	UART0_CTS	ADC15	TOUCH1	-	-	-
GPIO14	14	GPIO14	SDIO_CLK	SPI0_SCK	I2C1_SCL	RGB_DCLK/ I8080_D15	BT_ANT0	SEG16
GPIO15	16	GPIO15	SDIO_CMD	SPI0_CSN	I2C1_SDA	RGB_DISP/ I8080_D14	BT_ANT1	SEG15
GPIO16	13	GPIO16	SDIO_DATA0	SPI0_MOSI	-	RGB_DE/ I8080_D13	BT_ANT2	SEG14
GPIO17	35	GPIO17	SDIO_DATA1	SPI0_MISO	-	RGB_HSYNC/ I8080_D12	BT_ANT3	SEG13
GPIO18	32	GPIO18	SDIO_DATA2	PWMG0_PWM0	-	RGB_VSYNC/ I8080_D11	-	SEG12
GPIO19	44	GPIO19	SDIO_DATA3	PWMG0_PWM1	-	RGB_R7/ I8080_D10	-	SEG11
GPIO20	9	GPIO20	I2C0_SCL	-	-	RGB_R6/ I8080_D9	-	SEG10
GPIO21	59	GPIO21	I2C0_SDA	ADC6	-	RGB_R5/ I8080_D8	-	SEG9
GPIO22	28	GPIO22	PWMG0_PWM2	ADC5	CLK26M	RGB_R4/ I8080_CSX	QSPI0_SCK	SEG8
GPIO23	27	GPIO23	PWMG0_PWM3	ADC3	-	RGB_R3/ I8080_RESET	QSPI0_CS	SEG7
GPIO24	60	GPIO24	PWMG0_PWM4	ADC2	LPO_CLK	RGB_G7/ I8080_RSX	QSPI0_IO0	SEG6
GPIO25	61	GPIO25	PWMG0_PWM5	ADC1	IRDA	RGB_G6/ I8080_WRX	QSPI0_IO1	SEG5

GPIO26	62	GPIO26	WIFI_TX_EN	-	-	RGB_G5/ I8080_RDX	QSPI0_IO2	SEG4
GPIO27	74	GPIO27	CIS_MCLK	CLK_AUXS_CIS	ENET_PHY_INT	-	QSPI0_IO3	SEG17
GPIO28	4	GPIO28	WIFI_RX_EN	I2S_MCLK	TOUCH2	ADC4	CLK_AUXS_CIS	SEG18
GPIO29	73	GPIO29	CIS_PCLK	-	ENET_MDC	TOUCH3	-	SEG19
GPIO30	72	GPIO30	CIS_HSYNC	UART2_RX	LIN_RXD	TOUCH4	SC_CLK	SEG20
GPIO31	71	GPIO31	CIS_VSYNC	UART2_TX	LIN_TXD	TOUCH5	SC_IO	SEG21
GPIO32	70	GPIO32	CIS_PXD0	PWMG1_PWM0	ENET_MDIO	TOUCH6	SC_RSTN	SEG22
GPIO33	69	GPIO33	CIS_PXD1	PWMG1_PWM1	ENET_RXD0	TOUCH7	SPI0_SCK	SEG23
GPIO34	68	GPIO34	CIS_PXD2	PWMG1_PWM2	ENET_RXD1	TOUCH8	SPI0_CSN	SEG24
GPIO35	67	GPIO35	CIS_PXD3	PWMG1_PWM3	ENET_RXDV	TOUCH9	SPI0_MOSI	SEG25
GPIO36	66	GPIO36	CIS_PXD4	PWMG1_PWM4	ENET_TXD0	TOUCH10	SPI0_MISO	SEG26
GPIO37	65	GPIO37	CIS_PXD5	PWMG1_PWM5	ENET_TXD1	TOUCH11	-	SEG27
GPIO38	64	GPIO38	CIS_PXD6	I2C1_SCL	ENET_TXEN	TOUCH12	COM4	SEG28
GPIO39	63	GPIO39	CIS_PXD7	I2C1_SDA	ENET_REF_CLK	TOUCH13	COM5	SEG29
GPIO40	39	GPIO40	UART2_RX	I2S1_SCK	LIN_RXD	RGB_G4/ I8080_D7	SC_CLK	SEG3
GPIO41	40	GPIO41	UART2_TX	I2S1_SYNC	LIN_TXD	RGB_G3/ I8080_D6	SC_IO	SEG2

GPIO42	41	GPIO42	I2C1_SCL	I2S1_DIN	LIN_SLEEP	RGB_G2/ I8080_D5	SC_RSTN	SEG1
GPIO43	38	GPIO43	I2C1_SDA	I2S1_DOUT	-	RGB_B7/ I8080_D4	SC_VCC	SEG0
GPIO44	36	GPIO44	CAN_TX	SPI0_SCK	-	RGB_B6/ I8080_D3	COM3	I2S2_SCK
GPIO45	34	GPIO45	CAN_RX	SPI0_CSN	-	RGB_B5/ I8080_D2	COM2	I2S2_SYNC
GPIO46	33	GPIO46	CAN_STBY	SPI0_MOSI	ENET_PHY_INT	RGB_B4/ I8080_D1	COM1, TOUCH14	I2S2_DIN
GPIO47	49	GPIO47	TOUCH15	SPI0_MISO	ENET_MDC	RGB_B3/ I8080_D0	COM0	I2S2_DOUT
GPIO48	42	GPIO48	-	-	ENET_MDIO	RGB_R2/ I8080_D16	-	-
GPIO49	10	GPIO49	-	-	ENET_RXD0	RGB_R1/ I8080_D17	-	-
GPIO50	11	GPIO50	-	-	ENET_RXD1	RGB_R0	-	-
GPIO51	12	GPIO51	-	-	ENET_RXDV	RGB_G1	-	-
GPIO52	43	GPIO52	-	-	ENET_TXD0	RGB_G0	-	-
GPIO53	48	GPIO53	-	-	ENET_TXD1	RGB_B2	-	-
GPIO54	45	GPIO54	-	-	ENET_TXEN	RGB_B1	-	-
GPIO55	37	GPIO55	-	-	ENET_REF_CLK	RGB_B0	-	-

NOTE

1. All GPIOs support interrupting wakeup.
2. After the module is powered off, all of its GPIOs must be driven low. Otherwise, the current leakage may make the module enter an abnormal state.
3. For details about GPIO driving current configuration, see ***document [5]***.

3.4. Interface Definition

3.4.1. SPI Interfaces

In the case of multiplexing, the module integrates 2 SPIs (SPI0 and SPI1) that can operate in master or slave mode with maximum clock frequency of 30 MHz (master mode by default). The SPIs support 8-bit or 16-bit data width and 4-wire or 3-wire (without CS pin) mode. Each pin of SPI0 has three GPIO choices.

Table 7: Pin Description of SPI Interfaces

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
GPIO14	14	SPI0_SCK	DIO	SPI0 clock	
GPIO16	16	SPI0_ CSN	DIO	SPI0 chip select	
GPIO15	13	SPI0_ MOSI	DIO	SPI0 master-out slave-in	In master mode, it is an output signal; In slave mode, it is an input signal. Other SPI configurations, see ***Table 6***.
GPIO17	35	SPI0_MISO	DIO	SPI0 master-in slave-out	In master mode, it is an input signal; In slave mode, it is an output signal. Other SPI configurations, see ***Table 6***.
GPIO33	69	SPI0_SCK	DIO	SPI0 clock	
GPIO34	68	SPI0_ CSN	DIO	SPI0 chip select	
GPIO35	67	SPI0_ MOSI	DIO	SPI0 master-out slave-in	In master mode, it is an output signal; In slave mode, it is an input signal. Other SPI configurations, see ***Table 6***.
GPIO36	66	SPI0_MISO	DIO	SPI0 master-in slave-out	In master mode, it is an input signal;

					In slave mode, it is an output signal. Other SPI configurations, see ***Table 6***.
GPIO44	36	SPI0_SCK	DIO	SPI0 clock	
GPIO45	34	SPI0_ CSN	DIO	SPI0 chip select	
GPIO46	33	SPI0_ MOSI	DIO	SPI0 master-out slave-in	In master mode, it is an output signal; In slave mode, it is an input signal. Other SPI configurations, see ***Table 6***.
GPIO47	49	SPI0_MISO	DIO	SPI0 master-in slave-out	In master mode, it is an input signal; In slave mode, it is an output signal. Other SPI configurations, see ***Table 6***.
GPIO2	30	SPI1_SCK	DIO	SPI1 clock	
GPIO3	29	SPI1_CSN	DIO	SPI1 chip select	
GPIO4	20	SPI1_MOSI	DIO	SPI1 master-out slave-in	In master mode, it is an output signal; In slave mode, it is an input signal. Other SPI configurations, see ***Table 6***.
GPIO5	19	SPI1_MISO	DIO	SPI1 master-in slave-out	In master mode, it is an input signal; In slave mode, it is an output signal. Other SPI configurations, see ***Table 6***.

The following figure shows the connection between the host and the slave:

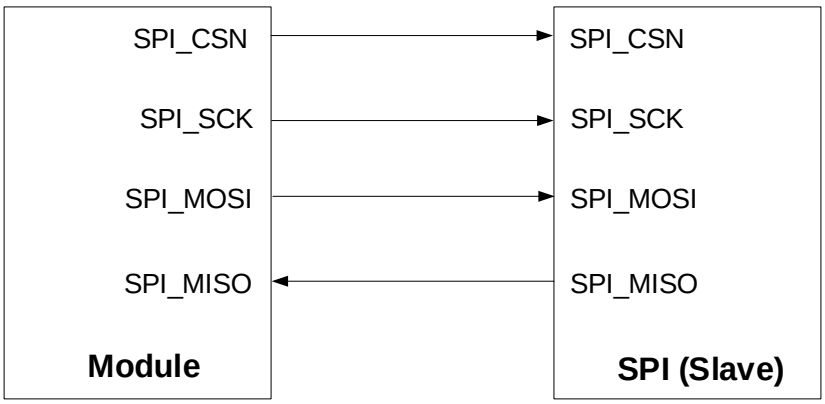


Figure 2: SPI Connection (Master Mode)

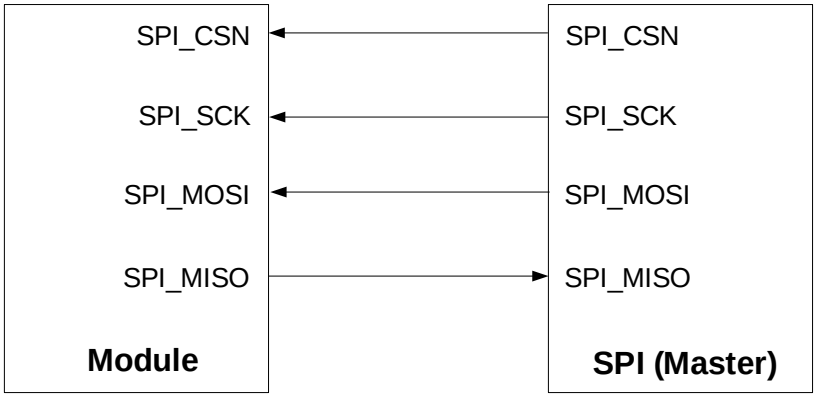


Figure 3: SPI Connection (Slave Mode)

3.4.2. QSPI Interfaces

In the case of multiplexing, the module embeds 2 Quad SPIs (QSPI0 and QSPI1) that support master mode only. It supports external flash, PSRAM and AMOLED display. The QSPI allows maximum clock frequency up to 80 MHz.

Table 8: Pin Description of QSPI Interfaces

Pin Name	Pin No.	Multiplexing Function	I/O	Description
GPIO22	28	QSPI0_SCK	DO	QSPI0 clock
GPIO23	27	QSPI0_CS	DO	QSPI0 chip select
GPIO24	60	QSPI0_IO0	DIO	QSPI0 data bit 0
GPIO25	61	QSPI0_IO1	DIO	QSPI0 data bit 1

GPIO26	62	QSPI0_IO2	DIO	QSPI0 data bit 2
GPIO27	74	QSPI0_IO3	DIO	QSPI0 data bit 3
GPIO2	30	QSPI1_SCK	DO	QSPI0 clock
GPIO3	29	QSPI1_CS	DO	QSPI0 chip select
GPIO4	20	QSPI1_IO0	DIO	QSPI0 data bit 0
GPIO5	19	QSPI1_IO1	DIO	QSPI0 data bit 1
GPIO6	18	QSPI1_IO2	DIO	QSPI0 data bit 2
GPIO7	17	QSPI1_IO3	DIO	QSPI0 data bit 3

The following figure shows the QSPI connection between the host and the slave:

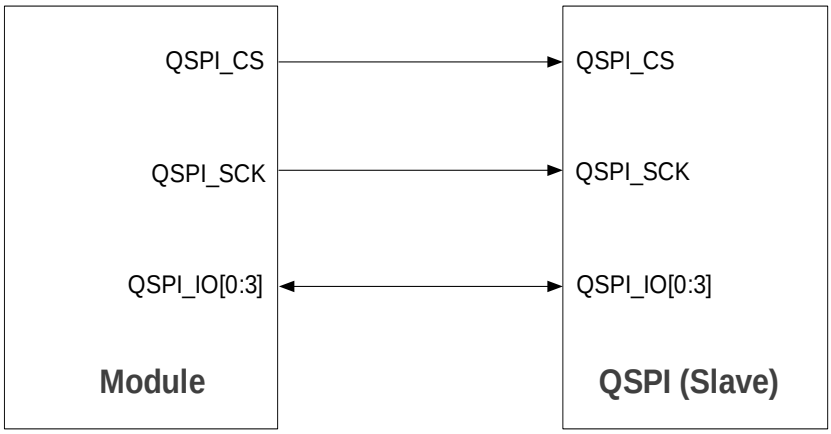


Figure 4: QSPI Connection (Master Mode)

3.4.3. UART Interfaces

The module provides 3 UART interfaces, among which UART0 is default configuration while UART1 and UART2 are multiplexed from the GPIOs. The interfaces support full-duplex asynchronous serial communication at a baud rate up to 6 Mbps. UART0 supports hardware flow control with RTS and CTS signals, flash download and debugging information output. Each UART embeds a 128-byte Tx FIFO and a 128-byte Rx FIFO. FIFO mode is disabled by default and can be enabled by software.

Table 9: Pin Description of UART Interfaces

Pin Name	Pin No.	Multiplexing Function	I/O	Comment
UART0_RXD	7	-	DI	UART0 receive
UART0_TXD	8	-	DO	UART0 transmit
GPIO12	5	UART0_RTS	DO	Request to send signal from the module
GPIO13	6	UART0_CTS	DI	Clear to send signal to the module
UART1_TXD	47	-	DO	UART1 transmit
UART1_RXD	46	-	DI	UART1 receive
GPIO40	39	UART2_RXD	DI	UART2 receive
GPIO41	40	UART2_TXD	DO	UART2 transmit

The UART0 can be used for command communication and data transmission. It is recommended to use the CH340 serial port tool and set the communication rate to 2,000,000 bps during flash download or firmware upgrading. The UART0 connection between the module and the MCU is illustrated below.

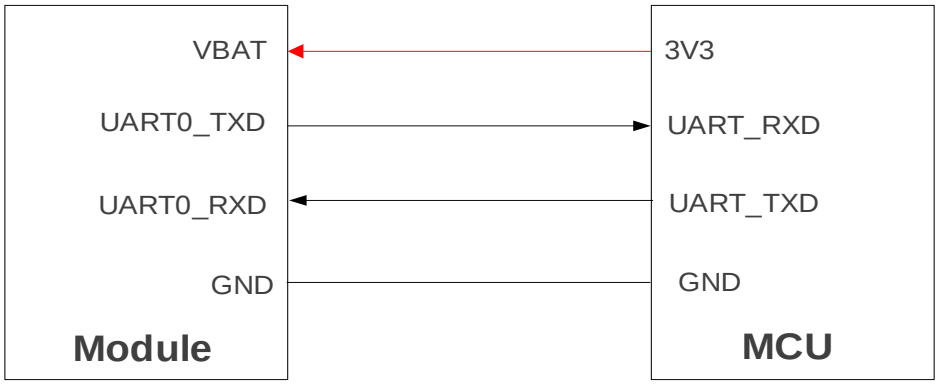


Figure 5: UART0 Connection

NOTE

To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

3.4.4. SDIO Interface

In the case of multiplexing, the module provides 1 SDIO 2.0 interface which can be used as a host to read external SD cards or as a slave to communicate with an external host. It allows a maximum 80 MHz clock speed and supports 1 bit (default) or 4 bits data bus mode. Each pin of SDIO has two GPIO choices.

Table 10: Pin Description of SDIO Interface

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
GPIO2	30	SDIO_CLK	DI	SDIO clock	Other SDIO configurations, see ***Table 6***.
GPIO3	29	SDIO_CMD	DIO	SDIO command	
GPIO4	20	SDIO_DATA0	DIO	SDIO data bit 0	
GPIO5	19	SDIO_DATA1	DIO	SDIO data bit 1	
UART0_RXD	7	SDIO_DATA2	DIO	SDIO data bit 2	
UART0_TXD	8	SDIO_DATA3	DIO	SDIO data bit 3	
GPIO14	14	SDIO_CLK	DI	SDIO clock	
GPIO15	16	SDIO_CMD	DIO	SDIO command	
GPIO16	13	SDIO_DATA0	DIO	SDIO data bit 0	
GPIO17	35	SDIO_DATA1	DIO	SDIO data bit 1	
GPIO18	32	SDIO_DATA2	DIO	SDIO data bit 2	
GPIO19	44	SDIO_DATA3	DIO	SDIO data bit 3	

The following figure shows the SDIO interface connection between the module and the host:

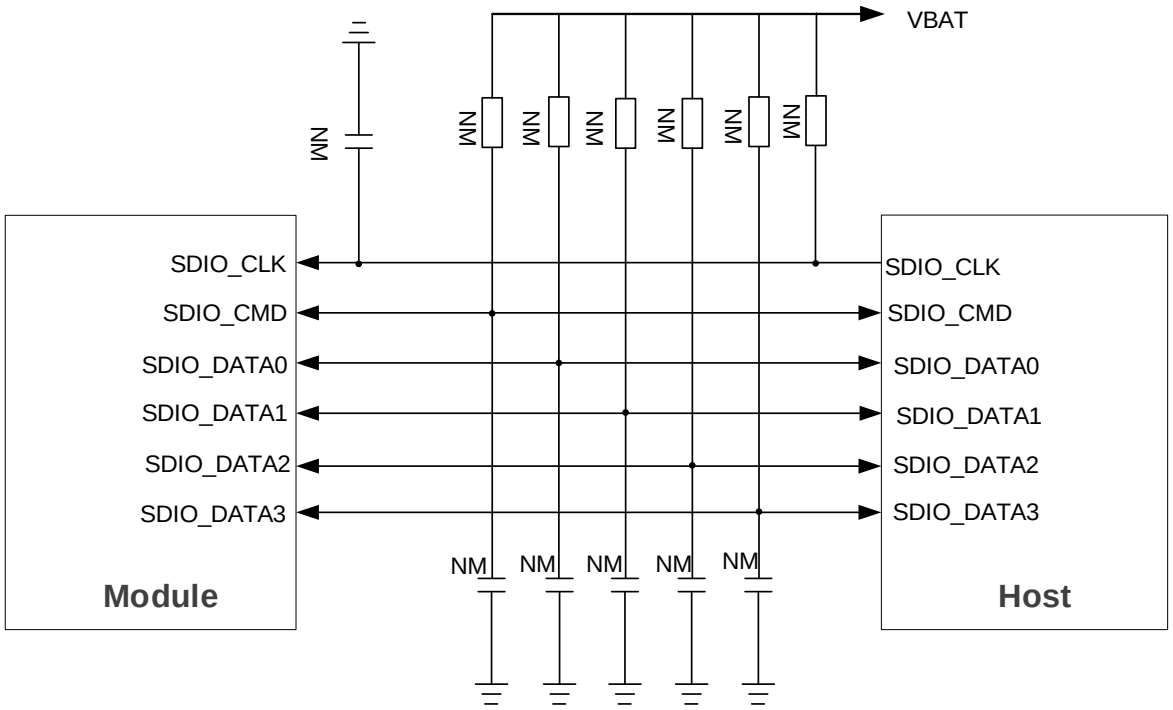


Figure 6: SDIO Interface Connection

To ensure compliance of interface design with the SDIO 2.0 specification, it is recommended to adopt the following principles:

- To minimize bus jitter, reserve 10–100 kΩ pull-up resistors (with a recommended value of 10 kΩ) on the SDIO_CMD, SDIO_DATA[0:3], and SDIO_CLK signal traces and pull them up to VDD of the module.
- It is recommended to route the SDIO traces in inner layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below. The impedance of SDIO signal trace is 50 Ω ±10 %. And the SDIO_CLK signal trace should be routed with ground surrounded separately.
- Route SDIO traces in parallel on the same layer whenever possible, ensuring that there are enough ground vias around the SDIO traces and connecting them to a ground plane.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noise signals such as clock signals and DC-DC signals.
- The distance between SDIO signals and other signals must be greater than twice the trace width, and the bus load capacitance must be less than 15 pF.
- SDIO signal traces (SDIO_CLK and SDIO_DATA[0:3]/SDIO_CMD) need to be equal in length (less than 0.5 mm distance between the traces).

3.4.5. I2C Interfaces

In the case of multiplexing, the module supports up to 2 I2C interfaces which can operate in master or

slave mode. The interfaces support standard (up to 100 kbps) and fast (up to 400 kbps) modes with 7-bit and 10-bit addressing. If low level on I2C0/1_SCL or bus idle duration is greater than a programmable threshold, it will generate interrupt to MCU. Each pin of I2C1 has four GPIO choices.

Table 11: Pin Description of I2C Interfaces

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
GPIO20	9	I2C0_SCL	OD	I2C0 serial clock	Other I2C configurations, see ***Table 6***.
GPIO21	59	I2C0_SDA	OD	I2C0 serial data	
UART1_TXD	47	I2C1_SCL	OD	I2C1 serial clock	
UART1_RXD	46	I2C1_SDA	OD	I2C1 serial data	
GPIO14	14	I2C1_SCL	OD	I2C1 serial clock	
GPIO15	16	I2C1_SDA	OD	I2C1 serial data	
GPIO38	64	I2C1_SCL	OD	I2C1 serial clock	
GPIO39	63	I2C1_SDA	OD	I2C1 serial data	
GPIO42	41	I2C1_SCL	OD	I2C1 serial clock	
GPIO43	38	I2C1_SDA	OD	I2C1 serial data	

NOTE

Reserve 1–10 kΩ pull-up resistors to VBAT when I2C0 and I2C1 interfaces are connected to an external equipment.

3.4.6. USB Interface

The module provides an USB interface compliant with USB 2.0 specifications. It can operate as a host or a slave device and supports high-speed operation (up to 480 Mbps).

Table 12: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	24	AIO	USB 2.0 differential data (+)	USB 2.0 compliant. Require 85–100 Ω differential impedance,

USB_DM	25	AIO	USB 2.0 differential data (-)	and 90 Ω is recommended. Test points must be reserved.

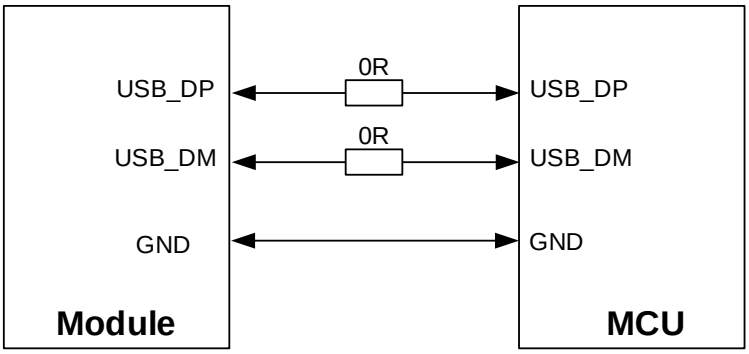


Figure 7: USB Interface Connection

The following principles should be complied with when design the USB interface, to meet USB 2.0 specifications.

- Route the USB signal traces as differential pairs with ground surrounded. The differential impedance of USB 2.0 is 90 Ω ±10 %.
- For USB 2.0 signal traces, the differential data pair matching should be less than 1 mm.
- Do not route signal traces under crystals, oscillators, magnetic devices, sensitive circuits/signals, such as RF circuits and analog signals, as well as noisy signals such as clock signals and DC-DC signals. Route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Junction capacitance of the ESD protection components might cause influences on USB data lines, so you should pay attention to the selection of the device. Typically, the stray capacitance should be less than 2.0 pF for USB 2.0.
- If possible, reserve a 0 Ω resistor on USB_DP and USB_DM traces respectively.

For more details about the USB 2.0 specifications, visit http://www.usb.org/home.

3.4.7. CAN Interface*

In the case of multiplexing, the module provides 1 CAN interface which is compliant with the CAN 2.0B specification. It can be configured to meet the specification of CAN with flexible data rate CAN FD. CAN 2.0 carries a data payload up to 8 bytes and CAN FD up to 64 bytes.

Table 13: Pin Description of CAN Interface

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
GPIO44	36	CAN_TX	DO	CAN transmit data	VBAT power domain.
GPIO45	34	CAN_RX	DI	CAN receive data	
GPIO46	33	CAN_STBY	DIO	CAN transceiver standby	

3.4.8. LCM Interface

In the case of multiplexing, the module supports an TFT-LCD display controller capable of providing a 24-bit parallel digital RGB (Red, Green, Blue) or an 18-bit I8080 interface. The controller supports YUV422/RGB565/RGB888 in RGB display.

Table 14: Pin Description of LCM_RGB Interface

Pin Name	Pin No.	Multiplexing Function	I/O	Description
GPIO14	14	RGB_DCLK	DO	RGB pixel clock
GPIO15	16	RGB_DISP	DO	RGB display switch
GPIO16	13	RGB_DE	DO	RGB data enable
GPIO17	35	RGB_HSYNC	DO	RGB horizontal sync
GPIO18	32	RGB_VSYNC	DO	RGB vertical sync
GPIO19	44	RGB_R7	DIO	RGB red data 7
GPIO20	9	RGB_R6	DIO	RGB red data 6
GPIO21	59	RGB_R5	DIO	RGB red data 5
GPIO22	28	RGB_R4	DIO	RGB red data 4
GPIO23	27	RGB_R3	DIO	RGB red data 3
GPIO24	60	RGB_G7	DIO	RGB green data 7
GPIO25	61	RGB_G6	DIO	RGB green data 6
GPIO26	62	RGB_G5	DIO	RGB green data 5

GPIO40	39	RGB_G4	DIO	RGB green data 4
GPIO41	40	RGB_G3	DIO	RGB green data 3
GPIO42	41	RGB_G2	DIO	RGB green data 2
GPIO43	38	RGB_B7	DIO	RGB blue data 7
GPIO44	36	RGB_B6	DIO	RGB blue data 6
GPIO45	34	RGB_B5	DIO	RGB blue data 5
GPIO46	33	RGB_B4	DIO	RGB blue data 4
GPIO47	49	RGB_B3	DIO	RGB blue data 3
GPIO48	42	RGB_R2	DIO	RGB red data 2
GPIO49	10	RGB_R1	DIO	RGB red data 1
GPIO50	11	RGB_R0	DIO	RGB red data 0
GPIO51	12	RGB_G1	DIO	RGB green data 1
GPIO52	43	RGB_G0	DIO	RGB green data 0
GPIO53	48	RGB_B2	DIO	RGB blue data 2
GPIO54	45	RGB_B1	DIO	RGB blue data 1
GPIO55	37	RGB_B0	DIO	RGB blue data 0

Table 15: Pin Description of LCM_I8080 Interface

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
GPIO14	14	I8080_D15	DIO	I8080 data bit 15	
GPIO15	16	I8080_D14	DIO	I8080 data bit 14	
GPIO16	13	I8080_D13	DIO	I8080 data bit 13	
GPIO17	35	I8080_D12	DIO	I8080 data bit 12	
GPIO18	32	I8080_D11	DIO	I8080 data bit 11	
GPIO19	44	I8080_D10	DIO	I8080 data bit 10	

GPIO20	9	I8080_D9	DIO	I8080 data bit 9	
GPIO21	59	I8080_D8	DIO	I8080 data bit 8	
GPIO22	28	I8080_CSX	DO	I8080 chip select	Active low.
GPIO23	27	I8080_RESET	DO	I8080 reset	
GPIO24	60	I8080_RSX	DO	I8080 data/command select	
GPIO25	61	I8080_WRX	DO	I8080 write data	Active low.
GPIO26	62	I8080_RDX	DO	I8080 read data	
GPIO40	39	I8080_D7	DIO	I8080 data bit 7	
GPIO41	40	I8080_D6	DIO	I8080 data bit 6	
GPIO42	41	I8080_D5	DIO	I8080 data bit 5	
GPIO43	38	I8080_D4	DIO	I8080 data bit 4	
GPIO44	36	I8080_D3	DIO	I8080 data bit 3	
GPIO45	34	I8080_D2	DIO	I8080 data bit 2	
GPIO46	33	I8080_D1	DIO	I8080 data bit 1	
GPIO47	49	I8080_D0	DIO	I8080 data bit 0	
GPIO48	42	I8080_D16	DIO	I8080 data bit 16	
GPIO49	10	I8080_D17	DIO	I8080 data bit 17	

3.4.9. Camera Interface

In the case of multiplexing, the module supports 1 camera interface. The 8-bit CMOS Image Sensor (CIS) Digital Video Port (DVP) camera interface provides 8-bit parallel port interface to sensors, together with main clock (MCLK), pixel clock (PCLK), horizontal SYNC (HSYNC) and vertical SYNC (VSYNC) signals.

The YUV sensor's input will be directly fed to the hardware JPEG encoder, and the JPEG encoder output is written to data memory directly by a dedicated DMA channel. The YUV signal format could be YUYV, UYVY, YYUV and UVYY. The module supports RGB565. HSYNC and VSYNC level could be set independently.

Table 16: Pin Description of Camera Interface

Pin Name	Pin No.	Multiplexing Function	I/O	Description
GPIO27	74	CIS_MCLK	DO	CIS master clock
GPIO29	73	CIS_PCLK	DO	CIS pixel clock
GPIO30	72	CIS_HSYNC	DO	CIS horizontal sync
GPIO31	71	CIS_VSYNC	DO	CIS vertical sync
GPIO32	70	CIS_PXD0	DIO	CIS data bit 0
GPIO33	69	CIS_PXD1	DIO	CIS data bit 1
GPIO34	68	CIS_PXD2	DIO	CIS data bit 2
GPIO35	67	CIS_PXD3	DIO	CIS data bit 3
GPIO36	66	CIS_PXD4	DIO	CIS data bit 4
GPIO37	65	CIS_PXD5	DIO	CIS data bit 5
GPIO38	64	CIS_PXD6	DIO	CIS data bit 6
GPIO39	63	CIS_PXD7	DIO	CIS data bit 7

3.4.10. PWM Interfaces

In the case of multiplexing, the module supports 2 PWM groups, and each group includes 4 independent PWM channels. Each mode of each channel is multiplexed with 32-bit counting. Each PWM channel has three modes: Timer mode, PWM mode, and Capture mode.

Table 17: Pin Description of PWM Interfaces

Pin Name	Pin No.	Multiplexing Function	I/O	Description
GPIO6/GPIO18	18/32	PWMG0_PWM0	DIO	PWMG0_PWM0 output
GPIO7/GPIO19	17/44	PWMG0_PWM1	DIO	PWMG0_PWM1 output
GPIO22	28	PWMG0_PWM2	DIO	PWMG0_PWM2 output
GPIO23	27	PWMG0_PWM3	DIO	PWMG0_PWM3 output

GPIO24	60	PWMG0_PWM4	DIO	PWMG0_PWM4 output
GPIO25	61	PWMG0_PWM5	DIO	PWMG0_PWM5 output
GPIO32	70	PWMG1_PWM0	DIO	PWMG1_PWM0 output
GPIO33	69	PWMG1_PWM1	DIO	PWMG1_PWM1 output
GPIO34	68	PWMG1_PWM2	DIO	PWMG1_PWM2 output
GPIO35	67	PWMG1_PWM3	DIO	PWMG1_PWM3 output
GPIO36	66	PWMG1_PWM4	DIO	PWMG1_PWM4 output
GPIO37	65	PWMG1_PWM5	DIO	PWMG1_PWM5 output

NOTE

1. It is not recommended to use GPIO22 and GPIO23 for LED and motor control.
2. When PWM2 and PWM3 are enabled simultaneously, they cannot generate waveforms with different duty cycles.
3. When PWM4 and PWM5 are enabled simultaneously, they cannot generate waveforms with different duty cycles.

3.4.11. I2S Interface

In the case of multiplexing, the module integrates two I2S interfaces. It supports master and slave modes with sample rates from 8 kHz to 384 kHz. The I2S interface supports both PCM mono channel mode and I2S stereo channel mode with programmable data width between 1 and 32 bits.

Table 18: Pin Description of I2S Interface

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
GPIO40	39	I2S1_SCK	DO	I2S1 serial clock	See ***Table 6*** for other GPIO pins multiplexed as I2S interface.
GPIO41	40	I2S1_SYNC	DIO	I2S1 frame synchronization	
GPIO42	41	I2S1_DIN	DI	I2S1 data in	
GPIO43	38	I2S1_DOUT	DO	I2S1 data out	
GPIO44	36	I2S2_SCK	DO	I2S2 serial clock	

GPIO45	34	I2S2_SYNC	DIO	I2S2 frame synchronization
GPIO46	33	I2S2_DIN	DI	I2S2 data in
GPIO47	49	I2S2_DOUT	DO	I2S2 data out
GPIO28	4	I2S_MCLK	DO	I2S master clock output

3.4.12. Analog Audio Interface

In the case of multiplexing, the module comes with a rich set of audio peripherals to enhance the listening experience, including a four-band digital equalizer, two analog-to-digital converters (ADC), one digital-to-analog converter (DAC), two microphone input amplifiers and a microphone bias, an audio amplifier, as well as an SBC decoder accelerator.

It contains two high-fidelity ADCs with sample rates of 8 kHz, 16 kHz, 44.1 kHz, or 48 kHz and also integrates one high-fidelity DAC with sample rates of 8 kHz, 16 kHz, 44.1 kHz, or 48 kHz.

The microphone signal can be amplified with gain from 0 to 32 dB with 2 dB/step. The module also provides a high-quality audio amplifier capable of driving 16 Ω speakers with up to 30 pF of load capacitance.

Table 19: Pin Description of Analog Audio Interfaces

Pin Name	Pin No.	I/O	Description
SPK_N	51	AO	Analog audio differential output (-)
SPK_P	52	AO	Analog audio differential output (+)
MIC1_P	53	AI	Microphone analog input1 (+)
MIC1_N	54	AI	Microphone analog input1 (-)
MIC2_N	55	AI	Microphone analog input2 (-)
MIC2_P	56	AI	Microphone analog input2 (+)
MIC_BIAS	57	AO	Bias voltage output for microphone

3.4.13. ADC Interfaces

The module embeds 12-bit general-purpose SAR ADC interfaces with programmable sampling rates

ranging from 12.5 kHz to 650 kHz. The ADC interfaces support up to 10 external input channels. It can operate in one-shot mode, software control mode and continuous mode. The ADC supports full scale input range (0 V to 2 × VREF).

Table 20: Pin Description of ADC Interfaces

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
GPIO25	61	ADC1	AI	General-purpose ADC interface	Channel 1
GPIO24	60	ADC2	AI	General-purpose ADC interface	Channel 2
GPIO23	27	ADC3	AI	General-purpose ADC interface	Channel 3
GPIO28	4	ADC4	AI	General-purpose ADC interface	Channel 4
GPIO22	28	ADC5	AI	General-purpose ADC interface	Channel 5
GPIO21	59	ADC6	AI	General-purpose ADC interface	Channel 6
UART1_TXD	47	ADC12	AI	General-purpose ADC interface	Channel 12
UART1_RXD	46	ADC13	AI	General-purpose ADC interface	Channel 13
GPIO12	5	ADC14	AI	General-purpose ADC interface	Channel 14
GPIO13	6	ADC15	AI	General-purpose ADC interface	Channel 15

Table 21: ADC Features

Parameter	Min.	Typ.	Max.	Unit
ADC Voltage Range	0	-	2.4	V
ADC Resolution	-	12	-	bit

3.4.14. Touch Sensor Interfaces

In the case of multiplexing, the module supports up to 16 capacitive-sensing touch sensor interfaces, which immediately detect capacitance changes induced by touch or proximity of objects.

Table 22: Pin Description of Touch Sensor Interfaces

Pin Name	Pin No.	Multiplexing Function	I/O	Description
GPIO12	5	TOUCH0	AI	Touch sensor 0
GPIO13	6	TOUCH1	AI	Touch sensor 1
GPIO28	4	TOUCH2	AI	Touch sensor 2
GPIO29	73	TOUCH3	AI	Touch sensor 3
GPIO30	72	TOUCH4	AI	Touch sensor 4
GPIO31	71	TOUCH5	AI	Touch sensor 5
GPIO32	70	TOUCH6	AI	Touch sensor 6
GPIO33	69	TOUCH7	AI	Touch sensor 7
GPIO34	68	TOUCH8	AI	Touch sensor 8
GPIO35	67	TOUCH9	AI	Touch sensor 9
GPIO36	66	TOUCH10	AI	Touch sensor 10
GPIO37	65	TOUCH11	AI	Touch sensor 11
GPIO38	64	TOUCH12	AI	Touch sensor 12
GPIO39	63	TOUCH13	AI	Touch sensor 13
GPIO46	33	TOUCH14	AI	Touch sensor 14
GPIO47	49	TOUCH15	AI	Touch sensor 15

3.4.15. Ethernet MAC Interface

In the case of multiplexing, the module provides a media access controller (MAC) for Ethernet LAN communications through a reduced medium-independent interface (RMII). The Ethernet MAC interface is compliant with the IEEE 802.3-2015 specification and can be used in applications such as network interface cards, and data center bridges and nodes. The module requires an external physical interface device (PHY) to connect to the physical LAN bus. The PHY is connected to the device RMII port using 9 signals, and can be clocked using the 25 MHz from the module or 25/50 MHz from an external crystal oscillator. The module supports 10 and 100 Mbps data transmission rates. Each signal of the RMII port has two GPIO choices.

Table 23: Pin Description of Ethernet MAC Interface

Pin Name	Pin No.	Multiplexing Function	I/O	Description
GPIO27	74	ENET_PHY_INT	DI	PHY interrupt
GPIO29	73	ENET_MDC	DO	Management data clock
GPIO32	70	ENET_MDIO	DIO	Management data input/output
GPIO33	69	ENET_RXD0	DI	Receive data 0
GPIO34	68	ENET_RXD1	DI	Receive data 1
GPIO35	67	ENET_RXDV	DI	Receive data valid
GPIO36	66	ENET_TXD0	DO	Transmit data 0
GPIO37	65	ENET_TXD1	DO	Transmit data 1
GPIO38	64	ENET_TXEN	DO	Transmit data enable
GPIO39	63	ENET_REF_CLK	DIO	Reference clock
GPIO46	33	ENET_PHY_INT	DI	PHY interrupt
GPIO47	49	ENET_MDC	DO	Management data clock
GPIO48	42	ENET_MDIO	DIO	Management data input/output
GPIO49	10	ENET_RXD0	DI	Receive data 0
GPIO50	11	ENET_RXD1	DI	Receive data 1
GPIO51	12	ENET_RXDV	DI	Receive data valid
GPIO52	43	ENET_TXD0	DO	Transmit data 0
GPIO53	48	ENET_TXD1	DO	Transmit data 1
GPIO54	45	ENET_TXEN	DO	Transmit data enable
GPIO55	37	ENET_REF_CLK	DIO	Reference clock

4 Operating Characteristics

4.1. Power Supply Interface

Power supply pin and ground pins of the module are defined in the following table.

Table 24: Pin Description of Power Supply and GND Pins

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT	2	PI	Power supply for the module	3.0	3.3	3.6	V
GND	1, 15, 23, 26, 50, 58, 75–83						

4.1.1. Reference Design for Power Supply

The module is powered by VBAT, and it is recommended to use a power supply chip that provides at least 0.5 A to ensure sufficient current. For better power supply performance, it is recommended to parallel a 22 μF decoupling capacitor, and two filter capacitors (1 μF and 100 nF) near the module's VBAT pin. And C4 is reserved for debugging and not mounted by default. In addition, it is recommended to add a TVS near the VBAT to improve the surge voltage bearing capacity of the module. In principle, the longer the VBAT trace is, the wider it should be.

VBAT reference circuit is shown below:

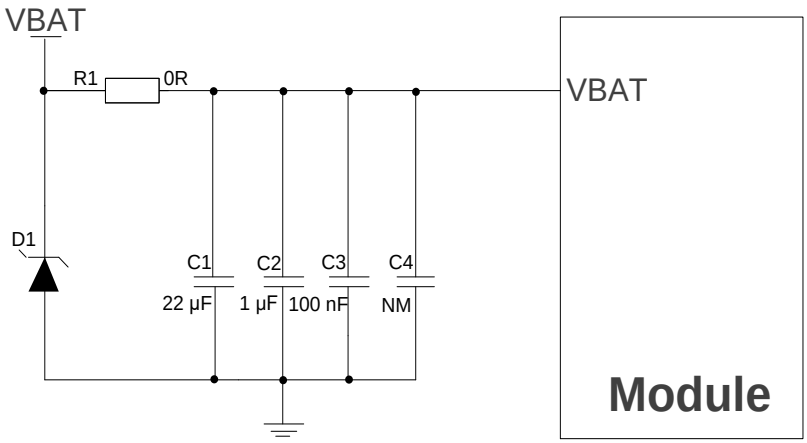


Figure 8: VBAT Reference Circuit

4.2. Turn-on

After the module VBAT is powered on, keep the CHIP_EN pin at high level to realize the automatic startup of the module.

Table 25: Pin Description of CHIP_EN

Pin Name	Pin No.	I/O	Description	Comment
CHIP_EN	3	DI	Module enable	Hardware enable. Internally pulled up to VBAT. Active high.

The turn-on timing is shown below:

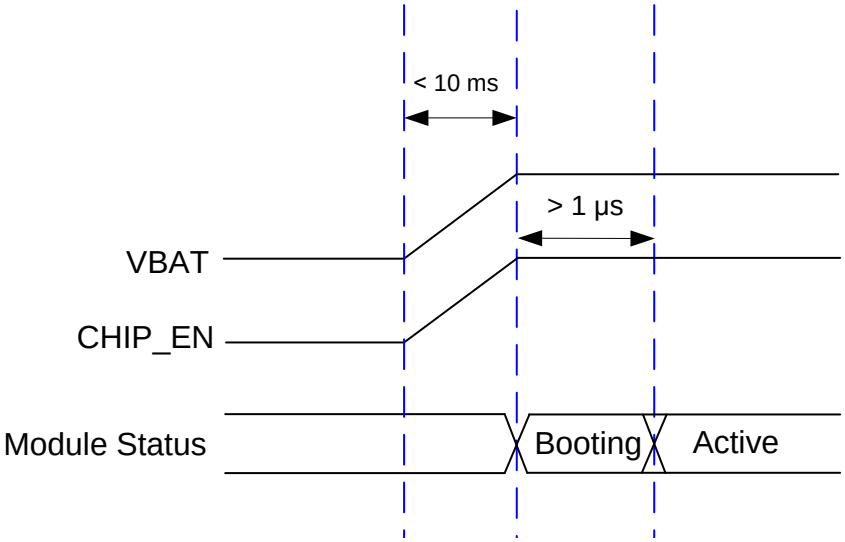


Figure 9: Turn-on Timing

4.3. Reset

When the voltage of CHIP_EN drops below 0.3 V or pull it down for at least 1 ms, the module can be reset. An open collector driving circuit is recommended to be used to control the CHIP_EN pin. The reference design for module reset is shown below.

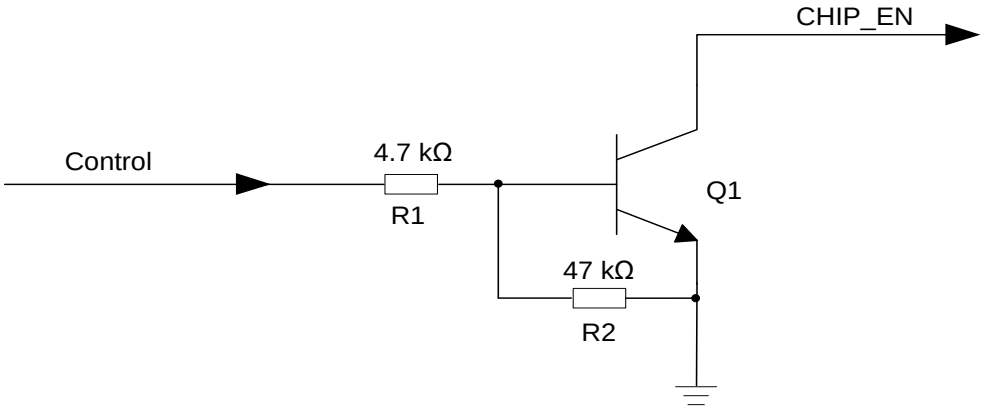


Figure 10: Reference Circuit of CHIP_EN by Using A Driving Circuit

Another way to control the CHIP_EN is by using a button directly. When pressing the button, an electrostatic strike may generate from finger. Therefore, a TVS component shall be placed near the button for ESD protection.

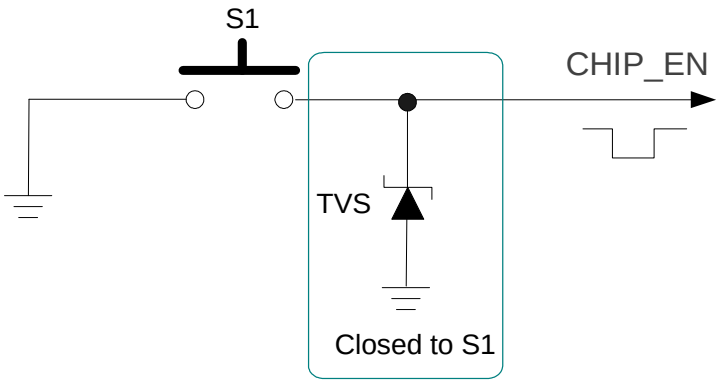


Figure 11: Reference Circuit of RESET with a Button

The module reset timing is illustrated in the following figure.

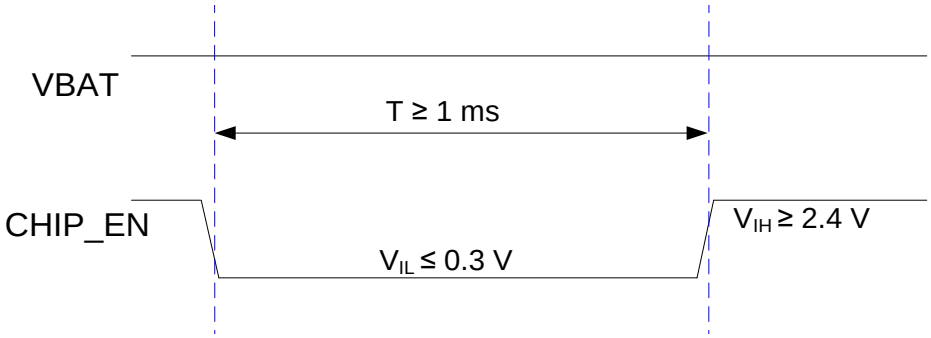


Figure 12: Reset Timing

5 RF Specifications

5.1. Wi-Fi Performances

Table 26: Wi-Fi Performances

Operating Frequency				
2.4 GHz: 2.400–2.4835 GHz				
Modulation				
DBPSK, DQPSK, CCK, BPSK, QPSK, 16QAM, 64QAM				
Encryption				
WPA/WPA2/WPA3-Personal				
Operating Mode				
● AP ● STA				
Transmission Data Rate				
● 802.11b: 1 Mbps, 2 Mbps, 5.5 Mbps, 11 Mbps ● 802.11g: 6 Mbps, 9 Mbps, 12 Mbps, 18 Mbps, 24 Mbps, 36 Mbps, 48 Mbps, 54 Mbps ● 802.11n: HT20 (MCS 0–7), HT40 (MCS 0–7) ● 802.11ax: HE20 (MCS 0–7), HE40 (MCS 0–7)				
Condition (VBAT = 3.3 V; Temp. 25 °C)		**EVM**	**Typ.; Unit: dBm; Tolerance: ±2 dB**	
			Transmitting Power	**Receiving Sensitivity**
2.4 GHz	802.11b @ 1 Mbps	≤ 35 %	17	TBD
	802.11b @ 11 Mbps		17	TBD
	802.11g @ 6 Mbps	≤ -5 dB	16	TBD
	802.11g @ 54 Mbps	≤ -25 dB	15	TBD

	802.11n, HT20 @ MCS 0, BPSK	≤ -5 dB	15	TBD
	802.11n, HT20 @ MCS 7, 64QAM	≤ -27 dB	14	TBD
	802.11n, HT40 @ MCS 0, BPSK	≤ -5 dB	15	TBD
	802.11n, HT40 @ MCS 7, 64QAM	≤ -27 dB	14	TBD
	802.11ax, HE20 @ MCS 0, BPSK	≤ -5 dB	14	TBD
	802.11ax, HE20 @ MCS 7, 64QAM	≤ -27 dB	13	TBD
	802.11ax, HE40 @ MCS 0, BPSK	≤ -5 dB	14	TBD
	802.11ax, HE40 @ MCS 7, 64QAM	≤ -27 dB	13	TBD

5.2. Bluetooth Performances

Table 27: Bluetooth Performances

Operating Frequency		
2.400–2.4835 GHz		
Modulation		
GFSK		
Operating Mode		
BLE		
Condition (VBAT = 3.3 V; Temp. 25 °C)	**Typ.; Unit: dBm; Tolerance: ±2 dB**	
	Transmitting Power	**Receiving Sensitivity**
BLE (1 Mbps)	7	TBD
BLE (2 Mbps)	7	TBD
BLE (125 kbps)	7	TBD
BLE (500 kbps)	7	TBD

5.3. Antenna

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The module is provided with one of the two antenna interface designs: RF coaxial connector and PCB antenna. The RF coaxial connector is not soldered on the module when the module is designed with PCB antenna. The impedance of antenna port is 50 Ω.

5.3.1. RF Coaxial Connector [5]

5.3.1.1. Antenna Connector Specifications

The mechanical dimensions of the receptacle supported by the module are as follows.

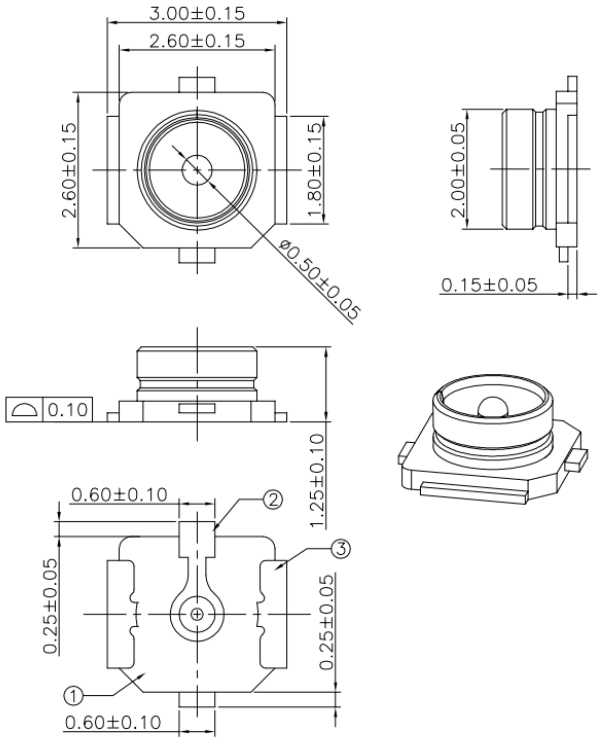


Figure 13: Dimensions of the Receptacle (Unit: mm)

[5] The module is provided with one of the two antenna interface designs. For more details, please contact Quectel Technical Support.

Table 28: Major Specifications of the RF Connector

Item	Specification
Nominal Frequency Range	DC to 6 GHz
Nominal Impedance	50 Ω
Temperature Rating	-40 °C to +85 °C
Voltage Standing Wave Ratio (VSWR)	Meet the requirements of: Max. 1.3 (DC–3 GHz) Max. 1.45 (3–6 GHz)

5.3.1.2. Antenna Connector Installation

The receptacle mounted on the module accepts two types of mated plugs that will meet a maximum height of 2.0 mm using a Ø 0.81 mm coaxial cable or a maximum height of 2.2 mm utilizing a Ø 1.13 mm coaxial cable.

The following figure shows the dimensions of mated plugs using Ø 0.81 mm coaxial cables.

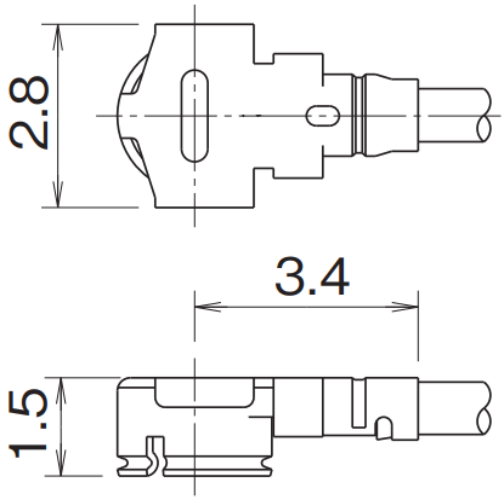


Figure 14: Dimensions of Mated Plugs (Ø 0.81 Coaxial Cables) (Unit: mm)

The following figure illustrates the connection between the receptacle on the module and the mated plug using a Ø 0.81 mm coaxial cable.

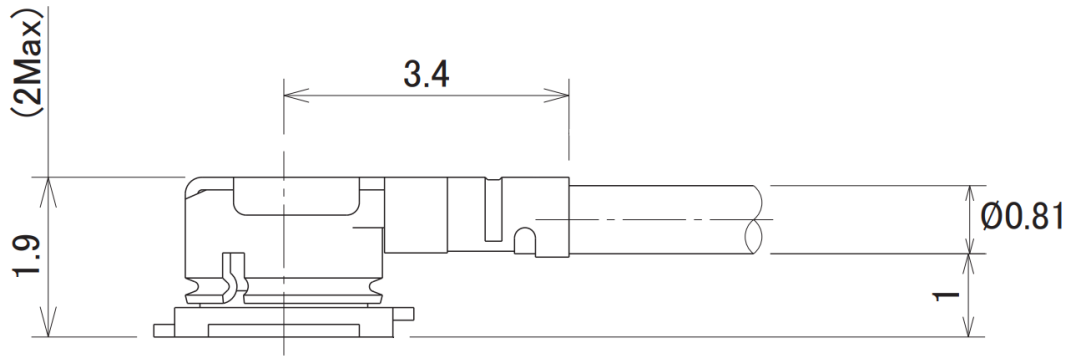


Figure 15: Space Factor of Mated Connectors (Ø 0.81 mm Coaxial Cables) (Unit: mm)

The following figure illustrates the connection between the receptacle mounted on the module and the mated plug using a Ø 1.13 mm coaxial cable.

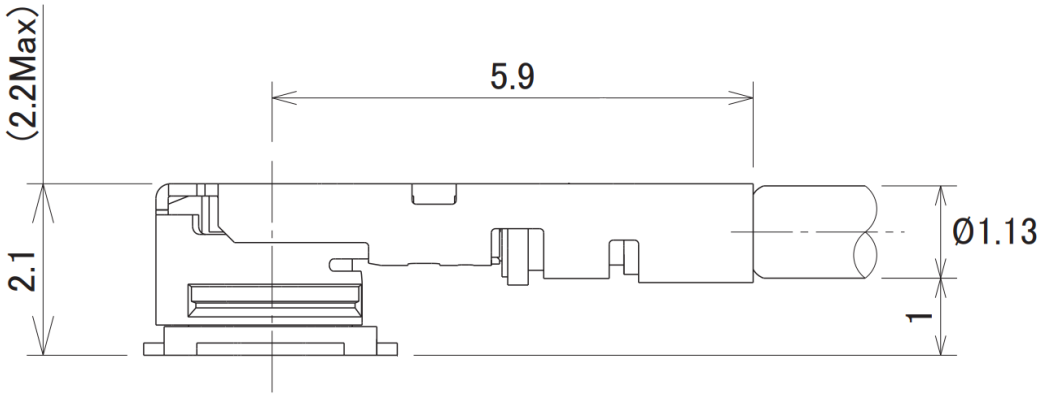


Figure 16: Space Factor of Mated Connectors (Ø 1.13 mm Coaxial Cables) (Unit: mm)

5.3.1.3. Recommended Manufacturers of RF Connector and Cable

RF connectors and cables by I-PEX are recommended. For more details, visit https://www.i-pex.com.

5.3.2. PCB Antenna

Table 29: PCB Antenna Specifications

Parameter	Requirement
Frequency Range (GHz)	2.4 GHz: 2.400–2.500

Input Impedance (Ω)	50
VSWR	≤ 3 (Typ.)
Gain (dBi)	2.4
Efficiency	53 %

The performance of the PCB antenna depends on the entire product, including the motherboard, case, other RF signals, etc., and it is recommended to verify it at the early stage of design. To ensure the performance and reliability when designed with PCB antenna, follow the basic principles below for module's placement and layout:

- The module should be placed on the edge of the motherboard.
- On the motherboard, all PCB layers under the PCB antenna and within at least 10 mm to the left and right should be designed as keepout areas.
- On the motherboard, ensure a minimum clearance of 16 mm between the PCB antenna and power connectors, Ethernet ports, USB ports, and other large form-factor components (if any).
- If using a plastic case, ensure a minimum clearance of 10 mm between the PCB antenna and the plastic case. If using a metal case, it is recommended to use an external antenna.

NOTE

If any of the above principles cannot be guaranteed, it is advisable to explore alternative antenna solutions for the module or seek assistance from the Quectel Antenna Team, who can offer design assistance and recommend suitable external antennas. Please feel free to contact Quectel Technical Support if necessary.

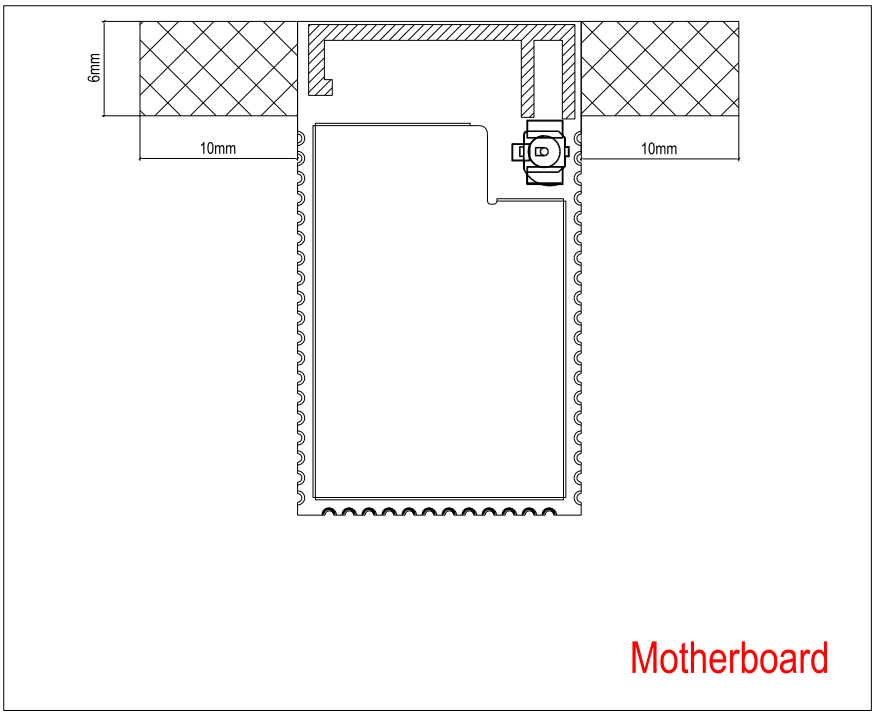


Figure 17: Keepout Area on Motherboard

To ensure module performance, do not route at the RF test point at the bottom of the module during PCB design. The prohibited area during routing is shown in the red box below:

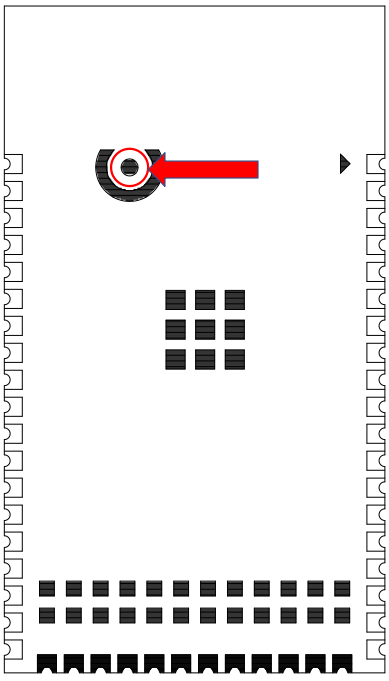


Figure 18: Prohibited Area for Routing

5.3.3. Requirements for Antenna Design

Table 30: Requirements Antenna Design

Parameter	Requirement
Frequency Range (GHz)	2.4 GHz: 2.400–2.4835
RF Coaxial Connector	Cable Insertion Loss (dB): < 1
	VSWR: ≤ 2 (Typ.)
	Gain (dBi): 1 (Typ.)
	Max. input power (W): 50
	Input impedance (Ω): 50
	Polarization type: Vertical

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on partial pins of the module are listed in the following table.

Table 31: Absolute Maximum Ratings (Unit: V)

Parameter	Min.	Max.
VBAT	-0.3	3.6
Voltage at Digital Pins	-0.3	3.6
Voltage at ADC[1:6], ADC[10:11]	0	VREF × 2

6.2. Power Supply Ratings

Table 32: Module Power Supply Ratings (Unit: V)

Parameter	Description	Condition	Min.	Typ.	Max.
VBAT	Power supply for the module	The actual input voltages must be kept between the minimum and maximum values.	3.0	3.3	3.6

6.3. Power Consumption

6.3.1. Wi-Fi Power Consumption [6]

Table 33: Power Consumption in Non-signaling Mode (Unit: mA)

Condition			I_{VBAT} (AVG)
2.4 GHz	802.11b	Tx 1 Mbps @ 17 dBm	TBD
		Tx 11 Mbps @ 17 dBm	TBD
	802.11g	Tx 6 Mbps @ 16 dBm	TBD
		Tx 54 Mbps @ 15 dBm	TBD
	802.11n	Tx HT20 MCS 0 @ 15 dBm	TBD
		Tx HT20 MCS 7 @ 14 dBm	TBD
	802.11n	Tx HT40 MCS 0 @ 15 dBm	TBD
		Tx HT40 MCS 7 @ 14 dBm	TBD
	802.11ax	Tx HE20 MCS 0 @ 14 dBm	TBD
		Tx HE20 MCS 7 @ 13 dBm	TBD
	802.11ax	Tx HE40 MCS 0 @ 14 dBm	TBD
		Tx HE40 MCS 7 @ 13 dBm	TBD

NOTE

1. Test conditions: ambient temperature 25 °C, and typical power domain.
2. The above power consumption data is the typical value for your reference only. Actual values may vary among different modules due to differences in internal components, software versions and test ambient temperatures. For more details, please contact Quectel Technical Support.

[6] The Bluetooth function is disabled when the Wi-Fi power consumption is tested.

6.3.2. Bluetooth Power Consumption [7]

Table 34: Power Consumption in Non-signaling Mode (Typ.; Unit: mA)

Condition	I_{VBAT}
BLE (1 Mbps) @ 10 dBm	TBD
BLE (2 Mbps) @ 10 dBm	TBD
BLE (125 kbps) @ 10 dBm	TBD
BLE (500 kbps) @ 10 dBm	TBD

NOTE

1. Test conditions: ambient temperature 25 °C, and typical power domain.
2. The above power consumption data is the typical value for your reference only. Actual values may vary among different modules due to differences in internal components, software versions and test ambient temperatures. For more details, please contact Quectel Technical Support.

6.4. Digital I/O Characteristics

Table 35: VBAT I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	0.7 × VBAT	VBAT + 0.3
V_{IL}	Low-level input voltage	-0.3	0.3 × VBAT
V_{OH}	High-level output voltage	0.9 × VBAT	-
V_{OL}	Low-level output voltage	-	0.1 × VBAT

[7] The Wi-Fi function is disabled when the Bluetooth power consumption is tested.

6.5. ESD Protection

Static electricity occurs naturally and may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 36: ESD Characteristics (Unit: kV)

Model	Test Result	Standard
Human Body Model (HBM)	±3	*ANSI/ESDA/JEDEC JS-001-2017*
Charged Device Model (CDM)	±0.5	*ANSI/ESDA/JEDEC JS-002-2018*

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeters (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

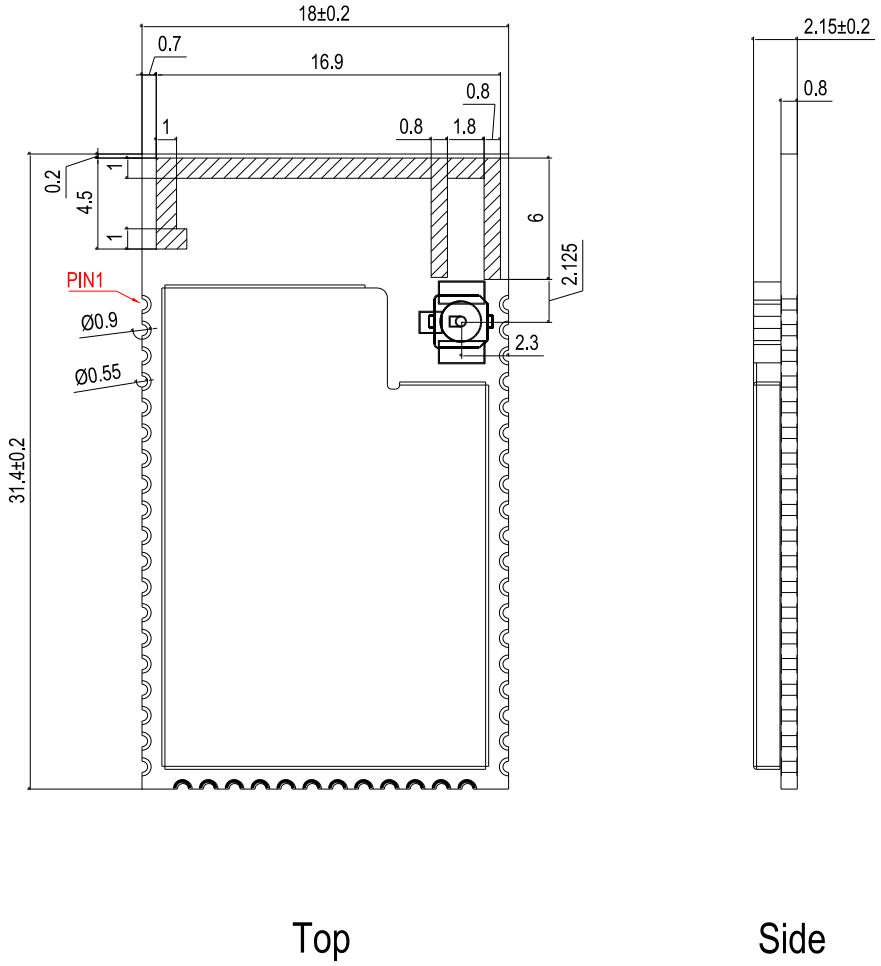


Figure 19: Top and Side Dimensions

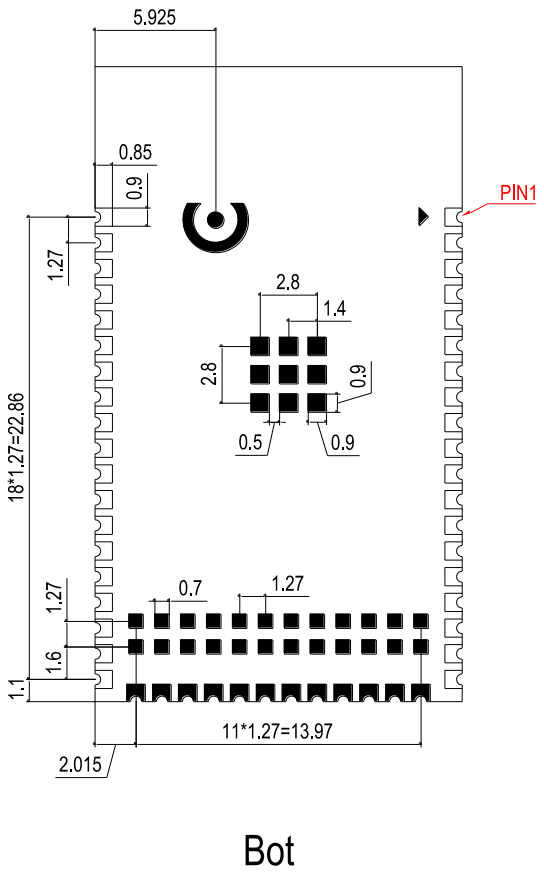


Figure 20: Bottom Dimensions (Bottom View)

NOTE

The module's coplanarity standard: ≤ 0.13 mm.

7.2. Recommended Footprint

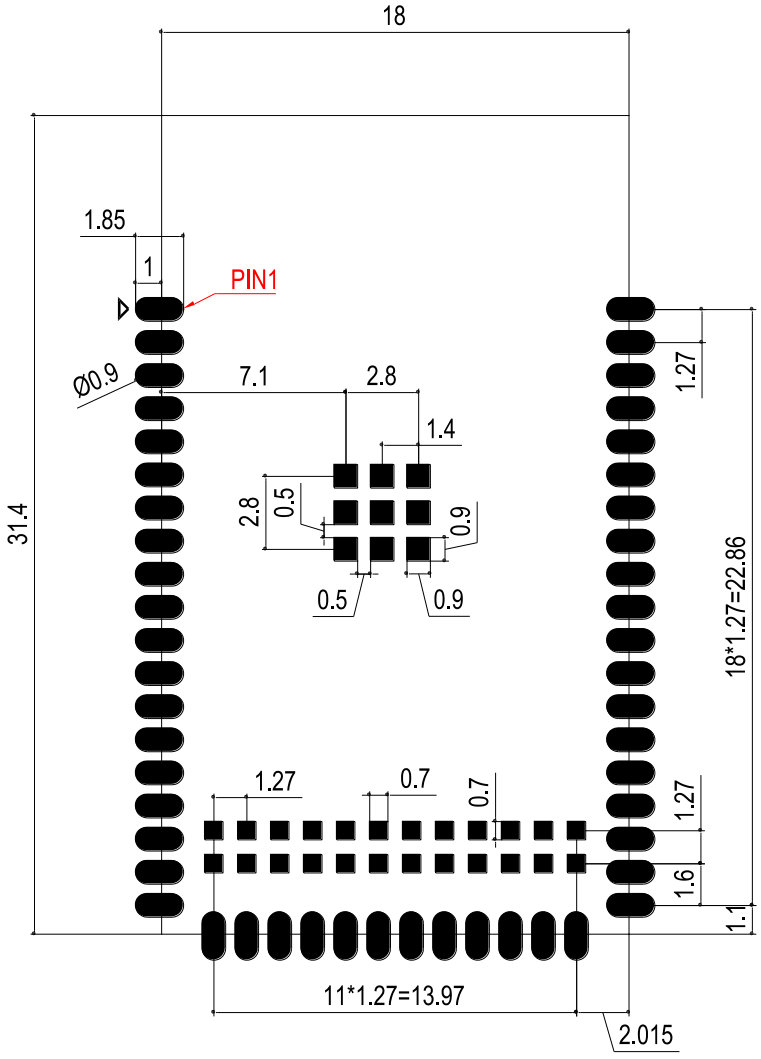


Figure 21: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

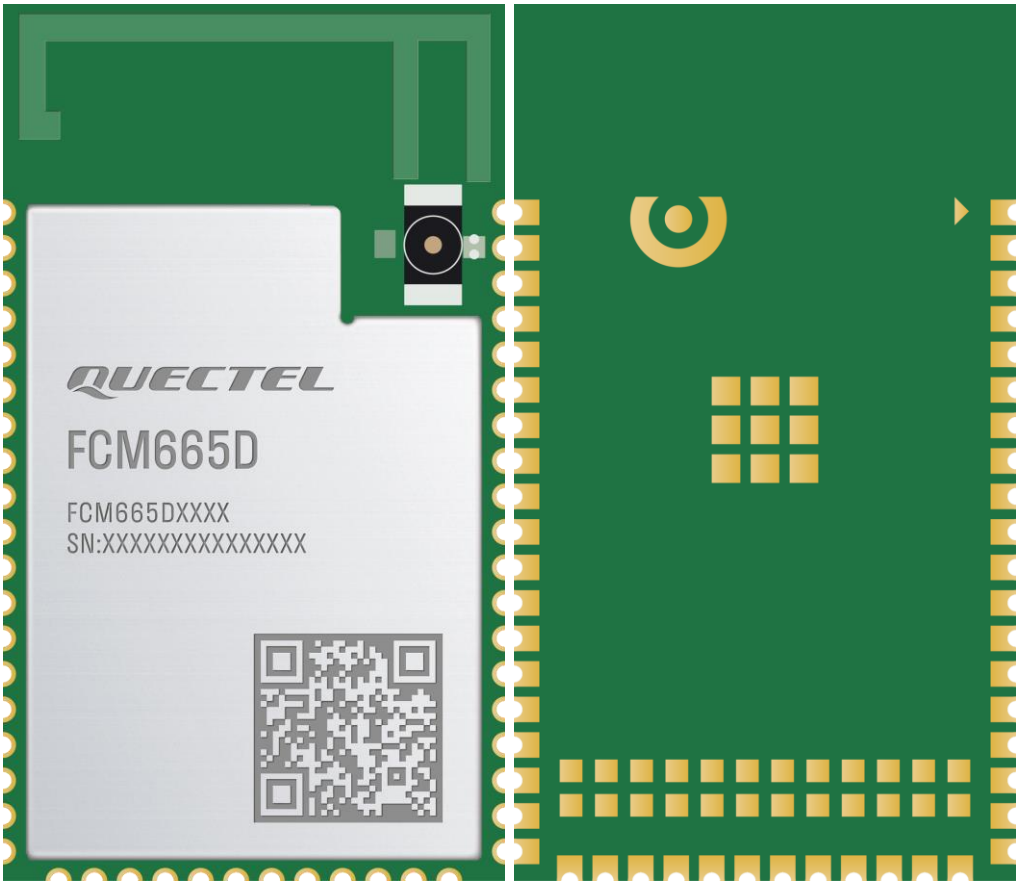


Figure 22: Top and Bottom Views (RF Coaxial Connector)

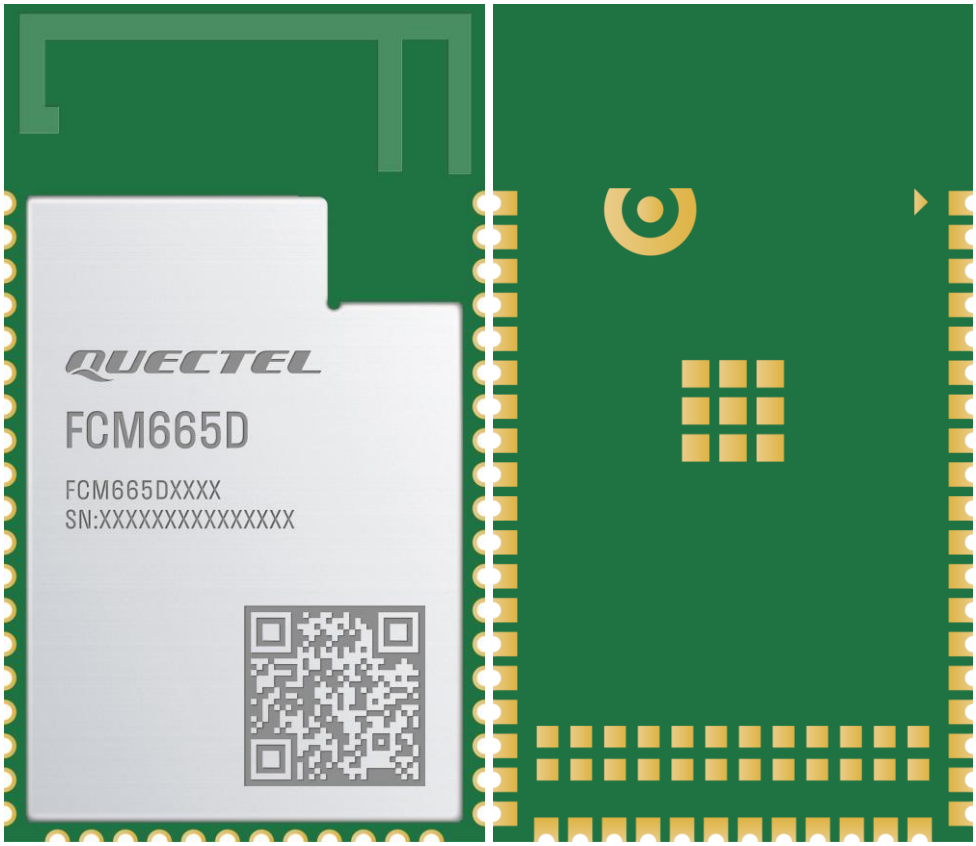


Figure 23: Top and Bottom Views (PCB Antenna)

NOTE

1. Images above are for illustrative purposes only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.
2. The RF coaxial connector is not soldered on the module when using PCB antenna interface.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [8] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[8] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see ***document [3]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

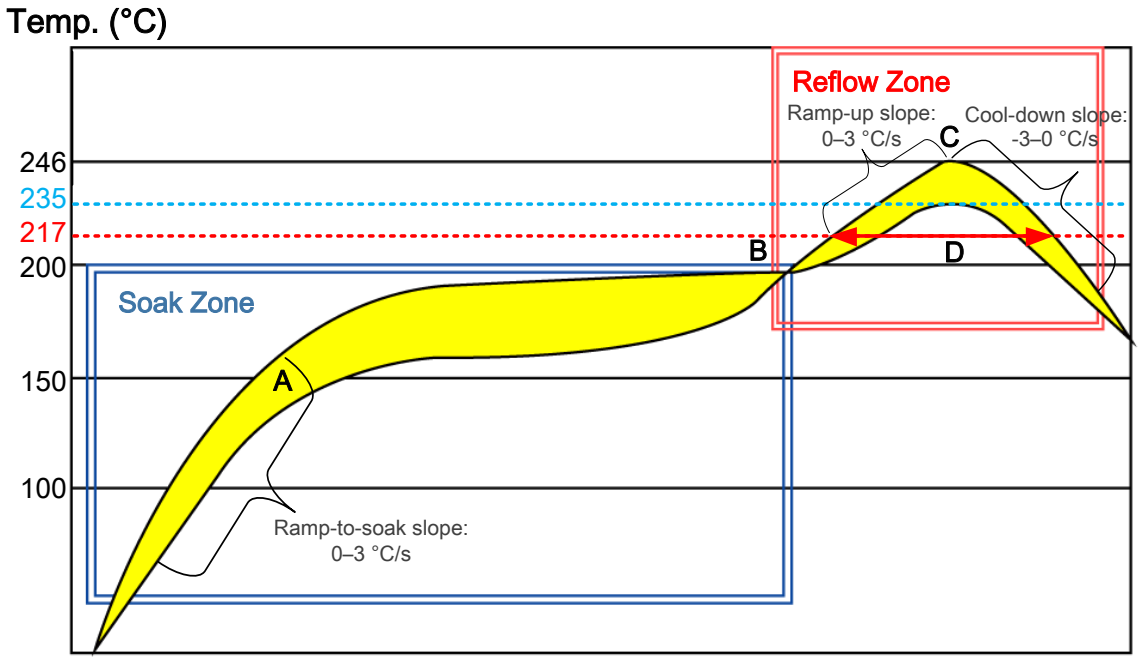


Figure 24: Recommended Reflow Soldering Thermal Profile

Table 37: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max. temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max. reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
8. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic

soldering) that is not mentioned in ***document [4]***.

8.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

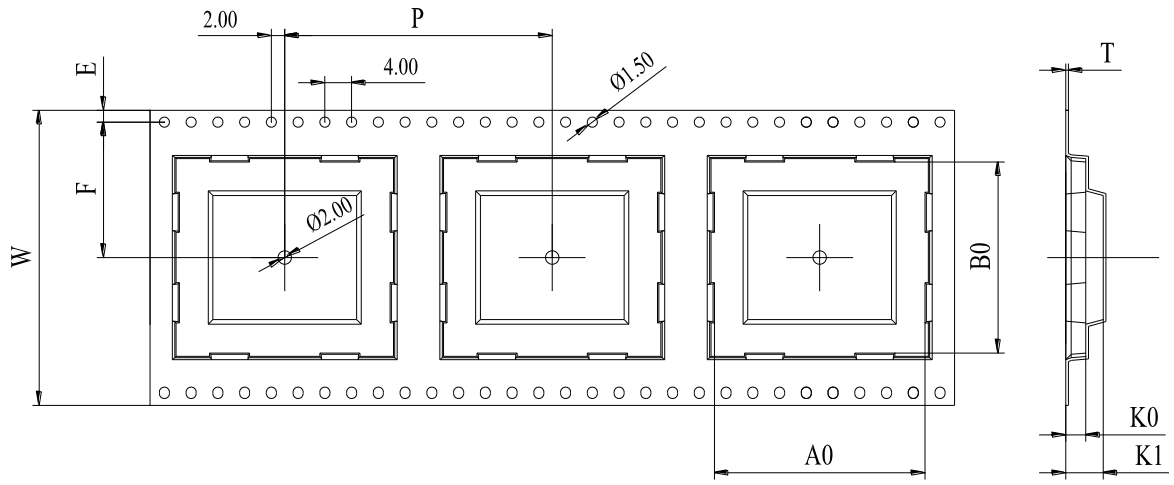


Figure 25: Carrier Tape Dimension Drawing (Unit: mm)

Table 38: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
56	24	0.4	18.5	31.9	2.65	3.15	26.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

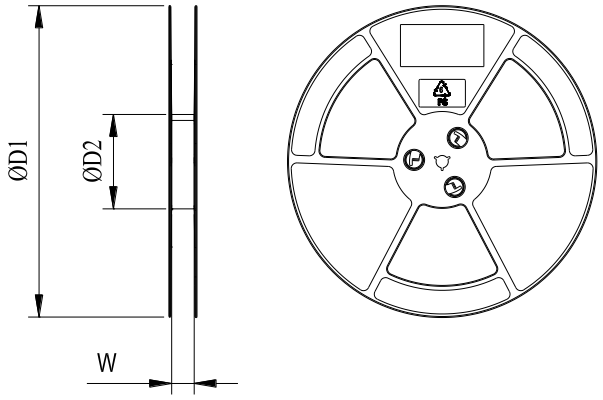


Figure 26: Plastic Reel Dimension Drawing

Table 39: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
380	100	56.5

8.3.3. Mounting Direction

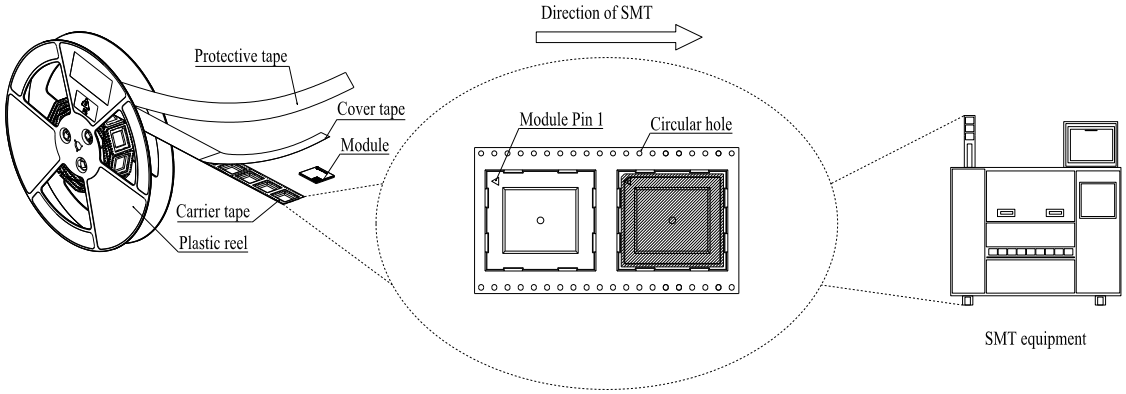
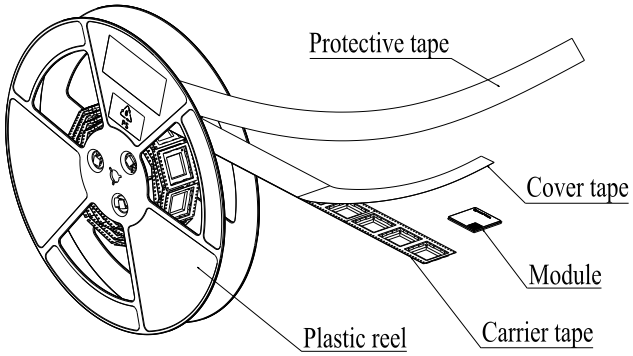


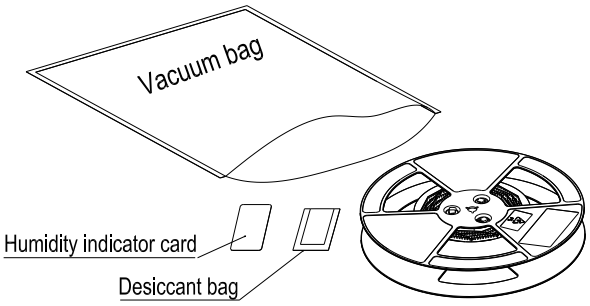
Figure 27: Mounting Direction

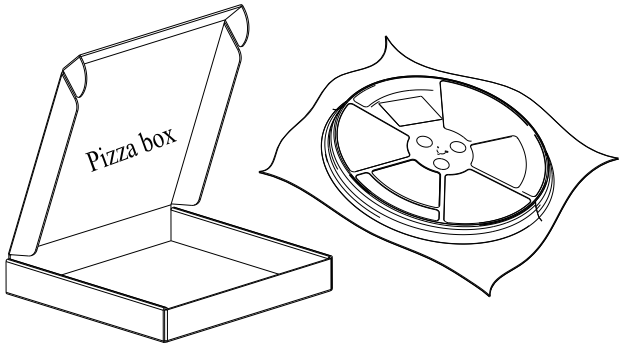
8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 1000 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 4000 modules.

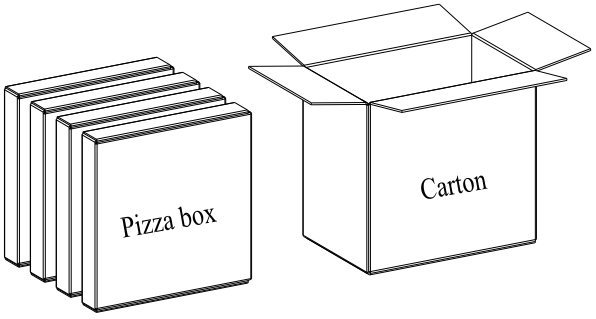


Figure 28: Packaging Process

9 Appendix References

Table 40: Reference Documents

Document Name
[1] Quectel_MCU_WIFI_EVB_User_Guide
[2] Quectel_RF_Layout_Application_Note
[3] Quectel_Module_Stencil_Design_Requirements
[4] Quectel_Module_SMT_Application_Note
[5] Quectel_FCM665D_QuecOpen(SDK)_Peripheral_Interface_Development_Guide

Table 41: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMOLED	Active Matrix/Organic Light Emitting Diode
AP	Access Point
BLE	Bluetooth Low Energy
BPSK	Binary Phase Shift Keying
CAN	Controller Area Network
CAN-FD	Controller Area Network with Flexible Data-Rate
CCK	Complementary Code Keying
CDM	Charged Device Model
CIS	CMOS image sensor
CMOS	Complementary Metal Oxide Semiconductor

CS	Chip Select
CTS	Clear To Send
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
DVP	Digital Video Port
EMAC	Ethernet Media Access Controller
ESD	Electrostatic Discharge
EVM	Error Vector Magnitude
FIFO	First Input First Output
GFSK	Gauss frequency Shift Keying
GND	Ground
GPIO	General-Purpose Input/Output
HE	High Efficiency
HSYNC	Horizontal Synchronization
HT	High Throughput
I/O	Input/Output
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IEEE	Institute of Electrical and Electronics Engineers
JPEG	Joint Photographic Experts Group
kbps	Kilobits Per Second
LCC	Leadless Chip Carrier (package)
TFT-LCD	Thin-film Transistor Liquid-crystal Display
LCM	Liquid Crystal Module
LGA	Land Grid Array
Mbps	Million Bits Per Second
MCLK	Master Clock

MCU	Microcontroller Unit
MISO	Master In Slave Out
MOSI	Master Out Slave In
OTA	Over-the-Air
PCB	Printed Circuit Board
PCLK	Pixel Clock
PSRAM	Pseudo Static Random-Access Memory
PWM	Pulse Width Modulation
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QSPI	Quad Serial Peripheral Interface
RF	Radio Frequency
RISC	Reduced Instruction-Set Computer
RoHS	Restriction of Hazardous Substances
ROM	Read Only Memory
RTC	Real-Time Clock
RTS	Request to Send
Rx	Receive
SAR	Successive Approximation Register
SBC	Sub-band Coding
SCLK	Serial Clock
SD	Secure Digital
SDIO	Secure Digital Input/Output
SMD	Surface Mount Device
SMT	Surface Mount Technology
SPI	Serial Peripheral Interface
SRAM	Static Random-Access Memory

STA	Station
TVS	Transient Voltage Suppressor
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
V_{IH}	High-level Input Voltage
V_{IL}	Low-level Input Voltage
Vmax	Maximum Voltage
Vmin	Minimum Voltage
Vnom	Nominal Voltage Value
V_{OH}	High-level Output Voltage
V_{OL}	Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
VSYNC	Vertical Synchronization
Wi-Fi	Wireless Fidelity
WPA	Wi-Fi Protected Access

FCC Statement

Warning: Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.

However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one

or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

The device must not be co-located or operating in conjunction with any other antenna or transmitter. This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions : (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Radiation Exposure Statement

This equipment should be installed and operated with minimum distance 20cm between the radiator and your body.

Does not comply with the use restrictions of the product:

Portable devices used close with human’s body (within 20cm), Like Cell phone, Notebook etc.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01

2.2 List of applicable FCC rules

FCC Part 15 Subpart C 15.247 & 15.209.

2.3 Specific operational use conditions

The module can be used for mobile applications with a maximum 2.4dBi antenna. The host manufacturer installing this module into their product must ensure that the final compos it product complies with the FCC requirements by a technical assessment or evaluation to the FCC rules, including the transmitter operation. The host manufacturer has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module The end user manual shall include all required regulatory information/warning as show in this manual.

2.4 Limited module procedures

Not applicable The module is a Single module and complies with the requirement of FCC Part 15 212.

2.5 Trace antenna designs

Not applicable The module has its own antenna, and doesn’t need a hosts printed board micro strip trace antenna etc.

2.6 RF exposure considerations

The module must be installed in the host equipment such that at least 20cm is maintained between the antenna and users" body; and if RF exposure statement or module layout is changed, then the host product manufacturer required to take responsibility of the module through a change in FCC ID or new application The FCC ID of the module cannot be used on the final product In these circumstances, the host manufacturer will be responsible for reevaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

2.7 Antennas

Antenna Specification are as follows:

Type: PCB Antenna

Gain: 2.4G: 2.4dBi max

This device is intended only for host manufacturers under the following conditions: The transmitter module may not be co-located with any other transmitter or antenna; The module shall be only used with the internal antenna(s) that has been originally tested and certified with this module. The antenna must be either permanently attached or employ a “unique" antenna coupler.

As long as the conditions above are met, further transmitter test will not be required However, the host manufacturer is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc).

2.8 Label and compliance information

Host product manufacturers need to provide a physical or e-label stating "Contains FCC ID: XMR2025FCM665D" with their finished product.

2.9 Information on test modes and additional testing requirements

Host manufacturer must perform test of radiated & conducted emission and spurious emission, e.t.c according to the actual test modes for a stand-alone modular transmitter in a host, as well as for multiple simultaneously transmitting modules or other transmitters in a host product. Only when all the test results of test modes comply with FCC requirements, then the end product can be sold legally.

2.10 Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only FCC authorized for FCC Part 15 Subpart C 15.247 & 15 209 and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

Federal Communication Commission Statement (FCC, U S)

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules These limits are designed to provide reasonable protection against harmful interference in a residential installation This equipment generates, uses and can

radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications However, there is no guarantee that interference will not occur in a particular installation If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

This device complies with Part 15 of the FCC Rules Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Caution:

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

IMPORTANT NOTES

Co-location warning:

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

OEM integration instructions:

This device is intended only for OEM integrators under the following conditions:

The transmitter module may not be co-located with any other transmitter or antenna The module shall be only used with the external antenna(s) that has been originally tested and certified with this module.

As long as the conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

Validity of using the module certification:

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization for this module in combination with the host equipment is no longer considered valid and the FCC ID of the module cannot be used on the final product In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End product labeling:

The final end product must be labeled in a visible area with the following: "Contains Transmitter Module **FCC ID: XMR2025FCM665D**"

Information that must be placed in the end user manual:

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module The end user manual shall include all required regulatory information/warning as show in this manual.

IC: 10224A-2025FCM665D

This device complies with ISED license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d' ISED applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :(1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

The device is compliance with RF field strength limits, users can obtain Canadian information on RF exposure and compliance.

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

Déclaration d' exposition aux radiations:

Cet équipement est conforme aux limites d' exposition aux rayonnements IC établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains IC: 10224A-2025FCM665D".

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 10224A-2025FCM665D ".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module. Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.