EC200A-xxV1 Series

Hardware Design

LTE Standard Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2024-06-05	Thor LEI/ Elvish HUANG/ Yule DENG	Creation of the document
1.0	2024-06-20	Julian TANG/ Elvish HUANG/ Yule DENG	First official release
1.1.0	2025-01-09	Julian TANG/ Leon LIANG/ Yule DENG	1. Added the applicable module EC200A-EL and related information. 2. Updated the module coplanarity requirement (Chapter 7.1). 3. Updated the pre-baking time to 24 h (Chapter 8.1).

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1 Introduction

This document defines the EC200A-xxV1 series (consisting of EC200A-CNV1, EC200A-EUV1, EC200A-ELV1 and EC200A-AUV1) module and describes its air interfaces and hardware interfaces which are connected with your applications.

It can help you quickly understand interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, you can use this module to design and to set up mobile applications easily.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

EC200A-xxV1 series is an LTE/WCDMA/GSM wireless communication module with receiving diversity, which provides data connectivity on LTE-FDD, LTE-TDD, HSDPA, HSUPA, HSPA+, WCDMA, EDGE and GPRS network data connection. You can choose a dedicated type based on the region or operator. The following table shows the frequency bands of the module.

Table 2: Brief Introduction of the Module

Categories	
Packaging and pins number	80 LCC pins; 64 LGA pins
Dimensions	(29.0 ±0.15) mm × (32.0 ±0.15) mm × (2.4 ±0.2) mm
Weight	Approx. 4.2 g
Wireless network functions	LTE/WCDMA/GSM
Variants	EC200A-CNV1, EC200A-EUV1, EC200A-ELV1, EC200A-AUV1

2.1. Frequency Bands and Functions

Table 3: Wireless Network Types

Wireless Network Types	EC200A-CNV1	EC200A-EUV1	EC200A-ELV1	EC200A-AUV1
LTE-FDD	B1/B3/B5/B8	B1/B3/B5/B7/B8/B20/B28	B1/B3/B5/B7/B8/B20/B28	B1/B2/B3/B4/B5/B7/B8/B28/B66
LTE-TDD	B34/B38/B39/B40/B41	B38/B40/B41	B38/B40/B41	B40
WCDMA	B1/B5/B8	B1/B5/B8	B1/B5/B8	B1/B2/B4/B5/B8

GSM [1]	B3/B8	B3/B8	-	B2/B3/B5/B8

NOTE

LTE-TDD B41 only supports 140 MHz (2535–2675 MHz).
B40 is not used for FCC&IC.

2.2. Key Features

Table 4: Key Features

Category	Description
Power Supply	● Supply voltage: 3.4–4.3 V ● Typical supply voltage: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: module by default ● Only supports SGS SNS
USB Interface	● Compliant with USB 2.0 specification (only serves as slave device); the data transmission rate can reach up to 480 Mbps ● Used for AT command communication, data transmission, software debugging and firmware upgrade ● Supports USB serial driver for Windows 8.1/10/11, Linux 2.6–6.7 and Android 4.x–13.x systems
(U)SIM Interface	Supports (U)SIM card: 1.8/3.0 V
I2C Interface*	● Supports one I2C interface ● Complies with *The I2C-bus Specification* (100/400 kHz)
SPI*	● Supports one SPI ● Maximum clock frequency: 52 MHz ● Supports master mode only
UART	**Main UART:** ● Used for AT command communication and data transmission ● Baud rate: 115200 bps by default, Max. 921600 bps ● Supports RTS and CTS hardware flow control

[1] For EC200A-CNV1, GSM is optional.

	Debug UART: ● Used for the output of partial logs ● Baud rate: 115200 bps
SDIO Interface	● SD card application interface: supports SD 3.0 protocol ● WLAN application interface*: supports SDIO interface for WLAN function
ADC Interfaces*	● Supports two ADC interfaces ● Voltage range: 0 V–VBAT_BB
Network Indication	● NET_MODE indicates the module's network registration mode ● NET_STATUS indicates network connectivity status
AT Commands	● Compliant with *3GPP TS 27.007*, *3GPP TS 27.005* ● Compliant with Quectel enhanced AT commands
Rx-diversity	Supports LTE Rx-diversity
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● Rx-diversity antenna interface (ANT_DRX) ● 50 Ω characteristic impedance
Transmitting Power	● GSM850/EGSM900: Class 4 (33 dBm ±2 dB) ● DCS1800/PCS1900: Class 1 (30 dBm ±2 dB) ● GSM850/EGSM900 (8-PSK): Class E2 (27 dBm ±3 dB) ● DCS1800/PCS1900 (8-PSK): Class E2 (26 dBm ±3 dB) ● WCDMA: Class 3 (23 dBm ±2 dB) ● LTE-FDD: Class 3 (23 dBm ±2 dB) ● LTE-TDD: Class 3 (23 dBm ±2 dB)
LTE Features	● Supports 3GPP Rel-9 non-CA Cat 4 FDD and TDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Supports MIMO in DL direction ● Supports UL QPSK and 16QAM modulations ● Supports DL QPSK, 16QAM and 64QAM modulations ● Maximum transmission data rates: – LTE-FDD: Max. 150 Mbps (DL)/50 Mbps (UL) – LTE-TDD: Max. 130 Mbps (DL)/30 Mbps (UL)
UMTS Features	● Supports 3GPP Rel-7 HSPA+/HSDPA/HSUPA and WCDMA ● Supports QPSK, 16QAM and 64QAM modulations ● HSPA+: Max. 21 Mbps (DL) ● HSUPA: Max. 5.76 Mbps (UL) ● WCDMA: Max. 384 kbps (DL)/384 kbps (UL)
GSM Features [2]	**GPRS:** ● Supports GPRS multi-slot class 12 ● Coding scheme: CS 1–4 ● Max. 85.6 kbps (DL)/85.6 kbps (UL) **EDGE:**

[2] For EC200A-CNV1, GSM is optional.

	● Supports EDGE multi-slot class 12 ● Modulation: GMSK and 8–PSK ● Downlink coding schemes: MCS 1–9 ● Uplink coding schemes: MCS 1–9 ● Max. 236.8 kbps (DL)/236.8 kbps (UL)
Internet Protocol Features	● Supports TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/ HTTPS/FTPS/SSL/FILE/MQTT/MMS*/SMTP*/SMTPS* protocols ● Supports PAP and CHAP for PPP connection
Temperature Range	● Operating temperature range [3]: -35 to +75 °C ● Extended temperature range [4]: -40 to +85 °C ● Storage temperature range: -40 to +90 °C
Firmware Upgrade	USB interface or DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

[3] Within this range, the module's indicators comply with 3GPP specification requirements.
[4] Within this range, the module retains the ability to establish and maintain functions such as SMS* and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

2.3. Pin Assignment

The following figure illustrates the pin assignment of the module.

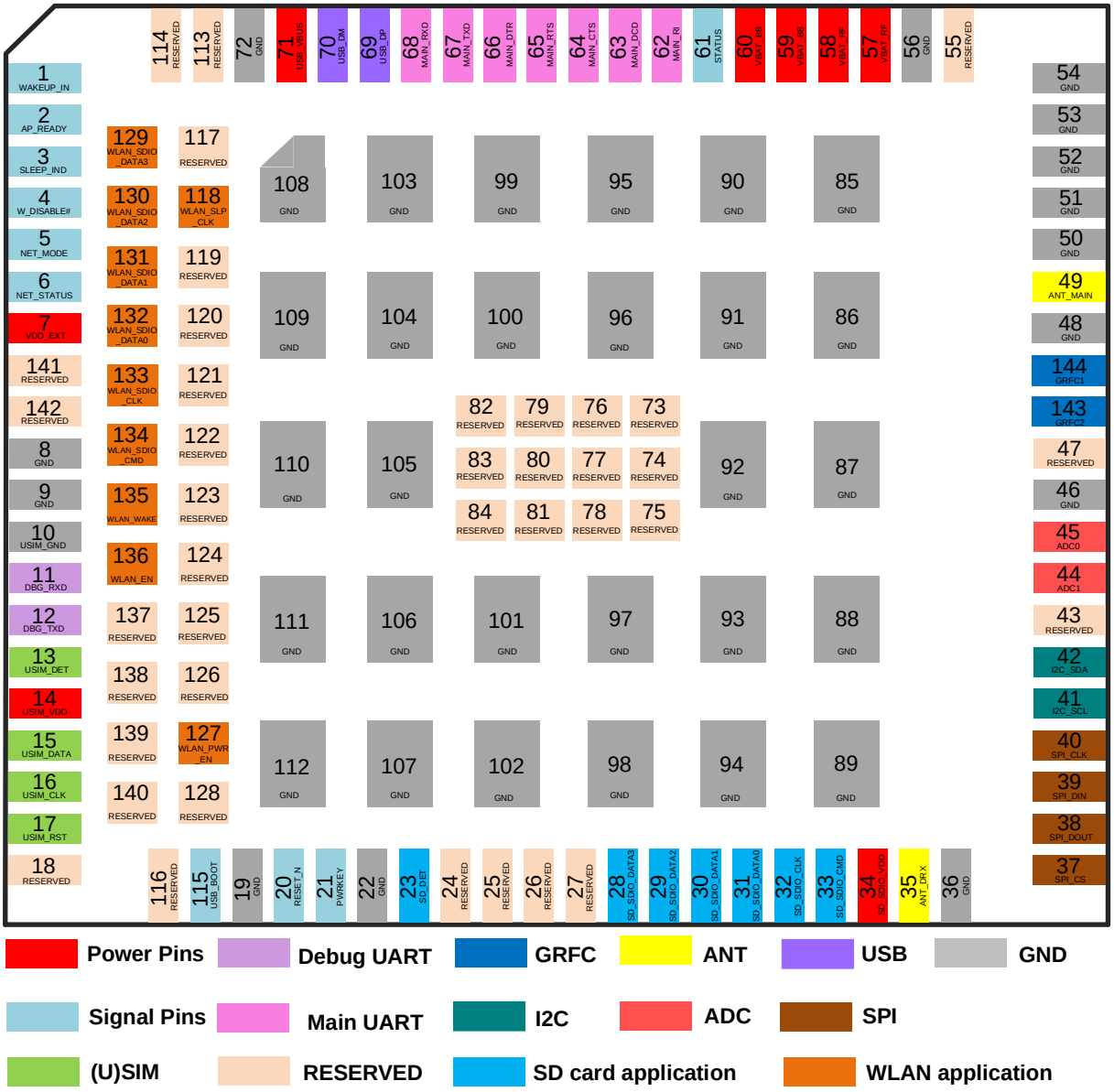


Figure 1: Pin Assignment (Top View)

NOTE

Ensure that the pull-up power supply of the module's pins is VDD_EXT or controlled by VDD_EXT, and there is no current sink on the module's pins before the module turns on. For more details, contact Quectel Technical Support.

2.4. Pin Definitions

Table 5: Parameter Definition

Parameter	Description
AI	Analog Input
AIO	Analog Input/Output
AO	Analog Output
DI	Digital Input
DIO	Digital Input/Output
DO	Digital Output
OD	Open Drain
PI	Power Input
PO	Power Output
PD	Pull-down
PU	Pull-up
H	High Level
L	Low Level

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply						
Pin Name	**Pin No.**	**I/O**	**Status after Reset**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	59, 60	PI	-	Power supply for the module's BB part	Vmax = 4.3 V Vmin = 3.4 V Vnom = 3.8 V	It must be provided with sufficient current of at least 0.8 A. A test point is

						recommended to be reserved.
VBAT_RF	57, 58	PI	-	Power supply for the module's RF part		It must be provided with sufficient current of at least 2.0 A. A test point is recommended to be reserved.
VDD_EXT	7	PO	-	Provide 1.8 V for external circuits	Vnom = 1.8 V $I_O$max = 50 mA	It can provide a pull-up power to the external GPIO. A test point is recommended to be reserved.
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 85–112					
Turn on/off						
Pin Name	**Pin No.**	**I/O**	**Status after Reset**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	21	DI	-	Turn on/off the module	V_{IL}max = 0.5 V	VBAT power domain. Active low. A test point is recommended to be reserved.
RESET_N	20	DI	-	Reset the module		1.8 V power domain. Active low after turn-on. A test point is recommended to be reserved if unused.
Indication Interfaces						
Pin Name	**Pin No.**	**I/O**	**Status after Reset**	**Description**	**DC Characteristics**	**Comment**
STATUS	61	OD	L	Indicate the module's operation status	VDD_EXT	If unused, keep them open.

NET_STATUS	6	DO	L	Indicate the module's network activity status		
NET_MODE	5	DO	PD	Indicate the module's network registration mode		
SLEEP_IND	3	DO	PD	Indicate the module's sleep mode		
USB Interface						
Pin Name	**Pin No.**	**I/O**	**Status after Reset**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	71	AI	-	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	A test point must be reserved.
USB_DP	69	AIO	-	USB 2.0 differential data (+)		90 Ω differential impedance. USB 2.0 compliant. Test points must be reserved.
USB_DM	70	AIO	-	USB 2.0 differential data (-)		
(U)SIM Interface						
Pin Name	**Pin No.**	**I/O**	**Status after Reset**	**Description**	**DC Characteristics**	**Comment**
USIM_VDD	14	PO	-	(U)SIM card power supply	**Low-voltage:** Vmin = 1.67 V Vnom = 1.8 V Vmax = 1.93 V **High-voltage:** Vmin = 2.7 V Vnom = 3.0 V Vmax = 3.3 V	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM_DATA	15	DIO	PU	(U)SIM card data	USIM_VDD	
USIM_CLK	16	DO	PU	(U)SIM card clock		

USIM_RST	17	DO	PU	(U)SIM card reset		
USIM_DET	13	DI	PU	(U)SIM card hot-plug detect	VDD_EXT	If unused, keep it open.
USIM_GND	10	-	-	Specified ground for (U)SIM card		Connect to the ground of (U)SIM card.
SDIO Interface (SD Card Application)						
Pin Name	**Pin No.**	**I/O**	**Status after Reset**	**Description**	**DC Characteristics**	**Comment**
SD_SDIO_CLK	32	DO	PD	SD card SDIO clock	SD_SDIO_VDD	If unused, keep them open.
SD_SDIO_CMD	33	DIO	PU	SD card SDIO command		
SD_SDIO_DATA0	31	DIO	PU	SD card SDIO data bit 0		
SD_SDIO_DATA1	30	DIO	PU	SD card SDIO data bit 1		
SD_SDIO_DATA2	29	DIO	PU	SD card SDIO data bit 2		
SD_SDIO_DATA3	28	DIO	PU	SD card SDIO data bit 3		
SD_SDIO_VDD	34	PO	-	SD card SDIO power supply	**Low-voltage:** Vmin = 1.67 V Vnom = 1.8 V Vmax = 1.93 V **High-voltage:** Vmin = 2.7 V Vnom = 2.85 V Vmax = 3.1 V	
SD_DET	23	DI	PU	SD card hot-plug detect	VDD_EXT	If unused, keep it open. If it is used, an external 10 nF capacitor must be reserved.

Main UART						
Pin Name	**Pin No.**	**I/O**	**Status after Reset**	**Description**	**DC Characteristics**	**Comment**
MAIN_RI	62	DO	PU	Main UART ring indication	VDD_EXT	If unused, keep them open.
MAIN_DCD	63	DO	PU	Main UART data carrier detect		
MAIN_CTS	64	DO	PU	Clear to send signal from the module		Connect to the MCU's CTS. If unused, keep it open.
MAIN_RTS	65	DI	PU	Request to send signal to the module		Connect to the MCU's RTS. If unused, keep it open.
MAIN_DTR	66	DI	PU	Main UART data terminal ready		If unused, keep them open.
MAIN_RXD	68	DI	PU	Main UART receive		
MAIN_TXD	67	DO	PU	Main UART transmit		
Debug UART						
Pin Name	**Pin No.**	**I/O**	**Status after Reset**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	11	DI	PU	Debug UART receive	VDD_EXT	Test points must be reserved.
DBG_TXD	12	DO	H	Debug UART transmit		
SPI*						
Pin Name	**Pin No.**	**I/O**	**Status after Reset**	**Description**	**DC Characteristics**	**Comment**
SPI_CS	37	DO	PD	SPI chip select	VDD_EXT	If unused, keep them open.
SPI_DOUT	38	DO	PD	SPI data output		
SPI_DIN	39	DI	PD	SPI data input		
SPI_CLK	40	DO	PD	SPI clock		
I2C Interface*						

Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
I2C_SCL	41	OD	PU	I2C serial clock	VDD_EXT	An external 1.8 V pull-up resistor is needed.
I2C_SDA	42	OD	PU	I2C serial data		
SDIO Interface (WLAN Application)*						
Pin Name	**Pin No.**	**I/O**	**Status after Reset**	**Description**	**DC Characteristics**	**Comment**
WLAN_SLP_CLK	118	DO	PD	WLAN sleep clock	VDD_EXT	If unused, keep them open.
WLAN_PWR_EN	127	DO	PU	WLAN power supply enable control		
WLAN_SDIO_DATA3	129	DIO	PU	WLAN SDIO data bit 3		
WLAN_SDIO_DATA2	130	DIO	PU	WLAN SDIO data bit 2		
WLAN_SDIO_DATA1	131	DIO	PU	WLAN SDIO data bit 1		
WLAN_SDIO_DATA0	132	DIO	PU	WLAN SDIO data bit 0		
WLAN_SDIO_CLK	133	DO	PU	WLAN SDIO clock		
WLAN_SDIO_CMD	134	DIO	PU	WLAN SDIO command		
WLAN_WAKE	135	DI	PU	Wake up the host by an external Wi-Fi module		
WLAN_EN	136	DO	PU	WLAN function enable control		
RF Antenna Interfaces						
Pin Name	**Pin No.**	**I/O**	**Status after Reset**	**Description**	**DC Characteristics**	**Comment**
ANT_DRX	35	AI	-	Diversity antenna interface		50 Ω characteristic impedance.
ANT_MAIN	49	AIO	-	Main antenna interface		
ADC Interfaces*						

Pin Name	Pin No.	I/O	Status after Reset	Description	DC Characteristics	Comment
ADC0	45	AI	-	General-purpose ADC interface	Voltage Range: 0 V–VBAT_BB	If unused, keep them open.
ADC1	44	AI	-			
Other Interfaces						
Pin Name	**Pin No.**	**I/O**	**Status after Reset**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	115	DI	-	Force the module into download mode	VDD_EXT	Active High. A test point is recommended to be reserved.
WAKEUP_IN*	1	DI	PU	Wake up the module		If unused, keep it open.
AP_READY*	2	DI	PU	Application processor ready		
W_DISABLE#	4	DI	PU	Airplane mode control		Pull-up by default. In low voltage level, module can enter airplane mode. If unused, keep it open.
Antenna Tuner Control Interfaces						
Pin Name	**Pin No.**	**I/O**	**Status after Reset**	**Description**	**DC Characteristics**	**Comment**
GRFC1	144	DO	PU	Generic RF controller	VDD_EXT	If unused, keep it open.
GRFC2	143	DO	PU			
RESERVED Pins						
Pin Name	**Pin No.**					**Comment**
RESERVED	18, 24–27, 43, 47, 55, 73–84, 113, 114, 116, 117, 119–126, 128, 137–140, 141–142					Keep them open.

NOTE

1. The USB_BOOT cannot be pulled up to high level before the module is turned on successfully.
2. For more details about antenna tuner control interfaces, contact Quectel Technical Support.

3. Keep the unused and RESERVED pins open. Connect all GND pins to the ground.

2.5. EVB Kit

Quectel supplies an evaluation board (UMTS & LTE EVB) with accessories to develop and test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Operating Modes

Table 7: Overview of Operating Modes

Modes	Details	
Full Functionality Mode	Idle	Software is active. The module remains registered on the network but has no data interaction with the network.
	Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transmission rate.
Minimum Functionality Mode	**AT+CFUN=0** can set the module to a minimum functionality mode. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN=4** or W_DISABLE# pin can set the module to airplane mode. In this case, RF function will be invalid.	
Sleep Mode	In this mode, power consumption of the module will be reduced to an ultra-low level. In this mode, the module can still receive paging, SMS* and TCP/UDP data from network.	
Shutdown Mode	In this mode, the VBAT power supply is constantly turned on and the software stops working.	

NOTE

For more details about the AT command, see ***document [2]***.

3.2. Sleep Mode

In sleep mode, the module can reduce power consumption to an ultra-low level.

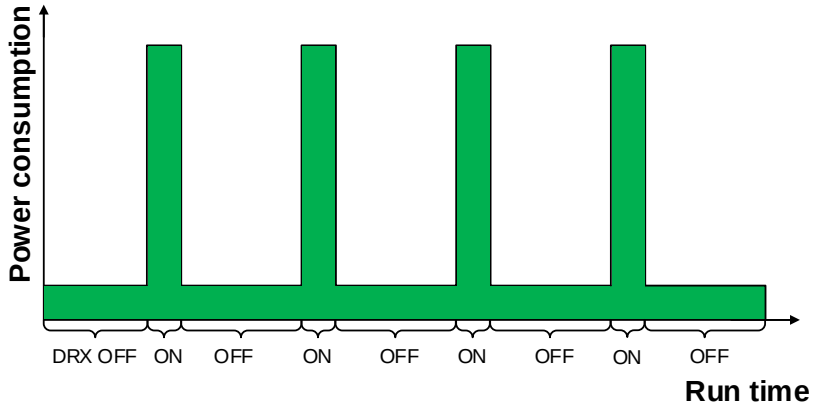


Figure 2: Module Power Consumption in Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

3.2.1. UART Application Scenario

If MCU communicates with module via UART interface, the following preconditions should be met to enable the module to enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Drive MAIN_DTR to high level.
- Ensure the USB_VBUS is kept at low level, or kept open.

The following figure shows the connection between the module and MCU.

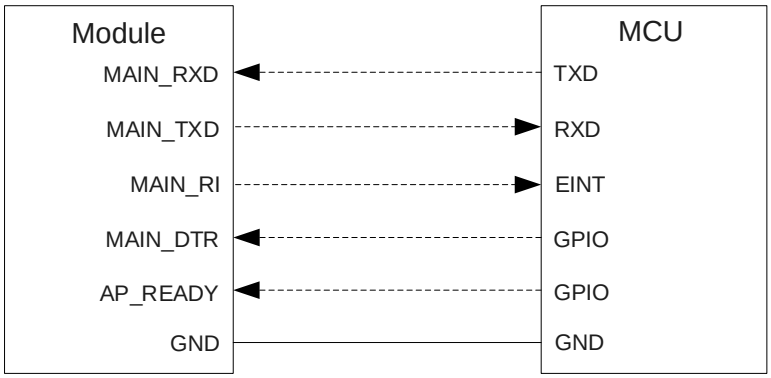


Figure 3: Sleep Mode Application via UART Interface

- Driving MAIN_DTR to low level by MCU will wake up the module.
- When the module has a URC to report, the URC will trigger the behavior of MAIN_RI pin. See ***Chapter 4.10*** for details about MAIN_RI behavior.

3.2.2. USB Application Scenarios

3.2.2.1. With USB Suspend/Resume and USB Remote Wakeup Function

If the host supports USB Suspend/Resume and remote wakeup functions, the following three preconditions must be met to make the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable the sleep mode.
- Ensure the MAIN_DTR is kept at high level or kept open.
- The host's USB bus, which is connected with the module's USB interface, enters Suspend state.

The following figure shows the connection between the module and the host.

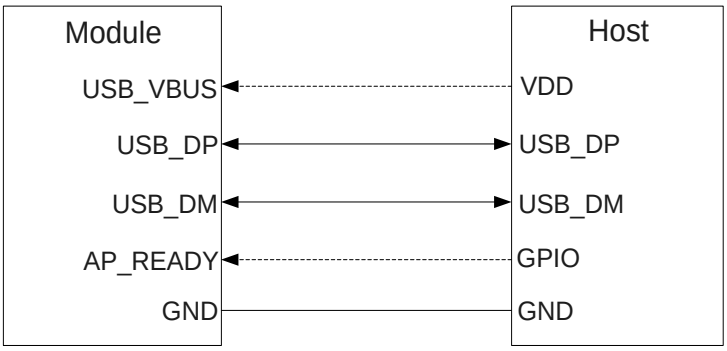


Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will send remote wakeup signals via USB bus to wake up the host.

3.2.2.2. Without USB Remote Wakeup Function

If the host supports USB Suspend/Resume, but does not support remote wakeup function, the MAIN_RI signal is needed to wake up the host.

There are three preconditions make let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable the sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters Suspend state.

The following figure shows the connection between the module and the host.

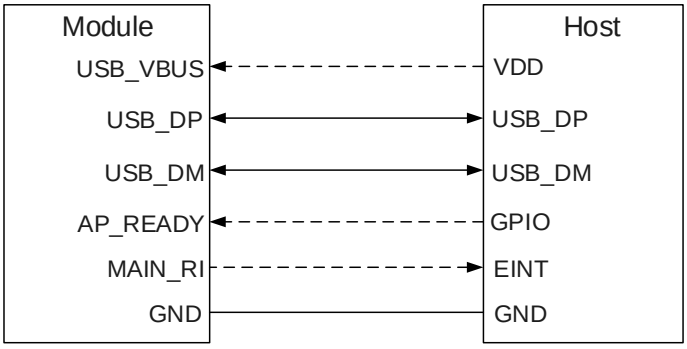


Figure 5: Sleep Mode Application with MAIN_RI

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the URC will trigger the behavior of MAIN_RI pin. See ***Chapter 4.10*** for details about MAIN_RI behavior.

3.2.2.3. Without USB Suspend Function

If the host does not support USB Suspend function, disconnect USB_VBUS with additional control circuit to make the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable the sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

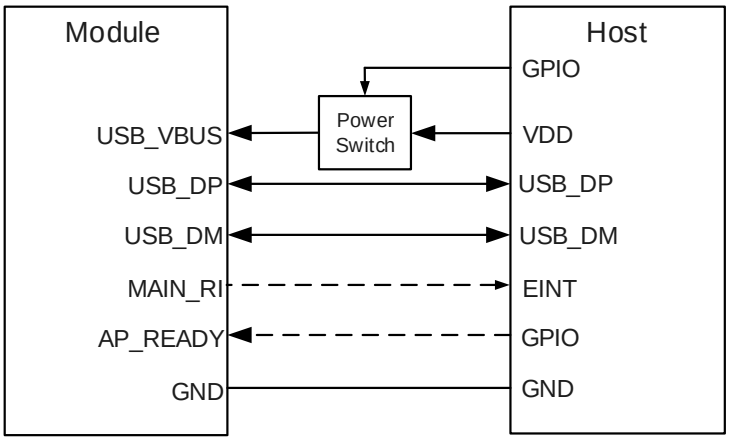


Figure 6: Sleep Mode Application Without Suspend Function

Turn on the power switch and supply power to USB_VBUS will wake up the module.

NOTE

1. Pay attention to the level match shown in dotted line between the module and the host.
2. For more details about the AT command, see ***document [2]***.

3.3. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default. Its control function for airplane mode is disabled by default, and **AT+QCFG="airplanecontrol",1** can be used to enable the function. Driving the pin to low level can make the module enter airplane mode. For more details about the AT command, see ***document [2]***.

Software:

AT+CFUN=<fun> provides choices of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode (Both (U)SIM and RF functions are disabled).
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode (RF function is disabled).

3.4. Power Supply

3.4.1. Power Supply Pins

The module provides four VBAT pins dedicated to the connection with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part.
- Two VBAT_BB pins for module's BB part.

Table 8: Pin Description of Power Supply

Pin Name	Pin No.	I/O	Description	Comment
VBAT_BB	59, 60	PI	Power supply for the module's BB part	It must be provided with sufficient current of at least 0.8 A. A test point is recommended to be reserved.
VBAT_RF	57, 58	PI	Power supply for the module's RF part	It must be provided with sufficient current of at least 2.0 A. A test point is recommended to be reserved.
VDD_EXT	7	PO	Provide 1.8 V for external circuits	It can provide a pull-up power to the external GPIO. A test point is recommended to be reserved.

3.4.2. Reference Design for Power Supply

The power source is critical to the module's performance. For the module that supports GSM frequency bands, the selected external power supply should be able to provide sufficient current of at least 2.8 A [5]. If the voltage difference between input voltage and the supply voltage is small, it is suggested to use an LDO; if the voltage difference is big, a buck converter is recommended.

The following figure shows a reference design for +5 V input power source.

[5] For the module that does not support GSM frequency bands, the selected external power supply should be able to provide sufficient current of at least 2.0 A.

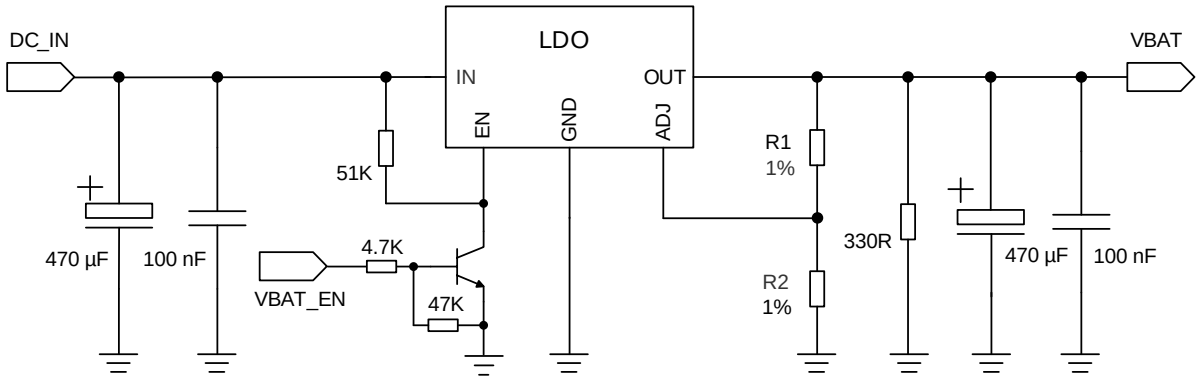


Figure 7: Reference Design of Power Supply

NOTE

It is recommended to add switch control for power supply.

3.4.3. Requirements for Voltage Stability

The power supply range of the module is from 3.4 V to 4.3 V. Ensure the input voltage will never drop below 3.4 V.

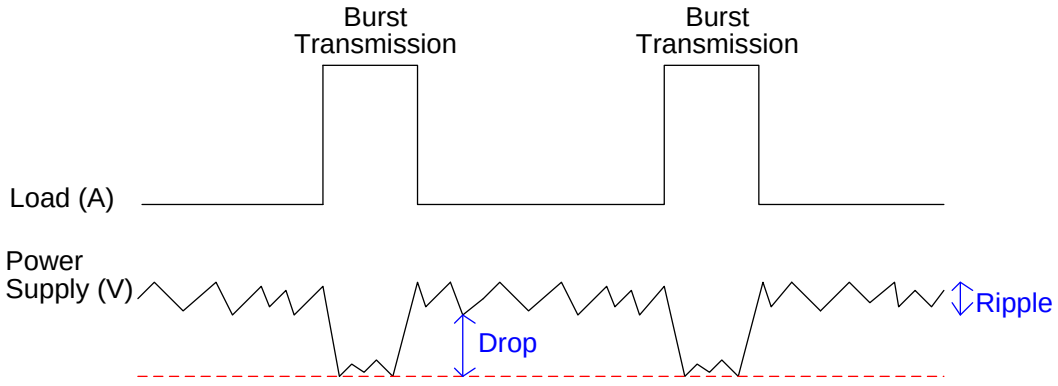


Figure 8: Power Supply Limits During Burst Transmission

To decrease voltage drop, use a bypass capacitor of about 100 µF with low ESR (ESR ≤ 0.7 Ω), and reserve a multi-layer ceramic chip (MLCC) capacitor array with ultra-low ESR. Use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to the VBAT_BB and VBAT_RF pins. The main power supply from an external application should be a single voltage source and can be expanded to two sub paths routed as the star configuration. The width of VBAT_BB trace and VBAT_RF trace should be at least 0.8 mm and 2 mm respectively. In principle,

the longer the VBAT trace is, the wider it should be.

In order to ensure the stability of the power supply to the module, add a TVS component with V_{RWM} = 4.5 V, P_{PP} = 2550 W at the front end of the power supply. The following figure shows the reference design of the power supply.

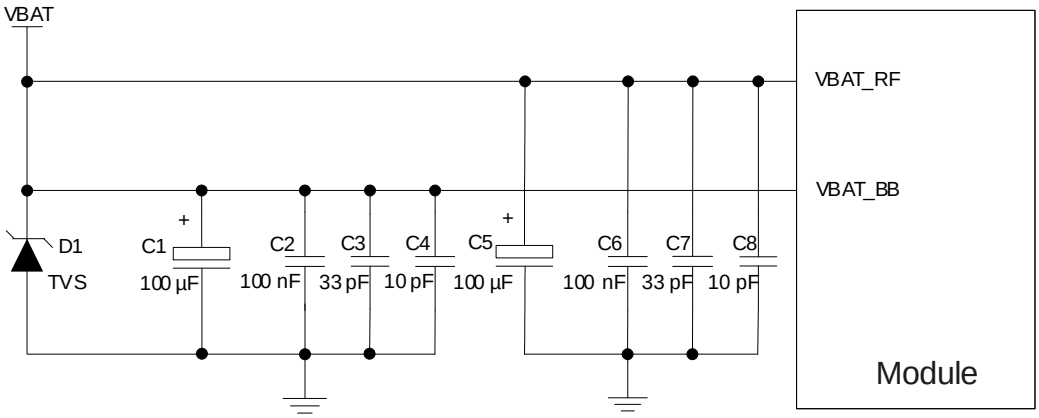


Figure 9: Reference Design of Power Supply

3.5. Turn-on

3.5.1. Turn-on with PWRKEY

Table 9: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	21	DI	Turn on/off the module	VBAT power domain. Active low. A test point is recommended to be reserved.

When the module is in turn-off mode, it can be turned on by driving the PWRKEY pin to a low level for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

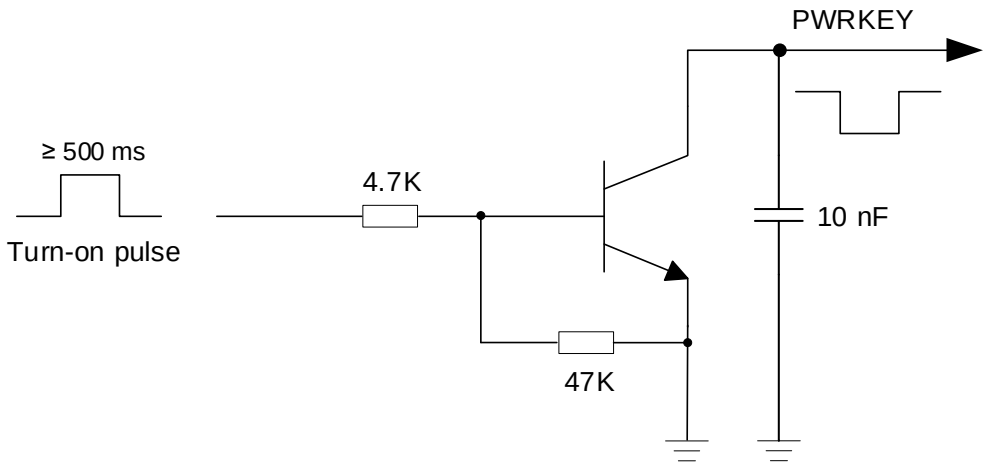


Figure 10: Reference Circuit of Turn-on with Driving Circuit

Another way to control the PWRKEY is using a button directly. When pressing the button, electrostatic strike may be generated from finger. Therefore, an ESD protection component should be placed near the button for electrostatic protection. The reference circuit is as follows.

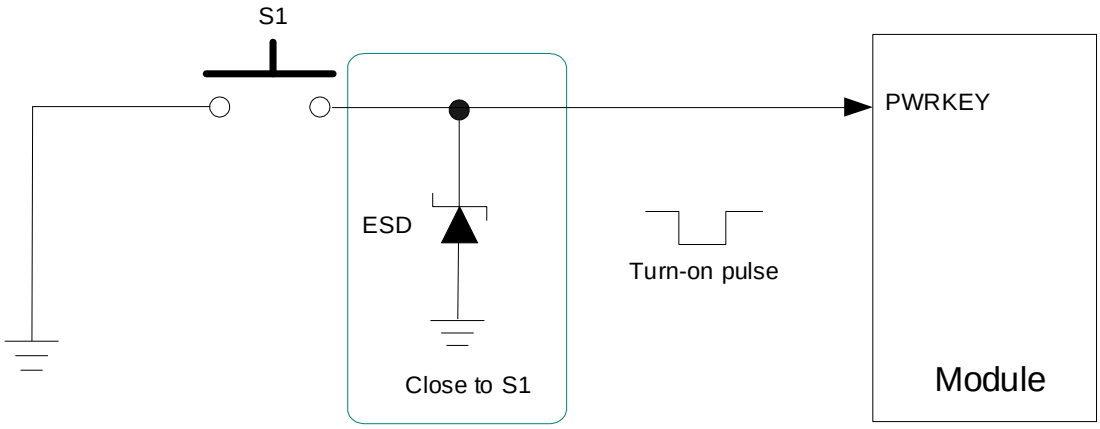


Figure 11: Reference Circuit of Turn-on with Button

The timing of turn-on with PWRKEY is illustrated in the following figure.

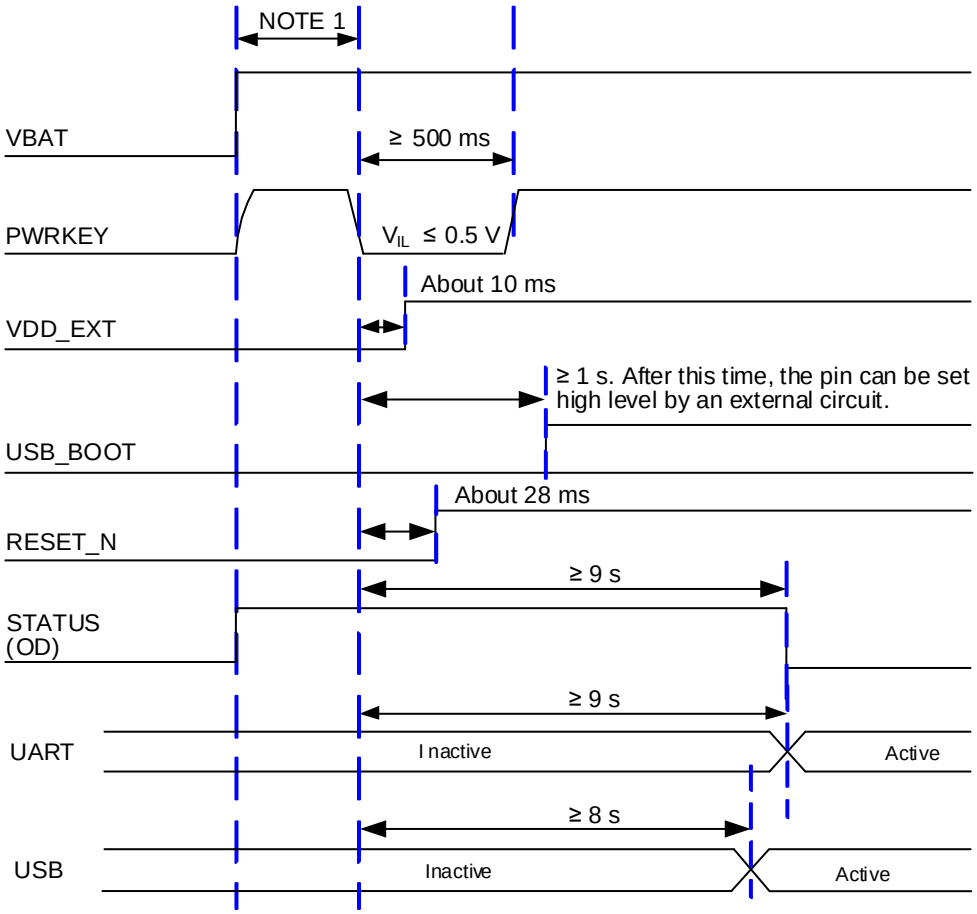


Figure 12: Timing of Turn-on with PWRKEY

NOTE

1. Ensure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time difference between powering VBAT up and pulling PWRKEY down is at least 30 ms.
2. If the module needs to turn on automatically but does not need turn-off function, PWRKEY can be driven low directly to ground with a recommended 4.7 kΩ resistor.

3.6. Turn-off

The following procedures can be used to turn off the module normally.

3.6.1. Turn-off with PWRKEY

Driving the PWRKEY to low level for at least 650 ms and then release it, and the module will execute power-down procedure. The timing of turn-off with PWRKEY is illustrated in the following figure.

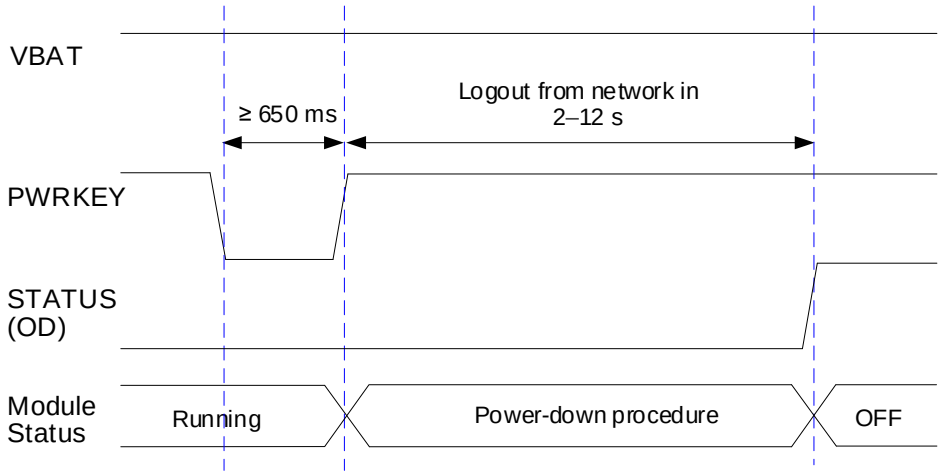


Figure 13: Timing of Turn-off with PWRKEY

During the turn-off process, the module needs to log out from network. The logout time is related to the current network state, which is measured to take about 2–12 s. Therefore, it is recommended to turn off or restart the module after 12 s to ensure that the important software data is saved before completely shutting down.

3.6.2. Turn off with AT Command

To turn off the module, you can also execute **AT+QPOWD**, which is similar to turning off the module via the PWRKEY pin.

For more details about the AT command, see ***document [2]***.

NOTE

1. To avoid corrupting the data of internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or AT command can you cut off the power supply.
2. When turning off module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on again after successfully turn-off.

3.7. RESET_N

RESET-N pin can be used to reset the module. Drive RESET_N low for at least 300 ms and then release it to reset the module. RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 10: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	20	DI	Reset the module	1.8 V power domain. Active low after turn-on. A test point is recommended to be reserved if unused.

The recommended circuit for reset function is similar to the PWRKEY control circuit. You can use an open drain/collector driver or a button to control the RESET_N.

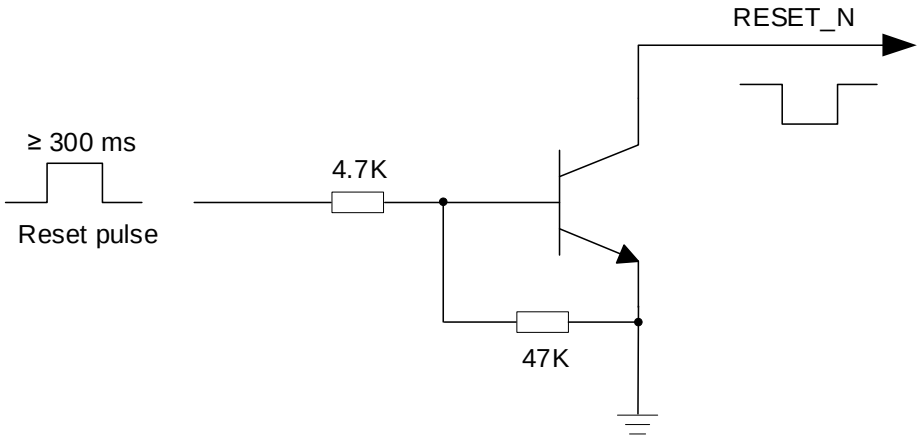


Figure 14: Reference Circuit of RESET_N with Driving Circuit

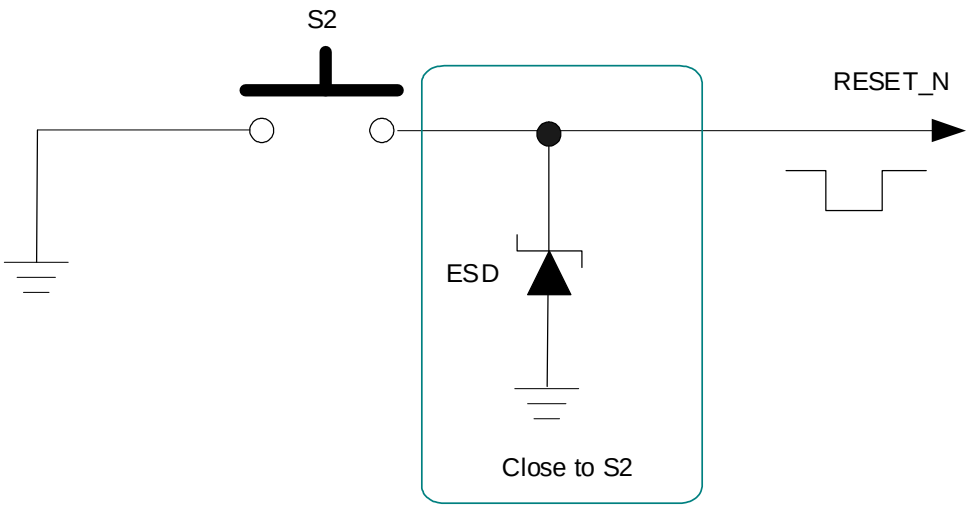


Figure 15: Reference Circuit of RESET_N with Button

The timing of resetting module is illustrated in the following figure.

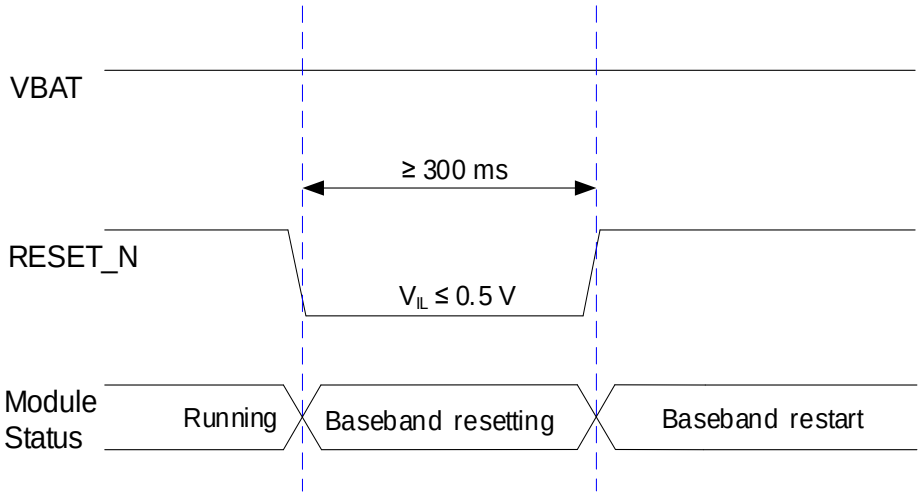


Figure 16: Timing of Reset

NOTE

1. Ensure that there is no large capacitance exceeding 10 nF on PWRKEY and RESET_N pins.
2. RESET_N pin only resets the baseband chip inside the module and does not reset the power management chip.

4 Application Interfaces

4.1. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports full-speed (12 Mbps) and high-speed (480 Mbps) modes. The USB interface can only serve as a slave device and is used for AT command communication, data transmission, software debugging and firmware upgrade.

The following table shows the pin description of USB interface.

Table 11: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	71	AI	USB connection detect	A test point must be reserved.
USB_DP	69	AIO	USB 2.0 differential data (+)	90 Ω differential impedance. USB 2.0 compliant. Test points must be reserved.
USB_DM	70	AIO	USB 2.0 differential data (-)	

For more details about the USB 2.0 specifications, visit http://www.usb.org/home.

Test points must be reserved for debugging and firmware upgrade in your designs. The following figure shows a reference circuit of USB interface.

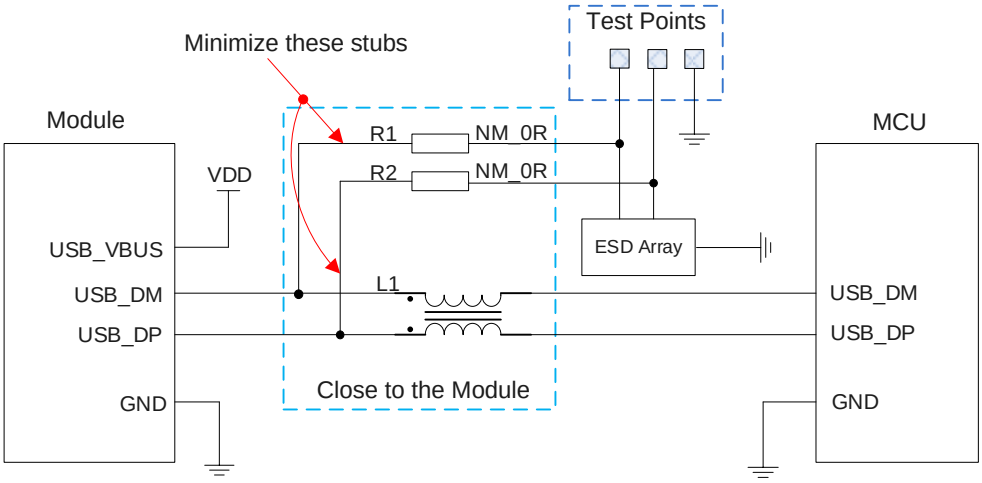


Figure 17: Reference Circuit of USB Interface

A common mode choke L1 is recommended to be added in series between the module and your MCU to suppress EMI. Meanwhile, the 0 Ω resistors (R1 and R2) should be added in series between the module and the test points to facilitate debugging, and the resistors are not mounted by default. To ensure the integrity of USB data trace signal, L1, R1 and R2 components must be placed close to the module, and also resistors R1 and R2 should be placed close to each other. The extra stubs of trace must be as short as possible.

To meet USB specifications, the following principles should be complied with when designing the USB interface.

- It is important to route the USB signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below.
- Junction capacitance of the ESD protection component might cause influences on USB data traces, so pay attention to the selection of the device. Typically, the stray capacitance should be less than 2 pF for USB.
- It is recommended to reserve a 0 Ω resistor on USB_DP and USB_DM lines respectively.

For more details about the USB specifications, visit http://www.usb.org/home.

4.2. USB_BOOT

The module provides a USB_BOOT pin. You can pull up USB_BOOT to VDD_EXT before turning on the module, thus the module will enter forced download mode. In this mode, the module supports firmware upgrade over USB interface.

Table 12: Pin Description of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	115	DI	Force the module into download mode	Active high. A test point is recommended to be reserved.

The following figure shows a reference circuit of USB_BOOT.

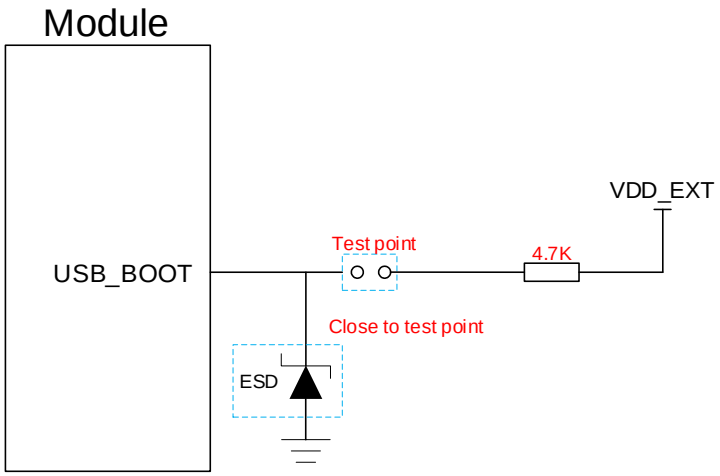


Figure 18: Reference Circuit of USB_BOOT

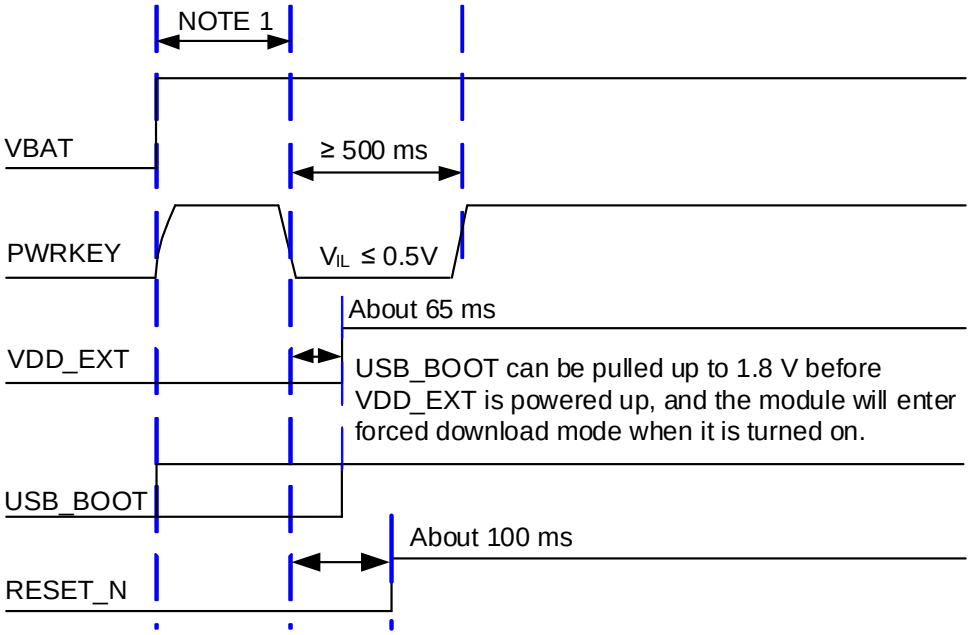


Figure 19: Timing for Entering Forced Download Mode

NOTE

1. Ensure that VBAT is stable before driving PWRKEY low. The time period between powering VBAT up and driving PWRKEY low shall be at least 30 ms.
2. Follow the above timing when using MCU to control the module to enter the forced download mode. It is not recommended to pull up USB_BOOT to 1.8 V before powering up VBAT. If you need to manually force the module to enter download mode, directly connect the test points as shown in ***Figure 18***.
3. If the module needs to start up normally, do not pull USB_BOOT up to a high level before the module starts up successfully.

4.3. (U)SIM Interface

The module provides one (U)SIM interface, which meets ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V (U)SIM card is supported.

Table 13: Pin Description of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	14	PO	(U)SIM card power supply	Either 1.8 V or 3.0 V (U)SIM card is

				supported and can be identified automatically by the module.
USIM_DATA	15	DIO	(U)SIM card data	
USIM_CLK	16	DO	(U)SIM card clock	
USIM_RST	17	DO	(U)SIM card reset	
USIM_DET	13	DI	(U)SIM card hot-plug detect	If unused, keep it open.
USIM_GND	10	-	Specified ground for (U)SIM card	Connect to the ground of (U)SIM card.

The module supports (U)SIM card hot-plug via the USIM_DET, and both high-level and low-level detections are supported. Hot-plug function is disabled by default and can be configured via **AT+QSIMDET**. See ***document [2]*** for more details.

The reference circuit of the 8-pin (U)SIM interface is as follows.

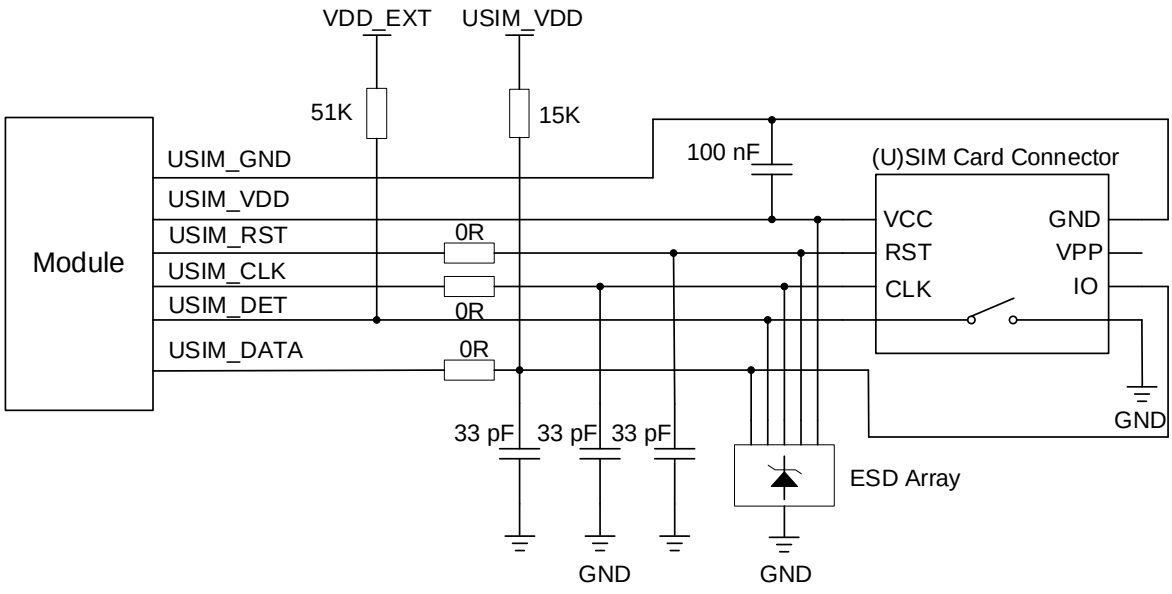


Figure 20: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If the (U)SIM card hot-plug detect function is not needed, keep USIM_DET open. A reference circuit of (U)SIM interface with a 6-pin (U)SIM card connector is as follow.

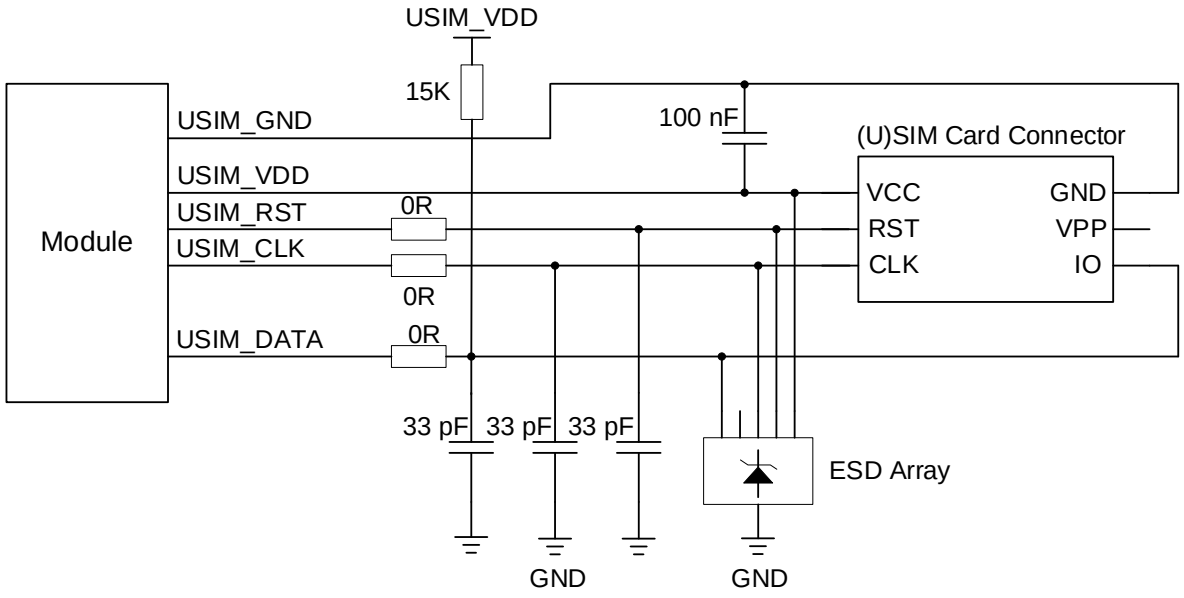


Figure 21: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, you should follow the principles below in (U)SIM circuit design:

- Place the (U)SIM card connector close to the module. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signal traces away from RF and power supply traces.
- The bypass capacitor of USIM_VDD should not exceed 1 μF.
- Ensure the tracing between the USIM_GND of module and the ground of (U)SIM card connector is short and wide. Keep the trace width of USIM_GND and USIM_VDD at least 0.5 mm to keep the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep the traces away from each other and shield them with surrounded ground.
- To offer better ESD protection, you can add an ESD array of which the parasitic capacitance should not exceed 15 pF. Add 0 Ω resistors in series between the module and the (U)SIM card connector to facilitate debugging. Additionally, add 33 pF capacitors in parallel among USIM_DATA, USIM_CLK and USIM_RST signal traces to filter out RF interference. Note that the (U)SIM peripheral circuit should be placed close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve the anti-jamming capability of the (U)SIM card. When the routing trace of (U)SIM card is too long, or there is a relatively close interference source, it is recommended to add a pull-up resistor near the (U)SIM card connector.

4.4. I2C Interface*

The module provides one I2C interface.

Table 14: Pin Description of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	41	OD	I2C serial clock	Used for external codec. An external 1.8 V pull-up resistor is needed.
I2C_SDA	42	OD	I2C serial data	

4.5. SPI*

The module provides one SPI that only supports master mode with a maximum clock frequency of 52 MHz.

Table 15: Pin Description of SPI

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	40	DO	SPI clock	If unused, keep them open.
SPI_CS	37	DO	SPI chip select	
SPI_DIN	39	DI	SPI data input	
SPI_DOUT	38	DO	SPI data output	

4.6. UART

The module provides two UARTs: main UART and debug UART. The main features of main UART and debug UART are described as follows:

- The main UART supports 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, 921600 bps baud rates. The default baud rate is 115200 bps. This interface is used for AT command communication and data transmission. Also, it supports RTS and CTS hardware flow control.

- The debug UART supports 115200 bps baud rate. It is used for the output of partial logs.

Table 16: Pin Description of Main UART

Pin Name	Pin No.	I/O	Description	Comment
MAIN_RI	62	DO	Main UART ring indication	If unused, keep them open.
MAIN_DCD	63	DO	Main UART data carrier detect	
MAIN_CTS	64	DO	Clear to send signal from the module	Connect to the MCU's CTS. If unused, keep it open.
MAIN_RTS	65	DI	Request to send signal to the module	Connect to the MCU's CTS. If unused, keep it open.
MAIN_DTR	66	DI	Main UART data terminal ready	If unused, keep them open.
MAIN_RXD	68	DI	Main UART receive	
MAIN_TXD	67	DO	Main UART transmit	

Table 17: Pin Description of Debug UART

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	11	DI	Debug UART receive	Test points must be reserved.
DBG_TXD	12	DO	Debug UART transmit	

The module provides a 1.8 V UART. You can use a voltage-level translator between the module and MCU’s UART if the MCU is equipped with a 3.3 V UART. A voltage-level translator TXS0108EPWR provided by *Texas Instruments* is recommended. The following figure shows a reference design.

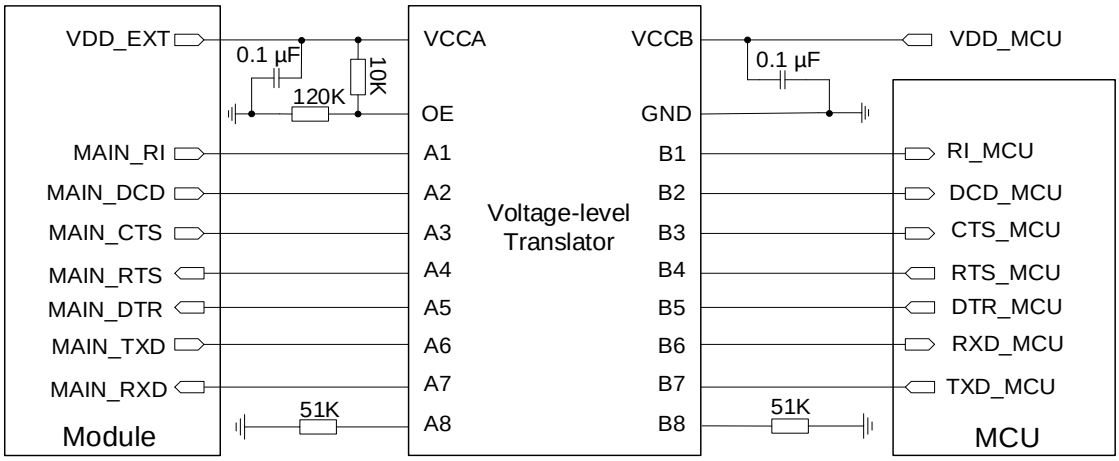


Figure 22: Reference Design of UART with a Voltage-level Translator (Main UART)

Visit http://www.ti.com for more information.

Another example with transistor circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

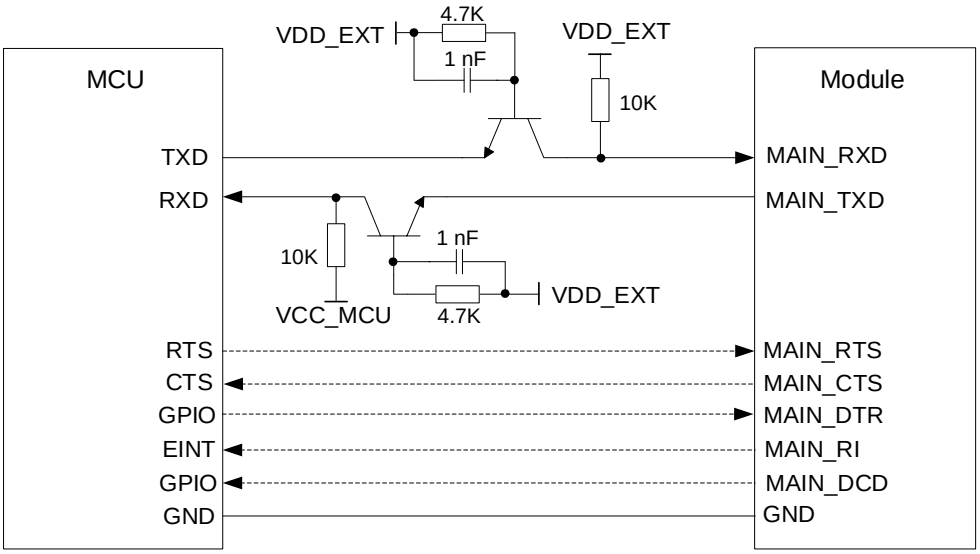


Figure 23: Reference Design of UART with Transistor Circuit (Main UART)

NOTE

1. Transistor circuit solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.
3. To increase the stability of UART communication, it is recommended to add UART hardware flow

control design.

4. The level-shifting circuits (***Figure 22*** and ***Figure 23***) take the main UART as an example. The circuits of the debug UART is connected in the same way as the main UART.

4.7. SDIO Interface

4.7.1. SD Card Application

The module provides one SD card application interface which supports SD 3.0 protocol.

Table 18: Pin Description of SD Card Application Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_SDIO_CLK	32	DO	SD card SDIO clock	If unused, keep them open.
SD_SDIO_CMD	33	DIO	SD card SDIO command	
SD_SDIO_DATA0	31	DIO	SD card SDIO data bit 0	
SD_SDIO_DATA1	30	DIO	SD card SDIO data bit 1	
SD_SDIO_DATA2	29	DIO	SD card SDIO data bit 2	
SD_SDIO_DATA3	28	DIO	SD card SDIO data bit 3	
SD_SDIO_VDD	34	PO	SD card SDIO power supply	
SD_DET	23	DI	SD card hot-plug detect	If unused, keep it open. If it is used, an external 10 nF capacitor must be reserved.

The following figure illustrates a reference design of SD card application interface.

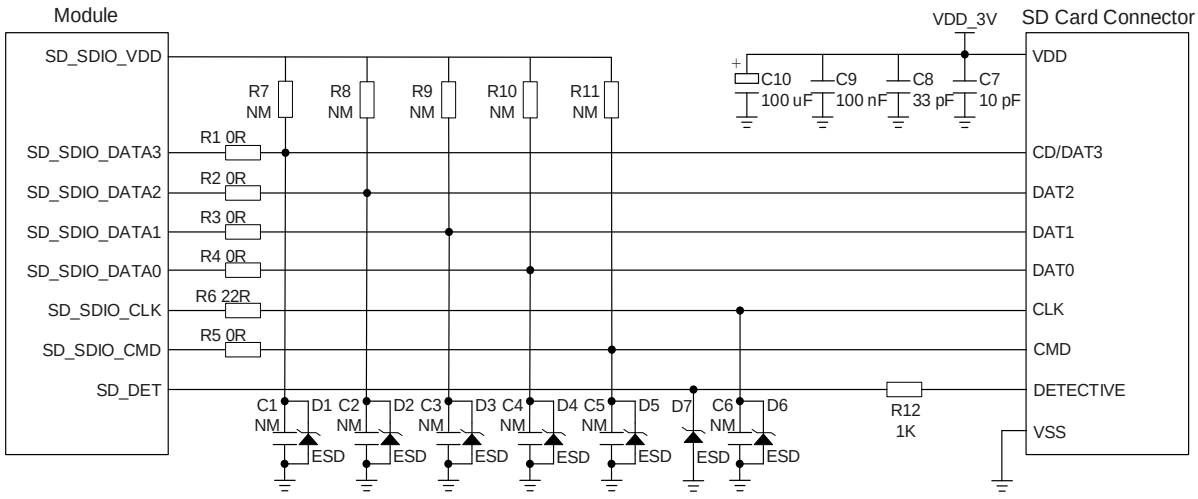


Figure 24: Reference Circuit of SD Card Application Interface

In SD card application interface design, in order to ensure good communication performance and reliability of SD card, the following design principles should be complied with:

- The voltage range of SD card power supply VDD_3V is 2.7–3.6 V and a sufficient current of at least 0.8 A should be provided. The maximum output current of SD_SDIO_VDD is 50 mA which can only be used for SDIO pull-up resistors. VDD_3V is provided externally.
- To avoid jitter of bus, resistors R7–R11 are not mounted by default and needed to pull up the SDIO to SD_SDIO_VDD. Value of these resistors is 10 kΩ to 100 kΩ and the recommended value is 100 kΩ. SD_SDIO_VDD should be used as the pull-up power.
- In order to improve signal quality, it is recommended to reserve 0 Ω resistors R1–R5 in series between the module and the SD card and add a 15–24 Ω resistor in series on SD_SDIO_CLK trace. The trace distance between the SD_SDIO_CLK pin and the resistor must be less than 5 mm. The bypass capacitors C1 to C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- In order to offer good ESD protection, it is recommended to add an ESD protection component on SD card pins near the SD card connector with junction capacitance less than 8 pF.
- It is important to route the SDIO signal traces with ground surrounded. The impedance of SDIO data trace is 50 Ω (±10 %).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, as well as noisy signals such as clock signals and DC-DC signals.
- It is recommended to keep the traces of SD_SDIO_CLK, SD_SDIO_DATA [0:3] and SD_SDIO_CMD with equal length (the difference among them is less than 1 mm) and the total routing length needs to be less than 50 mm.
- Make sure the adjacent trace spacing larger than two times the trace width and the load capacitance of SDIO bus should be less than 15 pF.

4.7.2. WLAN Application*

The module provides one low-power SDIO 3.0 WLAN application interface and one control interface.

Table 19: Pin Description of WLAN Application Interface

Pin Name	Pin No.	I/O	Description	Comment
WLAN_SLP_CLK	118	DO	WLAN sleep clock	If unused, keep them open.
WLAN_PWR_EN	127	DO	WLAN power supply enable control	
WLAN_SDIO_DATA3	129	DIO	WLAN SDIO data bit 3	
WLAN_SDIO_DATA2	130	DIO	WLAN SDIO data bit 2	
WLAN_SDIO_DATA1	131	DIO	WLAN SDIO data bit 1	
WLAN_SDIO_DATA0	132	DIO	WLAN SDIO data bit 0	
WLAN_SDIO_CLK	133	DO	WLAN SDIO clock	
WLAN_SDIO_CMD	134	DIO	WLAN SDIO command	
WLAN_WAKE	135	DI	Wake up the host by an external Wi-Fi module	
WLAN_EN	136	DO	WLAN function enable control	

To ensure good performance in WLAN application interface design, the following principles should be complied with:

- To avoid bus jitter, it is necessary to reserve a pull-up resistor on the SDIO signal traces, with a resistance range of 10–100 kΩ and a recommended value of 100 kΩ. It is recommended to select VDD_EXT for pull-up power supply.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO signal traces is 50 Ω ±10 %.
- Keep SDIO signal traces far away from other sensitive signals such as RF and analog signals, as well as noisy signals such as clock signals and DC-DC signals.
- It is recommended to keep the trace length difference between WLAN_SDIO_CLK, WLAN_SDIO_DATA[0:3] and WLAN_SDIO_CMD less than 1 mm and the total routing length less than 50 mm.
- In order to improve the signal quality, the WLAN_SDIO_CLK signal trace needs to be connected with 15–24 Ω resistors near the module in series, and the distance from the WLAN_SDIO_CLK pin to the resistor needs to be less than 5 mm.
- The spacing between SDIO signals and other signals needs to be greater than twice the trace width, and the load capacitance of SDIO bus is less than 15 pF.

4.8. ADC Interfaces*

The module provides two Analog-to-Digital Converter (ADC) interfaces. In order to improve the accuracy of ADC, the trace of ADC interfaces should be surrounded by ground.

Table 20: Pin Description of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	45	AI	General-purpose ADC interface	If unused, keep them open.
ADC1	44	AI		

The voltage value on ADC pins can be read via **AT+QADC=<port>**:

- **AT+QADC=0:** read the voltage value on ADC0
- **AT+QADC=1:** read the voltage value on ADC1

For more details about the AT command, see ***document [2]***.

The following table describes the characteristic of the ADC interfaces.

Table 21: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC0 Input Voltage Range	0	-	VBAT_BB	V
ADC1 Input Voltage Range	0	-	VBAT_BB	V
ADC Resolution	-	9	-	bits

NOTE

1. The input voltage of each ADC pin should not exceed its corresponding voltage range.
2. It is prohibited to directly supply any voltage to ADC interfaces when the module is not powered by the VBAT.

4.9. Indication Signals

The pin description of indication signals is as follows:

Table 22: Pin Description of Indication Signals

Pin Name	Pin No.	I/O	Description	Comment
STATUS	61	OD	Indicate the module's operation status	If unused, keep them open.
NET_MODE	5	DO	Indicate the module’s network registration status	
NET_STATUS	6	DO	Indicate the module's network activity status	
SLEEP_IND	3	DO	Indicate the module's sleep mode	

4.9.1. Network Status Indication

The module provides two network indication pins: NET_MODE for the module’s network registration status indication, and NET_STATUS for the module's network activity status indication. Both can drive corresponding network status indication LEDs.

Table 23: Network Status Indication Pin Level and Module Network Status

Pin Name	Status	Description
NET_MODE	Always High	Registered on LTE network
	Always Low	Others
NET_STATUS	Blink slowly (200 ms High/1800 ms Low)	Network searching
	Blink slowly (1800 ms High/200 ms Low)	Idle
	Blink quickly (125 ms High/125 ms Low)	Data transmission is ongoing

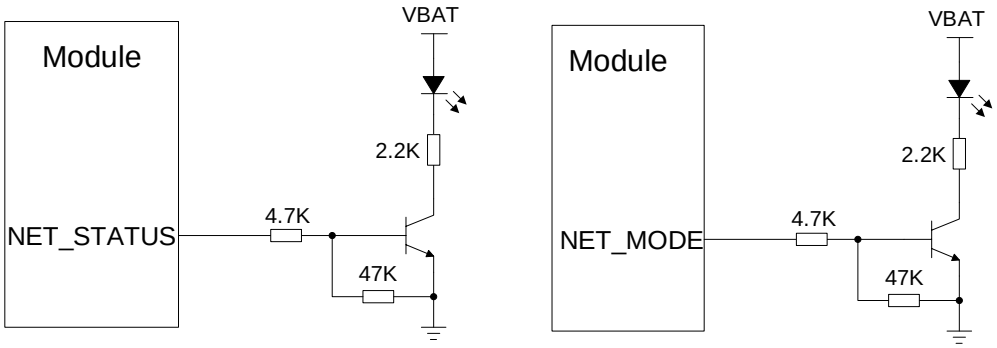


Figure 25: Reference Circuit of the Network Status Indication

4.9.2. STATUS

The STATUS pin is an open drain output for module's operation status indication. It can be connected to a GPIO of MCU with a pulled-up resistor, or used as an LED indication circuit as below. When the module is turned on normally, the STATUS outputs a low level; otherwise, the STATUS will present high-impedance state.

The following figure shows different circuit designs of STATUS, and you can choose either one according to the application demands.

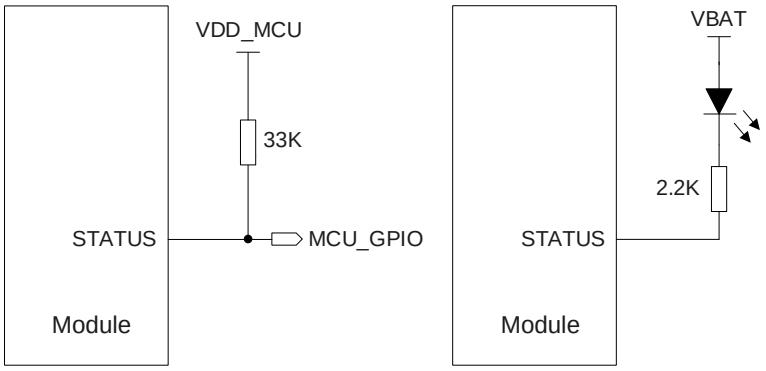


Figure 26: Reference Circuits of STATUS

NOTE

The STATUS pin cannot be used as indication of the module's shutdown status when VBAT is not available.

4.10. MAIN_RI

AT+QCFG="risignaltype","physical" can be used to configure MAIN_RI behavior. No matter on which port a URC is presented, the URC will trigger the behavior of MAIN_RI pin.

NOTE

The URC can be outputted via UART port, USB AT port and USB modem port, which can be set by **AT+QURCCFG**. The default port is USB AT port.

In addition, MAIN_RI behavior can be configured flexibly. The default behavior of the MAIN_RI is shown as below.

Table 24: MAIN_RI Level and Module Status

Module Status	MAIN_RI Level Status
Idle	MAIN_RI keeps at high level
URC	MAIN_RI outputs 120 ms low pulse when a new URC returns

The MAIN_RI behavior can be changed via **AT+QCFG**. See ***document [2]*** for details.

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Cellular Network

5.1.1. Antenna Interface & Frequency Bands

Table 25: Pin Description of Cellular Network Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_DRX	35	AI	Diversity antenna interface	50 Ω characteristic impedance.
ANT_MAIN	49	AIO	Main antenna interface	

Table 26: Operating Frequency of EC200A-CNV1

Operating Frequency	Transmit (MHz)	Receive (MHz)
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
WCDMA B1	1920–1980	2110–2170
WCDMA B5	824–849	869–894
WCDMA B8	880–915	925–960
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894

LTE-FDD B8	880–915	925–960
LTE-TDD B34	2010–2025	2010–2025
LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B39	1880–1920	1880–1920
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2535–2675	2535–2675

Table 27: Operating Frequency of EC200A-EUV1

Operating Frequency	Transmit (MHz)	Receive (MHz)
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
WCDMA B1	1920–1980	2110–2170
WCDMA B5	824–849	869–894
WCDMA B8	880–915	925–960
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960
LTE-FDD B20	832–862	791–821
LTE-FDD B28	703–748	758–803
LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2535–2675	2535–2675

Table 28: Operating Frequency of EC200A-ELV1

Operating Frequency	Transmit (MHz)	Receive (MHz)
WCDMA B1	1920–1980	2110–2170
WCDMA B5	824–849	869–894
WCDMA B8	880–915	925–960
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960
LTE-FDD B20	832–862	791–821
LTE-FDD B28	703–748	758–803
LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2535–2675	2535–2675

Table 29: Operating Frequency of EC200A-AUV1

Operating Frequency	Transmit (MHz)	Receive (MHz)
GSM850	824–849	869–894
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
PCS1900	1850–1910	1930–1990
WCDMA B1	1920–1980	2110–2170
WCDMA B2	1850–1910	1930–1990
WCDMA B4	1710–1755	2110–2155
WCDMA B5	824–849	869–894

WCDMA B8	880–915	925–960
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B2	1850–1910	1930–1990
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B4	1710–1755	2110–2155
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960
LTE-FDD B28	703–748	758–803
LTE-FDD B66	1710–1780	2110–2180
LTE-TDD B40	2300–2400	2300–2400

NOTE

LTE-TDD B41 only supports 140 MHz (2535–2675 MHz).

5.1.2. Transmitting Power

Table 30: Transmitting Power

Frequency	Max. Transmitting Power	Min. Transmitting Power
GSM850/EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800/PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
GSM850/EGSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800/PCS1900 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
WCDMA B1/B2/B4/B5/B8	23 dBm ±2 dB (Class 3)	< -49 dBm
LTE-FDD B1/B2/B3/B4/B5/B7/B8/ B20/B28/B66	23 dBm ±2 dB (Class 3)	< -39 dBm
LTE-TDD B34/B38/B39/B40/B41	23 dBm ±2 dB (Class 3)	< -39 dBm

NOTE

For GPRS transmission on 4 uplink timeslots, the maximum output power reduction is 4.0 dB. The design conforms to *3GPP TS 51.010-1* ***subclause 13.16***.

5.1.3. Receiver Sensitivity

Table 31: Conducted RF Receiver Sensitivity of EC200A-CNV1 (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)			3GPP Requirements (SIMO)
	Primary	Diversity	SIMO [6]	
WCDMA B1	-109.8	-	-	-106.7
WCDMA B5	-111.6	-	-	-104.7
WCDMA B8	-111.4	-	-	-103.7
LTE-FDD B1	-98	-98.8	-101.4	-96.3
LTE-FDD B3	-97.3	-98.3	-100.2	-93.3
LTE-FDD B5	-99	-99.8	-102.4	-94.3
LTE-FDD B8	-98.7	-98.8	-101.8	-93.3
LTE-TDD B34	-97.9	-98.4	-101	-96.3
LTE-TDD B38	-97.2	-98	-100	-96.3
LTE-TDD B39	-98.3	-98	-100.8	-96.3
LTE-TDD B40	-97.7	-98.6	-101.3	-96.3
LTE-TDD B41	-97.4	-97.9	-100.1	-94.3

Table 32: Conducted RF Receiver Sensitivity of EC200A-EUV1 (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)			3GPP Requirements (SIMO)
	Primary	Diversity	SIMO [6]	
EGSM900	-110.4	-	-	-102.4

[6] For the SIMO receiving sensitivity, LTE bands are tested with 2 Rx antennas.

DCS1800	-107.8	-	-	-102.4
WCDMA B1	-109.2	-	-	-106.7
WCDMA B5	-111.7	-	-	-104.7
WCDMA B8	-111.9	-	-	-103.7
LTE-FDD B1	-97.4	-98.4	-101.1	-96.3
LTE-FDD B3	-97	-97.8	-100.2	-93.3
LTE-FDD B5	-98.8	-100.2	-102.7	-94.3
LTE-FDD B7	-96.3	-97.3	-99.8	-94.3
LTE-FDD B8	-99	-99.5	-102.5	-93.3
LTE-FDD B20	-98.8	-99.1	-102.1	-93.3
LTE-FDD B28	-99.2	-99.7	-102.9	-94.8
LTE-TDD B38	-97.1	-98.4	-101.2	-96.3
LTE-TDD B40	-97	-98.7	-101.1	-96.3
LTE-TDD B41	-97	-97.7	-100.6	-94.3

Table 33: Conducted RF Receiver Sensitivity of EC200A-ELV1 (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)			3GPP Requirements (SIMO)
	Primary	Diversity	SIMO [6]	
WCDMA B1	-109.1	-	-	-106.7
WCDMA B5	-111.7	-	-	-104.7
WCDMA B8	-111.1	-	-	-103.7
LTE-FDD B1	-97.6	-98.9	-101.2	-96.3
LTE-FDD B3	-97	-97.7	-100.8	-93.3
LTE-FDD B5	-98.8	-99.9	-102.2	-94.3
LTE-FDD B7	-96	-97.9	-99.3	-94.3
LTE-FDD B8	-98.5	-99.2	-101.5	-93.3

LTE-FDD B20	-98.9	-98.3	-101.6	-93.3
LTE-FDD B28	-99	-99.8	-102.3	-94.8
LTE-TDD B38	-97.2	-97.9	-100.9	-96.3
LTE-TDD B40	-97.7	-98.9	-100.9	-96.3
LTE-TDD B41	-97.3	-97.8	-100.6	-94.3

Table 34: Conducted RF Receiver Sensitivity of EC200A-AUV1 (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)			3GPP Requirements (SIMO)
	Primary	Diversity	SIMO [6]	
GSM850	-110.1	-	-	-102.4
EGSM900	-110.4	-	-	-102.4
DCS1800	-108	-	-	-102.4
PCS1900	-107.8	-	-	-102.4
WCDMA B1	-109.1	-	-	-106.7
WCDMA B2	-109	-	-	-104.7
WCDMA B4	-110	-	-	-106.7
WCDMA B5	-111.5	-	-	-104.7
WCDMA B8	-111.5	-	-	-103.7
LTE-FDD B1	-97.4	-98.4	-101	-96.3
LTE-FDD B2	-97.2	-98.6	-101	-94.3
LTE-FDD B3	-97.3	-97.5	-100	-93.3
LTE-FDD B4	-98.3	-98.3	-101	-96.3
LTE-FDD B5	-98.6	-100.3	-102.2	-94.3
LTE-FDD B7	-95.6	-97.5	-99.5	-94.3
LTE-FDD B8	-98.6	-100	-102.5	-93.3
LTE-FDD B28	-98.5	-100	-102.2	-94.8

LTE-FDD B66	-97.6	-97.5	-100.5	-96.5
LTE-TDD B40	-97.5	-99.5	-101	-96.3

5.1.4. Reference Design

The module provides two RF antenna interfaces for antenna connection.

It is recommended to reserve a dual L-type matching circuit for better RF performance, and the dual L-type components (C1–C6 and R1, R2) should be placed as close to the antenna as possible. The capacitors C1–C4 are not mounted by default.

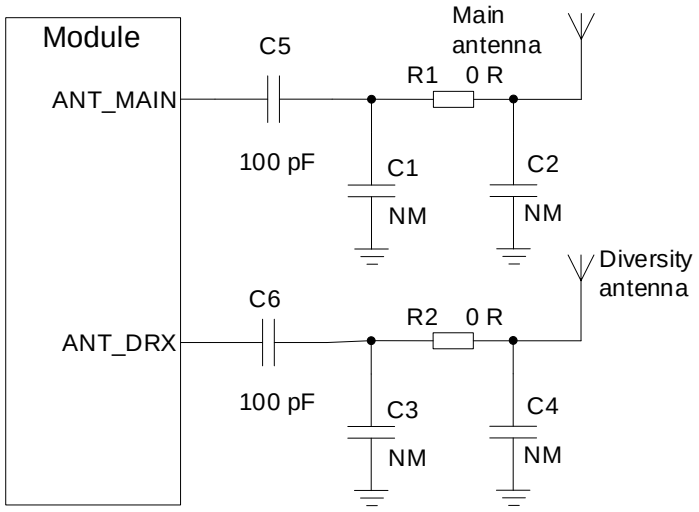


Figure 27: Reference Circuit for RF Antenna Interfaces

NOTE

If there is DC power at the antenna ports, C5 and C6 must be used for DC-blocking to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to actual requirements. If there is no DC power in the peripheral design, DC-blocking capacitors are not needed.

5.2. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF

traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

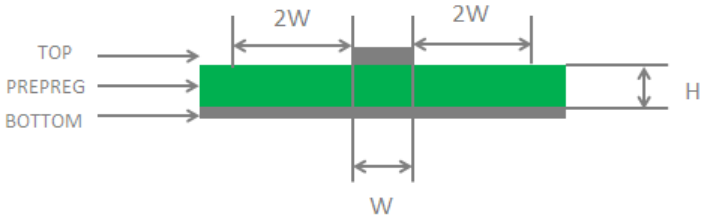


Figure 28: Microstrip Design on a 2-layer PCB

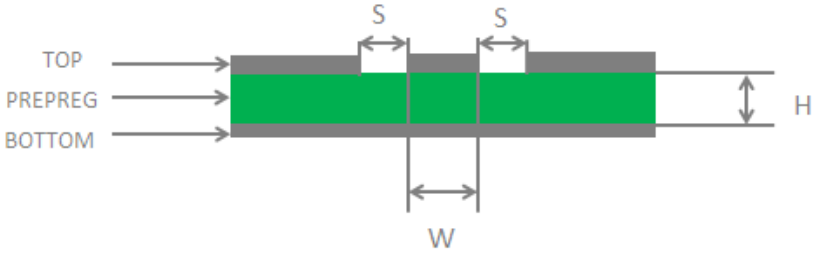


Figure 29: Coplanar Waveguide Design on a 2-layer PCB

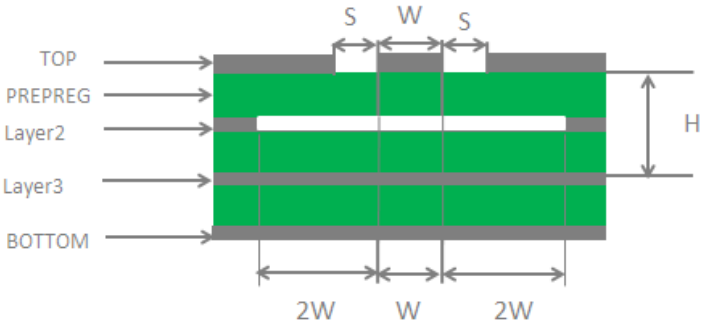


Figure 30: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

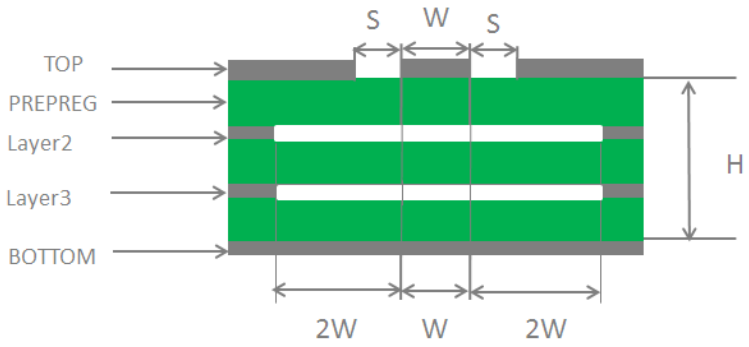


Figure 31: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, ground vias around RF traces and the reference ground improves RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [3]***.

5.3. Requirements for Antenna Design

Table 35: Requirements for Antenna Design

Antenna Type	Requirements
Cellular	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Gain: 1 dBi ● Max. input power: 50 W

- Input impedance: 50 Ω
- Polarization: vertical direction
- Cable insertion loss:
  < 1 dB：LB（< 1 GHz）
  < 1.5 dB：MB（1–2.3 GHz）
  < 2 dB：HB（> 2.3 GHz）

5.4. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT receptacle provided by Hirose.

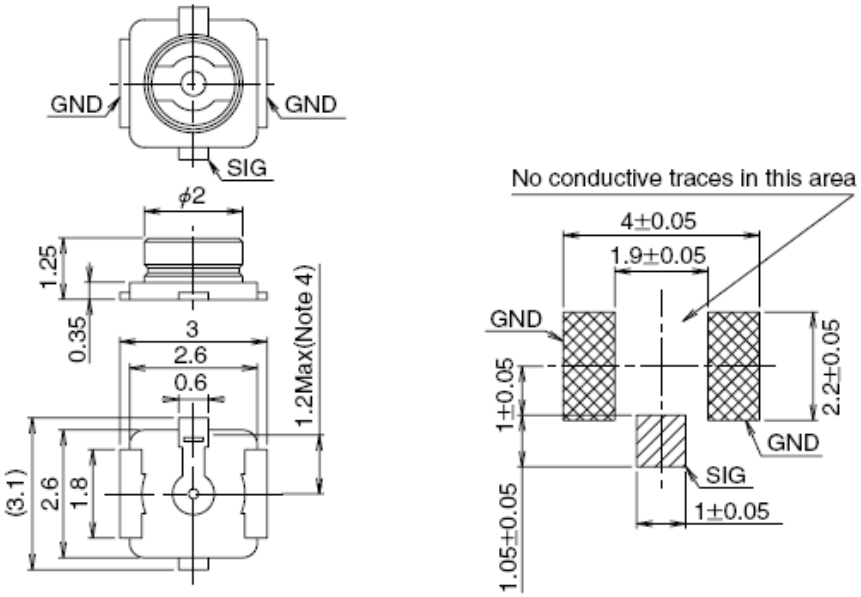


Figure 32: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

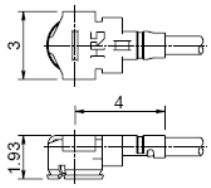
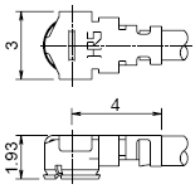
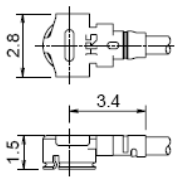
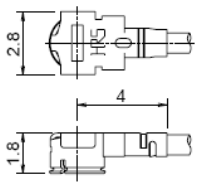
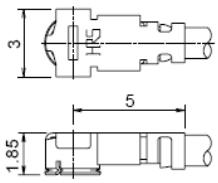
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 33: Specifications of Mated Plugs

The following figure describes the space factor of mated connector.

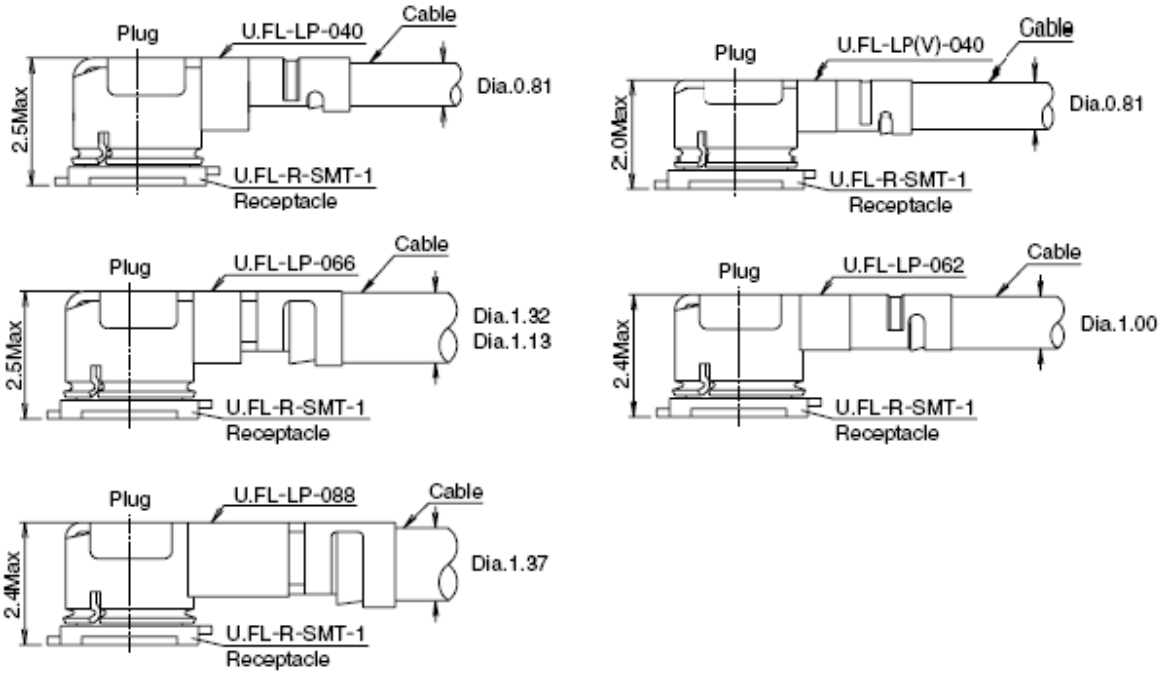


Figure 34: Space Factor of Mated Connector (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Table 36: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	5.5	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	0.8	A
Peak Current of VBAT_RF	-	2.0	A
Voltage on Digital Pins	-0.3	2.3	V
Input Voltage at ADC[0:1]	0	VBAT_BB	V

6.2. Power Supply Ratings

Table 37: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values	3.4	3.8	4.3	V
	Voltage drop during transmitting burst	At maximum power control level	0	0	400	mV

I_{VBAT_RF}	Peak supply current	At maximum power control level	-	-	2.0	A
USB_VBUS	USB connection detect	-	3.0	5.0	5.25	V

6.3. Power Consumption

Table 38: Power Consumption of EC200A-CNV1

Description	Conditions	Typ.	Unit
OFF State	Power down	8.05	μA
Sleep State	**AT+CFUN=0** (USB disconnected)	1.64	mA
	AT+CFUN=0 (USB suspended)	1.79	mA
	AT+CFUN=4 (USB disconnected)	1.94	mA
	AT+CFUN=4 (USB suspended)	2.11	mA
	WCDMA @ PF = 64 (USB disconnected)	3.98	mA
	WCDMA @ PF = 64 (USB suspended)	4.20	mA
	WCDMA @ PF = 128 (USB disconnected)	3.15	mA
	WCDMA @ PF = 256 (USB disconnected)	2.65	mA
	WCDMA @ PF = 512 (USB disconnected)	2.50	mA
	LTE-FDD @ PF = 32 (USB disconnected)	3.72	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.94	mA
	LTE-FDD @ PF = 64 (USB suspended)	3.05	mA
	LTE-FDD @ PF = 128 (USB disconnected)	2.66	mA
	LTE-FDD @ PF = 256 (USB disconnected)	2.42	mA
	LTE-TDD @ PF = 32 (USB disconnected)	3.67	mA
	LTE-TDD @ PF = 64 (USB disconnected)	3.12	mA

	LTE-TDD @ PF = 64 (USB suspended)	3.29	mA
	LTE-TDD @ PF = 128 (USB disconnected)	2.60	mA
	LTE-TDD @ PF = 256 (USB disconnected)	2.37	mA
Idle State	WCDMA @ PF = 64 (USB disconnected)	22.59	mA
	WCDMA @ PF = 64 (USB connected)	42.39	mA
	LTE-FDD @ PF = 64 (USB disconnected)	22.08	mA
	LTE-FDD @ PF = 64 (USB connected)	41.78	mA
	LTE-TDD @ PF = 64 (USB disconnected)	22.05	mA
	LTE-TDD @ PF = 64 (USB connected)	41.82	mA
WCDMA Data Transmission	WCDMA B1 HSDPA @ 22.58 dBm	635	mA
	WCDMA B5 HSDPA @ 22.38 dBm	618	mA
	WCDMA B8 HSDPA @ 22.49 dBm	597	mA
	WCDMA B1 HSUPA @ 22.19 dBm	634	mA
	WCDMA B5 HSUPA @ 22.22 dBm	596	mA
	WCDMA B8 HSUPA @ 22.23 dBm	578	mA
LTE Data Transmission	LTE-FDD B1 @ 23.39 dBm	743	mA
	LTE-FDD B3 @ 23.26 dBm	723	mA
	LTE-FDD B5 @ 22.87 dBm	713	mA
	LTE-FDD B8 @ 23.09 dBm	718	mA
	LTE-TDD B34 @ 23.03 dBm	365	mA
	LTE-TDD B38 @ 23.48 dBm	379	mA
	LTE-TDD B39 @ 23.07 dBm	344	mA
	LTE-TDD B40 @ 23.37 dBm	373	mA
	LTE-TDD B41 @ 23.24 dBm	376	mA

Table 39: Power Consumption of EC200A-EUV1

Description	Conditions	Typ.	Unit
OFF State	Power down	8.18	μA
Sleep State	**AT+CFUN=0** (USB disconnected)	1.71	mA
	AT+CFUN=0 (USB suspended)	1.83	mA
	AT+CFUN=4 (USB disconnected)	1.97	mA
	AT+CFUN=4 (USB suspended)	2.12	mA
	WCDMA @ PF = 64 (USB disconnected)	4.02	mA
	WCDMA @ PF = 64 (USB suspended)	4.18	mA
	WCDMA @ PF = 128 (USB disconnected)	3.10	mA
	WCDMA @ PF = 256 (USB disconnected)	2.67	mA
	WCDMA @ PF = 512 (USB disconnected)	2.49	mA
	LTE-FDD @ PF = 32 (USB disconnected)	3.78	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.92	mA
	LTE-FDD @ PF = 64 (USB suspended)	3.37	mA
	LTE-FDD @ PF = 128 (USB disconnected)	2.73	mA
	LTE-FDD @ PF = 256 (USB disconnected)	2.52	mA
	LTE-TDD @ PF = 32 (USB disconnected)	3.71	mA
	LTE-TDD @ PF = 64 (USB disconnected)	2.98	mA
	LTE-TDD @ PF = 64 (USB suspended)	3.10	mA
	LTE-TDD @ PF = 128 (USB disconnected)	2.72	mA
	LTE-TDD @ PF = 256 (USB disconnected)	2.51	mA
Idle State	WCDMA @ PF = 64 (USB disconnected)	21.93	mA
	WCDMA @ PF = 64 (USB connected)	41.81	mA
	LTE-FDD @ PF = 64 (USB disconnected)	21.59	mA

	LTE-FDD @ PF = 64 (USB connected)	41.22	mA
	LTE-TDD @ PF = 64 (USB disconnected)	21.57	mA
	LTE-TDD @ PF = 64 (USB connected)	41.24	mA
GPRS Data Transmission	EGSM900 4DL/1UL @ 32.70 dBm	257	mA
	EGSM900 3DL/2UL @ 32.71 dBm	452	mA
	EGSM900 2DL/3UL @ 31.02 dBm	544	mA
	EGSM900 1DL/4UL @ 29.18 dBm	590	mA
	DCS1800 4DL/1UL @ 29.51 dBm	173	mA
	DCS1800 3DL/2UL @ 29.51 dBm	287	mA
	DCS1800 2DL/3UL @ 27.77 dBm	340	mA
	DCS1800 1DL/4UL @ 25.79 dBm	368	mA
EDGE Data Transmission	EGSM900 4DL/1UL @ 28.17 dBm	193	mA
	EGSM900 3DL/2UL @ 27.82 dBm	316	mA
	EGSM900 2DL/3UL @ 25.74 dBm	382	mA
	EGSM900 1DL/4UL @ 23.77 dBm	436	mA
	DCS1800 4DL/1UL @ 26.29 dBm	166	mA
	DCS1800 3DL/2UL @ 26.34 dBm	274	mA
	DCS1800 2DL/3UL @ 24.76 dBm	359	mA
	DCS1800 1DL/4UL @ 22.25 dBm	440	mA
WCDMA Data Transmission	WCDMA B1 HSDPA @ 22.60 dBm	658	mA
	WCDMA B5 HSDPA @ 22.63 dBm	594	mA
	WCDMA B8 HSDPA @ 22.78 dBm	599	mA
	WCDMA B1 HSUPA @ 22.32 dBm	611	mA
	WCDMA B5 HSUPA @ 22.30 dBm	548	mA
	WCDMA B8 HSUPA @ 22.41 dBm	543	mA

LTE Data Transmission	LTE-FDD B1 @ 23.69 dBm	761	mA
	LTE-FDD B3 @ 23.41 dBm	752	mA
	LTE-FDD B5 @ 22.96 dBm	663	mA
	LTE-FDD B7 @ 23.10 dBm	771	mA
	LTE-FDD B8 @ 23.16 dBm	649	mA
	LTE-FDD B20 @ 22.82 dBm	650	mA
	LTE-FDD B28 @ 23.06 dBm	730	mA
	LTE-TDD B38 @ 23.71 dBm	364	mA
	LTE-TDD B40 @ 23.86 dBm	345	mA
	LTE-TDD B41 @ 23.64 dBm	366	mA

Table 40: Power Consumption of EC200A-ELV1

Description	Conditions	Typ.	Unit
OFF State	Power down	8.31	μA
Sleep State	**AT+CFUN=0** (USB disconnected)	7.85	mA
	AT+CFUN=0 (USB suspended)	1.52	mA
	AT+CFUN=4 (USB disconnected)	1.69	mA
	AT+CFUN=4 (USB suspended)	1.74	mA
	WCDMA @ PF = 64 (USB disconnected)	1.91	mA
	WCDMA @ PF = 64 (USB suspended)	1.83	mA
	WCDMA @ PF = 128 (USB disconnected)	2.92	mA
	WCDMA @ PF = 256 (USB disconnected)	2.51	mA
	WCDMA @ PF = 512 (USB disconnected)	2.24	mA
	LTE-FDD @ PF = 32 (USB disconnected)	3.58	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.81	mA

	LTE-FDD @ PF = 64 (USB suspended)	3.03	mA
	LTE-FDD @ PF = 128 (USB disconnected)	2.42	mA
	LTE-FDD @ PF = 256 (USB disconnected)	2.26	mA
	LTE-TDD @ PF = 32 (USB disconnected)	3.57	mA
	LTE-TDD @ PF = 64 (USB disconnected)	2.77	mA
	LTE-TDD @ PF = 64 (USB suspended)	2.96	mA
	LTE-TDD @ PF = 128 (USB disconnected)	2.41	mA
	LTE-TDD @ PF = 256 (USB disconnected)	2.14	mA
Idle State	WCDMA @ PF = 64 (USB disconnected)	22.17	mA
	WCDMA @ PF = 64 (USB connected)	41.91	mA
	LTE-FDD @ PF = 64 (USB disconnected)	21.70	mA
	LTE-FDD @ PF = 64 (USB connected)	41.32	mA
	LTE-TDD @ PF = 64 (USB disconnected)	21.70	mA
	LTE-TDD @ PF = 64 (USB connected)	41.34	mA
WCDMA Data Transmission	WCDMA B1 HSDPA @ 22.41 dBm	635	mA
	WCDMA B5 HSDPA @ 22.44 dBm	607	mA
	WCDMA B8 HSDPA @ 22.58 dBm	579	mA
	WCDMA B1 HSUPA @ 22.15 dBm	623	mA
	WCDMA B5 HSUPA @ 21.84 dBm	582	mA
	WCDMA B8 HSUPA @ 21.97 dBm	556	mA
LTE Data Transmission	LTE-FDD B1 @ 23.35 dBm	733	mA
	LTE-FDD B3 @ 23.58 dBm	727	mA
	LTE-FDD B5 @ 23.51 dBm	736	mA
	LTE-FDD B7 @ 23.01 dBm	846	mA
	LTE-FDD B8 @ 23.77 dBm	735	mA

	LTE-FDD B20 @ 23.09 dBm	627	mA
	LTE-FDD B28 @ 23.31 dBm	734	mA
	LTE-TDD B38 @ 23.78 dBm	362	mA
	LTE-TDD B40 @ 23.61 dBm	368	mA
	LTE-TDD B41 @ 23.68 dBm	362	mA

Table 41: Power Consumption of EC200A-AUV1

Description	Conditions	Typ.	Unit
OFF State	Power down	11.03	μA
Sleep State	**AT+CFUN=0** (USB disconnected)	1.59	mA
	AT+CFUN=0 (USB suspended)	1.80	mA
	AT+CFUN=4 (USB disconnected)	1.74	mA
	AT+CFUN=4 (USB suspended)	1.96	mA
	WCDMA @ PF = 64 (USB disconnected)	3.58	mA
	WCDMA @ PF = 64 (USB suspended)	3.73	mA
	WCDMA @ PF = 128 (USB disconnected)	2.62	mA
	WCDMA @ PF = 256 (USB disconnected)	2.34	mA
	WCDMA @ PF = 512 (USB disconnected)	2.10	mA
	LTE-FDD @ PF = 32 (USB disconnected)	3.34	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.58	mA
	LTE-FDD @ PF = 64 (USB suspended)	2.82	mA
	LTE-FDD @ PF = 128 (USB disconnected)	2.11	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.92	mA
	LTE-TDD @ PF = 32 (USB disconnected)	3.35	mA
	LTE-TDD @ PF = 64 (USB suspended)	2.68	mA

	LTE-TDD @ PF = 64 (USB suspended)	2.79	mA
	LTE-TDD @ PF = 128 (USB disconnected)	2.26	mA
	LTE-TDD @ PF = 256 (USB disconnected)	2.20	mA
Idle State	WCDMA @ PF = 64 (USB disconnected)	21.82	mA
	WCDMA @ PF = 64 (USB connected)	42.04	mA
	LTE-FDD @ PF = 64 (USB disconnected)	21.45	mA
	LTE-FDD @ PF = 64 (USB connected)	41.57	mA
	LTE-TDD @ PF = 64 (USB disconnected)	21.44	mA
	LTE-TDD @ PF = 64 (USB connected)	41.58	mA
GPRS Data Transmission	GSM850 4DL/1UL @ 32.70 dBm	295	mA
	GSM850 3DL/2UL @ 32.34 dBm	482	mA
	GSM850 2DL/3UL @ 30.95 dBm	585	mA
	GSM850 1DL/4UL @ 28.97 dBm	637	mA
	EGSM900 4DL/1UL @ 32.71 dBm	276	mA
	EGSM900 3DL/2UL @ 32.64 dBm	463	mA
	EGSM900 2DL/3UL @ 30.55 dBm	534	mA
	EGSM900 1DL/4UL @ 28.51 dBm	571	mA
	DCS1800 4DL/1UL @ 30.45 dBm	210	mA
	DCS1800 3DL/2UL @ 30.35 dBm	317	mA
	DCS1800 2DL/3UL @ 27.83 dBm	357	mA
	DCS1800 1DL/4UL @ 25.78 dBm	378	mA
	PCS1900 4DL/1UL @ 30.21 dBm	215	mA
	PCS1900 3DL/2UL @ 30.14 dBm	345	mA
	PCS1900 2DL/3UL @ 28.56 dBm	420	mA
	PCS1900 1DL/4UL @ 26.19 dBm	442	mA

EDGE Data Transmission	GSM850 4DL/1UL @ 27.62 dBm	222	mA
	GSM850 3DL/2UL @ 27.08 dBm	356	mA
	GSM850 2DL/3UL @ 24.55 dBm	494	mA
	GSM850 1DL/4UL @ 23.37 dBm	613	mA
	EGSM900 4DL/1UL @ 27.63 dBm	217	mA
	EGSM900 3DL/2UL @ 27.52 dBm	353	mA
	EGSM900 2DL/3UL @ 25.08 dBm	470	mA
	EGSM900 1DL/4UL @ 22.65 dBm	615	mA
	DCS1800 4DL/1UL @ 26.88 dBm	190	mA
	DCS1800 3DL/2UL @ 26.97 dBm	287	mA
	DCS1800 2DL/3UL @ 24.40 dBm	366	mA
	DCS1800 1DL/4UL @ 22.03 dBm	450	mA
	PCS1900 4DL/1UL @ 26.84 dBm	199	mA
	PCS1900 3DL/2UL @ 26.74 dBm	302	mA
	PCS1900 2DL/3UL @ 24.08 dBm	380	mA
	PCS1900 1DL/4UL @ 21.93 dBm	462	mA
WCDMA Data Transmission	WCDMA B1 HSDPA @ 22.13 dBm	615	mA
	WCDMA B2 HSDPA @ 22.15 dBm	654	mA
	WCDMA B4 HSDPA @ 22.13 dBm	602	mA
	WCDMA B5 HSDPA @ 22.21 dBm	564	mA
	WCDMA B8 HSDPA @ 22.45 dBm	530	mA
	WCDMA B1 HSUPA @ 21.84 dBm	564	mA
	WCDMA B2 HSUPA @ 21.94 dBm	601	mA
	WCDMA B4 HSUPA @ 21.99 dBm	552	mA
	WCDMA B5 HSUPA @ 21.90 dBm	519	mA

	WCDMA B8 HSUPA @ 22.04 dBm	479	mA
LTE Data Transmission	LTE-FDD B1 @ 23.11 dBm	776	mA
	LTE-FDD B2 @ 23.21 dBm	735	mA
	LTE-FDD B3 @ 22.98 dBm	742	mA
	LTE-FDD B4 @ 23.31 dBm	725	mA
	LTE-FDD B5 @ 23.12 dBm	651	mA
	LTE-FDD B7 @ 23.14 dBm	811	mA
	LTE-FDD B8 @ 23.07 dBm	643	mA
	LTE-FDD B28 @ 23.18 dBm	785	mA
	LTE-FDD B66 @ 23.2 dBm	743	mA
	LTE-TDD B40 @ 23.32 dBm	324	mA

6.4. Digital I/O Characteristics

Table 42: VDD_EXT I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	0.7 × VDD_EXT	VDD_EXT + 0.2	V
V_{IL}	Low-level input voltage	-0.3	0.3 × VDD_EXT	V
V_{OH}	High-level output voltage	VDD_EXT - 0.2	VDD_EXT	V
V_{OL}	Low-level output voltage	0	0.2	V

Table 43: (U)SIM High/Low-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	0.8 × USIM_VDD	USIM_VDD	V
V_{IL}	Low-level input voltage	-0.3	0.12 × USIM_VDD	V

V_{OH}	High-level output voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{OL}	Low-level output voltage	0	0.15 × USIM_VDD	V

Table 44: SDIO Low-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	0.7 × SD_SDIO_VDD	SD_SDIO_VDD + 0.2	V
V_{IL}	Low-level input voltage	-0.3	0.3 × SDIO_VDD	V
V_{OH}	High-level output voltage	SDIO_VDD - 0.2	SD_SDIO_VDD	V
V_{OL}	Low-level output voltage	0	0.2	V

Table 45: SDIO High-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	2.0	SD_SDIO_VDD + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.8	V
V_{OH}	High-level output voltage	2.4	SD_SDIO_VDD	V
V_{OL}	Low-level output voltage	0	0.3	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 46: Electrostatic Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±8	±10	kV

Antenna Interfaces	±5	±10	kV
Other Interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 47: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [7]	-35	+25	+75	°C
Extended Operating Temperature Range [8]	-40	-	+85	°C
Storage Temperature Range	-40	-	+90	°C

[7] Within this range, the module's indicators comply with 3GPP specification requirements.
[8] Within this range, the module retains the ability to establish and maintain functions such as SMS* and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

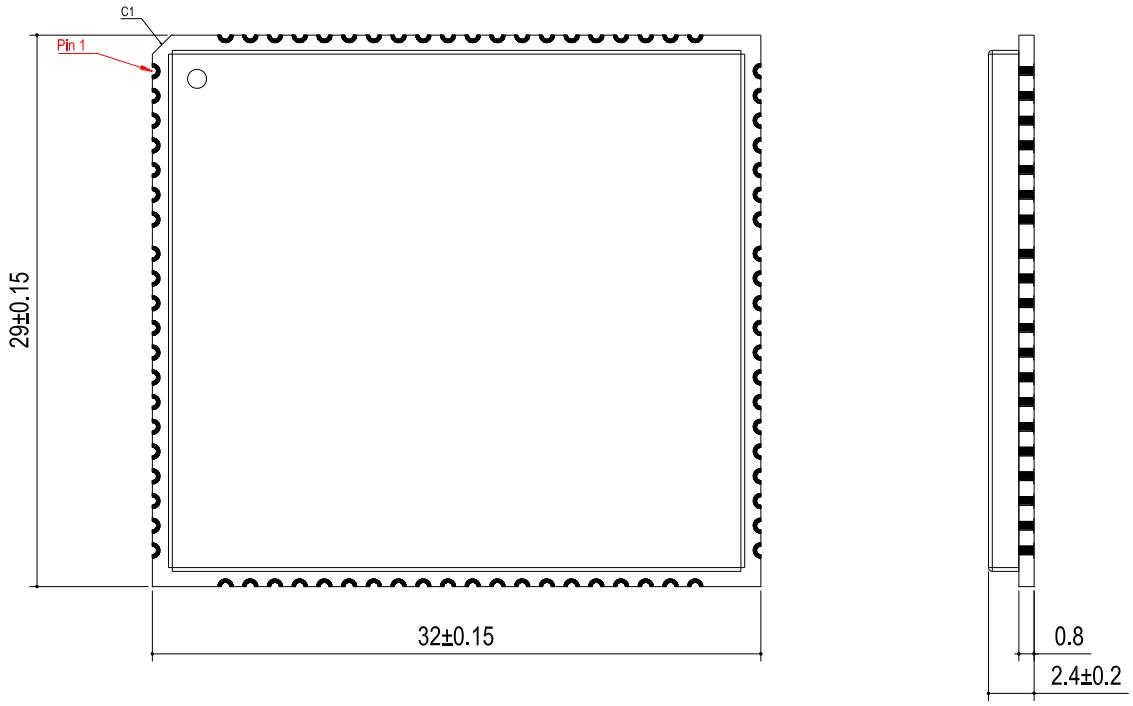


Figure 35: Top and Side Dimensions

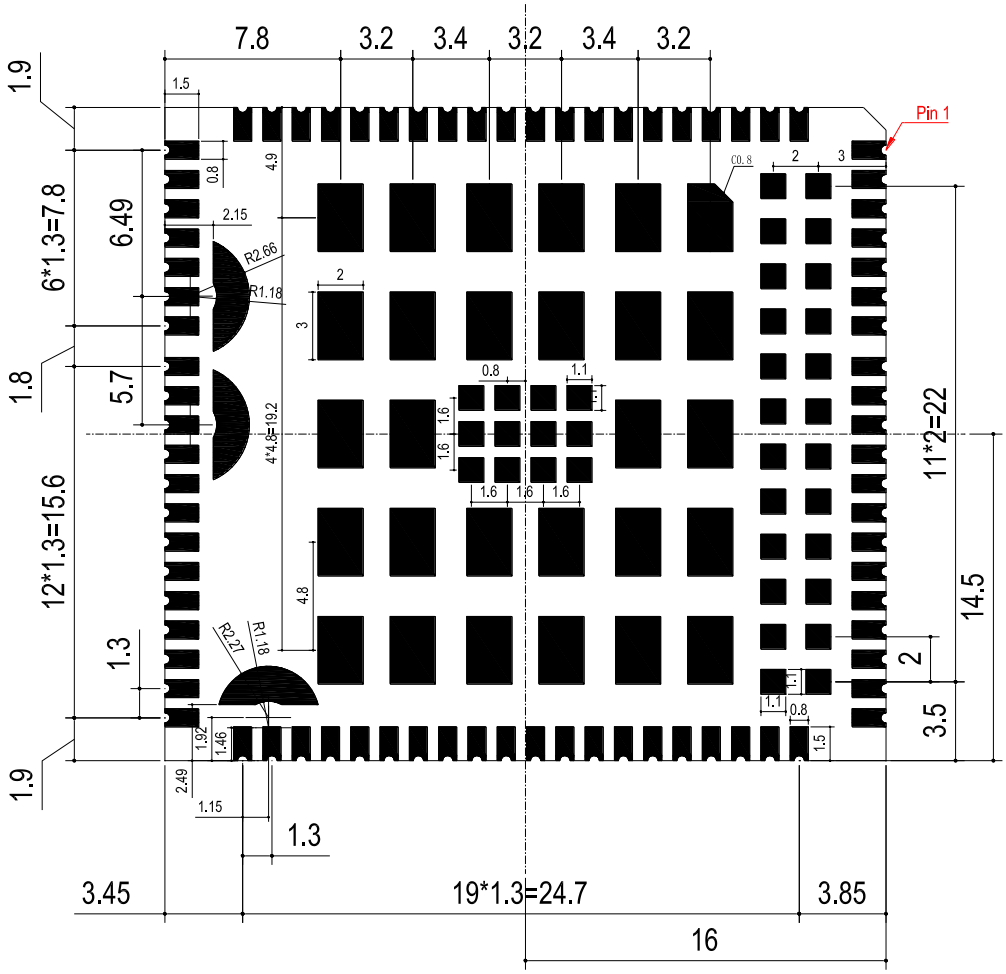


Figure 36: Bottom Dimension

NOTE

The module's coplanarity standard: ≤ 0.13 mm.

7.2. Recommended Footprint

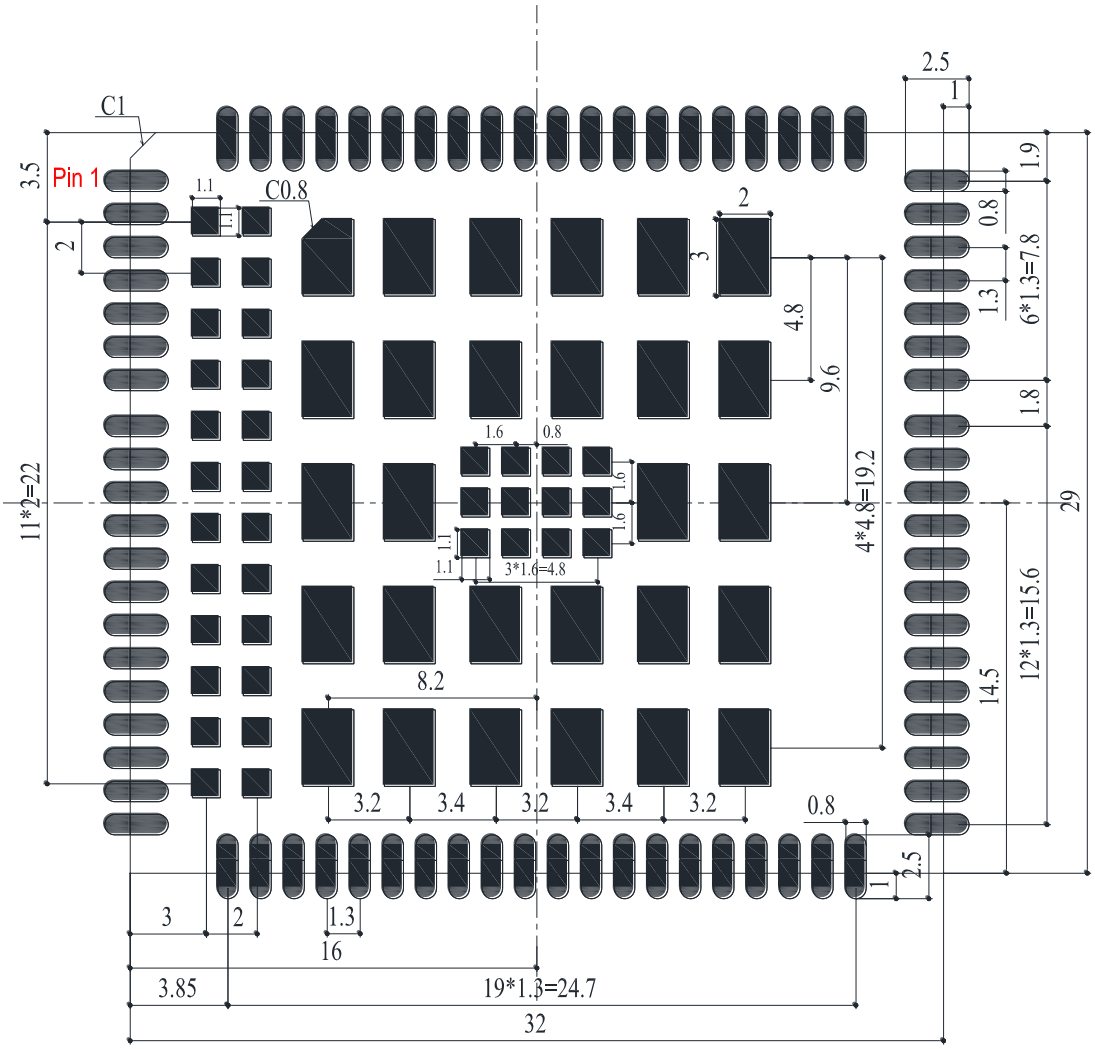


Figure 37: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

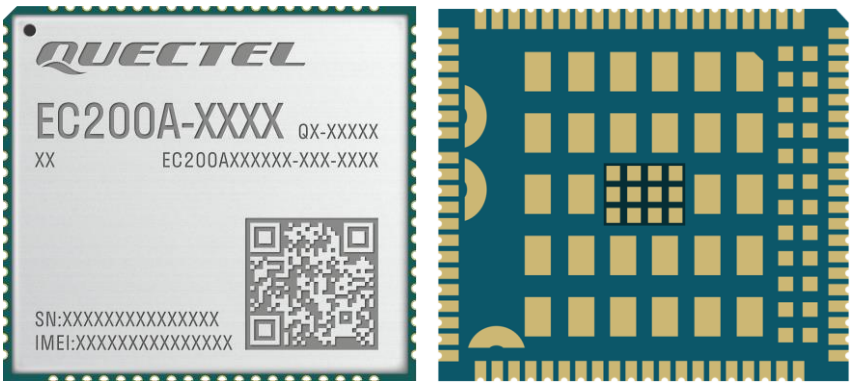


Figure 38: Top and Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [9] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 24 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[9] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.20 mm. For more details, see ***document [4]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below:

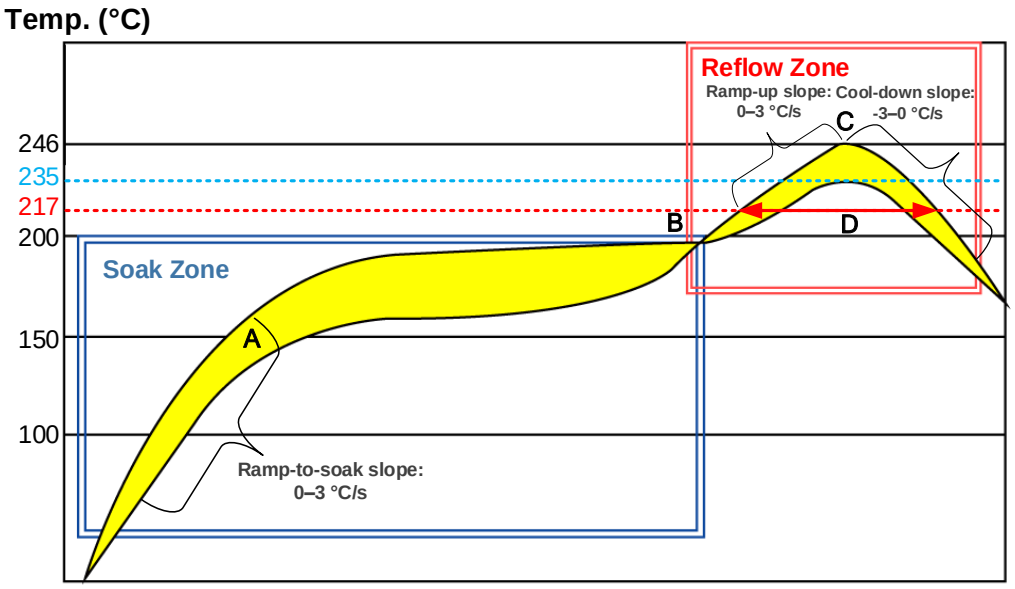


Figure 39: Recommended Reflow Soldering Thermal Profile

Table 48: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak Slope	0–3 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up Slope	0–3 °C/s
Reflow Time (D: over 217°C)	40–70 s
Max Temperature	235–246 °C
Cool-down Slope	-3–0 °C/s
Reflow Cycle	
Max Reflow Cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
8. Due to the complexity of the SMT process, contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering)

that is not mentioned in ***document [5]***.

8.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

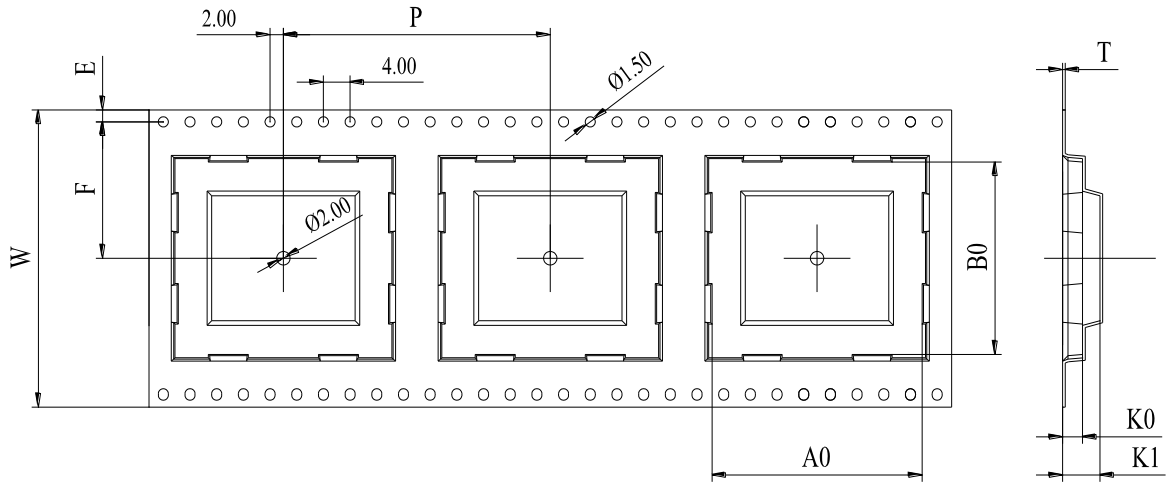


Figure 40: Carrier Tape Dimension Drawing (Unit: mm)

Table 49: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	44	0.35	32.5	29.5	3	3.8	20.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

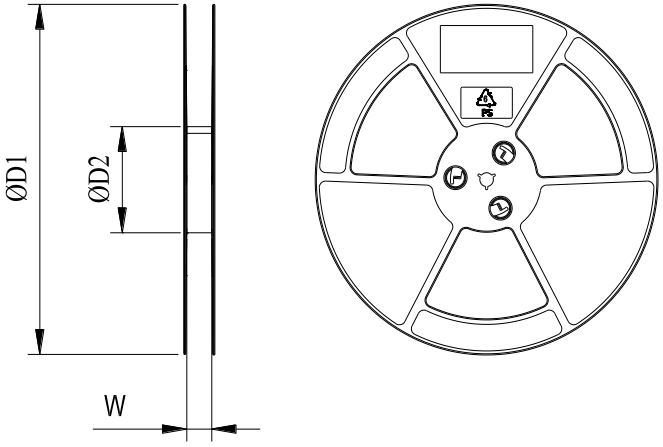


Figure 41: Plastic Reel Dimension Drawing

Table 50: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

8.3.3. Mounting Direction

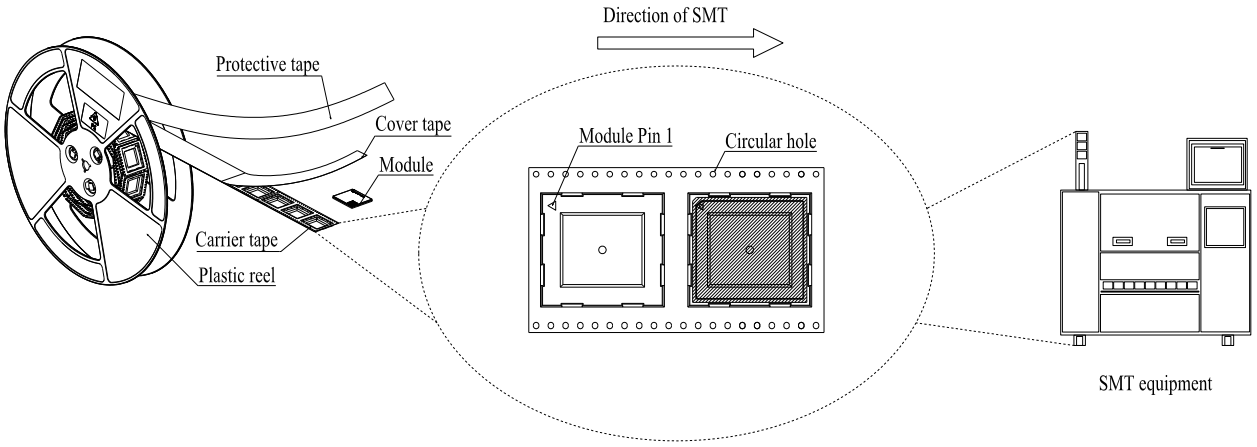
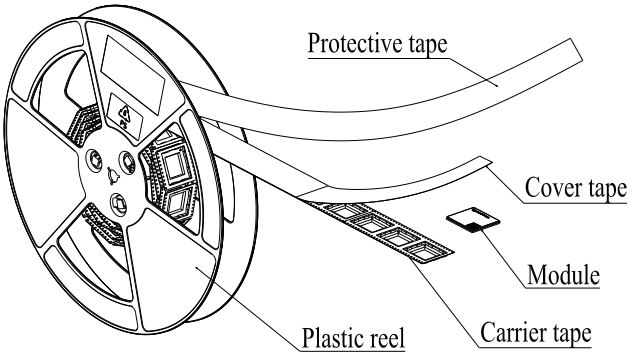


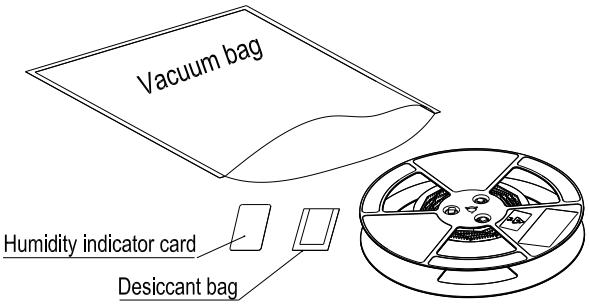
Figure 42: Mounting Direction

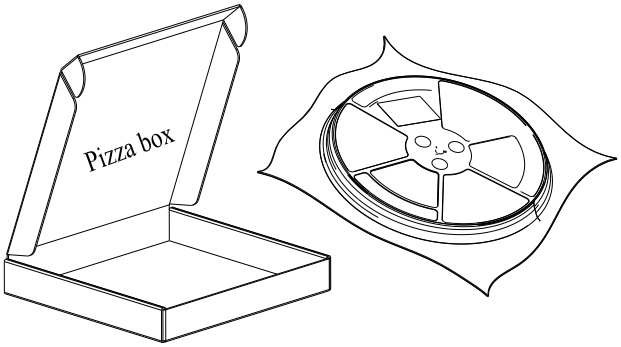
8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 1000 modules.

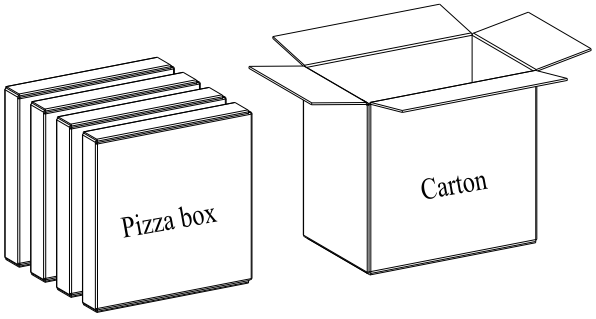


Figure 43: Packaging Process

9 Appendix References

Table 51: Related Documents

Document Name	
[1]	Quectel_UMTS&LTE_EVB_User_Guide
[2]	Quectel_EC200x&EC600M&EG800K&EG810M&EG91xN&EG912Y&EG950A_Series_AT_Commands_Manual
[3]	Quectel_RF_Layout_Application_Note
[4]	Quectel_Module_Stencil_Design_Requirements
[5]	Quectel_Module_SMT_Application_Note

Table 52: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
AMR	Adaptive Multi-Rate
bps	Bytes per second
CMUX	Connection Multiplexing
CS	Coding Scheme
CTS	Clear To Send
DFOTA	Delta Firmware Upgrade Over-The-Air
DRX	Discontinuous Reception
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
ESD	Electrostatic Discharge

EVB	Evaluation Board
FDD	Frequency Division Duplexing
FILE	File Protocol
FTP	File Transfer Protocol
FTPS	FTP over SSL
GMSK	Gaussian Filtered Minimum Shift Keying
GND	Ground
GSM	Global System for Mobile Communications
HSDPA	High Speed Downlink Packet Access
HSPA+	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
LGA	Land Grid Array
LTE	Long Term Evolution
MCS	Modulation and Coding Scheme
MMS	Multimedia Messaging Service
MQTT	Message Queuing Telemetry Transport
NITZ	Network Identity and Time Zone / Network Informed Time Zone.
NTP	Network Time Protocol
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PING	Packet Internet Groper
PPP	Point-to-Point Protocol
P_{PP}	Peak Pulse Power

PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RTS	Request To Send
SDIO	Secure Digital Input and Output Card
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
UDP	User Datagram Protocol
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnom	Nominal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum High-Level Input Voltage
V_{IH}min	Minimum High-Level Input Voltage
V_{IL}max	Maximum Low-Level Input Voltage
V_{IL}min	Minimum Low-Level Input Voltage
V_{OH}min	Minimum High-Level Output Voltage

V_{OL}max	Maximum Low-Level Output Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

FCC

Important Notice to OEM integrators

1.This module is limited to OEM installation ONLY.

2.This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).

3.The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations.

4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

Notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to XXXX that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: XMR2025EC200AAUV1” The FCC ID can be used only when all FCC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,

(2) The transmitter module may not be co-located with any other transmitter or antenna.

(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation

Band	MAX Gain (dBi)
GSM850	0.10
GSM1900	1.60
WCDMA Band II	1.60
WCDMA Band IV	1.10
WCDMA Band V	0.10
LTE Band 2	1.60
LTE Band 4	1.10
LTE Band 5	0.10
LTE Band 7	1.20
LTE Band 66	1.10

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24 and part 27 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions:(For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna. As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.