RG650E&RG650V Series
QuecOpen Hardware Design

5G Module Series

Version: 1.0

Date: 2024-01-29

Status: Released

At Quectel, our aim is to provide timely and comprehensive services to our customers. If you require any assistance, please contact our headquarters:

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2023-04-18	Iris MA/ Qiqi WANG/ Kun GE	Creation of the document
1.0	2024-01-29	Iris MA/ Qiqi WANG/ Aragorn QIAO Kun GE	First official release

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1 Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and price-performance ratio

The document defines RG650E and RG650V series modules in QuecOpen® solution and describes their air interfaces and hardware interfaces which are connected to your applications. This document can help you quickly understand interface specifications, RF characteristics, electrical and mechanical details, as well as other information of the module.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.

2 Product Overview

The module is an SMD module with compact packaging.

Table 2: Basic Information

RG650E & RG650V Series	
Packaging type	LGA
Pin counts	519
Dimensions	(46.0 ±0.2) mm × (53.0 ±0.2) mm × (3.05 ±0.2) mm
Weight	Approx. 17.3 g
Variants	RG650E-NA, RG650E-EU*, RG650V-NA, RG650V-EU

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

Wireless Network Type	RG650E-NA RG650V-NA	RG650E-EU* RG650V-EU
5G NR	n2/n5/n7/n12/n13/n14/n25/n26/n29/n30/ n38/n41/n48/n66/n70/n71/n77/n78	n1/n3/n5/n7/n8/n20/n26/n28/n38/n40/n41/ n71 (optional)/n75n76/n77/n78
LTE-FDD	B2/B4/B5/B7/B12/B13/B14/B17/B25/B26/ B29/B30/B66/B71	B1/B3/B5/B7/B8/B20/B28/B32/B71 (optional)
LTE-TDD	B38/B41/B42/B43/B48	B38/B40/B41/B42/B43
WCDMA	-	B1/B5/B8
GNSS (Optional)	GPS/GLONASS/BDS/Galileo/QZSS	GPS/GLONASS/BDS/Galileo/QZSS

2.2. Key Features

Table 4: Key Features

Feature	Details
Supply Voltage	● 3.3–4.4 V ● Typ.: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
USB Interface	● Complies with USB 3.1 and 2.0 specifications ● Data rates: – USB 2.0: up to 480 Mbps – USB 3.1 Gen 1: up to 5 Gbps – USB 3.1 Gen 2: up to 10 Gbps ● Use: AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB* ● USB serial drivers for USB drivers under Windows 7/8/8.1/10/11, Linux 2.6–6.5 and Android 4.x–13.x ● Supports OTG function*
Forced Download Interface	USB_BOOT
(U)SIM Interfaces	● (U)SIM1: 1.8/3.0 V (U)SIM; (U)SIM2: 1.8 V eSIM ● Dual SIM Single Standby ● Complies with ETSI and IMT-2000 requirements
UART Interfaces	**Main UART interface*:** ● Use: data transmission ● Baud rate: 115200 bps ● RTS and CTS hardware flow control **Debug UART interface:** ● Use: Linux console and log output ● Baud rate: 115200 bps **Bluetooth UART interface*:** ● Use: Bluetooth communication ● Baud rate: 115200 bps ● RTS and CTS hardware flow control
Audio Features*	● One digital audio interface ● WCDMA: AMR and AMR-WB ● LTE: AMR and AMR-WB ● Echo cancellation and noise suppression

PCM Interfaces*	● Two PCM interfaces: one is used for SLIC or codec, and the other is only used for Bluetooth audio ● Supports 16-bit linear data format ● Long and short frame synchronization ● Master and slave modes (but must be in master mode for long frame synchronization)
I2C Interfaces	● Two I2C interfaces: one is used for general I2C, and the other is used for TP I2C ● Complies with version 3.0 of I2C-bus specification
ADC Interfaces	Two ADC interfaces
USXGMII Interfaces	● Two USXGMII interfaces ● 100 Mbps, 1000 Mbps, 2500 Mbps, 5000 Mbps and 10000 Mbps Ethernet connection in full duplex mode ● *IEEE 802.3* compliant ● Max. data rates: – DL: 10 Gbps – UL: 10 Gbps
LCM Interface*	Supports SPI LCM
Touch Panel Interface*	Supports I2C TP
PCIe Interfaces	● Three PCIe interfaces ● Complies with *PCI Express Base Specification Revision 3.0* ● Data rate at 8 Gbps per lane for PCIe 3.0 ● PCIe0 and PCIe1 support 2 lanes, and PCIe2 supports 1 lane ● PCIe0 supports RC and EP modes, but PCIe1 and PCIe2 only support RC mode ● Use: connect to an external Ethernet IC (MAC and PHY) or Wi-Fi IC
SPIs	● Two SPIs: one is used for general SPI, and the other is used for LCM SPI ● Supports master mode only ● 1.8 V power domain ● Clock rate: up to 50 MHz
Network Indication	**NET_MODE:** ● Use: network registration status indication **NET_STATUS:** ● Use: network activity status indication
AT Commands	● Complies with the AT commands defined in *3GPP TS 27.007* and *3GPP TS 27.005* ● Complies with Quectel enhanced AT commands
Rx-diversity	5G NR, LTE and WCDMA [1]
Antenna Interfaces	● Cellular antenna interfaces (ANT0–ANT7)

[1] WCDMA is only supported by RG650E-EU* and RG650V-EU.

	• GNSS antenna interface (ANT_GNSS) • 50 Ω characteristic impedance
Transmitting Power	• 5G NR bands for HPUE: Class 2 (26 dBm +2/-3 dB) [2] – **RG650E-NA/RG650V-NA:** n2/n5/n7/n25/n38/n41/n66/n71/n77/n78 – **RG650E-EU*/RG650V-EU:** n1/n3/n5/n7/n28/n38/n40/n41/n77/n78 • 5G NR n38/n41/n77/n78: Class 1.5 (29 dBm +2/-3 dB) • 5G NR other Sub-6 bands: Class 3 (23 dBm ±2 dB) • LTE B38/B41/B42/B43 for HPUE [3]: Class 2 (26 dBm +2/-3 dB) • LTE other bands: Class 3 (23 dBm ±2 dB) • WCDMA [1]: Class 3 (23 dBm ±2 dB)
5G NR Features	• The module complies with 3GPP Rel-17 specification • DL modulations: QPSK, 16QAM, 64QAM and 256QAM • UL modulations: π/2-BPSK, QPSK, 16QAM, 64QAM and 256QAM • DL 4 × 4 MIMO – **RG650E-NA/RG650V-NA:** n2/n5/n7/n12/n13/n14/n25/n26/n29/n30/n38/n41/n48/n66/n70/n71/n77/n78 – **RG650E-EU*/RG650V-EU:** n1/n3/n5/n7/n8/n20/n26/n28/n38/n40/n41/n71(optional)/n75/n76*/n77/n78 • UL 2 × 2 MIMO [4] – **RG650E-NA/RG650V-NA:** n2/n5/n7/n25/n38/n41/n48/n66/n70/n71/n77/n78 – **RG650E-EU*/RG650V-EU:** n1/n3/n5/n7/n28/n38/n40/n41/n77/n78 • SCS: – FDD: 15 kHz – TDD: 30 kHz NSA and SA: • Option 3x, Option 3a, Option 3 and Option 2 • NSA max. data rates [5]: – **RG650E-NA/RG650E-EU*:** Max. 5.47 Gbps (DL)/730 Mbps (UL) – **RG650V-NA/RG650V-EU:** Max. 4.52 Gbps (DL)/730 Mbps (UL) • SA max. data rates [5]: – **RG650E-NA/RG650E-EU*:** Max. 7.01 Gbps (DL)/1.25 Gbps (UL)

[2] n1/n3/n5/n7/n28/n40 HPUE of RG650E-EU*/RG650V-EU and n2/n5/n7/n25/n66/n71 HPUE of RG650E-NA/RG650V-NA are achieved via dual Tx. Each Tx chain can only support Class 3 (23 dBm ±2 dB).
[3] LTE HPUE is only for single carrier.
[4] UL 2 × 2 MIMO is only supported in 5G SA mode.
[5] The maximum rates are theoretical and the actual values depend on the network configuration.

	– **RG650V-NA/RG650V-EU:** Max. 4.67 Gbps (DL)/1.25 Gbps (UL) ● SRS: – **RG650E-NA/RG650V-NA:** NSA: 1T4R (n38/n41/n48/n77/n78) SA: 2T4R (n38/n41/n48/n77/n78) – **RG650E-EU*/RG650V-EU:** NSA: 1T4R (n38/n40/n41/n77/n78) SA: 2T4R (n38/n40/n41/n77/n78)
LTE Features	● The module complies with 3GPP Rel-17 FDD and TDD ● Max. LTE categories: – DL CA: Cat 20 – UL CA: Cat 18 ● 1.4/3/5/10/15/20 MHz RF bandwidths ● DL modulations: QPSK, 16QAM, 64QAM and 256QAM ● UL modulations: QPSK, 16QAM, 64QAM and 256QAM ● DL 4 × 4 MIMO – **RG650E-NA/RG650V-NA:** B2/B4/B5/B7/B12/B13/B14/B17/B25/B26/B29/B30/B38/B41/B42/B43/B48/B66/B71 – **RG650E-EU*/RG650V-EU:** B1/B3/B5/B7/B8/B20/B28/B32/B38/B40/B41/B42/B43/B71(optional) ● LTE max. data rates [5]: – DL: 2.0 Gbps – UL: 211 Mbps
UMTS Features [1]	● The module complies with 3GPP Rel-17 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA ● Modulations: QPSK, 16QAM and 64QAM ● DC-HSDPA max. data rate [5]: 42 Mbps (DL) ● HSUPA max. data rate [5] : 5.76 Mbps (UL) ● WCDMA max. data rates [5]: – DL: 384 kbps – UL: 384 kbps
GNSS Features (Optional)	● GPS, GLONASS, BDS, Galileo and QZSS ● Triple-band GNSS: L1, L2 and L5 ● The module complies with NMEA 0183 protocol ● The data update rate is 1 Hz by default

Internet Protocol Features	● The module complies with NITZ, PING, QMI protocols ● The module supports PAP and CHAP for PPP connections
Temperature Ranges	● Normal operating temperature [6]: -30 °C to +75 °C ● Extended operating temperature [7]: -40 °C to +85 °C ● Storage temperature: -40 °C to +90 °C
Firmware Upgrade	● USB 2.0 and 3.1 interface ● FOTA
RoHS	All hardware components are fully complying with EU RoHS directive

[6] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heat sinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

[7] To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module retains the ability to establish and maintain functions such as voice, SMS, emergency call, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

2.3. Functional Diagram

The functional diagram illustrates the following major functional parts:

- Power management
- Baseband part
- DDR + EMMC flash
- Radio frequency part
- Peripheral interfaces

2.4. Pin Assignment

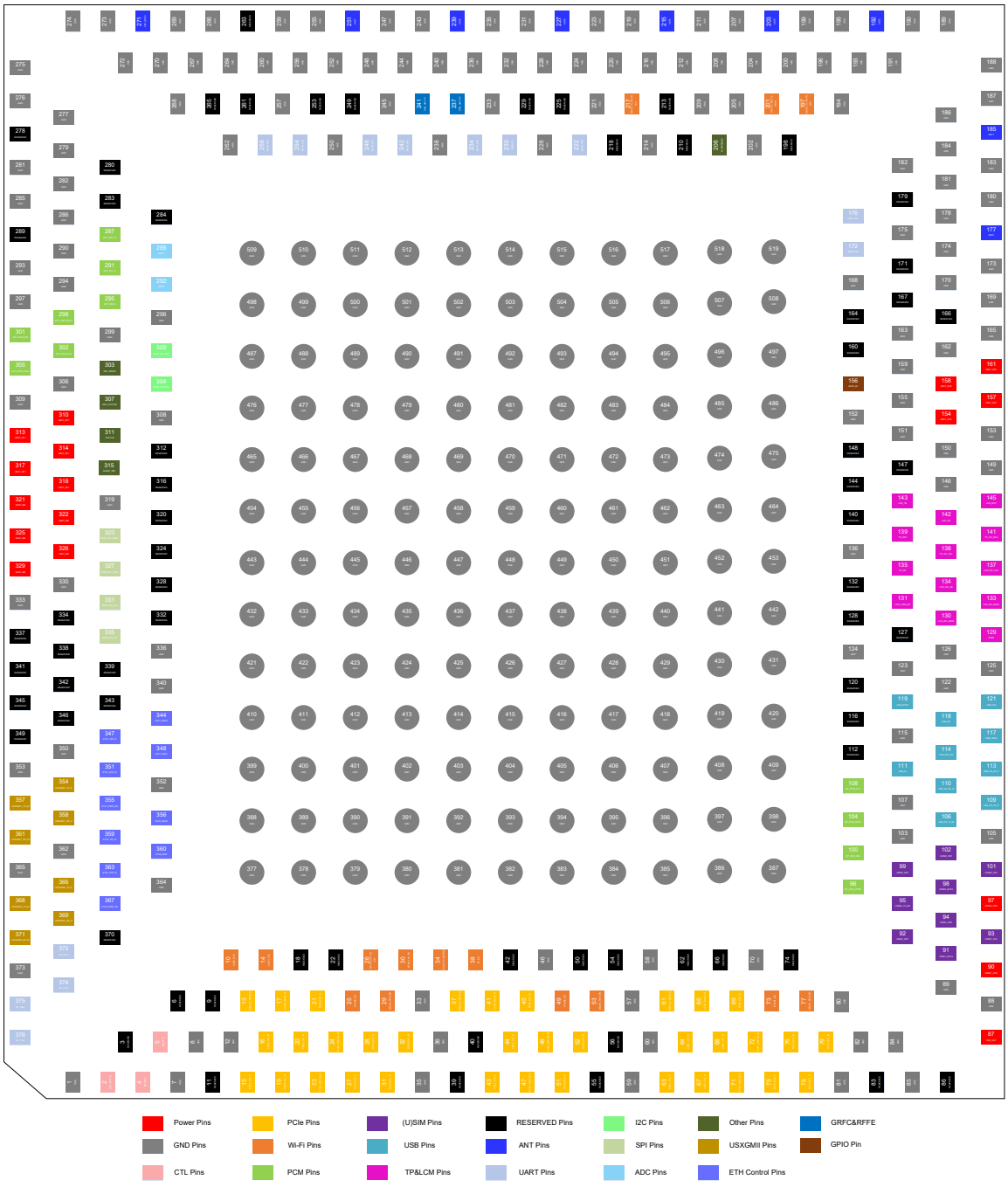


Figure 2: Pin Assignment (Top View)

NOTE

1. Keep all RESERVED pins and unused pins unconnected.
2. All GND pins should be connected to ground.

3. Ensure that the pull-up power supply of the module's pins is VDD_EXT or controlled by VDD_EXT, and there is no current sink on the module's pins before the module turns on. For more details, contact Quectel Technical Support.

2.5. Pin Description

Table 5: Parameter Definition

Parameter	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	321, 322, 325, 326, 329	PI	Power supply for the module’s BB part	Vmax = 4.4 V Vmin = 3.3 V Vnom = 3.8 V	
VBAT_RF1	310, 313, 314, 317, 318	PI	Power supply for the module’s RF part		

VBAT_RF2	154, 157, 158, 161	PI	Power supply for the module's RF part		
VDD_EXT	87	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V	Power supply for external GPIO's pull-up circuits. A test point is recommended to be reserved.
USIM1_VDD	90	PO	(U)SIM1 card power supply		Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module. If unused, keep it open.
USIM2_VDD	97	PO	(U)SIM2 card power supply		1.8 V eSIM is supported and can be identified automatically by the module. If unused, keep it open.
GND	1, 7, 8, 12, 33, 35, 36, 46, 57, 58, 59, 60, 70, 80, 81, 82, 84, 85, 88, 89, 103, 105, 107, 115, 122, 123, 124, 125, 126, 136, 146, 149, 150, 151, 152, 153, 155, 159, 162, 163, 165, 168, 169, 170, 173, 174, 175, 178, 180, 181, 182, 183, 184, 186, 187, 188, 189, 190, 191, 193, 194, 195, 196, 199, 200, 202, 204, 205, 207, 208, 209, 211, 212, 214, 216, 219, 220, 221, 223, 224, 226, 228, 231, 232, 233, 235, 236, 238, 240, 243, 244, 245, 247, 248, 250, 252, 255, 256, 257, 259, 260, 262, 264, 266, 267, 268, 269, 270, 272–277, 279, 281, 282, 285, 286, 290, 293, 294, 296, 297, 299, 306, 308, 309, 319, 330, 333, 336, 340, 350, 352, 353, 362, 364, 365, 373, 377–519				

Turn On/Off & Other Control Signals

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PWRKEY	4	DI	Turn on/off the module	0.7 V high level	Active low.
RESET_N	5	DI	Reset the module	1.2 V high level	Active low. A test point is recommended to be reserved if unused.

CBL_PWR_N	2	DI	Initiate power on when grounded		Internally pulled up to 1.8 V. Active low.
USB_BOOT	119	DI	Force the module into download mode	VDD_EXT	A test point is recommended to be reserved.
W_DISABLE#	206	DI	Airplane mode control	VDD_EXT	
Indication Signals					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	311	DO	Indicate the module's operation status	VDD_EXT	
NET_STATUS	307	DO	Indicate the module's network activity status	1.8 V	
SLEEP_IND	315	DO	Indicate the module’s sleep mode	VDD_EXT	
NET_MODE	303	DO	Indicate the module’s network registration mode		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	117	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.3 V Vnom = 5.0 V	Used for USB connection detection only, not for power supply. A test point must be reserved.
USB_DP	118	AIO	USB differential data (+)		Require differential impedance of 90 Ω. Test points must be reserved.
USB_DM	121	AIO	USB differential data (-)		
USB_SS_TX_P	109	AO	USB 3.1 SuperSpeed transmit (+)		Require differential impedance of

USB_SS_TX_M	106	AO	USB 3.1 SuperSpeed transmit (-)		90 Ω. If unused, keep them open.
USB_SS_RX_P	113	AI	USB 3.1 SuperSpeed receive (+)		
USB_SS_RX_M	110	AI	USB 3.1 SuperSpeed receive (-)		
USB_ID*	111	DI	USB ID detect	1.2 V	High level by default.
OTG_PWR_EN*	114	DO	OTG power control	1.8 V	
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_DATA	91	DIO	(U)SIM1 card data	1.8/3.0 V	
USIM1_CLK	93	DO	(U)SIM1 card clock		
USIM1_RST	94	DO	(U)SIM1 card reset		
USIM1_DET	92	DI	(U)SIM1 card hot-plug detect	VDD_EXT	If unused, keep it open.
USIM2_DATA	98	DIO	(U)SIM2 card data	1.8 V	
USIM2_CLK	101	DO	(U)SIM2 card clock		
USIM2_RST	102	DO	(U)SIM2 card reset		
USIM2_DET	99	DI	(U)SIM2 card hot-plug detect	VDD_EXT	If unused, keep it open.
USIM2_LS_EN	95	DO	(U)SIM2 level-shifting enable	1.8 V	
Main UART Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_CTS	246	DO	Clear to send signal from the module	VDD_EXT	Connect to the MCU's CTS.
MAIN_RTS	242	DI	Request to send signal to the module		Connect to the MCU's RTS.
MAIN_RXD	258	DI	Main UART receive		
MAIN_TXD	254	DO	Main UART transmit		

MAIN_RI	230	DO	Main UART ring indication		
MAIN_DTR	234	DI	Main UART data terminal ready		
MAIN_DCD	222	DO	Main UART data carrier detect		
Bluetooth UART Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BT_TXD	376	DO	Bluetooth UART transmit	1.2/1.8 V	1.8 V power domain by default.
BT_RXD	375	DI	Bluetooth UART receive		
BT_RTS	372	DI	Request to send signal to the module		Connect to the MCU's RTS. 1.8 V power domain by default.
BT_CTS	374	DO	Clear to send signal from the module		Connect to the MCU's CTS. 1.8 V power domain by default.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	172	DI	Debug UART receive	VDD_EXT	Test points must be reserved.
DBG_TXD	176	DO	Debug UART transmit		
I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_I2C_SCL	304	OD	I2C serial clock	VDD_EXT	Pull each of them up to VDD_EXT with an external 2.2 kΩ resistor. If unused, keep them open.
MAIN_I2C_SDA	300	OD	I2C serial data		
PCM Interfaces*					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
EXT_PCM_SYNC	305	DIO	PCM data frame sync	VDD_EXT	In master mode, it is an output signal. In slave mode, it is an input signal. Only used for SLIC and codec.
EXT_PCM_CLK	302	DIO	PCM clock		
EXT_PCM_DIN	301	DI	PCM data input		Only used for SLIC and codec.
EXT_PCM_DOUT	298	DO	PCM data output		
BT_PCM_SYNC	96	DIO	Bluetooth PCM data frame sync	1.2/1.8 V	Only used for Bluetooth audio. 1.8 V power domain by default. If unused, keep them open.
BT_PCM_CLK	108	DIO	Bluetooth PCM clock		
BT_PCM_DIN	100	DI	Bluetooth PCM data input		
BT_PCM_DOUT	104	DO	Bluetooth PCM data output		
EXT_MCLK	295	DO	Clock output for codec	VDD_EXT	If unused, keep them open.
EXT_RST_N	287	DO	External audio reset		
EXT_INT_N	291	DI	External audio interrupt		
PCIe Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE0_REFCLK_M	24	AIO	PCIe0 reference clock (-)		In RC mode, it is an output signal. In EP mode, it is an input signal. Require differential impedance of 100 Ω.
PCIE0_REFCLK_P	23	AIO	PCIe0 reference clock (+)		
PCIE0_RX0_M	28	AI	PCIe0 receive 0 (-)		Require differential impedance of 85 Ω.
PCIE0_RX0_P	27	AI	PCIe0 receive 0 (+)		
PCIE0_TX0_M	16	AO	PCIe0 transmit 0 (-)		

PCIE0_TX0_P	15	AO	PCIe0 transmit 0 (+)		If unused, keep them open.
PCIE0_RX1_M	32	AI	PCIe0 receive 1 (-)		
PCIE0_RX1_P	31	AI	PCIe0 receive 1 (+)		
PCIE0_TX1_M	20	AO	PCIe0 transmit 1 (-)		
PCIE0_TX1_P	19	AO	PCIe0 transmit 1 (+)		
PCIE0_RST_N	21	DIO	PCIe0 reset	1.2/1.8 V	1.8 V power domain by default. In RC mode, it is an output signal. In EP mode, it is an input signal.
PCIE0_WAKE_N	17	OD	PCIe0 wake up		1.8 V power domain by default. In RC mode, it is an input signal. In EP mode, it is an output signal.
PCIE0_CLKREQ_N	13	OD	PCIe0 clock request		
PCIE1_REFCLK_M	72	AO	PCIe1 reference clock (-)		Require differential impedance of 100 Ω.
PCIE1_REFCLK_P	71	AO	PCIe1 reference clock (+)		
PCIE1_RX0_M	76	AI	PCIe1 receive 0 (-)		Require differential impedance of 85 Ω. If unused, keep them open.
PCIE1_RX0_P	75	AI	PCIe1 receive 0 (+)		
PCIE1_TX0_M	64	AO	PCIe1 transmit 0 (-)		
PCIE1_TX0_P	63	AO	PCIe1 transmit 0 (+)		
PCIE1_RX1_M	79	AI	PCIe1 receive 1 (-)		
PCIE1_RX1_P	78	AI	PCIe1 receive 1 (+)		
PCIE1_TX1_M	68	AO	PCIe1 transmit 1 (-)		
PCIE1_TX1_P	67	AO	PCIe1 transmit 1 (+)		
PCIE1_RST_N	69	DO	PCIe1 reset	VDD_EXT	In RC mode, it is an output signal.
PCIE1_WAKE_N	65	OD	PCIe1 wake up		In RC mode, it is

PCIE1_CLKREQ_N	61	OD	PCIe1 clock request		an input signal.
PCIE2_REFCLK_M	48	AO	PCIe2 reference clock (-)		Require differential impedance of 100 Ω.
PCIE2_REFCLK_P	47	AO	PCIe2 reference clock (+)		
PCIE2_RX0_M	52	AI	PCIe2 receive 0 (-)		Require differential impedance of 85 Ω. If unused, keep them open.
PCIE2_RX0_P	51	AI	PCIe2 receive 0 (+)		
PCIE2_TX0_M	44	AO	PCIe2 transmit 0 (-)		
PCIE2_TX0_P	43	AO	PCIe2 transmit 0 (+)		
PCIE2_RST_N	45	DO	PCIe2 reset	VDD_EXT	In RC mode, it is an output signal.
PCIE2_WAKE_N	41	OD	PCIe2 wake up		In RC mode, it is an input signal.
PCIE2_CLKREQ_N	37	OD	PCIe2 clock request		
WWAN/WLAN Application Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN0_EN	25	DO	WLAN 5 GHz function enable control	1.2/1.8 V	1.8 V power domain by default.
WLAN0_PWR_EN	29	DO	WLAN 5 GHz power supply enable control	VDD_EXT	
WLAN1_EN	73	DO	WLAN 6 GHz function enable control		
WLAN1_PWR_EN	77	DO	WLAN 6 GHz power supply enable control		
WLAN2_EN	49	DO	WLAN 2.4 GHz function enable control		
WLAN2_PWR_EN	53	DO	WLAN 2.4 GHz power supply enable control		
BT_EN	38	DO	Bluetooth enable control	1.8 V	
WLAN_TX_EN_TO_LAA	217	DI	Notification from WLAN to LAA LNA	VDD_EXT	

			when WLAN transmitting to set LAA LNA to isolation mode		
WLAN_TX_EN_TO_N79	197	DI	Notification from WLAN to n79 LNA when WLAN transmitting to set n79 LNA to isolation mode		These pins are used for the coexistence of n79 and Wi-Fi 5 GHz. If n79 is needed in your future project with Quectel 5G modules, then these pins shall be pulled out and reserved; otherwise, these pins can be NC.
N79_TX_EN_TO_WLAN	201	DO	Notification from transceiver to WLAN when n79 transmitting to set WLAN 5G to isolation mode		
WLAN_LAA_RX	30	DO	SoC signal to set 5G xLNA to high gains or high isolation when both chains (LAA and 5G WLAN) are active simultaneously. No individual control for each chain.		
WLAN_LAA_AS_EN	26	DO	GPIO allows transceiver to power on monitoring for Wi-Fi SoC when WLAN is sleeping or disabled. Additionally, the control logic in WLAN AON domain allows transceiver to control 5G WLAN xLNA (LNA in FEMs)	1.2 V	
WLAN_PA_MUTING	34	DO	GPIO from SDX to disable WLAN PA		
COEX_TXD	14	DO	Coexistence UART transmit	1.2/1.8 V	Only for Qualcomm

COEX_RXD	10	DI	Coexistence UART receive		platform. Signal interface used for WWAN/WLAN coexistence mechanism. 1.8 V power domain by default.
LCM Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LCD_SPI_MISO	133	DI	LCD SPI master-in slave-out	VDD_EXT	Master mode only.
LCD_SPI_CS	134	DO	LCD SPI chip select		
LCD_SPI_CLK	137	DO	LCD SPI clock		
LCD_SPI_MOSI	130	DO	LCD SPI master-out slave-in		
PWM	129	DO	LCD backlight enable	1.8 V	If the default function is unused, it can be used for PWM output.
LCD_RS	142	DO	LCD data/command selection	VDD_EXT	
LCD_TE	143	DI	LCD tearing effect		
LCD_RST	145	DO	LCD reset		
LCD_PWR_EN	131	DO	LCD and TP power supply enable control		
Touch Panel Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TP_RST	139	DO	TP reset	VDD_EXT	
TP_INT	135	DI	TP interrupt		
TP_I2C_SCL	138	OD	TP I2C serial clock		Pull each of them up to VDD_EXT with an external
TP_I2C_SDA	141	OD	TP I2C serial data		

					2.2 kΩ resistor. If unused, keep them open.
ETH Control Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ETH0_MDIO	356	DIO	Ethernet PHY0 MDIO data	VDD_EXT	
ETH0_MDC	360	DO	Ethernet PHY0 MDIO clock		
ETH0_INT_N	359	DI	Ethernet PHY0 interrupt		
ETH0_RST_N	363	DO	Ethernet PHY0 reset		
ETH0_PWR_EN	367	DO	Ethernet PHY0 power supply enable control		
ETH1_MDIO	344	DIO	Ethernet PHY1 MDIO data		
ETH1_MDC	348	DO	Ethernet PHY1 MDIO clock		
ETH1_INT_N	347	DI	Ethernet PHY1 interrupt		
ETH1_RST_N	351	DO	Ethernet PHY1 reset		
ETH1_PWR_EN	355	DO	Ethernet PHY1 power supply enable control		
USXGMII Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USXGMII0_TX_M	368	AO	USXGMII0 transmit (-)		Require differential impedance of 100 Ω. If unused, keep them open.
USXGMII0_TX_P	366	AO	USXGMII0 transmit (+)		
USXGMII0_RX_P	369	AI	USXGMII0 receive (+)		
USXGMII0_RX_M	371	AI	USXGMII0 receive (-)		
USXGMII1_RX_P	358	AI	USXGMII1 receive (+)		
USXGMII1_RX_M	361	AI	USXGMII1 receive		

			(-)	
USXGMII1_TX_P	354	AO	USXGMII1 transmit (+)	
USXGMII1_TX_M	357	AO	USXGMII1 transmit (-)	
Antenna Interfaces for RG650E-NA/RG650V-NA [8]				
Pin Name	**Pin No.**	**I/O**	**Description**	**Comment**
ANT1	185	AIO	**Antenna 1 interface:** - **5G NR**: n41 TRX1 & n77/n78 TRX0 - **LTE**: LMB_TRX0 & HB_DRX & UHB_TRX0 - **Refarming**: LMB_TRX0 & HB_TRX1	50 Ω impedance.
ANT3	203	AIO	**Antenna 3 interface:** - **5G NR**: n41 DRX MIMO & n77/n78 PRX MIMO - **LTE**: LMB_PRX MIMO & HB_DRX MIMO & UHB_PRX MIMO **Refarming**: LMB_PRX MIMO & HB_DRX MIMO	
ANT5	227	AIO	**Antenna 5 interface:** - **5G NR**: n41 PRX MIMO & n77/n78 DRX MIMO - **LTE**: LMB_DRX MIMO & HB_PRX MIMO & UHB_DRX MIMO **Refarming**: LMB_DRX MIMO & HB_PRX MIMO	
ANT7	251	AIO	**Antenna 7 interface:** - **5G NR**: n41 TRX0 & n77/n78 TRX1 - **LTE**: LMB_TRX1 & HB_TRX0 & UHB_TRX1 - **Refarming**: LMB_TRX1 & HB_TRX0	
ANT0	177	AIO	**Antenna 0 interface:** - **5G NR**: n38/n41/n48/n77/n78 HORxD1	
ANT2	192	AIO	**Antenna 2 interface:** - **5G NR**: n38/n41/n48/n77/n78 HORxD2	
ANT4	215	AIO	**Antenna 4 interface:** - **5G NR**: n38/n41/n48/n77/n78 HORxD3	

[8] ANT0/2/4/6 are used for 8Rx optional design, which supports 4 × 8 MIMO that means 8Rx with 4 × 4 MIMO + 4HORxD.

ANT6	239	AIO	**Antenna 6 interface:** - **5G NR**: n38/n41/n48/n77/n78 HORxD4	
ANT_GNSS	271	AI	**GNSS antenna interface:** - L1/L2/L5	
Antenna Interfaces for RG650E-EU*/RG650V-EU [8]				
ANT1	185	AIO	**Antenna 1 interface:** - **5G NR**: n41 TRX1 & n77/n78 TRX0 - **LTE**: LMB_TRX0 & HB_DRX & UHB_TRX0 - **Reframing**: LMB_TRX0 & HB_TRX1 - **WCDMA**: LMB_TRX	
ANT3	203	AIO	**Antenna 3 interface:** - **5G NR**: n41 DRX MIMO & n77/n78 PRX MIMO - **LTE**: LMB_PRX MIMO & HB_DRX MIMO & UHB_PRX MIMO - **Reframing**: LMB_PRX MIMO & HB_DRX MIMO	
ANT5	227	AIO	**Antenna 5 interface:** - **5G NR:** n41 PRX MIMO & n77/n78 DRX MIMO - **LTE:** LMB_DRX MIMO & HB_PRX MIMO & UHB_DRX MIMO - **Reframing:** LMB_DRX MIMO & HB_PRX MIMO	50 Ω impedance.
ANT7	251	AIO	**Antenna 7 interface:** - **5G NR**: n41 TRX0 & n77/n78 TRX1 - **LTE**: LMB_TRX1 & HB_TRX0 & UHB_TRX1 - **Reframing**: LMB_TRX1 & HB_TRX0 - **WCDMA**: LMB_DRX	
ANT0	177	AIO	**Antenna 0 interface:** - **5G NR**: n38/n40/n41/n77/n78 HORxD1	
ANT2	192	AIO	**Antenna 2 interface:** - **5G NR**: n38/n40/n41/n77/n78 HORxD2	
ANT4	215	AIO	**Antenna 4 interface:** - **5G NR**: n38/n40/n41/n77/n78 HORxD3	
ANT6	239	AIO	**Antenna 6 interface:** - **5G NR**: n38/n40/n41/n77/n78	

			HORxD4		
ANT_GNSS	271	AI	**GNSS antenna interface:** - L1/L2/L5		
Antenna Tuner Control Interfaces*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDR_GRFC11	241	DO	GRFC interfaces dedicated for external antenna tuner control	1.8 V	If unused, keep them open.
SDR_GRFC12	237	DO			
SPI					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_SPI_CS	335	DO	SPI chip select	VDD_EXT	Master mode only. If unused, keep them open.
MAIN_SPI_CLK	331	DO	SPI clock		
MAIN_SPI_MOSI	327	DO	SPI master-out slave-in		
MAIN_SPI_MISO	323	DI	SPI master-in salve-out		
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	292	AI	General-purpose ADC interface	Voltage range: 0–1.875 V	If unused, keep them open.
ADC1	288	AI	General-purpose ADC interface		
GPIO					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO_90	156	DIO	General-purpose input/output	VDD_EXT	
Reserved Pins					
Pin Name	**Pin No.**				
RESERVED	3, 6, 9, 11, 18, 22, 39, 40, 42, 50, 54, 55, 56, 62, 66, 74, 83, 86, 112, 116, 120, 127, 128, 132, 140, 144, 147, 148, 160, 164, 166, 167, 171, 179, 198, 210, 213, 218, 225, 229, 249, 253, 261, 263, 265, 278, 280, 283, 284, 289, 312, 316, 320, 324, 328, 332, 334, 337, 338, 339, 341, 342, 343, 345, 346, 349, 370				

2.6. EVB Kit

Quectel supplies an evaluation board (5G-SOC-EVB) with accessories to develop and test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Operating Modes

Table 7: Operating Modes Overview

Mode	Description	
Full Functionality Mode	Idle	The module remains registered on the network but has no data interaction with the network. Software is active.
	Voice/Data	The module is connected to the network. Power consumption is decided by network settings and data rate.
Minimum Functionality Mode	**AT+CFUN=0** can set the module to the minimum functionality mode without removing the power supply. In this mode, both the RF function and the (U)SIM card are invalid.	
Airplane Mode	**AT+CFUN=4** or driving W_DISABLE# low can set the module to airplane mode. In this mode, RF function is disabled and all relevant AT commands are inaccessible.	
Sleep Mode	The module can still receive paging, SMS, voice call and TCP/UDP data from the network. In this mode, the power consumption of the module is reduced to an ultra-low level.	
Shutdown Mode	PMU shuts down the power supply. Software is inactive. However, the voltage supply (for VBAT_RF and VBAT_BB) remains connected.	

NOTE

Unless otherwise specified, see ***document [2]*** for details of all AT commands involved in this document.

3.2. Sleep Mode

With DRX technology, power consumption of the module will be reduced to an ultra-low level. The figure below shows the relationship between the DRX run time and the current consumption in sleep mode. The longer the DRX runs, the lower the current consumption is.

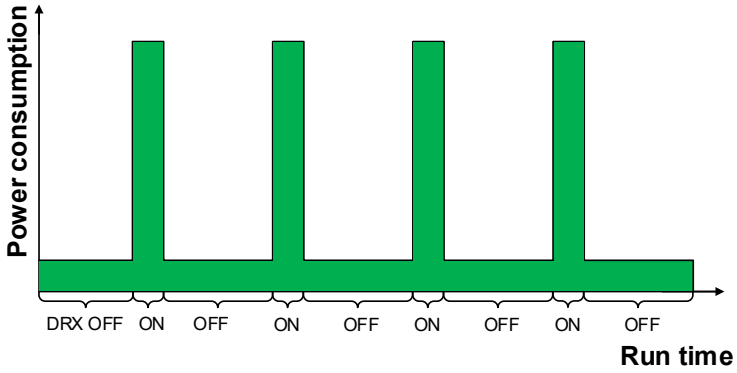


Figure 3: Module Power Consumption in Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

3.2.1. USB Application Scenarios

For the two situations ("USB application with USB Suspend/Resume and USB remote wakeup function" and "USB application with USB Suspend/Resume and MAIN_RI function") below, the following four preconditions must be met to make the module enter the sleep mode:

- Execute *QI_Autosleep_Enable(1)* to enable autosleep function.
- Execute **AT+QSCLK=1**.
- Ensure MAIN_DTR is held high or is kept unconnected.
- Ensure the host's USB bus, which is connected to the module's USB interface, enters Suspend state.

3.2.1.1. USB Application with USB Suspend/Resume and USB Remote Wakeup Function

The host supports USB Suspend/Resume and remote wakeup functions.

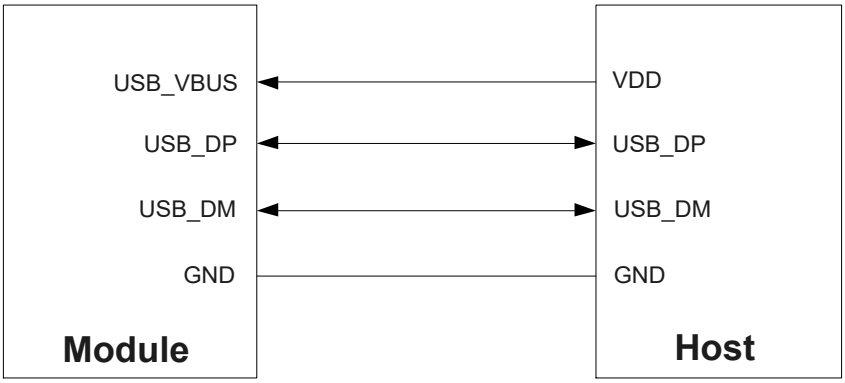


Figure 4: Block Diagram of Application with USB Remote Wakeup Function in Sleep Mode

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will send remote wakeup signals through USB bus to wake up the host.

3.2.1.2. USB Application with USB Suspend/Resume and MAIN_RI Function

If the host supports USB Suspend/Resume, but does not support remote wakeup function, the MAIN_RI signal is needed to wake up the host.

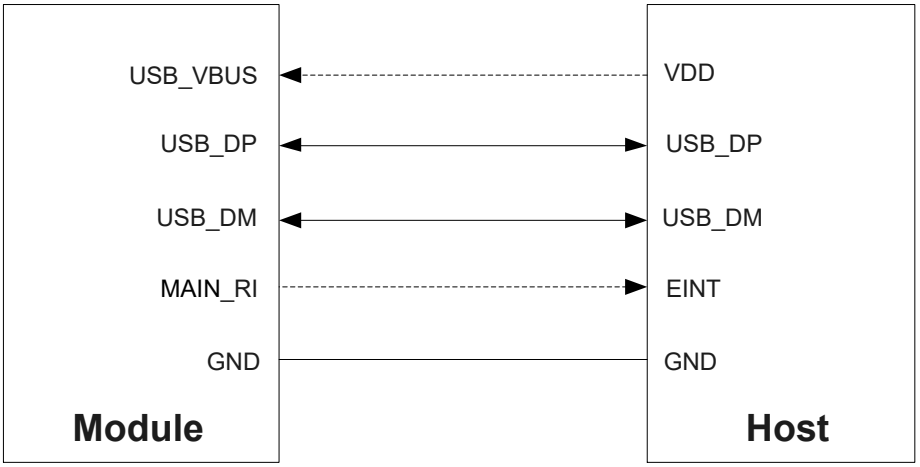


Figure 5: Block Diagram of Application with MAIN_RI Function in Sleep Mode

- Sending data to the module through USB will wake up the module.

- When the module has a URC to report, the module will wake up the host through MAIN_RI signal.

3.2.1.3. USB Application without USB Suspend Function

If the host does not support USB Suspend function, the following four preconditions must be met to make the module enter the sleep mode:

- Execute *QI_Autosleep_Enable(1)* to enable autosleep function.
- Execute **AT+QSCLK=1**.
- Ensure MAIN_DTR is held high or is kept unconnected.
- Ensure USB_VBUS is disconnected via the external control circuit.

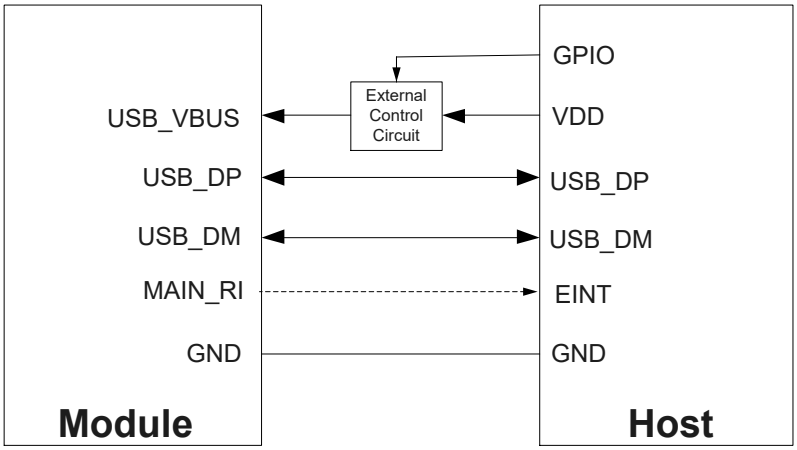


Figure 6: Block Diagram of Application Without USB Suspend Function in Sleep Mode

Restoring the power supply of USB_VBUS will wake up the module.

NOTE

1. Pay attention to the level match shown in the dotted line between the module and the host.
2. For more details about *QI_Autosleep_Enable(1)*, see ***document [3]***.

3.3. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. The following ways can be used to let the module enter airplane mode.

3.3.1. Hardware

The W_DISABLE# pin is pulled up by default. Driving it low will set the module enter airplane mode. See ***Chapter 4.15.1*** for details.

3.3.2. Software

AT+CFUN=<fun> provides choices of the functionality level through setting **<fun>** to **0**, **1** or **4**.

- **AT+CFUN=0:** Minimum functionality mode. Both RF function and (U)SIM function are disabled.
- **AT+CFUN=1:** Full functionality mode (default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

NOTE

The execution of **AT+CFUN** will not affect GNSS function.

3.4. Power Supply

3.4.1. Power Supply Pins

The module provides 14 VBAT pins dedicated to connecting with the external power supply. There are three separate voltage domains for VBAT.

- Five VBAT_RF1 pins and four VBAT_RF2 pins for RF part.
- Five VBAT_BB pins for BB part.

Table 8: VBAT and GND Pins

Pin Name	Pin No.	I/O	Description
VBAT_BB	321, 322, 325, 326, 329	PI	Power supply for the module's BB part
VBAT_RF1	310, 313, 314, 317, 318	PI	Power supply for the module's RF part
VBAT_RF2	154, 157, 158, 161	PI	Power supply for the module's RF part
GND	1, 7, 8, 12, 33, 35, 36, 46, 57, 58, 59, 60, 70, 80, 81, 82, 84, 85, 88, 89, 103, 105, 107, 115, 122, 123, 124, 125, 126, 136, 146, 149, 150, 151, 152, 153, 155, 159, 162, 163, 165, 168, 169, 170, 173, 174, 175, 178, 180, 181, 182, 183, 184, 186, 187, 188, 189, 190, 191, 193, 194, 195, 196, 199, 200, 202, 204, 205, 207, 208, 209, 211, 212, 214, 216, 219, 220, 221, 223, 224, 226, 228, 231, 232, 233, 235, 236, 238, 240, 243, 244,		

	245, 247, 248, 250, 252, 255, 256, 257, 259, 260, 262, 264, 266, 267, 268, 269, 270, 272–277, 279, 281, 282, 285, 286, 290, 293, 294, 296, 297, 299, 306, 308, 309, 319, 330, 333, 336, 340, 350, 352, 353, 362, 364, 365, 373, 377–519

3.4.2. Reference Design for Power Supply

The performance of the module largely depends on the power supply design. The continuous current of the power supply should be 3 A at least and the peak current should be 4 A at least.

The following figure shows a reference design for 5 V input power supply. The designed output of the power supply is about 3.8 V.

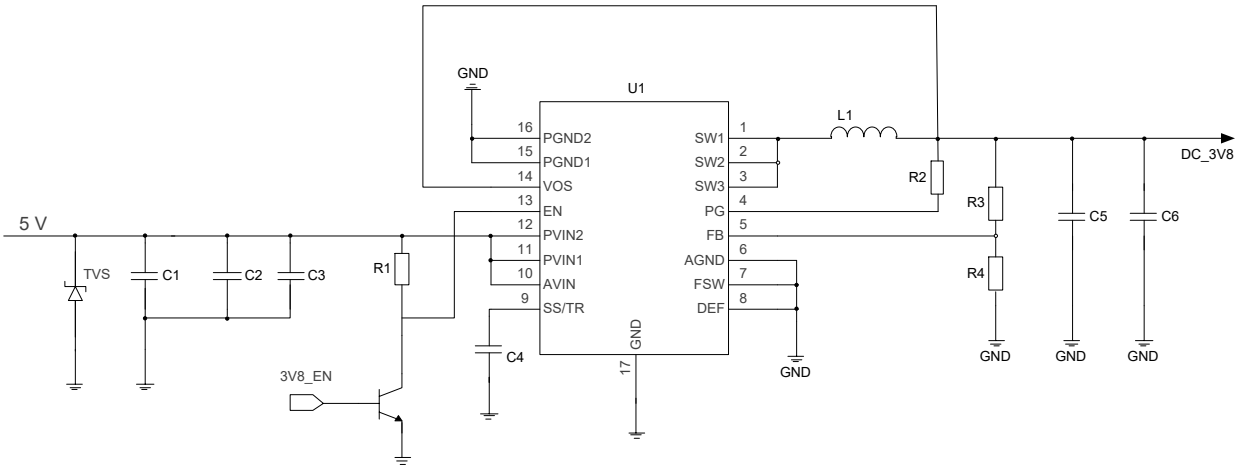


Figure 7: Reference Design of Power Input

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.
2. If you turn off the module by cutting off the power supply, do not power up the module until the power drops to 0 V, or there is a risk that the module cannot be turned on again.

3.4.3. Requirements for Voltage Stability

The power supply range of the module is from 3.3 V to 4.4 V. Ensure the input voltage never drops below 3.3 V.

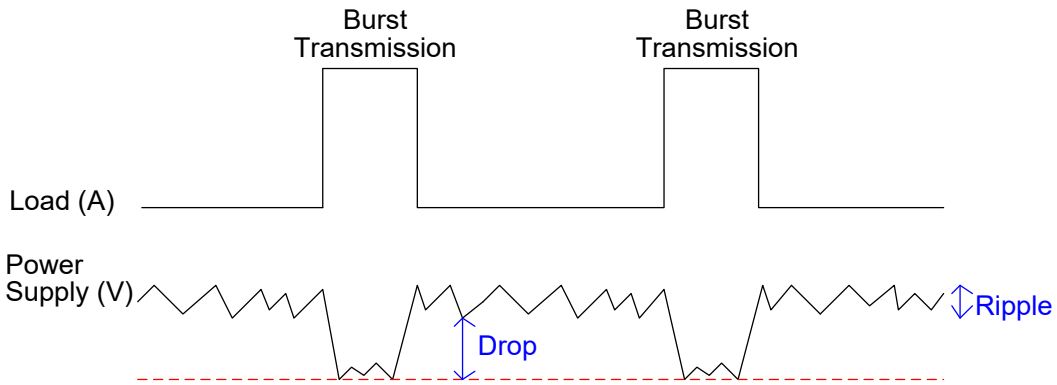


Figure 8: Power Supply Limits During Burst Transmission

To decrease the voltage drop, use decoupling capacitors of about 220 µF with low ESR and reserve decoupling capacitors of about 100 µF. In addition, a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. Use 16 ceramic capacitors for composing the MLCC array, and place these capacitors close to the VBAT pins. The main power supply from an external application must be a single voltage source that can supply power along two star-structured sub paths. The width of VBAT_BB, VBAT_RF1 and VBAT_RF2 traces should be at least 2 mm respectively. As per design rules, the longer the VBAT trace is, the wider it should be.

To avoid the ripple and surge and to ensure the stability of the power supply to the module, add a high-power rated TVS component at the front end of the power supply.

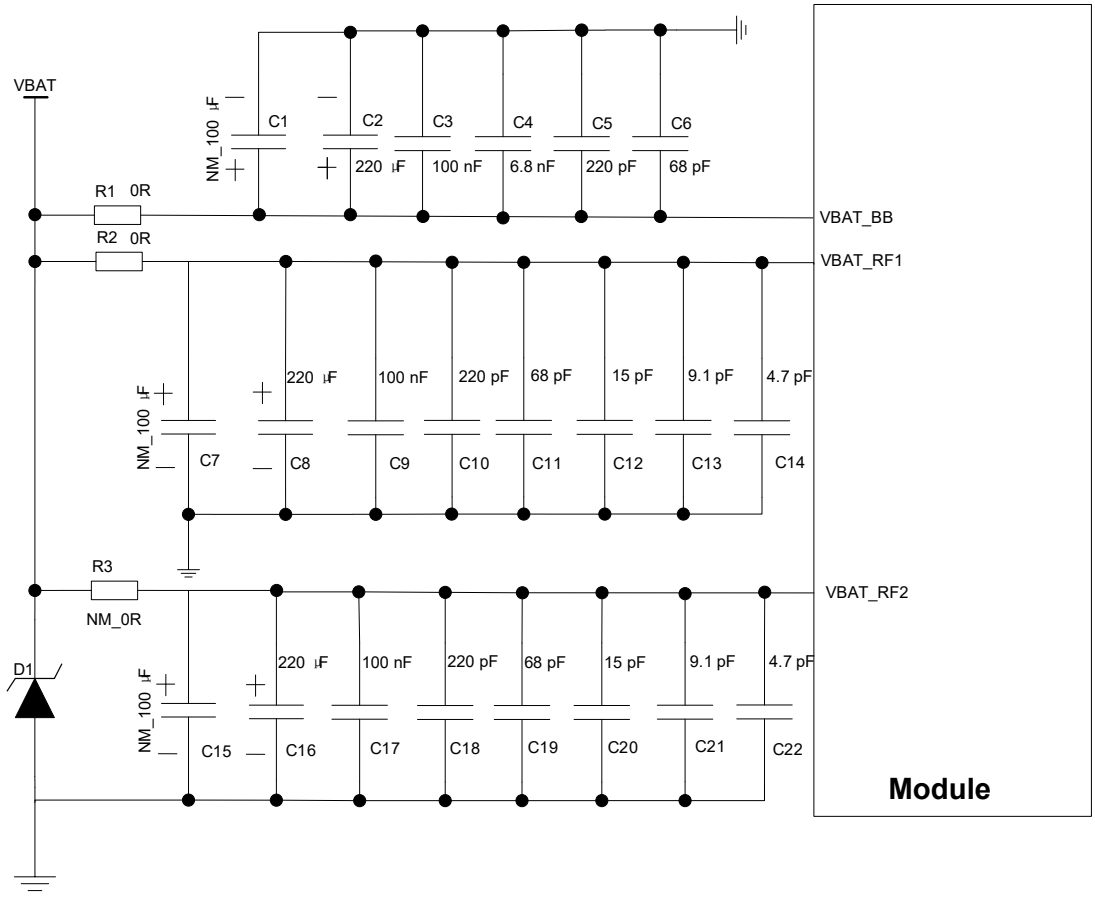


Figure 9: Reference Design of Power Supply

NOTE

1. Filter capacitors for VBAT_BB include 220 µF, 100 nF, 6.8 nF, 220 pF and 68 pF, and a 100 µF capacitor is reserved.
2. Filter capacitors for VBAT_RF1 and VBAT_RF2 respectively include 220 µF, 100 nF, 220 pF, 68 pF, 15 pF, 9.1 pF and 4.7 pF, and a 100 µF capacitor is reserved.
3. R3 needs to be reserved since power class 1.5 is designed and VBAT_RF2 should be connected to an external VBAT power supply.

3.4.4. Power Supply Voltage Monitoring

You can use **AT+CBC** to monitor and query the VBAT_BB voltage.

3.5. Turn On

3.5.1. Turn On with PWRKEY

Table 9: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	4	DI	Turn on/off the module	Active low.

When the module is in turn-off state, it can be turned on by driving PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control PWRKEY. After STATUS outputs a high-level voltage, PWRKEY can be released.

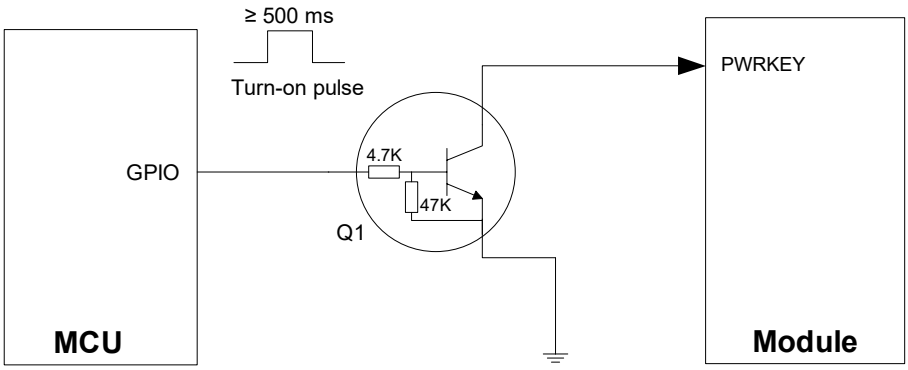


Figure 10: Reference Design of Turn-on with Driving Circuit

Another way to control PWRKEY is using a keystroke directly. When pressing the keystroke, an electrostatic strike may be generated from fingers. Therefore, place a TVS component near the keystroke for ESD protection.

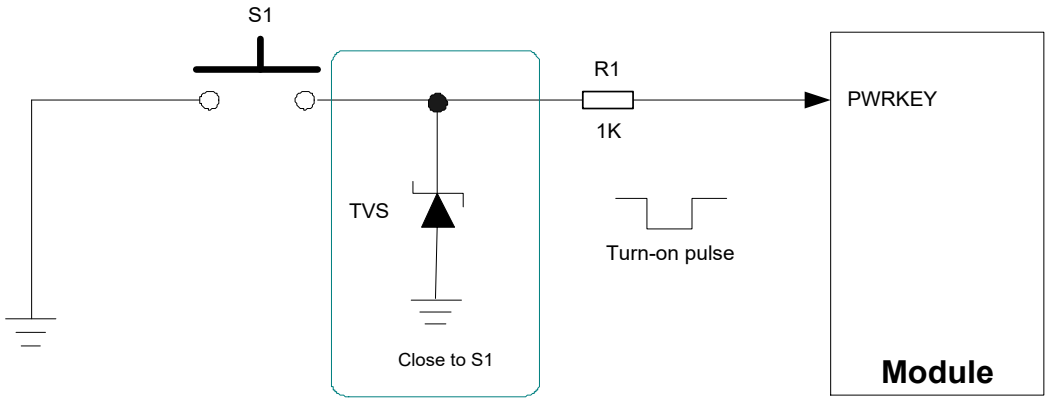


Figure 11: Reference Design of Turn-on with Keystroke

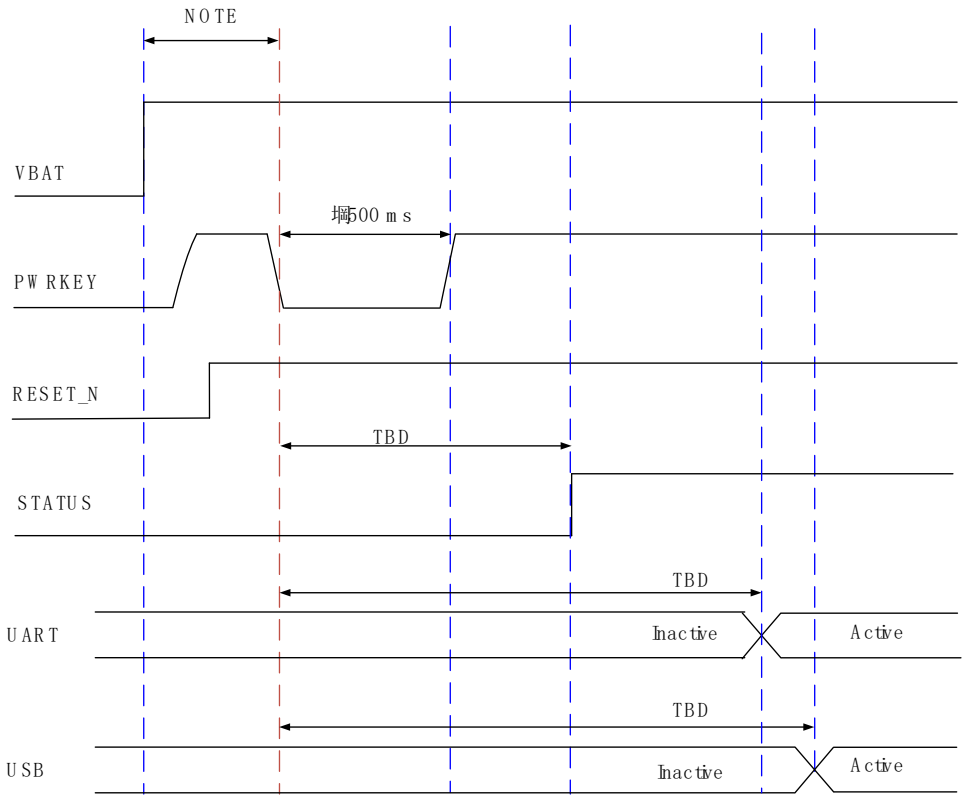


Figure 12: Timing of Turn-on with PWRKEY

NOTE

Ensure the voltage of VBAT is stable for at least 30 ms before driving PWRKEY low.

3.5.2. Turn On with CBL_PWR_N

Table 10: Pin Description of CBL_PWR_N

Pin Name	Pin No.	I/O	Description	Comment
CBL_PWR_N	2	DI	Initiate power on when grounded	Internally pulled up to 1.8 V. Active low.

NOTE

If the module needs to turn on automatically but does not need turn-off function, CBL_PWR_N can be driven low directly to ground with a recommended 4.7 kΩ resistor.

3.6. Turn Off

3.6.1. Turn Off with PWRKEY

Drive PWRKEY low for at least 800 ms, and then release it. After this, the module executes turn-off procedure.

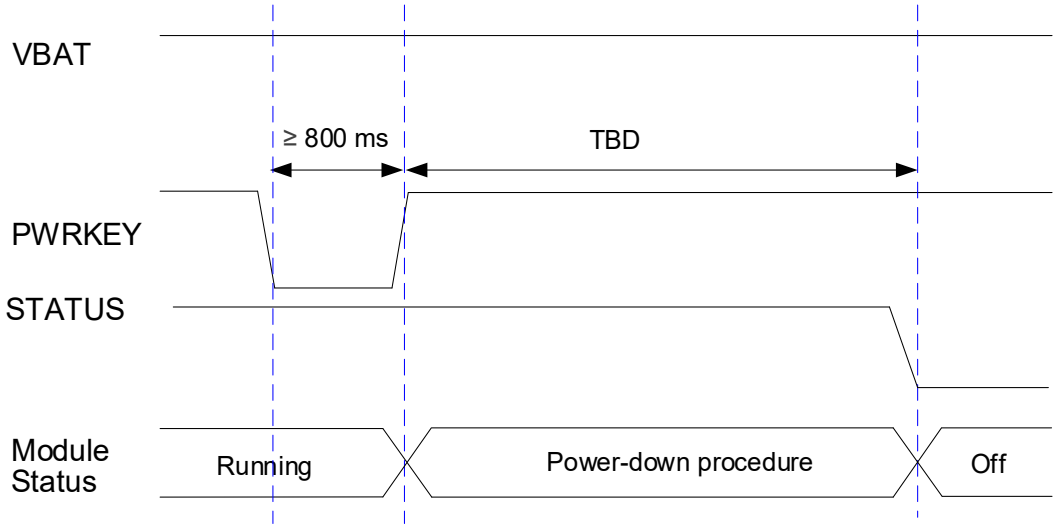


Figure 13: Timing of Turn-off with PWRKEY

3.6.2. Turn Off with AT Command

It is also a safe way to use **AT+QPOWD** to turn off the module, which is similar to turning off the module via the PWRKEY pin.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY or AT command can you switch off the power supply.
2. When turning off the module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on automatically again after successful turn-off.

3.7. RESET_N

Drive RESET_N low for at least 500 ms and then releasing it to reset the module. RESET_N signal is sensitive to interference, consequently it is recommended to route the trace as short as possible and surround it with ground.

Table 11: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	5	DI	Reset the module	Active low. A test point is recommended to be reserved if unused.

The recommended circuits for reset function are similar to the PWRKEY control circuits. You can use an open drain/collector driver or a keystroke to control RESET_N.

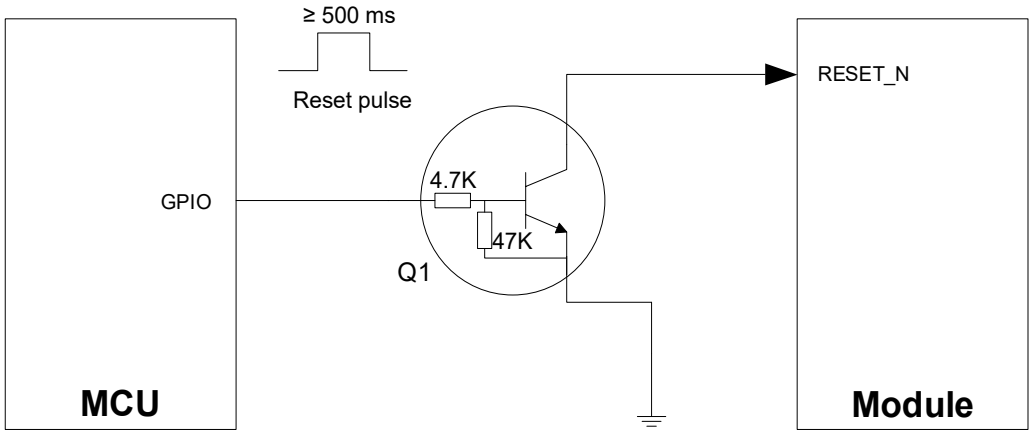


Figure 14: Reference Design of Reset with Driving Circuit

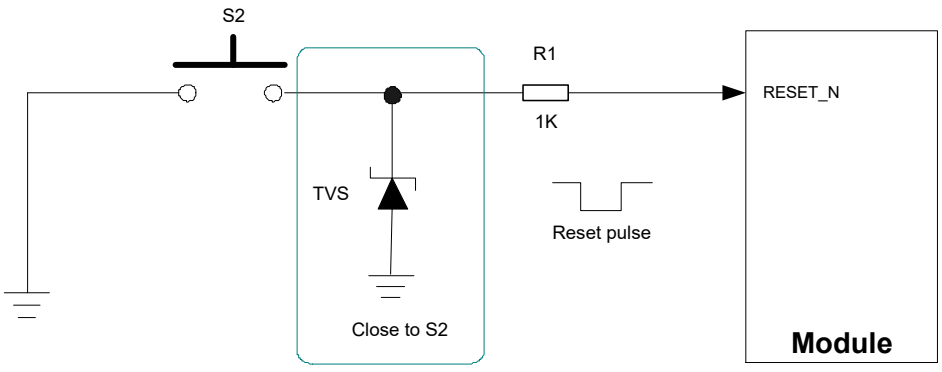


Figure 15: Reference Design of Reset with Keystroke

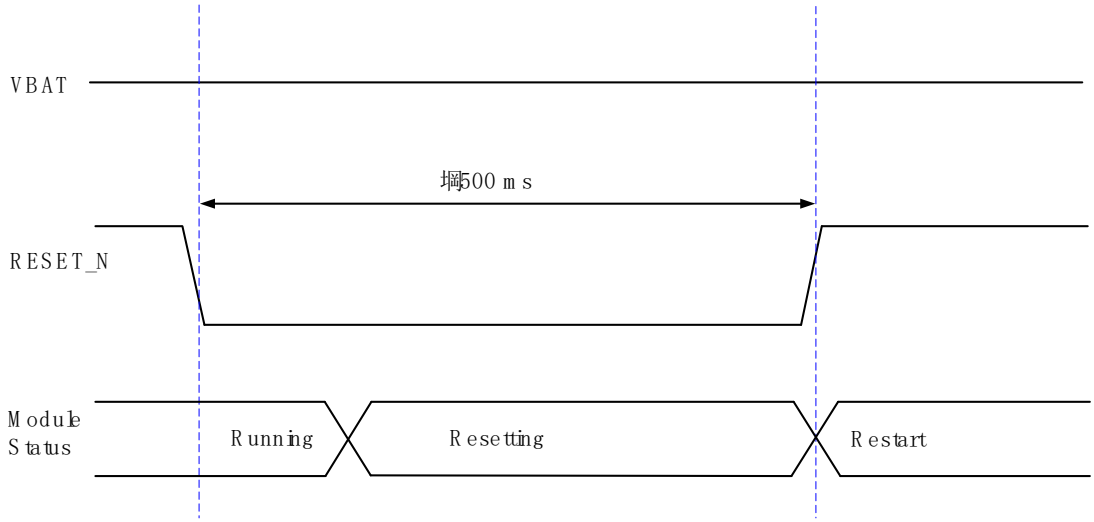


Figure 16: Timing of Reset

NOTE

1. Use RESET_N only when failing to turn off the module with **AT+QPOWD** and PWRKEY.
2. Ensure there is no large capacitance on PWRKEY and RESET_N.

4 Application Interfaces

4.1. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 3.1/2.0 specifications and supports SuperSpeed (10 Gbps) on USB 3.1 Gen 2 and 5 Gbps on USB 3.1 Gen 1, high-speed (480 Mbps) and full-speed (12 Mbps) modes on USB 2.0. The USB interface can be used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB*.

Pin definition of the USB interface is as follows.

Table 12: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	117	AI	USB connection detect	Used for USB connection detection only, not for power supply. A test point must be reserved.
USB_DP	118	AIO	USB differential data (+)	Require differential impedance of 90 Ω. Test points must be reserved.
USB_DM	121	AIO	USB differential data (-)	
USB_SS_TX_P	109	AO	USB 3.1 SuperSpeed transmit (+)	Require differential impedance of 90 Ω. If unused, keep them open.
USB_SS_TX_M	106	AO	USB 3.1 SuperSpeed transmit (-)	
USB_SS_RX_P	113	AI	USB 3.1 SuperSpeed receive (+)	
USB_SS_RX_M	110	AI	USB 3.1 SuperSpeed receive (-)	
USB_ID*	111	DI	USB ID detect	1.2 V power domain. High level by default.
OTG_PWR_EN*	114	DO	OTG power control	1.8 V power domain.

Test points must be reserved for software debugging and firmware upgrading in your design. The following figure shows a reference circuit of USB 2.0 interface.

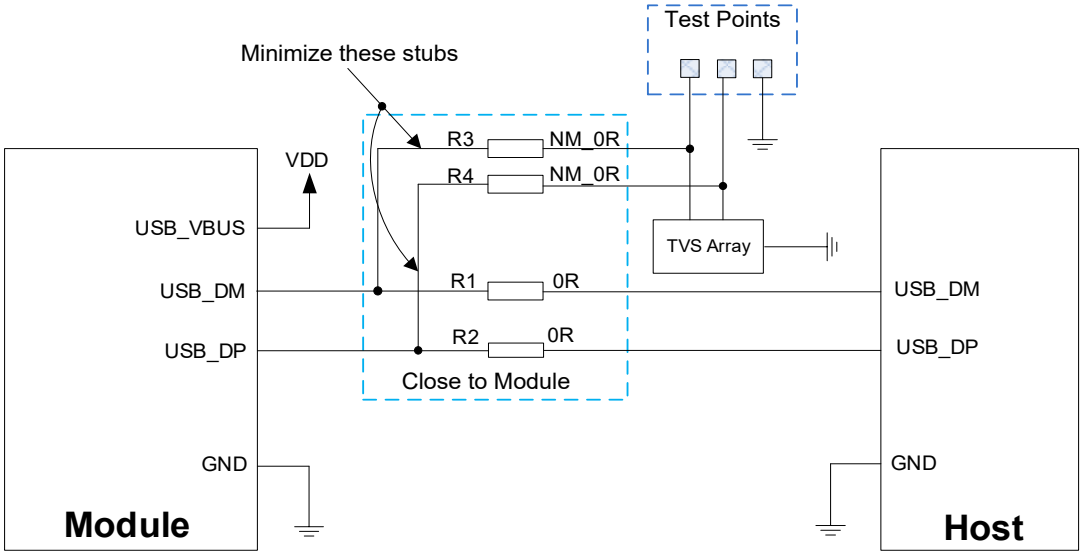
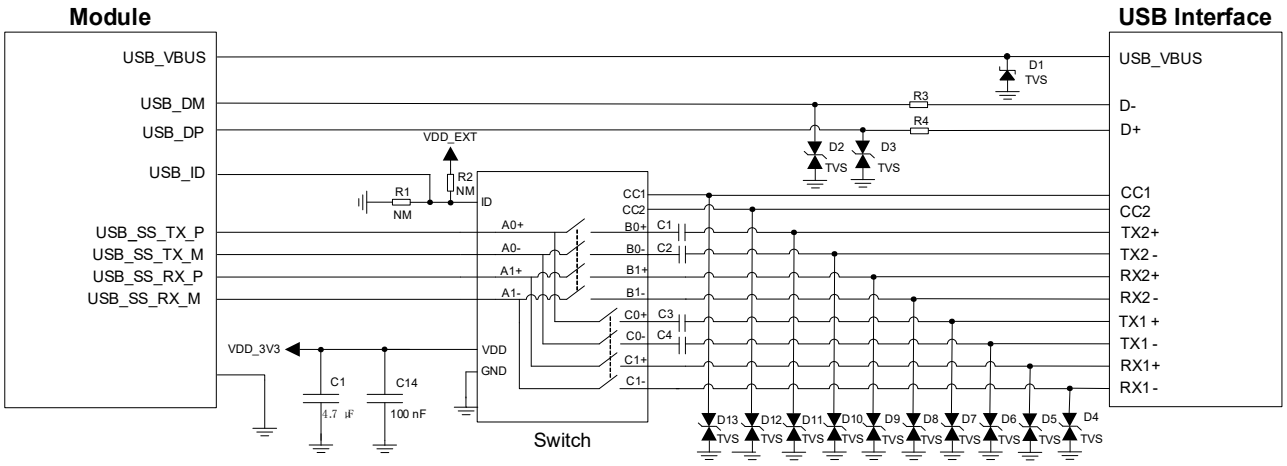


Figure 17: Reference Design of USB 2.0 Interface

To ensure signal integrity of USB 2.0 data transmission, place R1, R2, R3 and R4 close to the module. Moreover, keep extra stubs of trace as short as possible.



NOTE: The series capacitor of the module Rx is generally set on the Tx end of the external device. You need to confirm that there is a series capacitor on the entire Tx/Rx link between the module and external device.

Figure 18: Reference Design of USB Type-C Interface

Type-C interface USB_VBUS can charge the battery through the external charging circuit, and can also be used for module's USB insertion detection. Input voltage of the USB_VBUS power supply ranges from 3.3 V to 5.25 V. The voltage should be adjusted for high-voltage charging through divider circuit and

the recommended value is 5.0 V. The module supports charging management of a single Li-ion battery. Different charging parameters need to be set for batteries with different capacities. Meanwhile, the module also supports USB OTG mode. When USB_ID is held at high level by default, the module acts as USB slave device. When USB_ID is grounded, the module acts as USB master device. VBUS pin of the charging IC is the OTG power output.

To ensure performance, follow the below principles when designing USB interface:

- Route USB differential traces in the inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below. The impedance of USB 2.0 and 3.1 differential trace is 90 Ω.
- For USB 3.1 signal traces, length matching of each differential data pair (Tx/Rx) should be less than 0.7 mm (5 ps), while the matching between Tx and Rx should be less than 10 mm. For USB 2.0 signal traces, the trace length should be less than 250 mm, and length matching of the differential data pair (P/M) should be less than 2 mm (14 ps).
- For signal traces, provide clearance from power supply traces, crystal-oscillators, magnetic devices, and sensitive signals such as RF signals, analog signals and noise signals generated by clock, DC-DC.
- Pay attention to the impact caused by stray capacitance of the ESD protection components on USB data traces. Typically, the stray capacitance should be less than 1.0 pF for USB 2.0, and less than 0.15 pF for USB 3.1.
- If possible, add a 0 Ω resistor on USB_DP and USB_DM traces respectively.

For more details about the USB specifications, visit http://www.usb.org/home.

Table 13: USB Interface Trace Length Inside the Module (Unit: mm)

Pin No.	Pin Name	Length	Length Matching
118	USB_DP	TBD	TBD
121	USB_DM	TBD	TBD
109	USB_SS_TX_P	TBD	TBD
106	USB_SS_TX_M	TBD	TBD
113	USB_SS_RX_P	TBD	TBD
110	USB_SS_RX_M	TBD	TBD

NOTE

Both USB 3.1 interface and PCIe interface support data transmission, and USB 3.1 interface is used by default. If you want to use PCIe interface for communication, set it with **AT+QCFG="data_interface"** via USB 2.0.

4.2. Forced Download Interface

The module provides a USB_BOOT interface for forced download. Pulling up USB_BOOT to VDD_EXT before turning on the module, and then the module will enter forced download mode. In this mode, the module supports firmware upgrade over USB interface.

Table 14: Pin Description of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	119	DI	Force the module into download mode	A test point is recommended to be reserved.

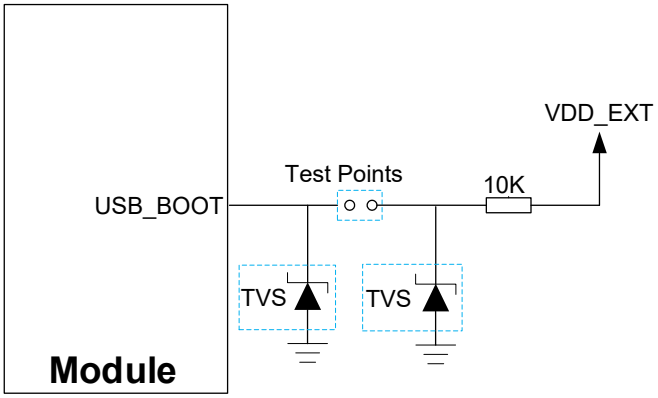


Figure 19: Reference Design of USB_BOOT

4.3. (U)SIM Interfaces

The (U)SIM interfaces meet ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V (U)SIM card is supported on (U)SIM1 interface, and only 1.8 V eSIM is supported on (U)SIM2 interface. Dual SIM Single Standby function is supported.

Table 15: Pin Description of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	90	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module. If unused, keep it open.
USIM1_DATA	91	DIO	(U)SIM1 card data	
USIM1_CLK	93	DO	(U)SIM1 card clock	
USIM1_RST	94	DO	(U)SIM1 card reset	
USIM1_DET	92	DI	(U)SIM1 card hot-plug detect	If unused, keep it open.
USIM2_VDD	97	PO	(U)SIM2 card power supply	1.8 V eSIM is supported and can be identified automatically by the module. If unused, keep it open.
USIM2_DATA	98	DIO	(U)SIM2 card data	
USIM2_CLK	101	DO	(U)SIM2 card clock	
USIM2_RST	102	DO	(U)SIM2 card reset	
USIM2_DET	99	DI	(U)SIM2 card hot-plug detect	If unused, keep it open.
USIM2_LS_EN	95	DO	(U)SIM2 level-shifting enable	

The module supports (U)SIM card hot-plug via USIM_DET, and both high-level and low-level detections are supported. Hot-plug function is disabled by default and you can use **AT+QSIMDET** to configure this function.

The following figure shows a reference design for (U)SIM1 interface with an 8-pin (U)SIM card connector.

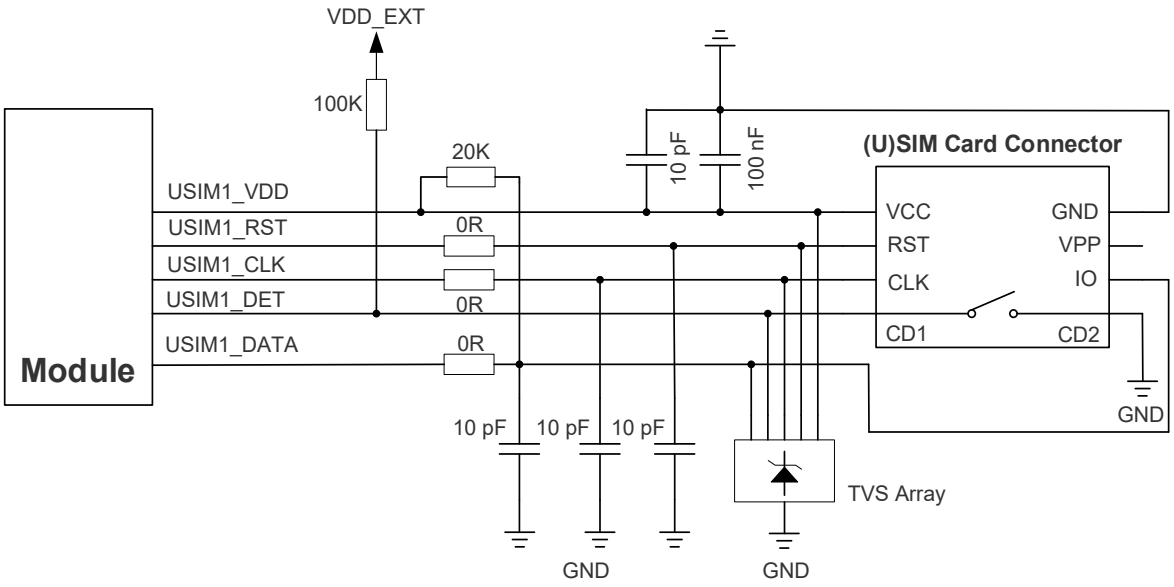


Figure 20: Reference Design of (U)SIM1 Interface with an 8-pin (U)SIM Card Connector

If the function of (U)SIM card hot-plug is not needed, keep USIM_DET disconnected. A reference circuit for (U)SIM1 interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

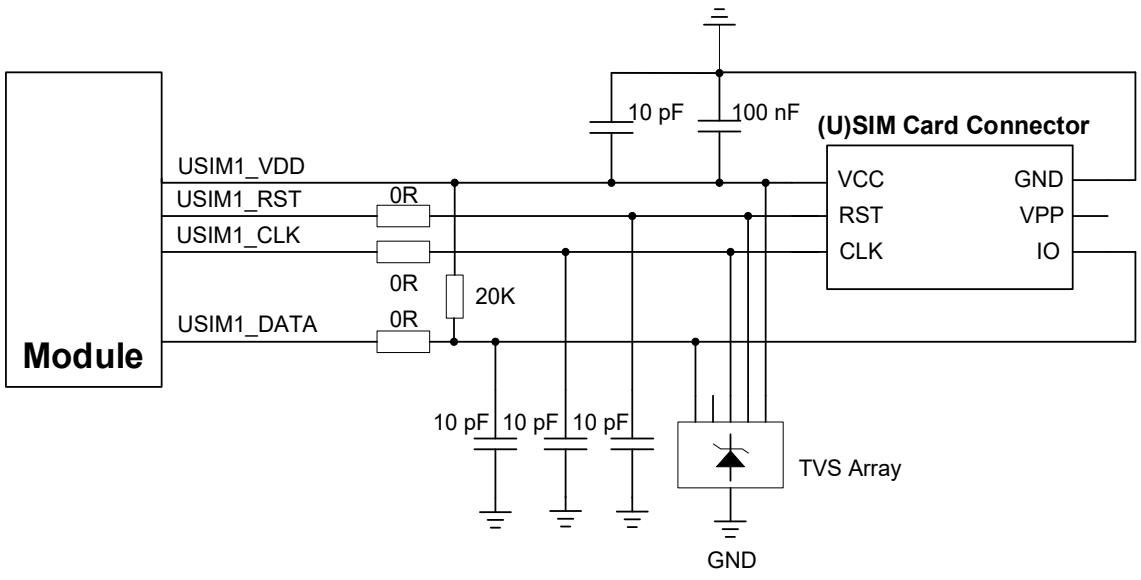


Figure 21: Reference Design of (U)SIM1 Interface with a 6-pin (U)SIM Card Connector

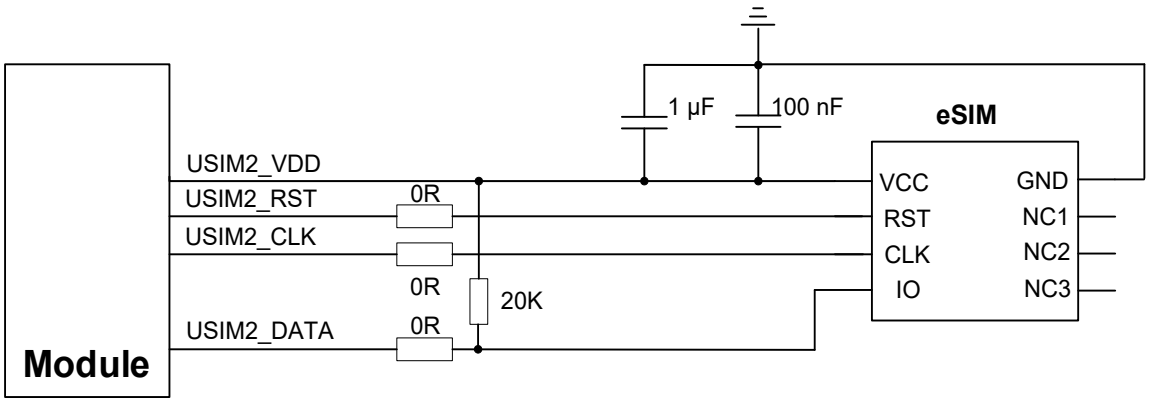


Figure 22: Reference Design of (U)SIM2 Interface with eSIM

To enhance the reliability and availability of the (U)SIM card and eSIM in applications, you should follow the principles below in the (U)SIM circuit design:

- Place the (U)SIM card connector or eSIM close to the module. Keep the trace length as short as possible, at most 200 mm.
- For signal traces, provide clearance from power supply traces, crystal-oscillators, magnetic devices, and sensitive signals such as RF signals, analog signals and noise signals generated by clock, DC-DC.
- Ensure the tracing between the (U)SIM card connector or eSIM and the module is short and wide. Keep the trace width of ground and USIM_VDD at least 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep the traces away from each other and shield them with surrounded ground.
- To offer better ESD protection, add a TVS array of which the parasitic capacitance should be less than 10 pF. Add 0 Ω resistors in series between the module and the (U)SIM card connector to suppress EMI and enhance ESD protection. Additionally, add 10 pF capacitors in parallel among USIM1_DATA, USIM1_CLK and USIM1_RST signal traces to filter out RF interference.
- For USIM_DATA, it is recommended to add a 20 kΩ pull-up resistor near the (U)SIM card connector or eSIM to improve the anti-jamming capability of the (U)SIM card or eSIM.

4.4. UART Interfaces

The module provides three UART interfaces: main UART interface*, debug UART interface, and Bluetooth UART interface*. The following shows their features.

Table 16: UART Information

UART Type	Default Baud Rate	Function
Main UART interface	115200 bps	Data transmission
Debug UART interface	115200 bps	Linux console and log output
Bluetooth UART interface	115200 bps	Bluetooth communication

Main UART interface and Bluetooth UART interface support RTS and CTS hardware flow control.

Pin definition of UART interfaces is as follows.

Table 17: Pin Description of UART Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	246	DO	Clear to send signal from the module	Connect to the MCU's CTS.
MAIN_RTS	242	DI	Request to send signal to the module	Connect to the MCU's RTS.
MAIN_RXD	258	DI	Main UART receive	
MAIN_TXD	254	DO	Main UART transmit	
MAIN_RI	230	DO	Main UART ring indication	
MAIN_DTR	234	DI	Main UART data terminal ready	
MAIN_DCD	222	DO	Main UART data carrier detect	
BT_TXD	376	DO	Bluetooth UART transmit	1.8 V power domain by default.
BT_RXD	375	DI	Bluetooth UART receive	
BT_RTS	372	DI	Request to send signal to the module	Connect to the MCU's RTS. 1.8 V power domain by

				default.
BT_CTS	374	DO	Clear to send signal from the module	Connect to the MCU's CTS. 1.8 V power domain by default.
DBG_RXD	172	DI	Debug UART receive	Test points must be reserved.
DBG_TXD	176	DO	Debug UART transmit	

The module provides 1.8 V UART interface. You can use a voltage-level translator between the module and MCU's UART interface if the MCU is equipped with a 3.3 V UART interface.

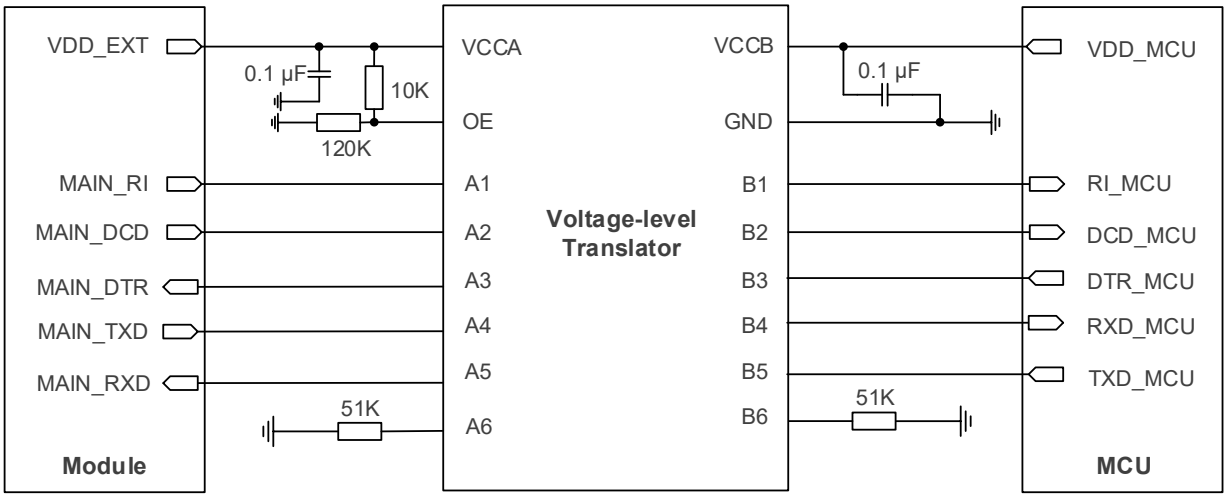


Figure 23: Reference Design with Translator Chip (Main UART)

Another example of level-shifting circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

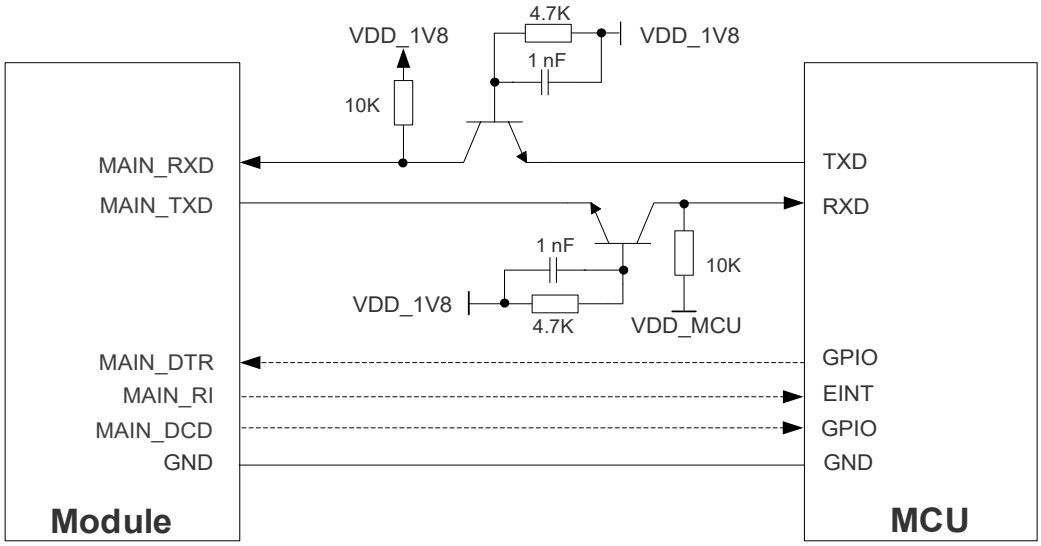


Figure 24: Reference Design Transistor Circuit (Main UART)

NOTE

1. Transistor circuit above is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.
3. The level-shifting circuits (***Figure 23*** and ***Figure 24***) take the main UART as an example. The circuits of the debug UART and the Bluetooth UART are connected in the same way as the main UART.

4.5. PCM Interfaces*

The module provides two PCM interfaces: one is used for SLIC or codec and the other is only for Bluetooth audio.

The PCM interfaces support the following modes:

- Short frame mode: the module works as both the slave and the master device
- Long frame mode: the module works as the master device only

The module supports 16-bit linear data format. The following figures are the short frame mode timing diagram (PCM_SYNC = 8 kHz, PCM_CLK = 2048 kHz) and the long frame mode timing diagram (PCM_SYNC = 8 kHz, PCM_CLK = 256 kHz).

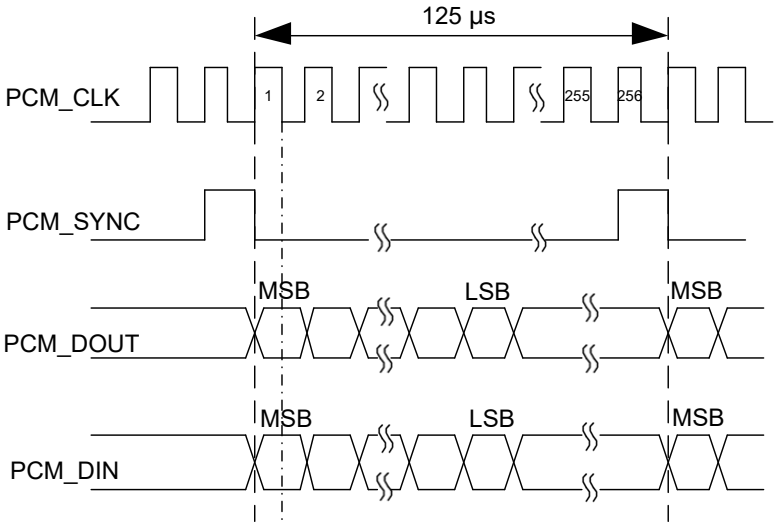


Figure 25: Timing of Short Frame Mode

In short frame mode, data is sampled on the falling edge of PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, PCM_CLK supports 256 kHz, 512 kHz, 1024 kHz and 2048 kHz when PCM_SYNC operates at 8 kHz, and also supports 4096 kHz when PCM_SYNC operates at 16 kHz.

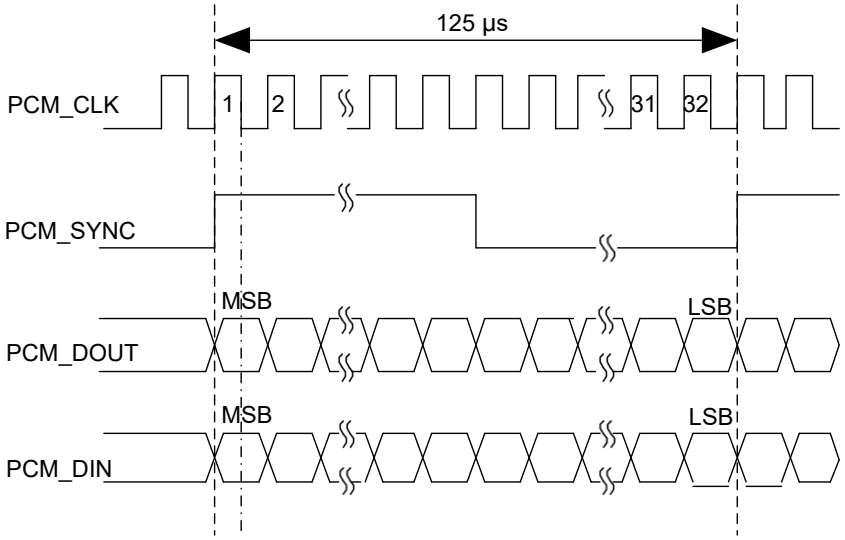


Figure 26: Timing of Long Frame Mode

In long frame mode, data is also sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. But in this mode, the PCM_SYNC rising edge represents the MSB. PCM_CLK supports 256 kHz, 512 kHz, 1024 kHz and 2048 kHz when PCM_SYNC reaches 8 kHz with a 50 % duty cycle.

The clock and mode of PCM can be configured by **AT+QDAI**, and the default configuration is short frame mode (PCM_CLK = 2048 kHz, PCM_SYNC = 8 kHz).

4.5.1. PCM for SLIC or Codec

The module provides one PCM interface for SLIC or codec. Pin definition is listed as follows.

Table 18: Pin Description of PCM Interface for SLIC or Codec

Pin Name	Pin No.	I/O	Description	Comment
EXT_PCM_SYNC	305	DIO	PCM data frame sync	In master mode, it is an output signal. In slave mode, it is an input signal.
EXT_PCM_CLK	302	DIO	PCM clock	
EXT_PCM_DIN	301	DI	PCM data input	
EXT_PCM_DOUT	298	DO	PCM data output	

The reference design is illustrated as follows:

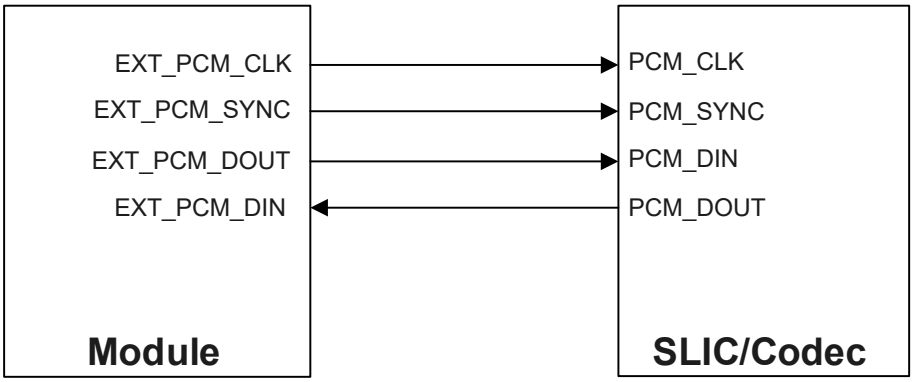


Figure 27: Reference Circuit of PCM Interface for SLIC or Codec

4.5.2. PCM for Bluetooth Audio

The module provides one PCM interface only used for Bluetooth audio. Pin definition is listed as follows:

Table 19: Pin Definition of PCM Interface for Bluetooth Audio

Pin Name	Pin No.	I/O	Description	Comment
BT_PCM_SYNC	96	DIO	Bluetooth PCM data frame sync	1.8 V power domain by default. If unused, keep them open.
BT_PCM_CLK	108	DIO	Bluetooth PCM clock	
BT_PCM_DIN	100	DI	Bluetooth PCM data input	
BT_PCM_DOUT	104	DO	Bluetooth PCM data output	

The reference design is illustrated as follows.

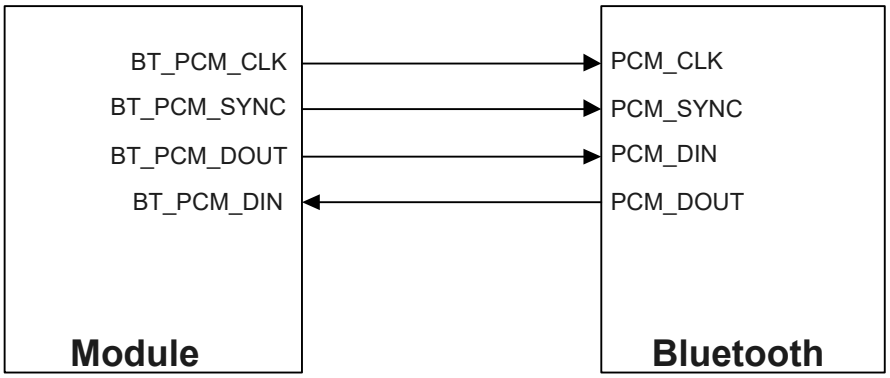


Figure 28: Reference Circuit of PCM Interface for Bluetooth Audio

4.6. I2C Interfaces

The module supports two I2C interfaces: one is used for general I2C, and the other is used for TP I2C. Both comply with version 3.0 of I2C-bus specification.

The below table gives the pin description of general I2C interface. For the other used for TP I2C, see ***Chapter 4.10*** for details.

Table 20: Pin Description of General I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_I2C_SCL	304	OD	I2C serial clock	Pull each of them up to VDD_EXT with an external 2.2 kΩ resistor. If unused, keep them open.
MAIN_I2C_SDA	300	OD	I2C serial data	

4.7. ADC Interfaces

The module provides two Analog-to-Digital Converter (ADC) interfaces. To improve the accuracy of ADC, surround the trace of ADC interfaces with ground.

Table 21: Pin Description of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	292	AI	General-purpose ADC interface	If unused, keep them open.
ADC1	288	AI	General-purpose ADC interface	

With **AT+QADC=<port>**, you can:

- **AT+QADC=0**: read the voltage value on ADC0.
- **AT+QADC=1**: read the voltage value on ADC1.

The following table describes the characteristics of the ADC interfaces.

Table 22: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC0 Input Voltage Range	0	-	1.875	V
ADC1 Input Voltage Range	0	-	1.875	V
ADC Input Resistance	10	-	-	MΩ
ADC Resolution	-	64.879	-	μV

NOTE

1. The input voltage of each ADC interface should not exceed its corresponding voltage range.
2. It is prohibited to directly supply any voltage to ADC interface when the module is not powered by VBAT.
3. It is recommended to use resistor divider circuit for ADC interface application. Resistance of the external resistor divider should not exceed 1 MΩ, or the measurement accuracy of ADC would be significantly reduced.

4.8. USXGMII and ETH Control Interfaces

The module includes two integrated Ethernet MAC with two USXGMII interfaces and two ETH MDIO management interfaces. Key features are shown below:

- *IEEE 802.3* compliant.
- Full duplex mode for 100 Mbps, 1000 Mbps, 2500 Mbps, 5000 Mbps and 10000 Mbps.
- Can be connected to an external Ethernet Switch or PHY.
- The ETH MDIO management interfaces and ETH interrupt/reset signals support 1.8 V power domain.

Table 23: Pin Description of USXGMII and ETH Control Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USXGMII0_TX_M	368	AO	USXGMII0 transmit (-)	Require differential impedance of 100 Ω. If unused, keep them open.
USXGMII0_TX_P	366	AO	USXGMII0 transmit (+)	
USXGMII0_RX_P	369	AI	USXGMII0 receive (+)	
USXGMII0_RX_M	371	AI	USXGMII0 receive (-)	
USXGMII1_RX_P	358	AI	USXGMII1 receive (+)	
USXGMII1_RX_M	361	AI	USXGMII1 receive (-)	
USXGMII1_TX_P	354	AO	USXGMII1 transmit (+)	
USXGMII1_TX_M	357	AO	USXGMII1 transmit (-)	
ETH0_MDIO	356	DIO	Ethernet PHY0 MDIO data	
ETH0_MDC	360	DO	Ethernet PHY0 MDIO clock	

ETH0_INT_N	359	DI	Ethernet PHY0 interrupt
ETH0_RST_N	363	DO	Ethernet PHY0 reset
ETH0_PWR_EN	367	DO	Ethernet PHY0 power supply enable control
ETH1_MDIO	344	DIO	Ethernet PHY1 MDIO data
ETH1_MDC	348	DO	Ethernet PH1 MDIO clock
ETH1_INT_N	347	DI	Ethernet PHY1 interrupt
ETH1_RST_N	351	DO	Ethernet PHY1 reset
ETH1_PWR_EN	355	DO	Ethernet PHY1 power supply enable control

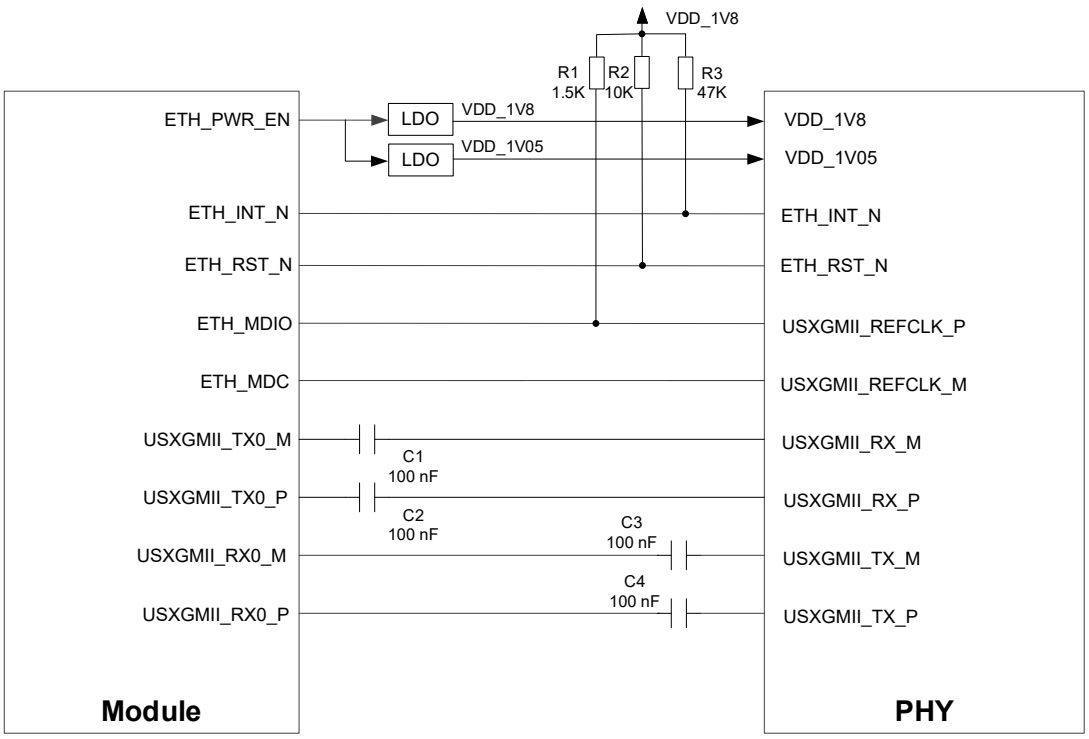


Figure 29: Reference Design of USXGMII and ETH Control Interfaces

To enhance the reliability and availability of your application, follow the criteria below in the Ethernet PHY circuit design:

- USXGMII signals must be protected from noise signals (clocks, DC-DC, RF and so forth). All other

sensitive/high-speed signals and circuits must be routed far away from USXGMII traces.

- The differential impedance of USXGMII data traces is 100 Ω ±10 %.
- For each differential pair, intra-lane length match should be less than 0.7 mm. The total bus length should be less than 144 mm.
- Inter-lane length match, that is, the trace length matching between the reference clock, Tx, and Rx pairs is not required.
- The spacing between Tx and Rx, and the spacing between USXGMII lanes and all other signals, should be larger than 4 times of the trace width.
- USXGMII Tx AC coupling capacitors can be anywhere along the trace, but better to be placed close to source or connector side to keep good signal integrity of main route on PCB. AC coupling capacitors should be 100 nF. Ensure not to stagger the capacitors. This can affect the differential integrity of the design and can create EMI.
- In the case of trace serpentines, one trace of a differential pair must be routed to make up a length delta, then it must be routed at the source (breakout) – this ensures that traces stay differential thereafter.
- To reduce the probability for layer-to-layer manufacturing variation, minimize layer transitions on the main route (in other words, apply layer transitions only at module breakouts and connectors to ensure minimum layer transitions on the main route).

Table 24: USXGMII Interface Trace Length Inside the Module (Unit: mm)

Pin No.	Pin Name	Length	Length Matching
368	USXGMII0_TX_M	TBD	TBD
366	USXGMII0_TX_P	TBD	TBD
369	USXGMII0_RX_P	TBD	TBD
371	USXGMII0_RX_M	TBD	TBD
358	USXGMII1_RX_P	TBD	TBD
361	USXGMII1_RX_M	TBD	TBD
354	USXGMII1_TX_P	TBD	TBD
357	USXGMII1_TX_M	TBD	TBD

4.9. LCM Interface*

The module provides one LCM interface, which supports LCD module with maximum resolution of 240 × 320. It also supports 4-lane SPI communication.

The pin definition of the LCM interface is shown below.

Table 25: Pin Description of LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
LCD_SPI_MISO	133	DI	LCD SPI master-in slave-out	Master mode only.
LCD_SPI_MOSI	130	DO	LCD SPI master-out slave-in	
LCD_SPI_CLK	137	DO	LCD SPI clock	
LCD_SPI_CS	134	DO	LCD SPI chip select	
PWM	129	DO	LCD backlight enable	If the default function is unused, it can be used for PWM output. 1.8 V power domain.
LCD_RS	142	DO	LCD data/command selection	
LCD_RST	145	DO	LCD reset	
LCD_PWR_EN	131	DO	LCD and TP power supply enable control	
LCD_TE	143	DI	LCD tearing effect	

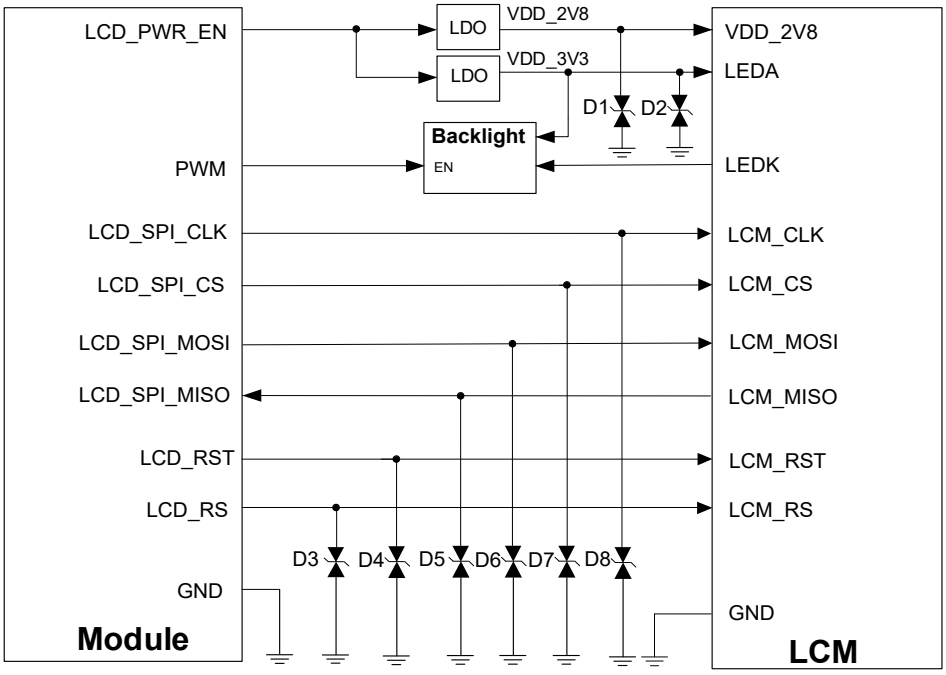


Figure 30: Reference Design of LCM Interface

4.10. Touch Panel Interface*

The module provides an I2C interface for connection with touch panel (TP) by default. Also, corresponding power supply pins, reset pins and interrupt pins are provided.

The pin definition of touch panel interface is illustrated below.

Table 26: Pin Description of Touch Panel Interface

Pin Name	Pin No.	I/O	Description	Comment
TP_I2C_SCL	138	OD	TP I2C serial clock	Pull each of them up to VDD_EXT with an external 2.2 kΩ resistor. If unused, keep them open.
TP_I2C_SDA	141	OD	TP I2C serial data	
LCD_PWR_EN	131	DO	LCD and TP power supply enable control	
TP_INT	135	DI	TP interrupt	

TP_RST	139	DO	TP reset

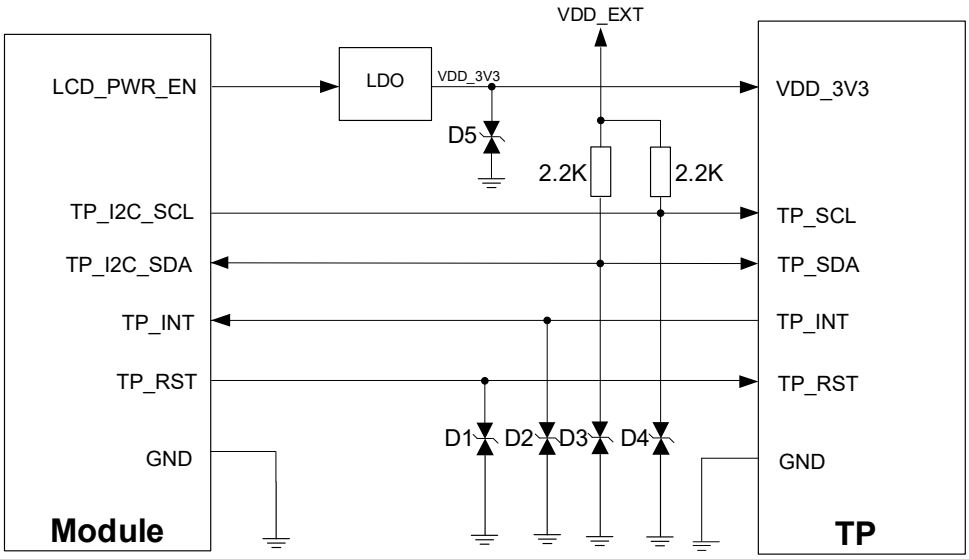


Figure 31: Reference Design of Touch Panel Interface

4.11. PCIe Interfaces

The module provides three PCIe interfaces. Key features of the PCIe interfaces are as below:

- *PCI Express Base Specification Revision 3.0* compliant.
- Data rate at 8 Gbps per lane for PCIe 3.0.
- PCIe0 and PCIe1 support 2 lanes, and PCIe2 supports 1 lane.
- PCIe0 supports RC and EP modes, but PCIe1 and PCIe2 only support RC mode.
- Can be used to connect to an external Ethernet IC (MAC and PHY) or Wi-Fi IC.

Table 27: Pin Description of PCIe Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCIE0_REFCLK_M	24	AIO	PCIe0 reference clock (-)	In RC mode, it is an output signal. In EP mode, it is an input signal. Require differential impedance of 100 Ω.
PCIE0_REFCLK_P	23	AIO	PCIe0 reference clock (+)	

PCIE0_RX0_M	28	AI	PCIe0 receive 0 (-)	Require differential impedance of 85 Ω. If unused, keep them open.
PCIE0_RX0_P	27	AI	PCIe0 receive 0 (+)	
PCIE0_TX0_M	16	AO	PCIe0 transmit 0 (-)	
PCIE0_TX0_P	15	AO	PCIe0 transmit 0 (+)	
PCIE0_RX1_M	32	AI	PCIe0 receive 1 (-)	
PCIE0_RX1_P	31	AI	PCIe0 receive 1 (+)	
PCIE0_TX1_M	20	AO	PCIe0 transmit 1 (-)	
PCIE0_TX1_P	19	AO	PCIe0 transmit 1 (+)	
PCIE0_RST_N	21	DIO	PCIe0 reset	1.8 V power domain by default. In RC mode, it is an output signal. In EP mode, it is an input signal.
PCIE0_WAKE_N	17	OD	PCIe0 wake up	1.8 V power domain by default. In RC mode, it is an input signal. In EP mode, it is an output signal.
PCIE0_CLKREQ_N	13	OD	PCIe0 clock request	
PCIE1_REFCLK_M	72	AO	PCIe1 reference clock (-)	Require differential impedance of 100 Ω.
PCIE1_REFCLK_P	71	AO	PCIe1 reference clock (+)	
PCIE1_RX0_M	76	AI	PCIe1 receive 0 (-)	Require differential impedance of 85 Ω. If unused, keep them open.
PCIE1_RX0_P	75	AI	PCIe1 receive 0 (+)	
PCIE1_TX0_M	64	AO	PCIe1 transmit 0 (-)	
PCIE1_TX0_P	63	AO	PCIe1 transmit 0 (+)	
PCIE1_RX1_M	79	AI	PCIe1 receive 1 (-)	
PCIE1_RX1_P	78	AI	PCIe1 receive 1 (+)	
PCIE1_TX1_M	68	AO	PCIe1 transmit 1 (-)	
PCIE1_TX1_P	67	AO	PCIe1 transmit 1 (+)	
PCIE1_RST_N	69	DO	PCIe1 reset	In RC mode, it is an output signal.

PCIE1_WAKE_N	65	OD	PCIe1 wake up	In RC mode, it is an input signal.
PCIE1_CLKREQ_N	61	OD	PCIe1 clock request	
PCIE2_REFCLK_M	48	AO	PCIe2 reference clock (-)	Require differential impedance of 100 Ω.
PCIE2_REFCLK_P	47	AO	PCIe2 reference clock (+)	
PCIE2_RX0_M	52	AI	PCIe2 receive 0 (-)	Require differential impedance of 85 Ω. If unused, keep them open.
PCIE2_RX0_P	51	AI	PCIe2 receive 0 (+)	
PCIE2_TX0_M	44	AO	PCIe2 transmit 0 (-)	
PCIE2_TX0_P	43	AO	PCIe2 transmit 0 (+)	
PCIE2_RST_N	45	DO	PCIe2 reset	In RC mode, it is an output signal.
PCIE2_WAKE_N	41	OD	PCIe2 wake up	In RC mode, it is an input signal.
PCIE2_CLKREQ_N	37	OD	PCIe2 clock request	

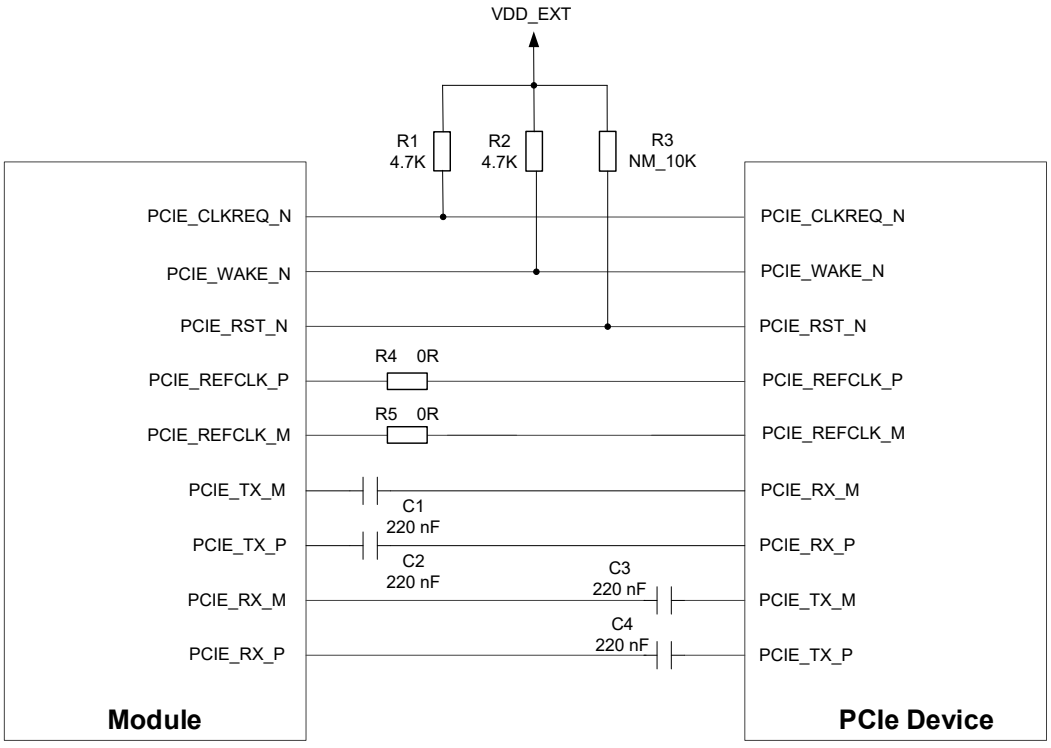


Figure 32: Reference Design of PCIe Interface Connection

To ensure the signal integrity of the PCIe interface, place C1 and C2 near the module and place C3 and

C4 near the PCIe device. Keep the traces as short as possible.

To ensure that the PCIe interface design meets PCIe specifications, you should follow the principles below:

- Route PCIe signal traces (Tx/Rx/REFCLK) as differential pairs with surrounded ground. The differential impedance should be 85 Ω ±10 % for Tx/Rx and 100 Ω ±10 % for REFCLK.
- PCIe signals must be protected from noise signals (clocks, DC-DC, RF and so forth). All other sensitive/high-speed signals and circuits must be routed far away from PCIe traces.
- For each differential pair, intra-lane length match should be less than 0.7 mm. The total bus length should be less than 300 mm for PCIe 3.0.
- The inter-lane length match, that is, the trace length matching among the reference clock, Tx and Rx pairs is not required.
- The spacing between Tx and Rx, and the spacing between PCIe lanes and all other signals, should be larger than 4 times of the trace width.
- PCIe Tx AC coupling capacitors can be anywhere along the trace, but better to be placed close to source or connector side to keep good signal integrity of main route on PCB. PCIe Tx AC coupling capacitors should be 220 nF for Gen 3 and 100 nF for Gen 2/Gen 1. Ensure not to stagger the capacitors. It will affect the differential integrity of the design and create EMI.
- In the case of trace serpentines, one trace of a differential pair must be routed to make up a length delta, then it must be routed at the source (breakout) – this ensures that traces stay differential thereafter.
- To reduce the probability for layer-to-layer manufacturing variation, minimize layer transitions on the main route (in other words, apply layer transitions only at module breakouts and connectors to ensure minimum layer transitions on the main route).

Table 28: PCIe Interface Trace Length Inside the Module (Unit: mm)

Pin No.	Pin Name	Length	Length Matching
24	PCIE0_REFCLK_M	TBD	TBD
23	PCIE0_REFCLK_P	TBD	TBD
28	PCIE0_RX0_M	TBD	TBD
27	PCIE0_RX0_P	TBD	TBD
16	PCIE0_TX0_M	TBD	TBD
15	PCIE0_TX0_P	TBD	TBD
32	PCIE0_RX1_M	TBD	TBD
31	PCIE0_RX1_P	TBD	TBD

20	PCIE0_TX1_M	TBD	TBD
19	PCIE0_TX1_P	TBD	TBD
72	PCIE1_REFCLK_M	TBD	TBD
71	PCIE1_REFCLK_P	TBD	TBD
76	PCIE1_RX0_M	TBD	TBD
75	PCIE1_RX0_P	TBD	TBD
64	PCIE1_TX0_M	TBD	TBD
63	PCIE1_TX0_P	TBD	TBD
79	PCIE1_RX1_M	TBD	TBD
78	PCIE1_RX1_P	TBD	TBD
68	PCIE1_TX1_M	TBD	TBD
67	PCIE1_TX1_P	TBD	TBD
48	PCIE2_REFCLK_M	TBD	TBD
47	PCIE2_REFCLK_P	TBD	TBD
52	PCIE2_RX0_M	TBD	TBD
51	PCIE2_RX0_P	TBD	TBD
44	PCIE2_TX0_M	TBD	TBD
43	PCIE2_TX0_P	TBD	TBD

NOTE

PCIe interfaces do not support hot-plug function.

4.12. SPIs

The module provides two SPIs: one is used for general SPI, and the other is used for LCM SPI. Both only support master mode with a maximum clock frequency up to 50 MHz.

The below table gives the pin description of general SPI. For the other used for LCM SPI, see ***Chapter 4.9*** for details.

Table 29: Pin Description of General SPI

Pin Name	Pin No.	I/O	Description	Comment
MAIN_SPI_CS	335	DO	SPI chip select	Master mode only. If unused, keep them open.
MAIN_SPI_CLK	331	DO	SPI clock	
MAIN_SPI_MOSI	327	DO	SPI master-out slave-in	
MAIN_SPI_MISO	323	DI	SPI master-in salve-out	

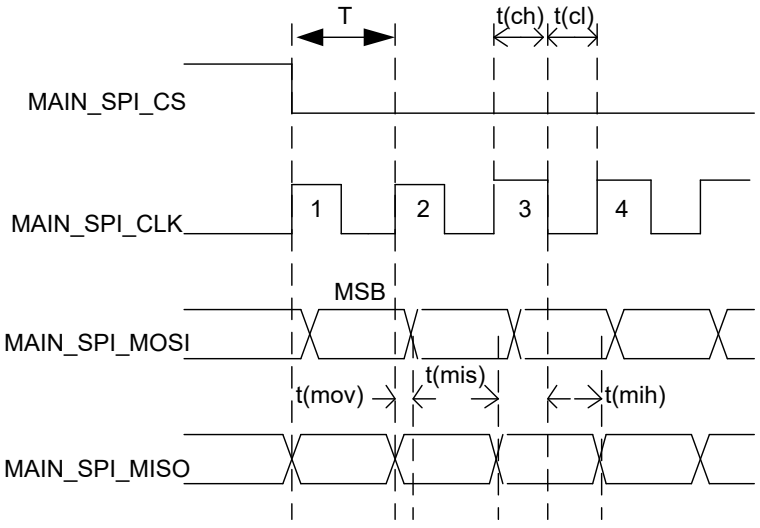


Figure 33: Timing of SPI

Table 30: Parameters of SPI Timing (Unit: ns)

Parameter	Description	Min.	Typ.	Max.
T	SPI clock cycle	TBD	TBD	TBD

t(ch)	SPI clock high-level period	TBD	TBD	TBD
t(cl)	SPI clock low-level period	TBD	TBD	TBD
t(mov)	Valid period of SPI master data output	TBD	TBD	TBD
t(mis)	Setup period of SPI master data input	TBD	TBD	TBD
t(mih)	Holding period of SPI master data input	TBD	TBD	TBD

The module provides a 1.8 V SPI. Use a voltage-level translator between the module and MCU if MCU is 3.3 V power domain. The following figure shows a reference design:

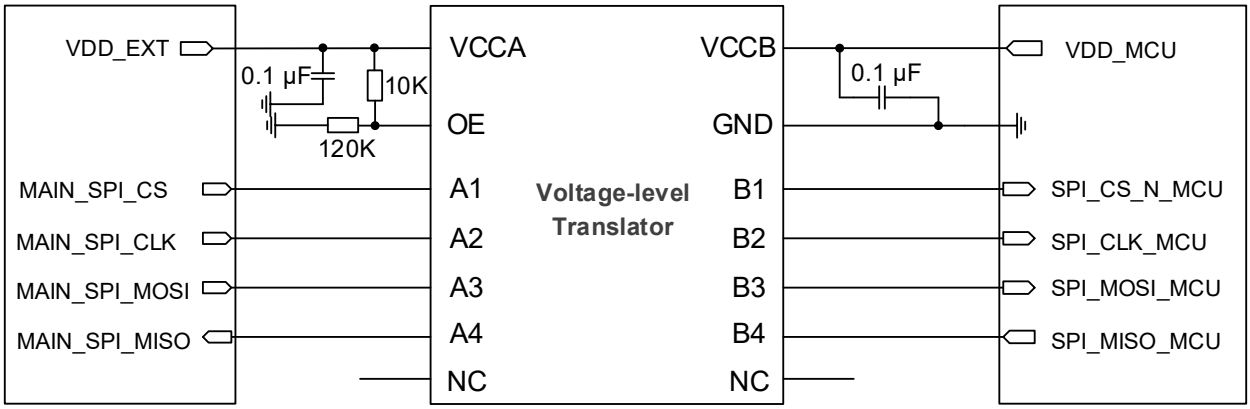


Figure 34: Reference Design of SPI with Translator Chip

4.13. GPIO

The module provides one GPIO:

Table 31: Pin Description of GPIO

Pin Name	Pin No.	I/O	Description
GPIO_90	156	DIO	General-purpose input/output

4.14. WWAN/WLAN Application Interface*

The module provides one WWAN/WLAN application interface for WLAN design. The following table shows the definition.

Table 32: Pin Definition of WWAN/WLAN Application Interface

Pin Name	Pin No.	I/O	Description	Comment
WLAN0_EN	25	DO	WLAN 5 GHz function enable control	1.8 V power domain by default.
WLAN0_PWR_EN	29	DO	WLAN 5 GHz power supply enable control	
WLAN1_EN	73	DO	WLAN 6 GHz function enable control	
WLAN1_PWR_EN	77	DO	WLAN 6 GHz power supply enable control	
WLAN2_EN	49	DO	WLAN 2.4 GHz function enable control	
WLAN2_PWR_EN	53	DO	WLAN 2.4 GHz power supply enable control	
WLAN_TX_EN_TO_LAA	217	DI	Notification from WLAN to LAA LNA when WLAN transmitting to set LAA LNA to isolation mode	
WLAN_TX_EN_TO_N79	197	DI	Notification from WLAN to n79 LNA when WLAN transmitting to set n79 LNA to isolation mode	These pins are used for the coexistence of n79 and Wi-Fi 5 GHz. If n79 is needed in your future project with Quectel 5G modules, then these pins shall be pulled out and reserved; otherwise, these pins can be NC.
N79_TX_EN_TO_WLAN	201	DO	Notification from transceiver to WLAN when n79 transmitting to set WLAN 5G to isolation mode	
COEX_RXD	10	DI	Coexistence UART receive	Only for Qualcomm platform. Signal interface used for WWAN/WLAN coexistence mechanism. 1.8 V power domain by default.
COEX_TXD	14	DO	Coexistence UART transmit	
WLAN_PA_MUTING	34	DO	GPIO from SDX to disable WLAN PA	1.2 V power domain.

WLAN_LAA_AS_EN	26	DO	GPIO allows transceiver to power on monitoring for Wi-Fi SoC when WLAN is sleeping or disabled. Additionally, the control logic in WLAN AON domain allows transceiver to control 5G WLAN xLNA (LNA in FEMs)	
WLAN_LAA_RX	30	DO	SoC signal to set 5G xLNA to high gains or high isolation when both chains (LAA and 5G WLAN) are active simultaneously. No individual control for each chain.	
BT_EN	38	DO	Bluetooth enable control	1.8 V power domain.

4.15. Control Signal

Pin definition of control signal is listed as follows:

Table 33: Pin Description of Control Signal

Pin Name	Pin No.	I/O	Description
W_DISABLE#	206	DI	Airplane mode control

4.15.1. W_DISABLE#

The module provides W_DISABLE# to enable or disable RF function. W_DISABLE# is pulled up by default. When the voltage level of W_DISABLE# is high, you can send **AT+CFUN=<fun>** to set the module's operating mode. Driving W_DISABLE# low will set the module to airplane mode.

Table 34: W_DISABLE# AT Command Configuration Information

W_DISABLE# Level Status	AT Command	RF Function Status	Module Operating Mode
High	**AT+CFUN=1**	Enabled	Full functionality mode
	AT+CFUN=0	Disabled	Minimum functionality mode

	AT+CFUN=4	Disabled	Airplane mode
Low	**AT+CFUN=0** **AT+CFUN=1** **AT+CFUN=4**	Disabled	Airplane mode

NOTE

The execution of **AT+CFUN** does not affect GNSS function.

4.16. Indication Signals

Pin definition of indication signals is listed as follows:

Table 35: Pin Description of Indication Signals

Pin Name	Pin No.	I/O	Description
STATUS	311	DO	Indicate the module's operation status
NET_STATUS	307	DO	Indicate the module's network activity status
SLEEP_IND	315	DO	Indicate the module’s sleep mode
NET_MODE	303	DO	Indicate the module’s network registration mode

4.16.1. Network Status Indication

The module provides two network status indication pins: NET_MODE and NET_STATUS. Both can drive corresponding LEDs.

Table 36: Network Status Indication Pin Level and Module Network Status

Pin Name	NET_MODE/NET_STATUS Level Status	Module Network Status
NET_MODE	Always high	Registered on network
	Always low	Others
NET_STATUS	Blink slowly (200 ms high/1800 ms low)	Network searching

	Blink slowly (1800 ms high/200 ms low)	Idle
	Blink quickly (125 ms high/125 ms low)	Data transmission is ongoing
	Always high	Voice calling
	Always low	Minimum functionality mode

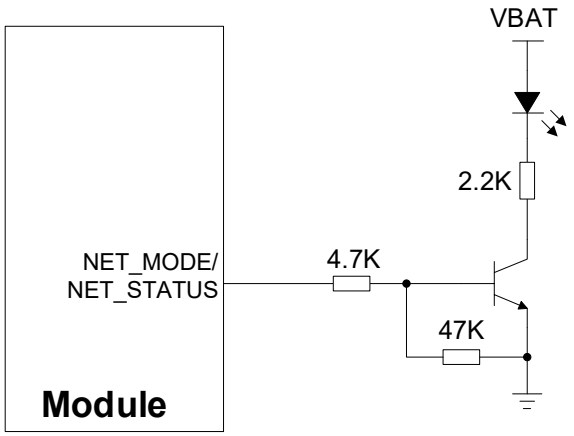


Figure 35: Reference Design of Network Status Indication

4.16.2. STATUS

The STATUS is used for indicating module's operation status. It outputs high level when the module is turned on successfully. A reference circuit is shown as below.

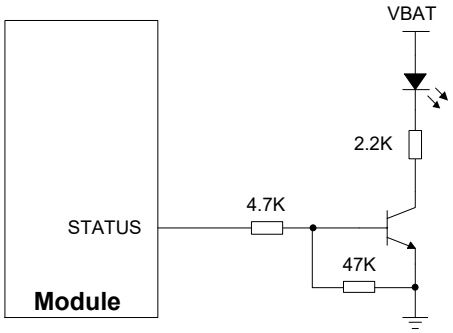


Figure 36: Reference Design of STATUS

4.17. MAIN_RI*

AT+QCFG="risignaltype","physical" can be used to configure MAIN_RI behavior. No matter on which port (USB AT port or USB modem port) a URC is presented, the URC will trigger MAIN_RI behavior.

NOTE

AT+QURCCFG can be used to set the USB AT port or USB modem port as URC output port. The USB AT port is the URC output port by default.

In addition, MAIN_RI behavior can be configured flexibly. The default behavior of MAIN_RI is shown as below.

Table 37: MAIN_RI Default Behavior

Module Status	MAIN_RI Level Status
Idle	High level
When a new URC returns	MAIN_RI outputs at least 120 ms low level. After the module outputs the data, the level status will become high.

If there is an incoming call, MAIN_RI behavior can be changed via **AT+QCFG="urc/ri/ring"**.

5 RF Specifications

Appropriate antenna type and design with matched antenna parameters should be used depending on application scenario. Comprehensive functional testing of RF design is required before mass production of terminal products. This chapter is provided for illustrative purposes only. Analysis and evaluation are necessary when designing target products.

5.1. Cellular Network

5.1.1. Antenna Interfaces & Frequency Bands

Table 38: Pin Description of Cellular Antenna Interfaces for RG650E-NA/RG650V-NA

Pin Name	Pin No.	I/O	Description	Frequency Range (MHz)
ANT1	185	AIO	**Antenna 1 interface:** - **5G NR**: n41 TRX1 & n77/n78 TRX0 - **LTE**: LMB_TRX0 & HB_DRX & UHB_TRX0 - **Reframing**: LMB_TRX0 & HB_TRX1	**LB**: 617–960 **MHB**: 1427–2690 **UHB**: 3300–4200
ANT3	203	AIO	**Antenna 3 interface:** - **5G NR**: n41 DRX MIMO & n77/n78 PRX MIMO - **LTE**: LMB_PRX MIMO & HB_DRX MIMO & UHB_PRX MIMO - **Reframing**: LMB_PRX MIMO & HB_DRX MIMO	**LB**: 617–960 **MHB**: 1427–2690 **UHB**: 3300–4200
ANT5	227	AIO	**Antenna 5 interface:** - **5G NR**: n41 PRX MIMO & n77/n78 DRX MIMO - **LTE**: LMB_DRX MIMO & HB_PRX MIMO & UHB_DRX MIMO - **Reframing**: LMB_DRX MIMO & HB_PRX MIMO	**LB**: 617–960 **MHB**: 1427–2690 **UHB**: 3300–4200

ANT7	251	AIO	**Antenna 7 interface:** - **5G NR**: n41 TRX0 & n77/n78 TRX1 - **LTE**: LMB_TRX1 & HB_TRX0 & UHB_TRX1 - **Reframing**: LMB_TRX1 & HB_TRX0	**LB**: 617–960 **MHB**: 1427–2690 **UHB**: 3300–4200
ANT0	177	AIO	**Antenna 0 interface:** - **5G NR**: n38/n41/n48/n77/n78 HORxD1	**n38/n41**: 2496–2690 **UHB**: 3300–4200
ANT2	192	AIO	**Antenna 2 interface:** - **5G NR**: n38/n41/n48/n77/n78 HORxD2	**n38/n41**: 2496–2690 **UHB**: 3300–4200
ANT4	215	AIO	**Antenna 4 interface:** - **5G NR**: n38/n41/n48/n77/n78 HORxD3	**n38/n41**: 2496–2690 **UHB**: 3300–4200
ANT6	239	AIO	**Antenna 6 interface:** - **5G NR**: n38/n41/n48/n77/n78 HORxD4	**n38/n41**: 2496–2690 **UHB**: 3300–4200

Table 39: Pin Description of Cellular Antenna Interfaces for RG650E-EU*/RG650V-EU

Pin Name	Pin No.	I/O	Description	Frequency Range (MHz)
ANT1	185	AIO	**Antenna 1 interface:** - **5G NR**: n41 TRX1 & n77/n78 TRX0 - **LTE**: LMB_TRX0 & HB_DRX & UHB_TRX0 - **Reframing**: LMB_TRX0 & HB_TRX1 - **WCDMA**: LMB_TRX	**LB**: 617–960 **MHB**: 1427–2690 **UHB**: 3300–4200
ANT3	203	AIO	**Antenna 3 interface:** - **5G NR**: n41 DRX MIMO & n77/n78 PRX MIMO - **LTE**: LMB_PRX MIMO & HB_DRX MIMO & UHB_PRX MIMO - **Reframing**: LMB_PRX MIMO & HB_DRX MIMO	
ANT5	227	AIO	**Antenna 5 interface:** - **5G NR**: n41 PRX MIMO & n77/n78 DRX MIMO - **LTE**: LMB_DRX MIMO & HB_PRX MIMO & UHB_DRX MIMO - **Reframing**: LMB_DRX MIMO & HB_PRX MIMO	

ANT7	251	AIO	**Antenna 7 interface:** - **5G NR**: n41 TRX0 & n77/n78 TRX1 - **LTE**: LMB_TRX1 & HB_TRX0 & UHB_TRX1 - **Reframing**: LMB_TRX1 & HB_TRX0 - **WCDMA**: LMB_DRX	
ANT0	177	AIO	**Antenna 0 interface:** - **5G NR**: n38/n40/n41/n77/n78 HORxD1	**n38/n40/n41**: 2300–2690 **UHB**: 3300–4200
ANT2	192	AIO	**Antenna 2 interface:** - **5G NR**: n38/n40/n41/n77/n78 HORxD2	**n38/n40/n41**: 2300–2690 **UHB**: 3300–4200
ANT4	215	AIO	**Antenna 4 interface:** - **5G NR**: n38/n40/n41/n77/n78 HORxD3	**n38/n40/n41**: 2300–2690 **UHB**: 3300–4200
ANT6	239	AIO	**Antenna 6 interface:** - **5G NR**: n38/n40/n41/n77/n78 HORxD4	**n38/n40/n41**: 2300–2690 **UHB**: 3300–4200

NOTE

1. The impedance of antenna interfaces is 50 Ω.
2. LTE L/M/H/UHB_TRX1 is activated when 5G NR FDD L/M/H/UHB bands are supported in NSA mode.
3. TRX0/1 = TX0/1 + PRX/DRX.
4. ANT0/2/4/6 are used for 8Rx optional design, which supports 4 × 8 MIMO that means 8Rx with 4 × 4 MIMO + 4HORxD.

5.1.2. Antenna Tuner Control Interfaces*

The module can use GRFC (generic RF control) interface to control external antenna tuner.

Table 40: Pin Description of Antenna Tuner Control Interfaces

Pin Name	Pin No.	I/O	Description	Comment
SDR_GRFC11	241	DO	GRFC interfaces dedicated for external antenna tuner control	1.8 V power domain. If unused, keep them open.
SDR_GRFC12	237	DO		

Table 41: Truth Table of Antenna Tuner Control Interfaces

SDR_GRFC11 Level	SDR_GRFC12 Level	Frequency Range (Unit: MHz)	Band
Low	Low	TBD	TBD
Low	High	TBD	TBD
High	Low	TBD	TBD
High	High	TBD	TBD

5.1.3. Transmitting Power

Table 42: RF Transmitting Power

Mode	Frequency Band	Max.	Min.
WCDMA [9]	WCDMA bands	23 dBm ±2 dB (Class 3)	< -50 dBm
LTE	LTE HPUE bands [10] (B38/B41/B42/B43)	26 dBm +2/-3 dB (Class 2)	< -40 dBm
	LTE other bands	23 dBm ±2 dB (Class 3)	< -40 dBm
5G NR	5G NR n38/n41/n77/n78	29 dBm +2/-3 dB (Class 1.5)	< -40 dBm
	5G NR other Sub-6 bands	23 dBm ±2 dB (Class 3)	< -40 dBm
	5G NR HPUE bands [11] – **RG650E-NA/RG650V-NA:** n2/n5/n7/n25/n38/n41/n66/n71/n77/n78 – **RG650E-EU*/RG650V-EU:** n1/n3/n5/n7/n28/n38/n40/n41/n77/n78	26 dBm +2/-3 dB (Class 2)	< -40 dBm

NOTE

For 5G NR bands, see the specifications as described in *Clause 6.3.1* of *TS 38.101-1*.

[9] WCDMA is only supported by RG650E-EU* and RG650V-EU.
[10] LTE HPUE is only for single carrier.
[11] n1/n3/n5/n7/n28/n40 HPUE of RG650E-EU*/RG650V-EU and n2/n5/n7/n25/n66/n71 HPUE of RG650E-NA/RG650V-NA are achieved via dual Tx. Each Tx chain can only support Class 3 (23 dBm ±2 dB).

5.1.4. Receiver Sensitivity

Table 43: Conducted RF Receiver Sensitivity of RG650E-NA/RG650V-NA (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)			3GPP Requirements (SIMO)
	Primary	Diversity	SIMO [12]	
LTE-FDD B2 (10 MHz)	-97.8	-98	-100.8	-94.3
LTE-FDD B4 (10 MHz)	-97	-97.2	-100.1	-96.3
LTE-FDD B5 (10 MHz)	-98.2	-98.5	-101.3	-94.3
LTE-FDD B7 (10 MHz)	-95.3	-95.7	-98.1	-94.3
LTE-FDD B12 (10 MHz)	-98.3	-98.6	-101.3	-93.3
LTE-FDD B13 (10 MHz)	-97.5	-98	-100.7	-93.3
LTE-FDD B14 (10 MHz)	-97.6	-98	-100.7	-93.3
LTE-FDD B17 (10 MHz)	-98.3	-98.6	-101.3	-93.3
LTE-FDD B25 (10 MHz)	-97.6	-98.1	-100.9	-92.8
LTE-FDD B26 (10 MHz)	-98	-98.3	-101.1	-93.8
LTE-FDD B29 (10 MHz)	-98.5	-99	-101.6	TBD
LTE-FDD B30 (10 MHz)	-95	-95.3	-98.2	-95.3
LTE-TDD B38 (10 MHz)	-95.9	-95.8	-98.9	-96.3
LTE-TDD B41 (10 MHz)	-95.8	-95.6	-98.5	-94.3
LTE-TDD B42 (10 MHz)	-98.2	-98.4	-101.1	-95.0
LTE-TDD B43 (10 MHz)	-98.2	-98.4	-101.1	-95.0
LTE-TDD B48 (10 MHz)	-98.4	-98.6	-101.3	-95.0
LTE-FDD B66 (10 MHz)	-97.5	-97.3	-100.3	-95.8
LTE-FDD B71 (10 MHz)	-98.4	-98.9	-101.5	-93.5
5G NR FDD n2 (20 MHz)	-93.2	-93.3	-99.2	-94.5

[12] For the SIMO receiver sensitivity, LTE bands are tested with 2 Rx antennas, 5G n2/n7/n25/n30/n38/n41/n48/n66/n70/n77/n78 bands are tested with 4 Rx antennas and 5G n5/n12/n13/n14/n26/n29/n71 bands are tested with 2 Rx antennas.

5G NR FDD n5 (20 MHz)	-94.5	-94.3	-97.3	-90.8
5G NR FDD n7 (40 MHz)	-87.8	-89.6	-95.1	-91.3
5G NR FDD n12 (10 MHz)	-98.2	-98.5	-101.2	-93.8
5G NR FDD n13 (10 MHz)	-97.5	-98.2	-100.5	TBD
5G NR FDD n14 (10 MHz)	-97.6	-98.2	-100.5	-93.8
5G NR FDD n25 (20 MHz)	-93.7	-93.9	-99.7	-90.3
5G NR FDD n26 (20 MHz)	-94.5	-94.3	-97.4	-87.6
5G NR FDD n29 (10 MHz)	-98	-98.2	-100.9	TBD
5G NR FDD n30 (10 MHz)	-94.8	-95.3	-101	-95.8
5G NR TDD n38 (40 MHz)	-89.4	-89.7	-96.2	-93.4
5G NR TDD n41 (100 MHz)	-85.2	-85.3	-92	-84.7
5G NR TDD n48 (40 MHz)	-92.6	-92.5	-98.4	-92.1
5G NR FDD n66 (40 MHz)	-91.7	-91.5	-97.2	-93
5G NR FDD n70 (20 MHz)	-94.5	-94.4	-100.2	-93.8
5G NR FDD n71 (20 MHz)	-95.1	-95.6	-98.1	-86.0
5G NR TDD n77 (100 MHz)	-87.3	-87.1	-93.1	-87.3
5G NR TDD n78 (100 MHz)	-88	-88.1	-94.1	-87.8

Table 44: Conducted RF Receiver Sensitivity of RG650E-EU*/RG650V-EU (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)			3GPP Requirement (SIMO)
	Primary	Diversity	SIMO [13]	
WCDMA B1	-109.4	-109.5	-112	-106.7
WCDMA B5	-110.5	-110.5	-113.5	-104.7
WCDMA B8	-110.5	-110.5	-113.5	-103.7
LTE-FDD B1 (10 MHz)	-96.5	-97.0	-99.8	-96.3
LTE-FDD B3 (10 MHz)	-96.2	-96	-99	-93.3
LTE-FDD B5 (10 MHz)	-98	-98.8	-101.2	-94.3
LTE-FDD B7 (10 MHz)	-95.2	-96	-98.5	-94.3
LTE-FDD B8 (10 MHz)	-98	-99	-101	-93.3
LTE-FDD B20 (10 MHz)	-97.8	-98.0	-101	-93.3
LTE-FDD B28 (10 MHz)	-96.8	-97.2	-99.8	-94.8
LTE-FDD B32 (10 MHz)	TBD	TBD	TBD	TBD
LTE-TDD B38 (10 MHz)	-95.3	-96	-98.2	-96.3
LTE-TDD B40 (10 MHz)	-94.8	-95	-97.8	-96.3
LTE-TDD B41 (10 MHz)	-95.3	-95.8	-98.2	-94.3
LTE-TDD B42 (10 MHz)	-97.0	-98	-100	-95.0
LTE-TDD B43 (10 MHz)	-96.8	-97.8	-99.8	-95.0
LTE-FDD B71 (10 MHz)	-97.8	-98	-100.9	-93.5
5G NR FDD n1 (40 MHz)	-90.2	-90.5	-96	-93.3
5G NR FDD n3 (40 MHz)	-89	-89.5	-95.6	-85
5G NR FDD n5 (20 MHz)	-95	-95.5	-98.5	-90.8
5G NR FDD n7 (40 MHz)	-89.5	-90	-96.8	-91.3
5G NR FDD n8 (20 MHz)	-95.5	-96.2	-98.5	-90.0

[13] For the SIMO receiver sensitivity, WCDMA and LTE bands are tested with 2 Rx antennas, and 5G n1/n3/n7/n38/n40/n41/n77/n78 bands are tested with 4 Rx antennas and 5G n5/n8/n20/n28/n75/n76 bands are tested with 2 Rx antennas.

5G NR FDD n20 (20 MHz)	-95.2	-95.4	-98.2	-89.8
5G NR FDD n26 (20 MHz)	-95.5	-95.8	-98.5	-87.6
5G NR FDD n28 (30 MHz)	-93.0	-93.3	-96.5	-78.5
5G NR TDD n38 (40 MHz)	-90.5	-90	-97.0	-93.4
5G NR TDD n40 (100 MHz)	-84.5	-84.5	-91.5	-90.3
5G NR TDD n41 (100 MHz)	-85.0	-85.5	-92.0	-87.4
5G NR FDD n71 (20 MHz)	-95	-95	-98.0	-86.0
5G NR FDD n75 (20 MHz)	TBD	TBD	TBD	-93.8
5G NR FDD n76 (5 MHz)	TBD	TBD	TBD	-100
5G NR TDD n77 (100 MHz)	-87.5	-88	-93.8	-87.3
5G NR TDD n78 (100 MHz)	-88	-88.5	-94	-87.8

5.1.5. Reference Design

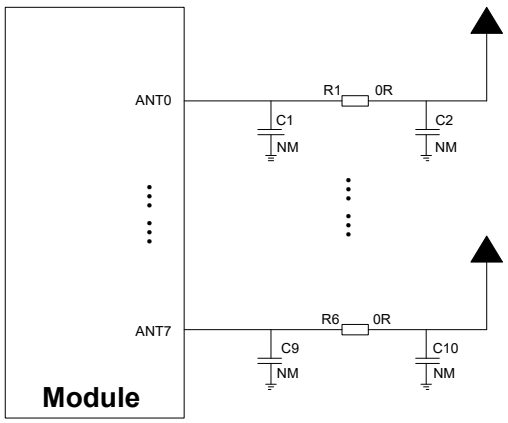


Figure 37: Reference Design of Cellular Antennas

NOTE

1. Use a π-type circuit for all the antenna circuits to facilitate future debugging.
2. Keep the impedance of the cellular antennas (ANT0–ANT7) traces as 50 Ω when routing.

3. Keep at least 15 dB isolation between cellular antennas to improve the receiver sensitivity, and at least 20 dB isolation between 5G NR UL MIMO antennas.
4. The isolation between each antenna trace on PCB is recommended to be more than 75 dB.
5. Keep digital circuits such as switch mode power supply, (U)SIM card, USB interface, camera module, display connector and SD card away from the antenna traces.
6. It is recommended that the straight-line distance between the antenna and the module be greater than 15 mm to achieve better wireless performance of the whole device.

5.2. GNSS (Optional)

GNSS information of the module is as follows:

- Supports GPS, GLONASS, BDS, Galileo, QZSS positioning systems.
- Supports NMEA 0183 protocol and outputs NMEA sentences via USB interface (data update rate for positioning: 1–10 Hz, 1 Hz by default).
- The module's GNSS function is OFF by default. It must be ON via **AT+QGPS=1**.

For more details about GNSS function's technology and configurations, see ***document [4]***.

5.2.1. Antenna Interface & Frequency Bands

Table 45: Pin Description of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	271	AI	**GNSS antenna interface:** - L1/L2/L5	50 Ω impedance.

Table 46: GNSS Frequency (Unit: MHz)

Antenna Type	Frequency
GPS	1575.42 ±1.023 (L1) 1227.60 ±1.023 (L2) 1176.45 ±10.23 (L5)
GLONASS	1597.5–1605.8
BDS	1561.098 ±2.046 (B1I)
Galileo	1575.42 ±2.046 (E1) 1176.45 ±10.23 (E5a)

QZSS	1575.42 ±1.023 (L1) 1176.45 ±10.23 (L5)

5.2.2. GNSS Performance

Table 47: GNSS Performance

Parameter	Mode	Condition	Typ.	Unit
Sensitivity	Acquisition	Autonomous	-147	dBm
	Reacquisition		-158	
	Tracking		-158	
TTFF	Cold start @ open sky	Autonomous	33.46	s
		XTRA start	8.12	
	Warm start @ open sky	Autonomous	33.49	
		XTRA start	1.22	
	Hot start @ open sky	Autonomous	1.09	
		XTRA start	0.82	
Accuracy	CEP-50	Autonomous @ open sky	1.5	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.2.3. Reference Design

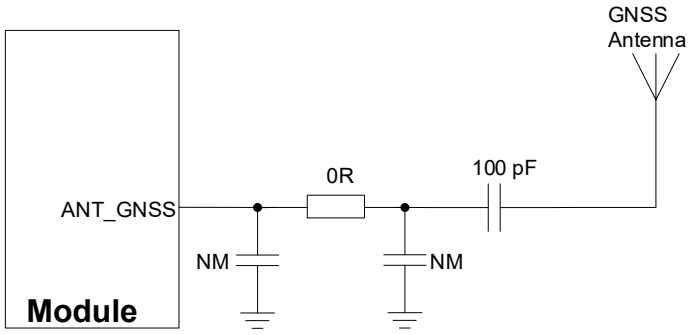


Figure 38: Reference Design of GNSS Antenna

NOTE

1. It is not recommended to add an external LNA when using a passive GNSS antenna.
2. Keep the characteristic impedance for ANT_GNSS trace as 50 Ω when routing.
3. Place the π-type matching components as close to the antenna as possible.
4. Keep digital circuits such as switch mode power supply, (U)SIM card, USB interface, camera module, display connector and SD card away from the antenna traces.
5. The isolation between each antenna trace on PCB is recommended to be more than 75 dB.
6. Keep at least 15 dB isolation between GNSS and cellular antennas to improve receiver sensitivity.
7. It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

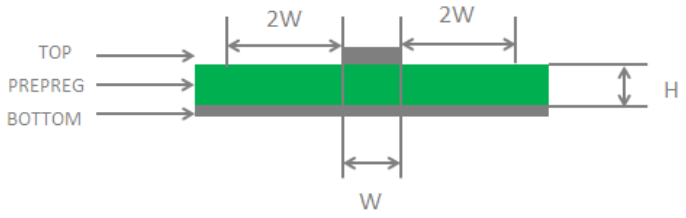


Figure 39: Microstrip Design on a 2-layer PCB

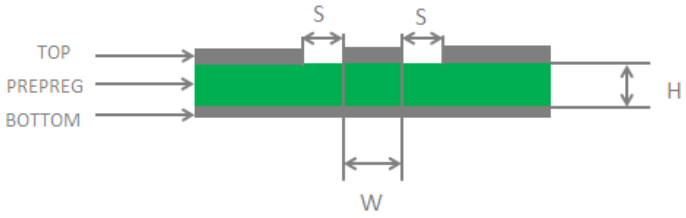


Figure 40: Coplanar Waveguide Design on a 2-layer PCB

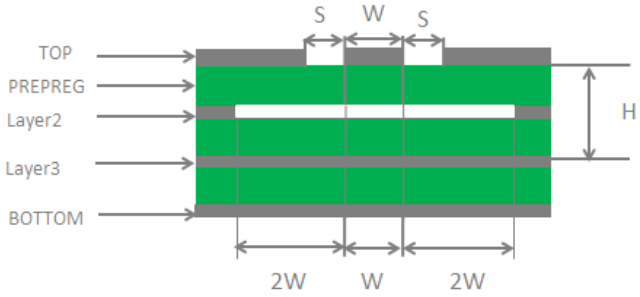


Figure 41: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

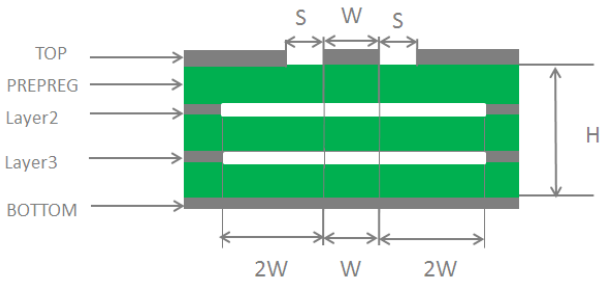


Figure 42: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [5].***

5.4. Requirements for Antenna Design

Table 48: Requirements for Antenna Design

Antenna Type	Requirements
GNSS (Optional)	• **Frequency ranges:** – L1: 1559–1609 MHz – L2: 1226–1229 MHz – L5: 1166–1187 MHz • RHCP or linear polarization • VSWR: ≤ 2 (Typ.)
	• **For passive antenna usage:** – Passive antenna gain: > 0 dBi
Cellular	• VSWR: ≤ 2 • Efficiency: > 30 % • Gain: 1 dBi • Max input power: 50 W • Input impedance: 50 Ω • Vertical polarization • **Cable insertion loss:** – < 1 dB: LB (< 1 GHz) – < 1.5 dB: MB (1–2.3 GHz) – < 2 dB: HB (> 2.3 GHz)

5.5. RF Connector Recommendation

The receptacle dimensions are illustrated as below.

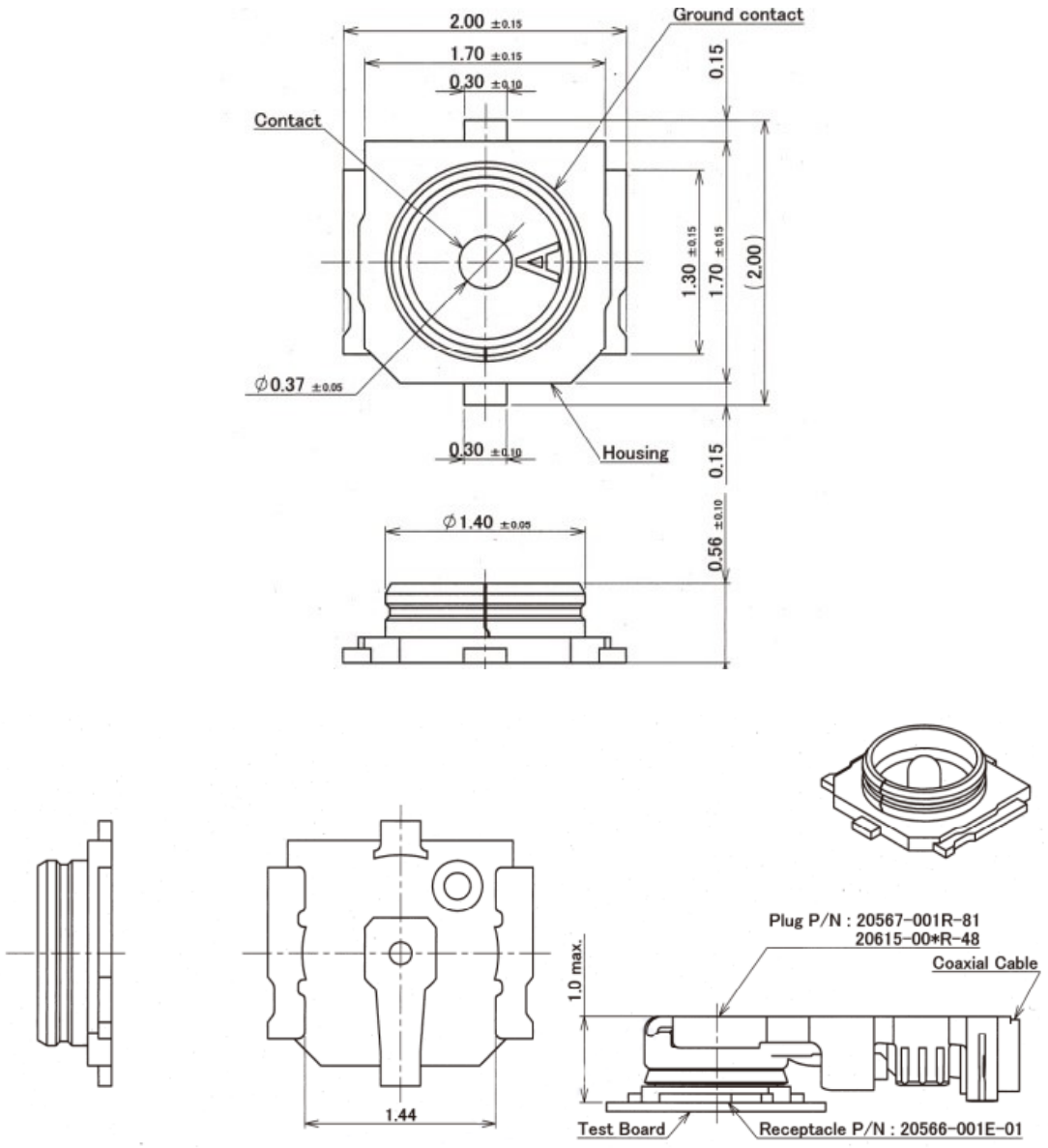


Figure 43: Dimensions of the Receptacles (Unit: mm)

The following figure shows the dimensions of mated plugs using Ø0.81 mm coaxial cables.

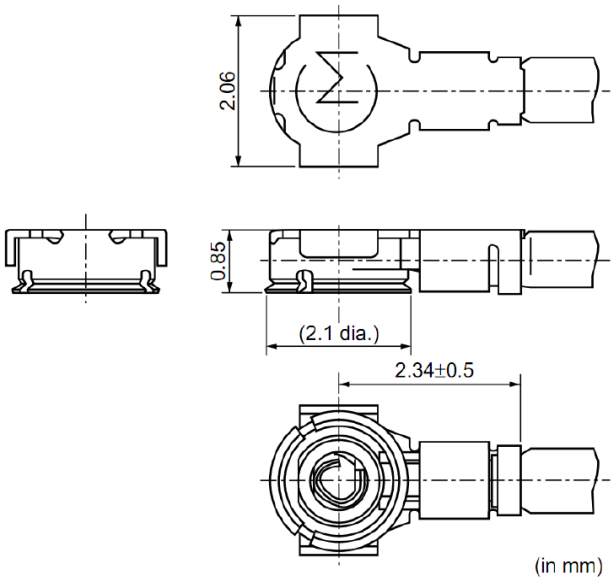


Figure 44: Dimensions of Mated Plugs Using Ø0.81 mm Coaxial Cables

5.5.1. Recommended RF Connector for Installation

5.5.1.1. Assemble Coaxial Cable Plug Manually

The illustration for plugging in a coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

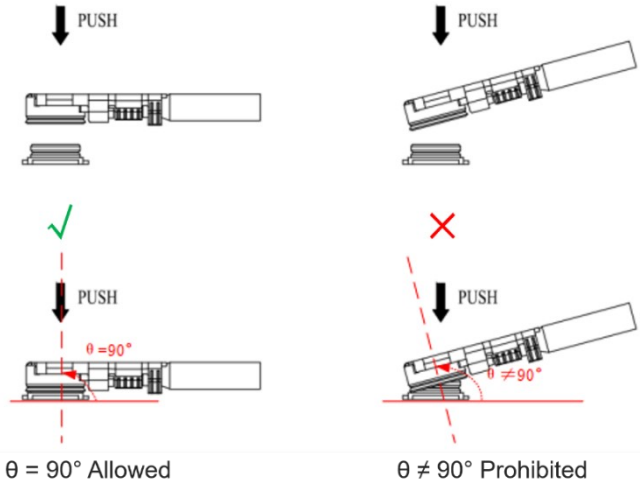


Figure 45: Plug in a Coaxial Cable Plug

The illustration of pulling out the coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

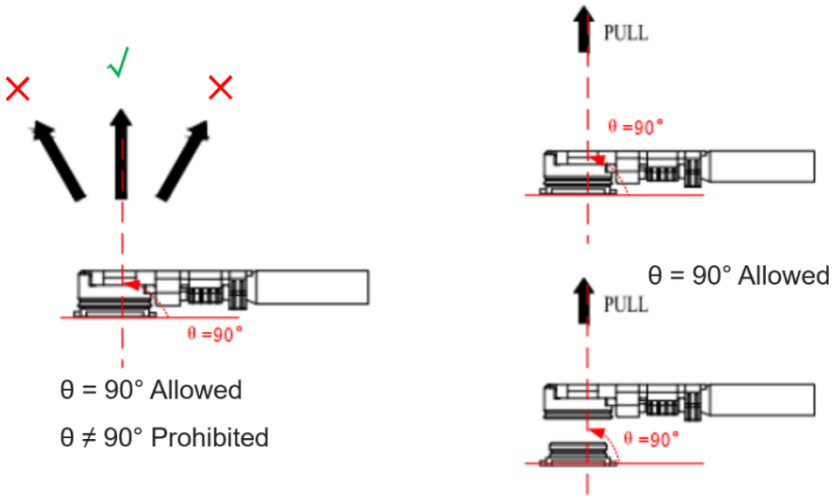


Figure 46: Pull out a Coaxial Cable Plug

5.5.1.2. Assemble Coaxial Cable Plug with Jig

The pictures of installing the coaxial cable plug with a jig is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

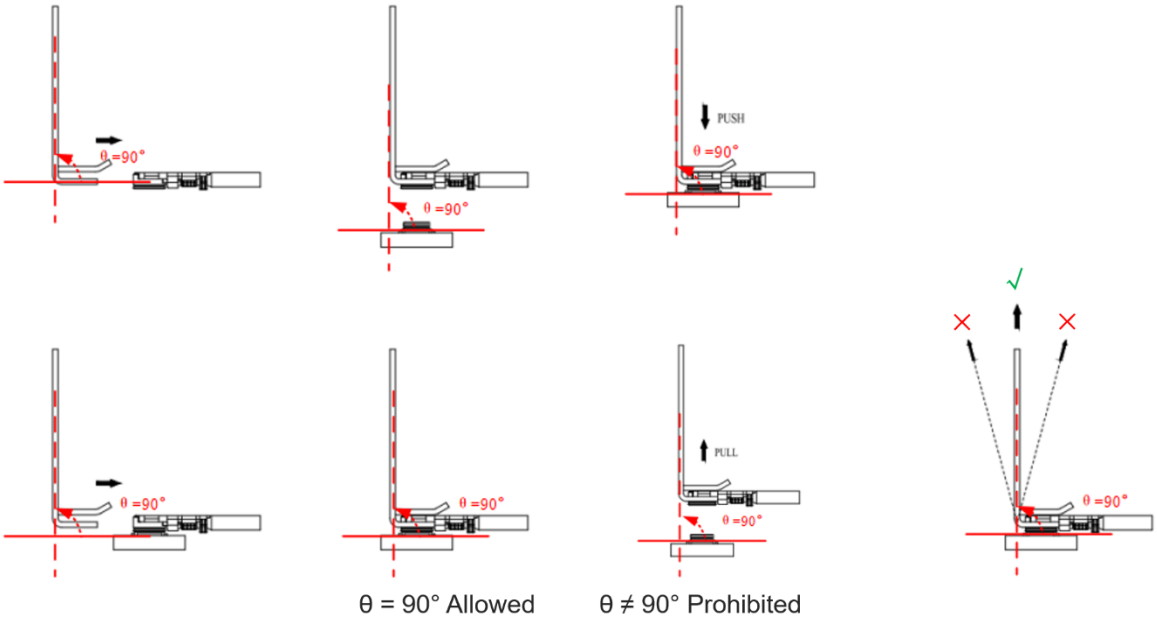


Figure 47: Install the Coaxial Cable Plug with Jig

5.5.2. Recommended Manufacturers of RF Connector and Cable

RF connectors and cables by I-PEX4 are recommended. For more details, visit https://www.i-pex.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Table 49: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Voltage at VBAT_RF/VBAT_BB	-0.5	6.0	V
Voltage at USB_VBUS	TBD	TBD	V
Voltage at digital pins	TBD	TBD	V
Voltage at ADC0	TBD	TBD	V
Voltage at ADC1	-0.5	2.2	V
Peak Current at VBAT_BB	-	TBD	A
Peak Current at VBAT_RF1/VBAT_RF2	-	TBD	A

6.2. Power Supply Ratings

Table 50: Module's Power Supply Ratings

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltage must be within this range	3.3	3.8	4.4	V
USB_VBUS	USB connection detection		3.3	5.0	5.25	V

6.3. Power Consumption

Table 51: RG650E-NA/RG650V-NA Power Consumption

Mode	Condition	Band/Combination	Typ.	Unit
Turn off	Turn off	-	TBD	μA
Sleep mode	**AT+CFUN=0** (USB 3.0 Suspend)	-	TBD	mA
	AT+CFUN=4 (USB 3.0 Suspend)	-	TBD	mA
	SA FDD PF = 64 (USB 3.0 Suspend)	-	TBD	mA
	SA TDD PF = 64 (USB 3.0 Suspend)	-	TBD	mA
Idle mode	SA PF = 64 (USB 2.0 active)	-	TBD	mA
	SA PF = 64 (USB 3.0 active)	-	TBD	mA
LTE	LTE LB @ 23 dBm	B5	TBD	mA
	LTE MB @ 23 dBm	B2	TBD	mA
	LTE HB @ 23 dBm	B7	TBD	mA
LTE CA	DL 3CA, 256QAM	CA_2A-66A-30A	TBD	mA
	UL 1CA, 256QAM			
	Tx power @ 23 dBm			
5G SA FR1 (1 Tx)	5G NR LB @ 23 dBm	n5	TBD	mA
	5G NR, MB @ 23 dBm	n2	TBD	mA
	5G NR HB @ 23 dBm	n7	TBD	mA
	5G NR UHB @ 26 dBm	n78	TBD	mA
5G SA FR1 (2 Tx)	5G NR UL 2 × 2 MIMO @ 26 dBm	n78	TBD	mA
5G SA FR1 CA	DL 2CA, 256QAM	n78C	TBD	mA
	UL 1CA, 256QAM			

	Tx power @ 26 dBm			
LTE + 5G FR1 EN-DC	LTE DL, 256QAM	DC_2A_n78A	TBD	mA
	LTE UL, QPSK			
	NR DL, 256QAM			
	NR UL, QPSK			
	LTE Tx Power @ 23 dBm			
	NR Tx Power @ 23 dBm			

Table 52: RG650E-EU*/RG650V-EU Power Consumption

Mode	Condition	Band/Combination	Typ.	Unit
Turn off	Turn off	-	TBD	μA
Sleep mode	**AT+CFUN=0** (USB 3.0 Suspend)	-	TBD	mA
	AT+CFUN=4 (USB 3.0 Suspend)	-	TBD	mA
	SA FDD PF = 64 (USB 3.0 Suspend)	-	TBD	mA
	SA TDD PF = 64 (USB 3.0 Suspend)	-	TBD	mA
Idle mode	SA PF = 64 (USB 2.0 active)	-	TBD	mA
	SA PF = 64 (USB 3.0 active)	-	TBD	mA
LTE	LTE LB @ 23 dBm	B5	585	mA
	LTE MB @ 23 dBm	B1	690	mA
	LTE HB @ 23 dBm	B7	820	mA
LTE CA	DL 3CA, 256QAM	CA_1A-3A-7A	700	mA
	UL 1CA, 256QAM			
	Tx power @ 23 dBm			
5G SA FR1	5G NR LB @ 23 dBm	n5	680	mA

(1 Tx)	5G NR, MB @ 23 dBm	n1	720	mA
	5G NR HB @ 23 dBm	n7	850	mA
	5G NR UHB @ 26 dBm	n78	420	mA
5G SA FR1 (2 Tx)	5G NR UL 2 × 2 MIMO @ 26 dBm	n78	580	mA
5G SA FR1 CA	DL 2CA, 256QAM	n78C	TBD	mA
	UL 1CA, 256QAM			
	Tx power @ 26 dBm			
LTE + 5G FR1 EN-DC	LTE DL, 256QAM	DC_3A_n78A	950	mA
	LTE UL, QPSK			
	NR DL, 256QAM			
	NR UL, QPSK			
	LTE Tx Power @ 23 dBm			
	NR Tx Power @ 23 dBm			

6.4. Digital I/O Characteristics

Table 53: 1.2 V I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	0.84	1.50
V_{IL}	Low-level input voltage	-0.30	0.36
V_{OH}	High-level output voltage	0.90	1.20
V_{OL}	Low-level output voltage	0	0.30

Table 54: 1.8 V I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	1.26	2.10
V_{IL}	Low-level input voltage	-0.30	0.54
V_{OH}	High-level output voltage	1.35	1.80
V_{OL}	Low-level output voltage	0	0.45

Table 55: (U)SIM High-voltage I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	TBD	TBD
V_{IL}	Low-level input voltage	TBD	TBD
V_{OH}	High-level output voltage	TBD	TBD
V_{OL}	Low-level output voltage	TBD	TBD

Table 56: (U)SIM Low-voltage I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	TBD	TBD
V_{IL}	Low-level input voltage	TBD	TBD
V_{OH}	High-level output voltage	TBD	TBD
V_{OL}	Low-level output voltage	TBD	TBD

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 57: ESD Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %; Unit: kV)

Test Point	Contact Discharge	Air Discharge
VBAT, GND	±5	±10
All antenna interfaces	±4	±8
Other interfaces	±0.5	±1

6.6. Operating and Storage Temperatures

Table 58: Operating and Storage Temperatures (Unit: °C)

Parameter	Min.	Typ.	Max.
Normal Operating Temperature [14]	-30	+25	+75
Extended Operating Temperature [15]	-40	-	+85
Storage Temperature	-40	-	+90

6.7. Thermal Dissipation

The module offers the best performance when all internal IC chips are working within their operating temperatures. When the IC chip reaches or exceeds the maximum junction temperature, the module may still work but the performance and functions (such as RF output power, data rate.) will be affected to a certain extent. Therefore, the thermal design should be maximally optimized to ensure all internal IC chips always work within the recommended operating temperature range.

The following principles for thermal consideration are provided for reference:

- Keep the module away from heat sources on your PCB, especially high-power components such as processor, power amplifier, and power supply.

[14] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

[15] To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module remains the ability to establish and maintain functions such as voice, SMS, emergency call, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module's related indicators will meet 3GPP specifications again.

- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Follow the principles below when the heatsink is necessary:
  - Do not place large size components in the area where the module is mounted on your PCB to reserve enough place for heatsink installation.
  - Attach the heatsink to the shielding cover of the module; In general, the base plate area of the heatsink should be larger than the module area to cover the module completely;
  - Choose the heatsink with adequate fins to dissipate heat;
  - Choose a TIM (Thermal Interface Material) with high thermal conductivity, good softness and good wettability and place it between the heatsink and the module;
  - Fasten the heatsink with four screws to ensure that it is in close contact with the module to prevent the heatsink from falling off during the drop, vibration test, or transportation.

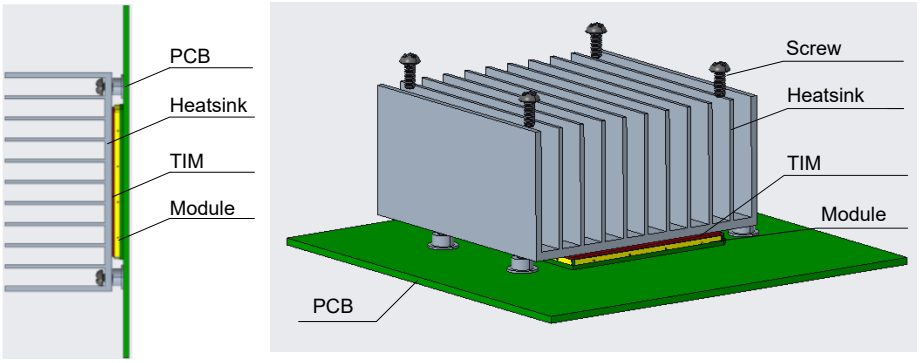


Figure 48: Placement and Fixing of the Heatsink

Table 59: Maximum Junction Temperature for Main Chips (Unit: °C)

BB	PMU	MCP	WTR	PA-1	PA-2
105	125	100	TBD	TBD	TBD

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

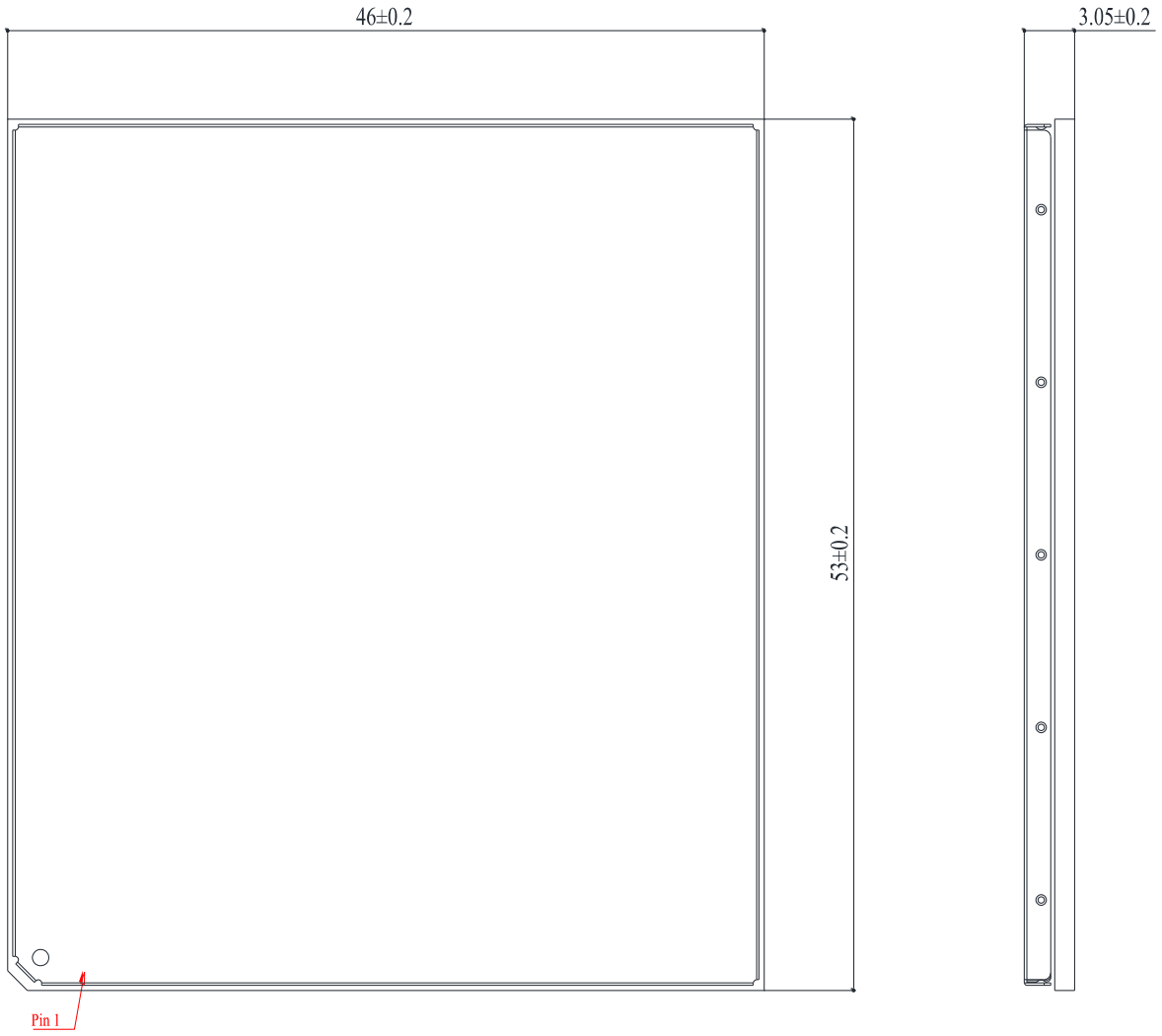


Figure 49: Top and Side Dimensions

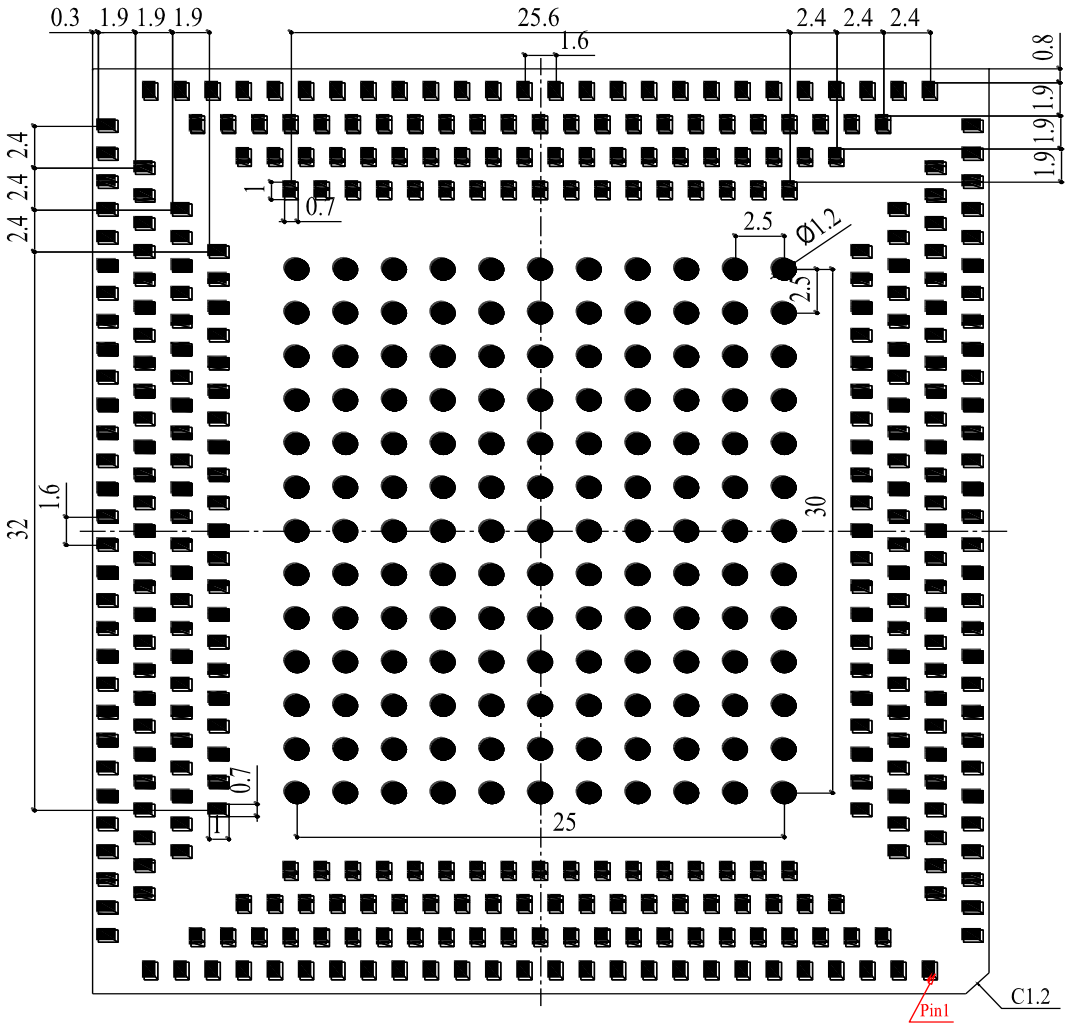


Figure 50: Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module refers to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

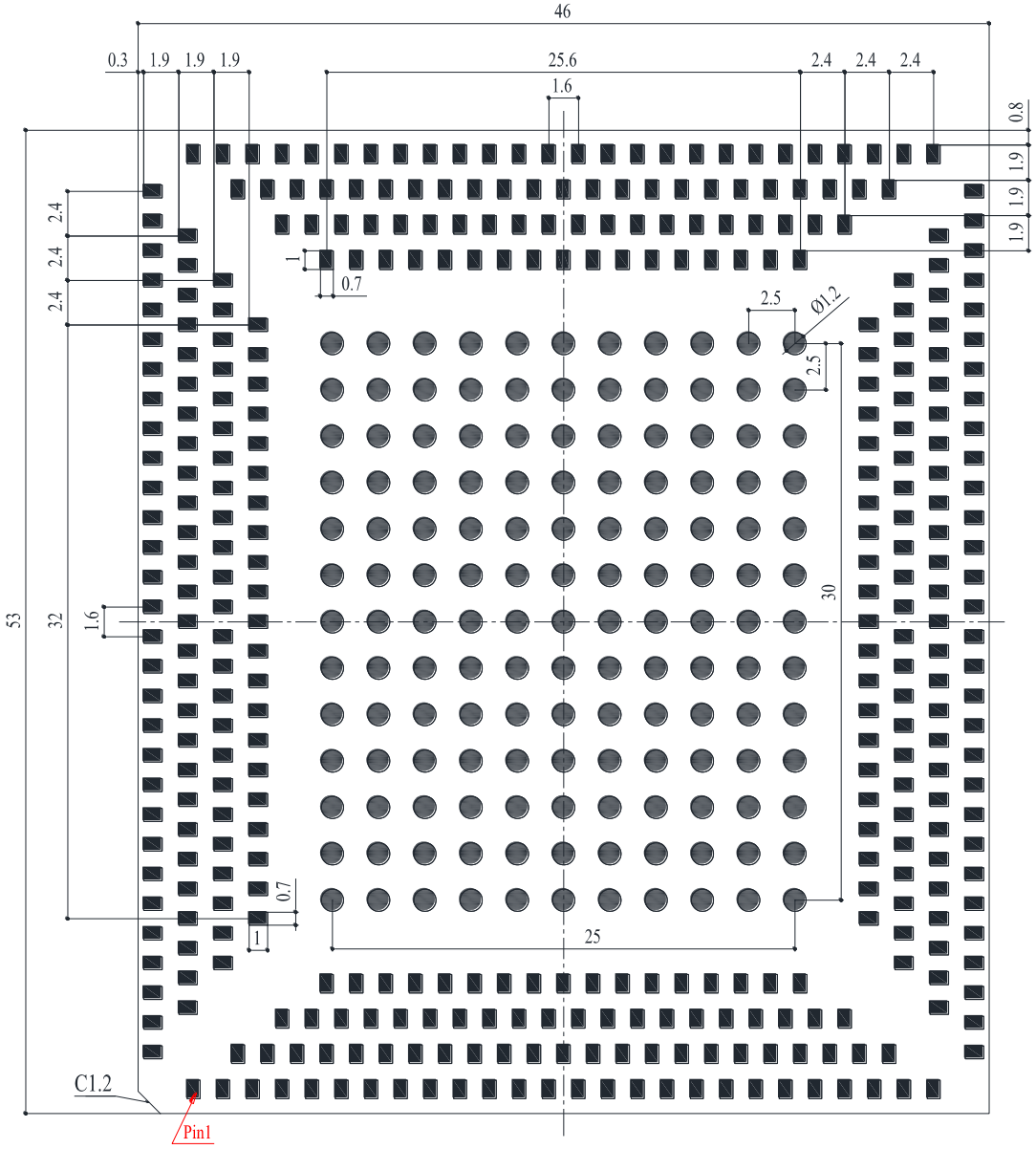


Figure 51: Recommended Footprint

NOTE

1. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.
2. To keep the reliability of the mounting and soldering, keep the motherboard thickness as at least 1.2 mm.

7.3. Top and Bottom Views

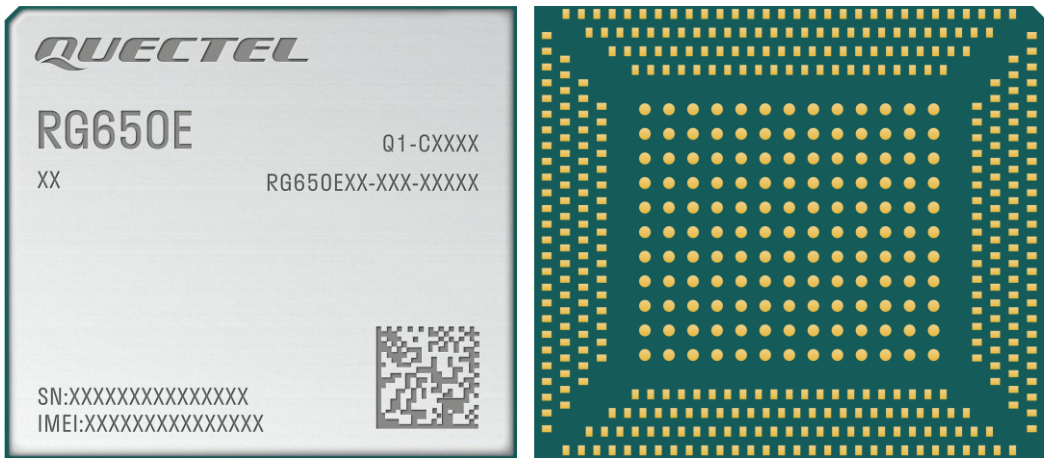


Figure 52: Top & Bottom Views of RG650E Series

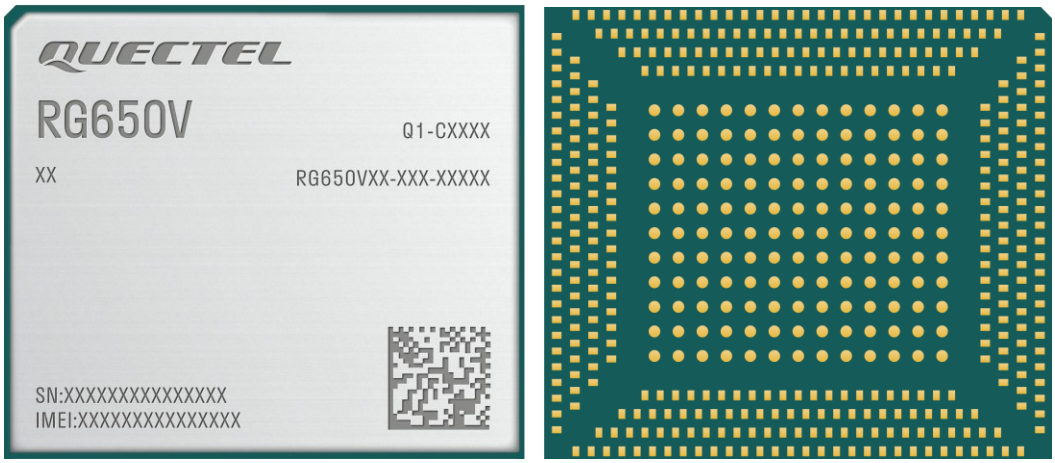


Figure 53: Top & Bottom Views of RG650V Series

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [16] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[16] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see ***document [6].***

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below:

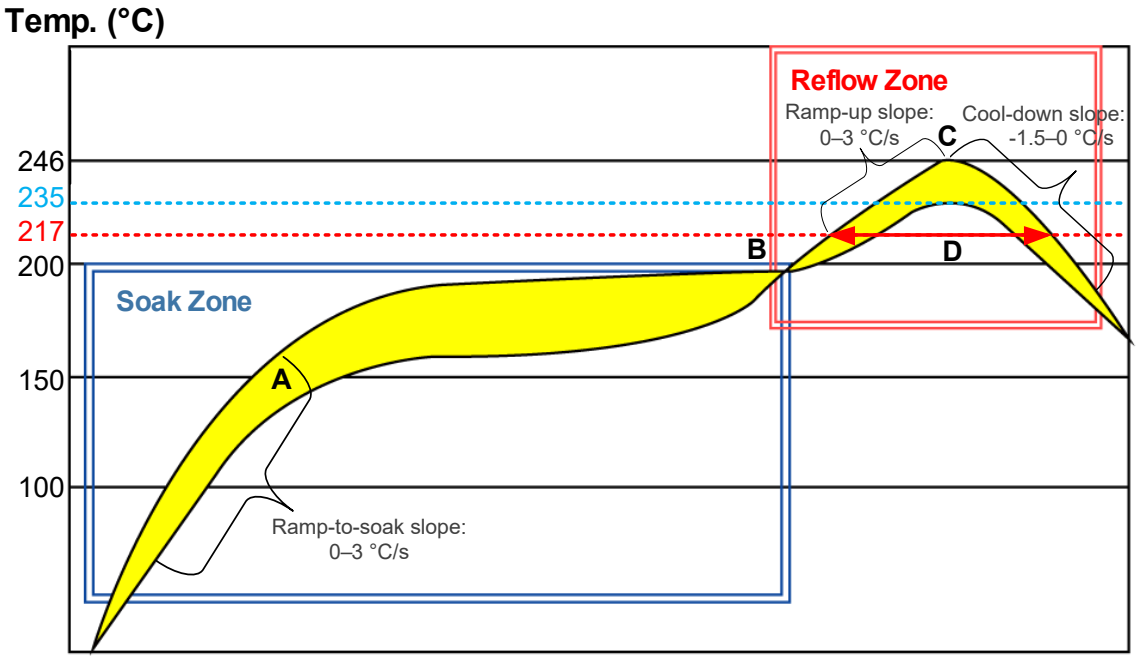


Figure 54: Recommended Reflow Soldering Thermal Profile

Table 60: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak Slope	0–3 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up Slope	0–3 °C/s
Reflow Time (D: over 217°C)	40–70 s
Max Temperature	235–246 °C
Cool-down Slope	-1.5–0 °C/s
Reflow Cycle	
Max Reflow Cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. If a conformal coating is necessary for the module, do not use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
3. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
4. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
5. Due to the complexity of the SMT process, contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective wave soldering, ultrasonic soldering) that is not mentioned in ***document [6].***

8.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

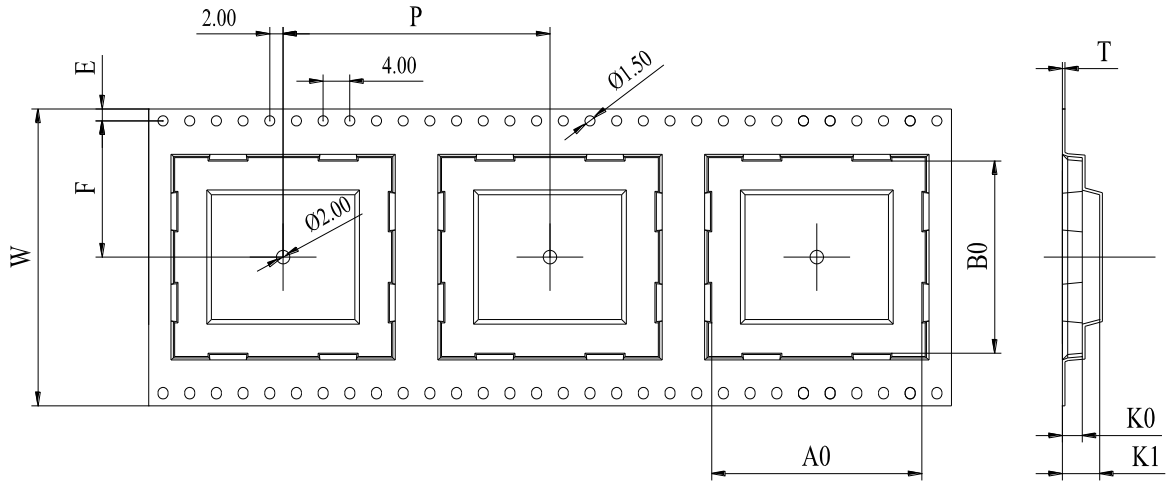


Figure 55: Carrier Tape Dimension Drawing (Unit: mm)

Table 61: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
380	180	72.5	380	180	72.5	380	180	72.5

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

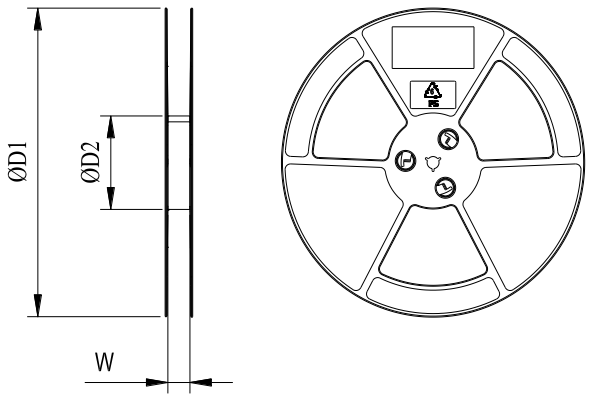


Figure 56: Plastic Reel Dimension Drawing

Table 62: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
380	180	72.5

8.3.3. Mounting Direction

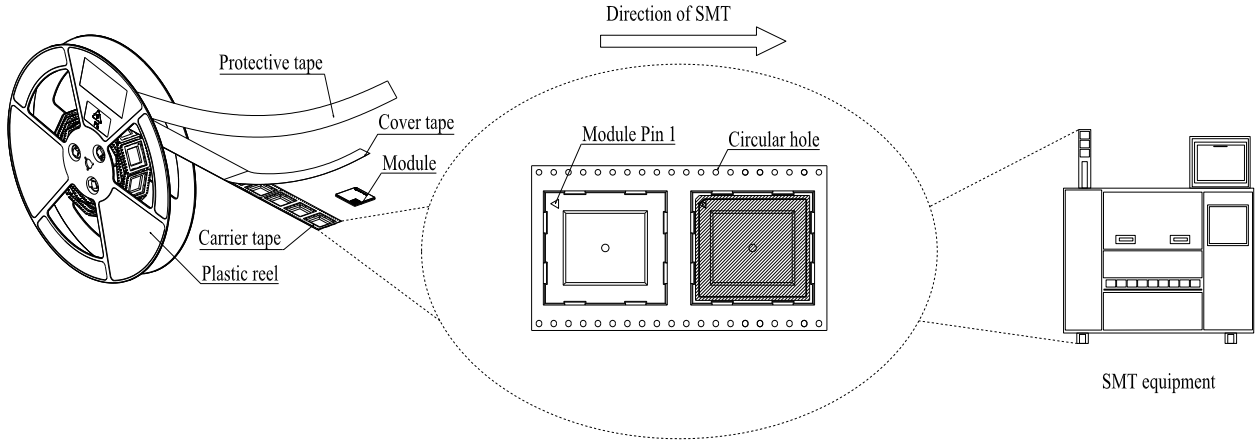
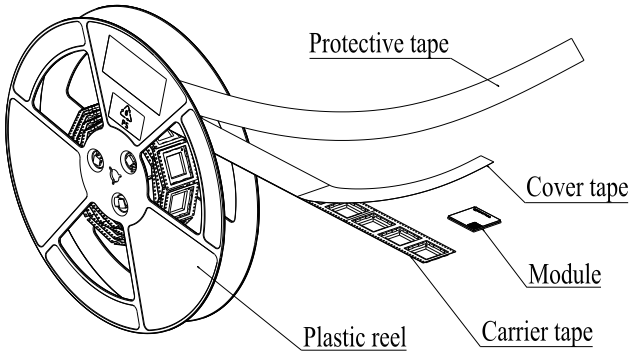


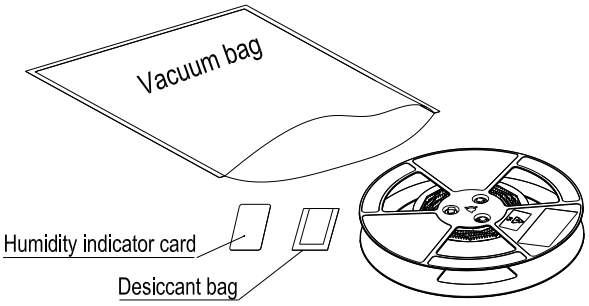
Figure 57: Mounting Direction

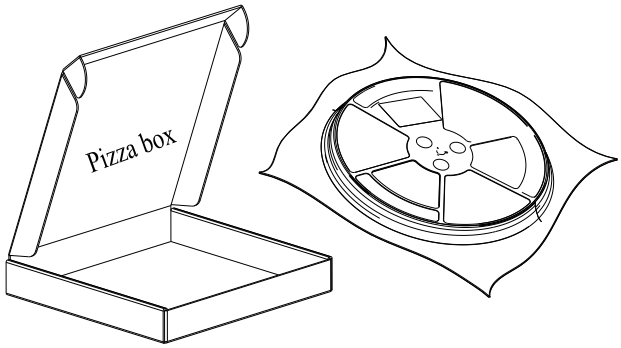
8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 100 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 400 modules.

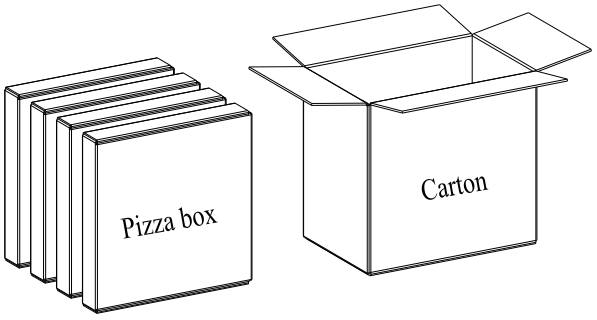


Figure 58: Packaging Process

9 Appendix A References

Table 63: Related Documents

Document Name
[1] Quectel_5G_SOC_EVB_User_Guide
[2] Quectel_RG650E&RG650V_Series_AT_Commands_Manual
[3] Quectel_RG650E&RG650V_Series_QuecOpen(SDK)_Low_Power_Mode_Development_Guide
[4] Quectel_RG650E&RG650V_Series_GNSS_Application_Note
[5] Quectel_RF_Layout_Application_Note
[6] Quectel_Module_SMT_Application_Note

Table 64: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR-WB	Adaptive Multi-Rate Wideband
AON	Active Optical Network
AP	Appliation Processor
BB	Baseband
BDS	BeiDou Navigation Satellite System
bps	Bits Per Second
BPSK	Binary Phase Shift Keying
CA	Carrier Aggregation
CHAP	Challenge Handshake Authentication Protocol

CMUX	Connection Multiplexing
CS	Coding Scheme
CTS	Clear To Send
DCE	Data Communications Equipment
DC-HSDPA	Dual-carrier High Speed Downlink Packet Access
DDR	Double Data Rate
DL	Downlink
DRX	Discontinuous Reception
DRX	Diversity Receive
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
EMI	Electromagnetic Interference
EP	Extended Profile
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
EVB	Evaluation Board
FDD	Frequency Division Duplex
FEM	Front-End Module
FILE	File Protocol
FOTA	Firmware Upgrade Over The Air
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP-SSL: FTP over SSL / FTP Secure
Galileo	Galileo Satellite Navigation System (EU)

GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GRFC	General RF Control
GSM	Global System for Mobile Communications
HB	High Band
HORxD	High Order Rx Diversity
HPUE	High Power User Equipment
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
IC	Integrated Circuit
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
I/O	Input/Output
LAA	License Assisted Access
LB	Low Band
LCM	"LCD Module" /liquid crystal monitor
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LDO	Low-dropout Regulator

LGA	Land Grid Array
LMHB	Low/Middle/High Band
LNA	Low Noise Amplifier
LTE	Long Term Evolution
M2M	Machine to Machine
MAC	Media Access Control
MB	Middle Band
MCU	Microcontroller Unit
MDC	Management Data Clock
MDIO	Management Data Input/Output
MHB	Middle/High Band
MLCC	Multi-layer Ceramic Capacitor
MIMO	Multiple Input Multiple Output
MMS	Multimedia Messaging Service
MO	Mobile Originated
MQTT	Message Queuing Telemetry Transport
MSB	Most Significant Bit
MT	Mobile Terminated
NITZ	Network Identity and Time Zone / Network Informed Time Zone
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
NR	New Radio
NSA	Non-Stand Alone
NTP	Network Time Protocol
OTA	Over-the-air programming
OTG	On-The-Go

PA	Power Amplifier
PAP	Password Authentication Protocol
PC	Personal Computer
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PHY	Physical Layer
PING	Packet Internet Groper
PMU	Power Management Unit
PMIC	Power Management Integrated Circuit
PPP	Point-to-Point Protocol
PRX	Primary Receive
QAM	Quadrature Amplitude Modulation
QMI	Qualcomm Message Interface
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RI	Ring Indicator
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
RHCP	Right Hand Circularly Polarized
RTS	Ready To Send/Request to Send
Rx	Receive
SA	Stand Alone

SCS	Sub-Carrier Space
SD	Secure Digital
SIMO	Single Input Multiple Output
SMD	Surface Mount Device
SMS	Short Message Service
SMT	Surface Mount Technology
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SoC	System on Chip
SPI	Serial Peripheral Interface
SRS	Sounding Reference Signal
SSL	Secure Sockets Layer
STB	Set Top Box
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
TRX	Transmit & Receive
TVS	Transient Voltage Suppressor
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UHB	Ultra High Band
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus

(U)SIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
WWAN	Wireless Wide Area Network
XTRA	eXTended Receiver Assistance

10 Appendix B Operating Frequency

Table 65: Operating Frequencies (5G)

5G	Duplex Mode	Uplink Operating Band	Downlink Operating Band	Unit
n1	FDD	1920–1980	2110–2170	MHz
n2	FDD	1850–1910	1930–1990	MHz
n3	FDD	1710–1785	1805–1880	MHz
n5	FDD	824–849	869–894	MHz
n7	FDD	2500–2570	2620–2690	MHz
n8	FDD	880–915	925–960	MHz
n12	FDD	699–716	729–746	MHz
n13	FDD	777–787	746–756	MHz
n14	FDD	788–798	758–768	MHz
n18	FDD	815–830	860–875	MHz
n20	FDD	832–862	791–821	MHz
n24	FDD	1626.5–1660.5	1525–1559	MHz
n25	FDD	1850–1915	1930–1995	MHz
n26	FDD	814–849	859–894	MHz
n28	FDD	703–748	758–803	MHz
n29	SDL	-	717–728	MHz
n30	FDD	2305–2315	2350–2360	MHz
n34	TDD	2010–2025	2010–2025	MHz
n38	TDD	2570–2620	2570–2620	MHz

n39	TDD	1880–1920	1880–1920	MHz
n40	TDD	2300–2400	2300–2400	MHz
n41	TDD	2496–2690	2496–2690	MHz
n46	TDD	5150–5925	5150–5925	MHz
n47	TDD	5855–5925	5855–5925	MHz
n48	TDD	3550–3700	3550–3700	MHz
n50	TDD	1432–1517	1432–1517	MHz
n51	TDD	1427–1432	1427–1432	MHz
n53	TDD	2483.5–2495	2483.5–2495	MHz
n65	FDD	1920–2010	2110–2200	MHz
n66	FDD	1710–1780	2110–2200	MHz
n67	SDL	-	738–758	MHz
n70	FDD	1695–1710	1995–2020	MHz
n71	FDD	663–698	617–652	MHz
n74	FDD	1427–1470	1475–1518	MHz
n75	SDL	-	1432–1517	MHz
n76	SDL	-	1427–1432	MHz
n77	TDD	3300–4200	3300–4200	MHz
n78	TDD	3300–3800	3300–3800	MHz
n79	TDD	4400–5000	4400–5000	MHz
n80	SUL	1710–1785	-	MHz
n81	SUL	880–915	-	MHz
n82	SUL	832–862	-	MHz
n83	SUL	703–748	-	MHz
n84	SUL	1920–1980	-	MHz
n85	FDD	698–716	728–746	MHz

n86	SUL	1710–1780	-	MHz
n89	SUL	824–849	-	MHz
n90	TDD	2496–2690	2496–2690	MHz
n91	FDD	832–862	1427–1432	MHz
n92	FDD	832–862	1432–1517	MHz
n93	FDD	880–915	1427–1432	MHz
n94	FDD	880–915	1432–1517	MHz
n95	SUL	2010–2025	-	MHz
n96	TDD	5925–7125	5925–7125	MHz
n97	SUL	2300–2400	-	MHz
n98	SUL	1880–1920	-	MHz
n99	SUL	1626.5–1660.5	-	MHz
n257	-	26.50–29.50	26.50–29.50	GHz
n258	-	24.25–27.50	24.25–27.50	GHz
n260	-	37.00–40.00	37.00–40.00	GHz
n261	-	27.50–28.35	27.50–28.35	GHz

Table 66: Operating Frequencies (2G + 3G + 4G; Unit: MHz)

2G	3G	4G	Duplex Mode	Uplink Operating Band	Downlink Operating Band
-	B1	B1	FDD	1920–1980	2110–2170
PCS1900	B2/BC1	B2	FDD	1850–1910	1930–1990
DCS1800	B3	B3	FDD	1710–1785	1805–1880
-	B4	B4	FDD	1710–1755	2110–2155
GSM850	B5/BC0	B5	FDD	824–849	869–894
-	B6	-	FDD	830–840	875–885
-	B7	B7	FDD	2500–2570	2620–2690

EGSM900	B8	B8	FDD	880–915	925–960
-	B9	B9	FDD	1749.9–1784.9	1844.9–1879.9
-	B10	B10	FDD	1710–1770	2110–2170
-	B11	B11	FDD	1427.9–1447.9	1475.9–1495.9
-	B12	B12	FDD	699–716	729–746
-	B13	B13	FDD	777–787	746–756
-	B14	B14	FDD	788–798	758–768
-	-	B17	FDD	704–716	734–746
-	-	B18	FDD	815–830	860–875
-	B19	B19	FDD	830–845	875–890
-	B20	B20	FDD	832–862	791–821
-	B21	B21	FDD	1447.9–1462.9	1495.9–1510.9
-	B22	B22	FDD	3410–3490	3510–3590
-	-	B24	FDD	1626.5–1660.5	1525–1559
-	B25	B25	FDD	1850–1915	1930–1995
-	B26	B26	FDD	814–849	859–894
-	-	B27	FDD	807–824	852–869
-	-	B28	FDD	703–748	758–803
-	-	B29	FDD [17]	-	717–728
-	-	B30	FDD	2305–2315	2350–2360
-	-	B31	FDD	452.5–457.5	462.5–467.5
-	-	B32	FDD [17]	-	1452–1496
-	B33	B33	TDD	1900–1920	1900–1920
-	B34	B34	TDD	2010–2025	2010–2025
-	B35	B35	TDD	1850–1910	1850–1910

[17] Restricted to E-UTRA operation when carrier aggregation is configured. The downlink operating band is paired with the uplink operating band (external) of the carrier aggregation configuration that is supporting the configured Pcell.

-	B36	B36	TDD	1930–1990	1930–1990
	B37	B37	TDD	1910–1930	1910–1930
-	B38	B38	TDD	2570–2620	2570–2620
-	B39	B39	TDD	1880–1920	1880–1920
-	B40	B40	TDD	2300–2400	2300–2400
-	-	B41	TDD	2496–2690	2496–2690
-	-	B42	TDD	3400–3600	3400–3600
-	-	B43	TDD	3600–3800	3600–3800
-	-	B44	TDD	703–803	703–803
-	-	B45	TDD	1447–1467	1447–1467
-	-	B46	TDD	5150–5925	5150–5925
-	-	B47	TDD	5855–5925	5855–5925
-	-	B48	TDD	3550–3700	3550–3700
-	-	B50	TDD	1432–1517	1432–1517
-	-	B51	TDD	1427–1432	1427–1432
-	-	B52	TDD	3300–3400	3300–3400
-	-	B65	FDD	1920–2010	2110–2200
-	-	B66	FDD [18]	1710–1780	2110–2200
-	-	B67	FDD 17	-	738–758
-	-	B68	FDD	698–728	753–783
-	-	B69	FDD 17	-	2570–2620
-	-	B70	FDD [19]	1695–1710	1995–2020
-	-	B71	FDD	663–698	617–652
-	-	B72	FDD	451–456	461–466

[18] The range 2180–2200 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured.
[19] The range 2010–2020 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured and Tx-Rx separation is 300 MHz. The range 2005–2020 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured and Tx-Rx separation is 295 MHz.

-	-	B73	FDD	450–455	460–465
-	-	B74	FDD	1427–1470	1475–1518
-	-	B75	FDD [17]	-	1432–1517
-	-	B76	FDD [17]	-	1427–1432
-	-	B85	FDD	698–716	728–746
-	-	B87	FDD	410–415	420–425
-	-	B88	FDD	412–417	422–427

11.1 FCC

11.1.1. Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations.
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).

The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

11.1.2. Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to XXXX that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

11.1.3. End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: XMR2024RG650VNA”

The FCC ID can be used only when all FCC compliance requirements are met.

11.1.4. Antenna Installation

(1)The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2)The transmitter module may not be co-located with any other transmitter or antenna.
(3)Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

Band	MAX Gain (dBi)
LTE B2/2C/NR N2	8.00
LTE B4	5.00
LTE B5/5B	9.41
LTE B7/7C/NR N7	8.00
LTE B12/12B	8.70
LTE B13/NR N13	9.16
LTE B14/NR N14	9.23
LTE B17	8.74
LTE B25/NR N25	8.00
LTE B26(814-824)	9.36
LTE B26(824-849)	9.41
LTE B30/NR N30	-0.02
LTE B38/NR N38	5.00
LTE B38C	8.00
LTE B41/NR N41	5.00
LTE B41C	8.00
LTE B42	2.00
LTE B42C	5.00
LTE B43	2.00
LTE B43C	5.00
LTE B48/48C/48B/NR N48/NR N48 MIMO	-2.00
LTE B66/66B/66C/NR N66	5.00
LTE B71/NR N71	8.48
NR N2 MIMO	5.00
NR N5	9.42
NR N5 MIMO	6.42
NR N7 MIMO	5.00
NR N12	8.71
NR N25 MIMO	5.00
NR N26(814-824)	9.37
NR N26(824-849)	9.42
NR N38 MIMO	3.00
NR N41 MIMO	3.00
NR N66 MIMO	2.00
NR N70/N70 MIMO	5.00

NR N71	8.48
NR N71 MIMO	5.48
NR N77(3450-3550)	2.00
NR N77(3450-3550) MIMO	0.00
NR N77(3700-3980)	2.00
NR N77(3700-3980) MIMO	0.00
NR N78(3450-3550)	2.00
NR N78(3450-3550) MIMO	0.00
NR N78(3700-3800)	2.00
NR N78(3700-3800) MIMO	0.00

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

11.1.5. Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

11.1.6. Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

11.1.7. List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90 and part 96 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

11.1.8. This device is intended only for OEM integrators under the following conditions:(For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

11.1.9. Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

11.2. IC

11.2.1. Industry Canada Statement

This device complies with Industry Canada’s licence-exempt RSSs. Operation is subject to the following two conditions:

(1) This device may not cause interference; and

(2) This device must accept any interference, including interference that may cause undesired operation of the device

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

(1) l'appareil ne doit pas produire de brouillage, et

(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

11.2.2. Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

11.2.3. Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

11.2.4. This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

11.2.5. Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1)L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et

2)Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

11.2.6. IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

11.2.7. NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada

11.2.8. End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 10224A-024RG650VNA”.

11.2.9.Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 10224A-024RG650VNA ".

11.2.10.Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install

or remove this RF module in the user's manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as show in this manual.

11.2.11.Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

11.2.12 Antenna Requirements

The following antennae were approved with the prototype:
This radio transmitter [10224A-024RG650VNA] has been approved by innovation, Science and development Economic Canada to operate with the types of antennas listed below, with the maximum allowable gain indicated. The types of antennas not included in this list that have a gain of any type listed are strictly prohibited for use with this device.

Les antennes suivantes ont été approuvées avec le prototype:
Cet émetteur radio [10224A-024RG650VNA] a été approuvé par innovation, Science et développement économique Canada pour fonctionner avec les types d'antennes énumérés ci-dessous, avec le gain maximal autorisé indiqué. Les types d'antennes non inclus dans cette liste qui ont un gain tout type lis ted sont strictement interdits pour une utilisation avec cet appareil.

Band	Description	Gain (dBi)
LTE B2/2C/NR N2	External Antenna	1.6
LTE B4		1.2
LTE B5/5B/NR N5		0.7
LTE B7/7C/NR N7		2.7
LTE B12/12B/NR N12		0.5
LTE B13/NR N13		0.2
LTE B14/NR N14		0.1
LTE B17		0.5
LTE B25/NR N25		1.7
LTE B26/NR N26		0.7
LTE B30/NR N30		-5.7
LTE B38/38C/NR N38		2.4
LTE B41/41C/NR N41		2.7
LTE B42/42C		-2.01
LTE B43/43C		-7.1
LTE B48/48C/48B/NR N48		-6.12
LTE B66/66C/66B/NR N66		1.4
LTE B71/NR N71		1.22
NR N77		-0.64
NR N78		-0.64