EC300R-LA QuecOpen

Hardware Design

LTE Standard Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.

Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.

Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.

Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.

The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.

In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2024-02-22	Felix QIN/ Dakang YUAN/ Asa WANG	Creation of the document
1.0.0	2024-02-22	Felix QIN/ Dakang YUAN/ Asa WANG	Preliminary

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1 Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and price-performance ratio

This document defines the EC300R-LA module in QuecOpen® solution and describes its air interface and hardware interfaces which relate to your applications.

It can help you quickly understand interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, you can use this module to design and to set up mobile applications easily.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

The module is an LTE/WCDMA/GSM wireless communication module that supports Rx-diversity. It also supports LTE-FDD, LTE-TDD, HSDPA, HSUPA, HSPA+, WCDMA, EDGE and GPRS network data connection, and provides voice functionality for your specific applications. The information of the module is as follows:

Table 2: Basic Information

EC300R-LA	
Packaging Type & Pin Counts	LCC: 87 pins; LGA: 74 pins
Dimensions	(30.0 ±0.15) mm × (30.0 ±0.15) mm × (2.4 ±0.2) mm
Weight	Approx. 4.5 g
Wireless Network Mode	LTE/WCDMA/GSM

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

Wireless Network Type	EC300R-LA
LTE-FDD	B1/B2/B3/B4/B5/B7/B8/B28/B66
WCDMA	B1/B2/B4/B5/B8
GSM	GSM850/EGSM900/DCS1800/PCS1900

2.2. Key Features

Table 4: Key Features

Feature	Description
Supply Voltage	● 3.4–4.3 V ● Typ.: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: stored in (U)SIM card and ME, ME by default
USB Interface	● Complies with USB 2.0 specification (master mode* and slave mode) ● Data rate: up to 480 Mbps ● Used for AT command communication, data transmission, software debugging and firmware upgrade ● Supports USB serial driver for: Windows 8/8.1/10/11, Linux 2.6–6.5 and Android 4.x–13.x systems
USB_BOOT	Supports one forced download interface
(U)SIM Card Interfaces	● Supports two (U)SIM cards: 1.8 V and 3.0 V ● Supports Dual SIM Single Standby
Audio Features	● Supports digital audio interface and analog audio interface ● GSM: HR/FR/EFR/AMR/AMR-WB ● WCDMA: AMR/AMR-WB ● LTE: AMR/AMR-WB ● Supports echo cancellation and noise suppression
Digital Audio Interface	● Used for audio data transmission with external codec ● Supports 16-bit linear data format ● Supports short frame synchronization ● Supports master mode and slave* mode
I2C Interfaces	● Supports three I2C interfaces, among which two are used by default, one is multiplexed from other interfaces. ● Complies with *The I2C-bus Specification* (100/400 kHz mode) ● Supports master device only, multi-master mode is not supported
Analog Audio Interface	Supports one analog audio input and one analog audio output
MIPI DSI Interface	● Supports one 2-lane MIPI DSI high-speed differential data transmission ● Supports up to WVGA (480 × 854) resolution
UARTs	● Supports four UARTs, among which main UART and debug UART are used by default, and other two UARTs are multiplexed from other interfaces. F

	Main UART: ● Used for AT command communication and data transmission ● Baud rate: 115200 bps by default, up to 921600 bps ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for partial log output ● Baud rate: 115200 bps
SDIO Interfaces	**SD Card Application Interface:** ● Supports one SD card application interface that complies with SD 3.0 protocol **WLAN Application Interface:** ● Supports one low-power SDIO 3.0 WLAN application interface and one control interface
ADC Interfaces	● Supports three ADC interfaces ● Voltage range of ADC0 and ADC1: 0–VBAT-BB ● Voltage range of ADC2: 0–1.2 V
SPI	● Supports three SPIs, among which one is used by default, and other two are multiplexed from other interfaces ● Supports master mode and slave* mode ● 1.8 V power domain ● Clock rate: up to 52 MHz
RGMII*/RMII Interface	● Supports one RGMII/RMII interface ● 1.8 V power domain for RGMII; 1.8/3.3 V power domain for RMII
Camera interface	● Supports SPI single- or dual-line data transmission ● Supports up to VGA (640 × 480) resolution
Indication Signal	● NET_STATUS indicates network activity status ● STATUS indicates module operation status
AT command	Complies with the AT commands defined in *3GPP TS 27.007* and *3GPP TS 27.005* and Quectel enhanced AT commands
Rx-diversity	Supports LTE Rx-diversity
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● Rx-diversity antenna interface (ANT_DRX) ● 50 Ω characteristic impedance
Transmitting Power	● GSM850: Class 4 (33 dBm ±2 dB) ● EGSM900: Class 4 (33 dBm ±2 dB) ● DCS1800: Class 1 (30 dBm ±2 dB) ● PCS1900: Class 1 (30 dBm ±2 dB) ● GSM850 8-PSK: Class E2 (27 dBm ±3 dB) ● EGSM900 8-PSK: Class E2 (27 dBm ±3 dB) ● DCS1800 8-PSK: Class E2 (26 dBm ±3 dB) ● PCS1900 8-PSK: Class E2 (26 dBm ±3 dB) ● WCDMA: Class 3 (23 dBm ±2 dB) ● LTE-FDD: Class 3 (23 dBm ±2 dB)

	● LTE-TDD: Class 3 (23 dBm ±2 dB)
LTE Features	● Supports 3GPP Rel-9 non-CA Cat 4 FDD and TDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidths ● Supports DL MIMO ● Supports UL QPSK and 16QAM modulations ● Supports DL QPSK, 16QAM and 64QAM modulations ● Max. data rates: – LTE-FDD: 150 Mbps (DL)/50 Mbps (UL) – LTE-TDD: 130 Mbps (DL)/30 Mbps (UL)
UMTS Features	● Complies with 3GPP Rel-7 HSPA+, HSDPA, HSUPA and WCDMA ● Supports QPSK, 16 QAM and 64 QAM modulations ● Max. data rates: – HSPA+: 21 Mbps (DL) – HSUPA: 5.76 Mbps (UL) – WCDMA: 384 kbps (DL)/384 kbps (UL)
GSM Features	**GPRS:** ● Supports GPRS multi-slot class 12 ● Coding scheme: CS 1–4 ● Max. data rates: 85.6 Mbps (DL)/85.6 Mbps (UL) **EDGE:** ● Supports EDGE multi-slot class 12 ● Supports GMSK and 8-PSK modulation coding scheme ● DL coding schemes: MCS 1–9 ● UL coding schemes: MCS 1–9 ● Max. data rates: 236.8 Mbps (DL)/236.8 Mbps (UL)
Internet Protocol Features	● Complies with TCP/UDP/PPP/NITZ/FTP*/HTTP*/PING*/CMUX*/ HTTPS*/SSL*/MMS*/SMTP*/SMTPS* protocols ● Supports PAP and CHAP for PPP connections
Temperature Ranges	● Normal operating temperature [1]: -35 °C to +75 °C ● Extended operating temperature [2]: -40 °C to +85 °C ● Storage temperature: -40 °C to +90 °C
Firmware Upgrade	Via USB interface or FOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

[1] Within this range, the module's indicators comply with 3GPP specification requirements.
[2] Within this range, the module retains the ability to establish and maintain functions such as voice, SMS, data transmission and emergency call, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as Pout, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

2.3. Pin Assignment

The following is the pin assignment of the module:

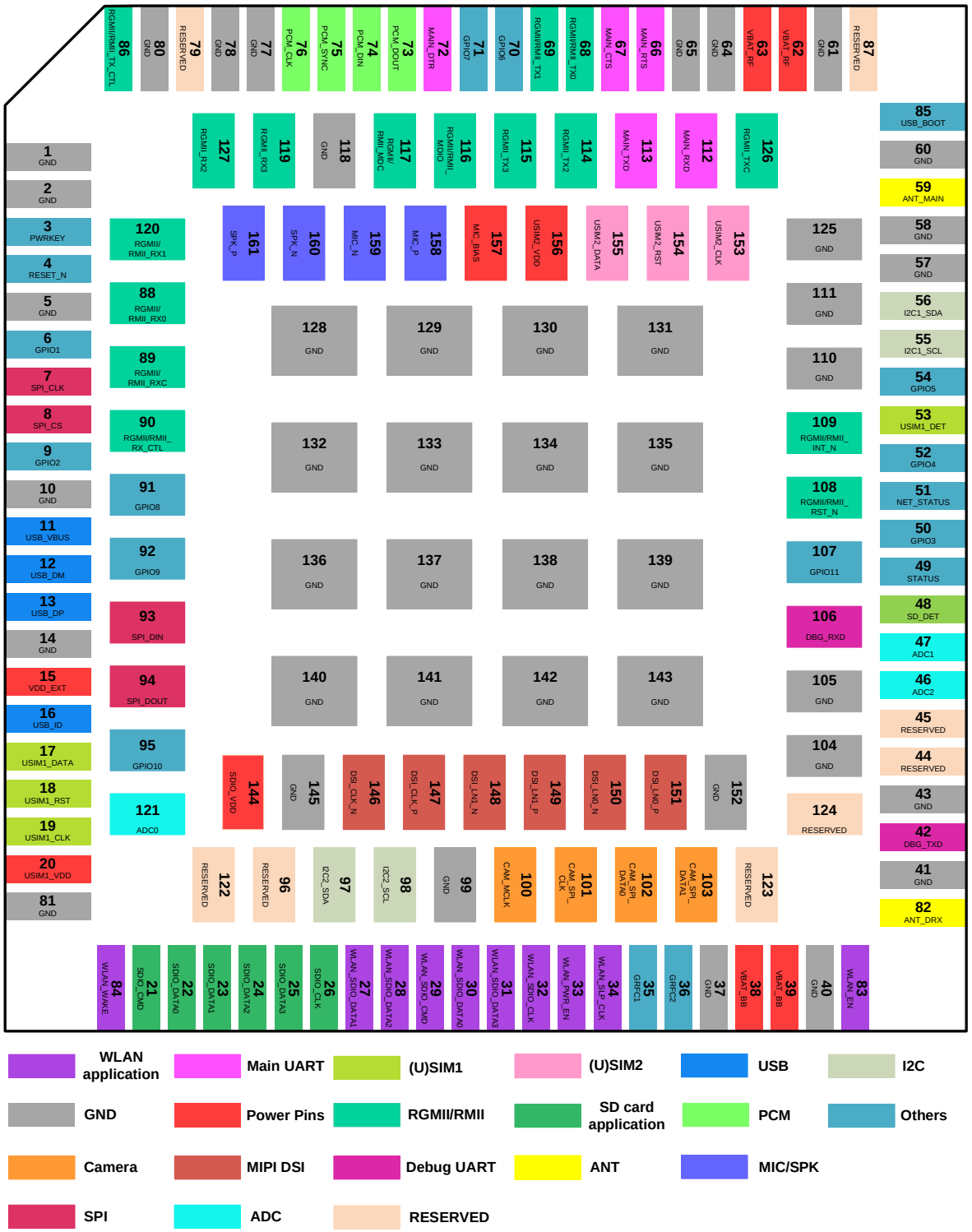


Figure 1: Pin Assignment (Top View)

NOTE

1. If the module needs to start up normally, do not pull USB_BOOT (pin 85) down to a low level before the module starts up successfully.
2. Keep all RESERVED and unused pins open. Connect GND to ground.
3. GRFC (pin 35, 36) interface is optional, if you need this function, contact Quectel Technical Support.
4. Ensure that the pull-up power supply of the module's pins is VDD_EXT or controlled by VDD_EXT, and there is no current sink on the module's pins before the module turns on. For more details, contact Quectel Technical Support.

2.4. Pin Description

The following tables describe the power supply characteristics and pin definition.

Table 5: Parameter Definition

Parameter	Description
AI	Analog Input
AIO	Analog Input/Output
AO	Analog Output
DI	Digital Input
DIO	Digital Input/Output
DO	Digital Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	38, 39	PI	Power supply for the module's BB part	Vmax = 4.3 V Vmin = 3.4 V Vnom = 3.8 V	External power supply must be able to provide sufficient current of at least 1.5 A. A test point is recommended to be reserved.
VBAT_RF	62, 63	PI	Power supply for the module's RF part		External power supply must be able to provide sufficient current of at least 2.0 A. A test point is recommended to be reserved.
VDD_EXT	15	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. A test point is recommended to be reserved.
GND	1, 2, 5, 10, 14, 37, 40, 41, 43, 57, 58, 60, 61, 64, 65, 77, 78, 80, 81, 99, 104, 105, 110, 111, 118, 125, 128–143, 145, 152				
Turn on/off/Reset					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	3	DI	Turn on/off the module	VBAT power domain V_{IL}max = 0.5 V	Active low. A test point is recommended to be reserved.
RESET_N	4	DI	Reset the module	1.8 V power domain V_{IL}max = 0.5 V	Active low. A test point is recommended to be reserved if unused.

Indication Signal					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NET_STATUS	51	DO	Indicate the module's network activity status	VDD_EXT	If unused, keep them open.
STATUS	49	DO	Indicate the module's operation status		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	11	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	A test point must be reserved.
USB_DP	13	AIO	USB 2.0 differential data (+)		90 Ω differential impedance is required. Test points must be reserved.
USB_DM	12	AIO	USB 2.0 differential data (-)		
USB_ID*	16	DI	USD ID detect		Used for OTG function only. Compliant with USB 2.0 specification. If unused, keep it open.
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	20	PO	(U)SIM1 card power supply	**Low-voltage:** Vmin = 1.67 V Vnom = 1.8 V Vmax = 1.93 V **High-voltage:** Vmin = 2.7 V Vnom = 3.0 V Vmax = 3.3 V	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_DATA	17	DIO	(U)SIM1 card data	USIM1_VDD	
USIM1_CLK	19	DO	(U)SIM1 card clock		

USIM1_RST	18	DO	(U)SIM1 card reset		
USIM1_DET	53	DI	(U)SIM1 card hot-plug detect	VDD_EXT	If unused, keep it open.
USIM2_VDD*	156	PO	(U)SIM2 card power supply	**Low-voltage:** Vmin = 1.67 V Vnom = 1.8 V Vmax = 1.93 V **High-voltage:** Vmin = 2.7 V Vnom = 3.0 V Vmax = 3.3 V	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM2_DATA*	155	DIO	(U)SIM2 card data	USIM2_VDD	
USIM2_CLK*	153	DO	(U)SIM2 card clock		
USIM2_RST*	154	DO	(U)SIM2 card reset		
Analog Audio Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC_BIAS	157	PO	Bias voltage output for microphone		
MIC_P	158	AI	Microphone analog input (+)		
MIC_N	159	AI	Microphone analog input (-)		
SPK_P	161	AO	Analog audio differential output (+)		
SPK_N	160	AO	Analog audio differential output (-)		
MIPI DSI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DSI_CLK_N	146	AO	LCD MIPI clock (-)		100 Ω differential impedance is required. If unused, keep them open.
DSI_CLK_P	147	AO	LCD MIPI clock (+)		
DSI_LN0_N	150	AIO	LCD MIPI data 0 (-)		
DSI_LN0_P	151	AIO	LCD MIPI data 0 (+)		
DSI_LN1_N	148	AO	LCD MIPI data 1 (-)		

DSI_LN1_P	149	AO	LCD MIPI data 1 (+)		
Camera Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CAM_MCLK	100	DO	Camera master clock	VDD_EXT	If unused, keep them open.
CAM_SPI_CLK	101	DI	Camera SPI clock		
CAM_SPI_DATA0	102	DI	Camera SPI data bit 0		
CAM_SPI_DATA1	103	DI	Camera SPI data bit 1		
SDIO Interface (SD Card Application)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDIO_CLK	26	DO	SDIO clock	SDIO_VDD	If unused, keep them open.
SDIO_CMD	21	DIO	SDIO command		
SDIO_DATA0	22	DIO	SDIO data bit 0		
SDIO_DATA1	23	DIO	SDIO data bit 1		
SDIO_DATA2	24	DIO	SDIO data bit 2		
SDIO_DATA3	25	DIO	SDIO data bit 3		
SDIO_VDD	144	PO	SDIO power supply	**Low-voltage:** Vmin = 1.67 V Vnom = 1.8 V Vmax = 1.93 V **High-voltage:** Vmin = 2.7 V Vnom = 2.85 V Vmax = 3.05 V	Provides a pull-up power supply for external SDIO interface. It cannot be used as a power supply. If unused, keep it open.
SD_DET*	48	DI	SD card hot-plug detect	VDD_EXT	If unused, keep it open.
Main UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_CTS	67	DI	Clear to send signal to the module	VDD_EXT	If unused, keep them open.

MAIN_RTS	66	DO	Request to send signal from the module		
MAIN_RXD	112	DI	Main UART receive		Test points are recommended to be reserved.
MAIN_TXD	113	DO	Main UART transmit		
MAIN_DTR	72	DI	Main UART data terminal ready		If unused, keep it open.
Debug UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	106	DI	Debug UART receive	VDD_EXT	Test points must be reserved.
DBG_TXD	42	DO	Debug UART transmit		
I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C1_SCL	55	OD	I2C1 serial clock	VDD_EXT	Used for external codec. An external 1.8 V pull-up resistor is needed. If unused, keep them open.
I2C1_SDA	56	OD	I2C1 serial data		
I2C2_SCL	98	OD	I2C2 serial clock		An external 1.8 V pull-up resistor is needed. If unused, keep them open.
I2C2_SDA	97	OD	I2C2 serial data		
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_SYNC	75	DIO	PCM data frame sync	VDD_EXT	When the module serves as the master device, the pin is in output state; When the module serves as the slave device*, the pin is in input state.
PCM_CLK	76	DIO	PCM clock		

					If unused, keep them open.
PCM_DIN	74	DI	PCM data input		If unused, keep them open.
PCM_DOUT	73	DO	PCM data output		
SDIO Interface (WLAN Application)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_SLP_CLK	34	DO	WLAN sleep clock	VDD_EXT	If unused, keep them open.
WLAN_PWR_EN	33	DO	WLAN power supply enable control		
WLAN_SDIO_DATA3	31	DIO	WLAN SDIO data bit 3		
WLAN_SDIO_DATA2	28	DIO	WLAN SDIO data bit 2		
WLAN_SDIO_DATA1	27	DIO	WLAN SDIO data bit 1		
WLAN_SDIO_DATA0	30	DIO	WLAN SDIO data bit 0		
WLAN_SDIO_CLK	32	DO	WLAN SDIO clock		
WLAN_SDIO_CMD	29	DIO	WLAN SDIO command		
WLAN_WAKE	84	DI	WLAN wake up the module		
WLAN_EN	83	DO	WLAN enable control		
RGMII*/RMII Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RGMII/RMII_RX0	88	DI	RGMII/RMII receive data bit 0	**1.8 V RGMII/RMII:** V_{IL}min = -0.3 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V V_{OL}max = 0.2 V V_{OH}min = 1.6 V **3.3 V RMII:** V_{IL}min = -0.3 V	RGMII supports 1.8 V power domain. RMII supports 1.8/3.3 V power domain. If unused, keep them open.
RGMII/RMII_RX1	120	DI	RGMII/RMII receive data bit 1		
RGMII/RMII_RXC	89	DI	RGMII/RMII receive clock		
RGMII/RMII_RX_CTL	90	DI	RGMII/RMII receive control		
RGMII/RMII_TX0	68	DO	RGMII/RMII transmit data bit 0		
RGMII/RMII_TX1	69	DO	RGMII/RMII transmit		

			data bit 1	V_{IL}max = 0.8 V V_{IH}min = 2.0 V V_{IH}max = 3.6 V V_{OL}max = 0.4 V V_{OH}min = 2.4 V	
RGMII/RMII_TX_CTL	86	DO	RGMII/RMII transmit control		
RGMII/RMII_INT_N	109	DI	RGMII/RMII interrupt		
RGMII/RMII_MDC	117	DO	RGMII/RMII management data clock		
RGMII/RMII_MDIO	116	DIO	RGMII/RMII management data input/output		
RGMII_RX2	127	DI	RGMII receive data bit 2	VDD_EXT	
RGMII_RX3	119	DI	RGMII receive data bit 3		
RGMII_TX2	114	DO	RGMII transmit data bit 2		
RGMII_TX3	115	DO	RGMII transmit data bit 3		
RGMII_TXC	126	DO	RGMII transmit clock		
RGMII/RMII_RST_N	108	DO	RGMII/RMII external PHY reset		If unused, keep it open.
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_DRX	82	AI	Rx-diversity antenna interface		50 Ω characteristic impedance.
ANT_MAIN	59	AIO	Main antenna interface		
SPI					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CLK	7	DIO	SPI clock	VDD_EXT	When the module serves as the master device, the pin is in output state; When the module serves as the slave device*, the pin is in input state.
SPI_CS	8	DIO	SPI chip select		

					If unused, keep them open.
SPI_DIN	93	DI	SPI data input		If unused, keep them open.
SPI_DOUT	94	DO	SPI data output		
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	121	AI	General-purpose ADC interface	Voltage range: 0 V–VBAT_BB	If unused, keep them open.
ADC1	47	AI			
ADC2	46	AI		voltage range: 0–1.2 V	
USB_BOOT					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	85	DI	Force the module into download mode	VDD_EXT	Active low. Do not pull it down to a low level before the module starts up successfully. It can be multiplexed as GPIO after the module starts up successfully. A test point is recommended to be reserved.
Antenna Tuner Control Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC1	35	DO	Generic RF controller	VDD_EXT	If unused, keep them open.
GRFC2	36	DO			
GPIO Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO1	6	DIO	General-purpose input/output	VDD_EXT	If unused, keep them open.

GPIO2	9	DIO	General-purpose input/output
GPIO3	50	DIO	General-purpose input/output
GPIO4	52	DIO	General-purpose input/output
GPIO5	54	DIO	General-purpose input/output
GPIO6	70	DIO	General-purpose input/output
GPIO7	71	DIO	General-purpose input/output
GPIO8	91	DIO	General-purpose input/output
GPIO9	92	DIO	General-purpose input/output
GPIO10	95	DIO	General-purpose input/output
GPIO11	107	DIO	General-purpose input/output

RESERVED Pins		
Pin Name	**Pin No.**	**Comment**
RESERVED	44, 45, 79, 87, 96, 122, 123, 124	Keep them open.

2.5. EVB Kit

Quectel supplies an evaluation board (LTE OPEN EVB) with accessories to develop and test the module.

3 Operating Characteristics

3.1. Operating Modes

The following table briefly describes the different operating modes of the module.

Table 7: Operating Mode Overview

Mode	Description	
Full Functionality Mode	Idle	The module remains registered on the network but has no data interaction with the network. In this mode, the software is active
	Voice/Data	The network is connected to the network. In this mode, the power consumption is decided by network setting and data rates.
Minimum Functionality Mode	**AT+CFUN=0** can set the module to the minimum functionality mode without removing the power supply. In this mode, both (U)SIM card and RF function are disabled.	
Airplane Mode	**AT+CFUN=4** can set the module to airplane mode. In this mode, RF function is disabled and all relevant AT commands are inaccessible.	
Sleep Mode	The module can still receive paging, SMS, voice call and TCP/UDP data from the network. In this mode, power consumption of the module is minimized.	
Shutdown Mode	In this mode, software is not active. However, the voltage supply (for VBAT_RF and VBAT_BB) remains connected.	

3.2. Sleep Mode

With DRX technology, power consumption of the module can be reduced to an ultra-low level.

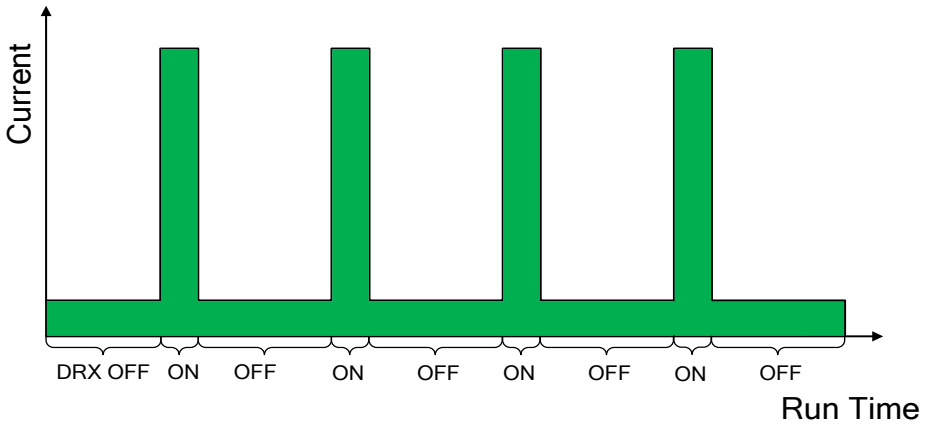


Figure 2: Module Power Consumption in Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

3.2.1. USB Application with USB Suspend/Resume Function and USB Remote Wakeup Function

If the host supports USB Suspend/Resume and USB remote wakeup function, the following three preconditions must be met to enable the module to enter sleep mode:

- Enable sleep function through related API.
- Ensure the level of pins configured to wakeup function is in non-wakeup status.
- Ensure the host's USB bus, which is connected to the module's USB interface, enters Suspend state.

The reference design is as follows:

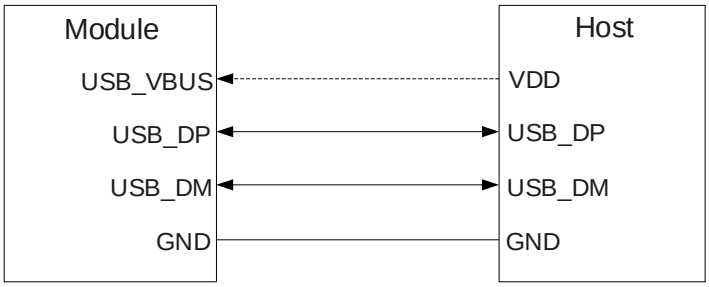


Figure 3: Block Diagram of Application with USB Remote Wakeup Function in Sleep Mode

- Sending data to the module through the USB interface will wake up the module.
- When the module has a URC to report, the module will wake up the host through USB bus.

3.2.2. USB Application with USB Suspend/Resume Function

If the host supports USB Suspend/Resume, but does not support remote wakeup function, the GPIO signal is needed to wake up the host. the following three preconditions must be met to enable the module to enter sleep mode:

- Enable sleep function through related API.
- Ensure the level of pins configured to wakeup function is in non-wakeup status.
- Ensure the host's USB bus, which is connected to the module's USB interface, enters Suspend state.

The following figure illustrates the connection between the module and the host.

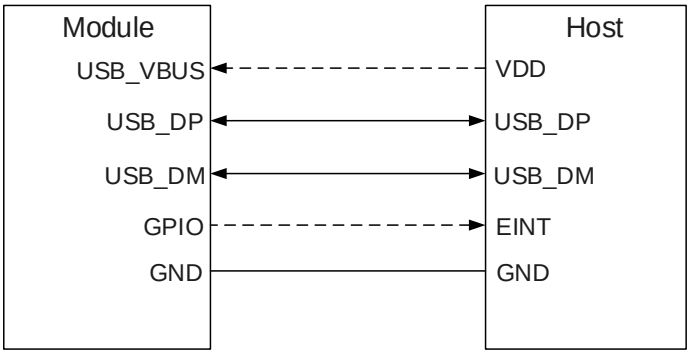


Figure 4: Block Diagram of Application without USB Remote Wakeup Function in Sleep Mode

- Sending data to the module through the USB interface will wake up the module.
- When the module has a URC to report, the module will wake up the host through GPIO signal.

3.2.3. USB Application Without USB Suspend Function

If the host does not support USB Suspend function, USB_VBUS should be disconnected through an external control circuit to set the module enter sleep mode. The following three preconditions must be met to enable the module to enter sleep mode:

- Enable sleep function through related API.
- Ensure the level of pins configured to wakeup function is in non-wakeup status.
- Ensure USB_VBUS is disconnected

The following figure illustrates the connection between the module and the host.

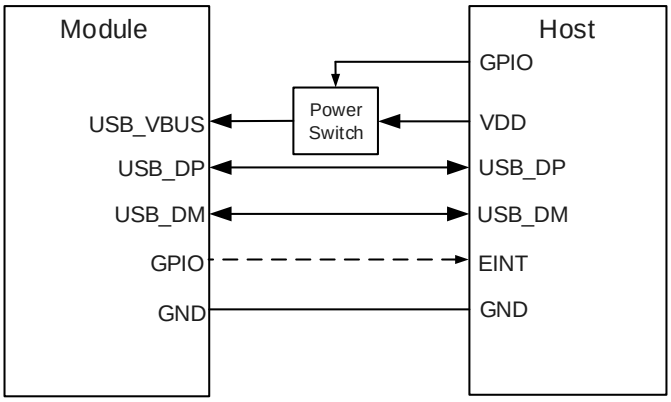


Figure 5: Block Diagram of Application without USB Suspend Function in Sleep Mode

Restore the power supply of USB_VBUS will wake up the module.

NOTE

1. Pay attention to the level match shown in the dotted line between the module and the host.

3.3. Airplane Mode

When the module enters airplane mode, the RF function does not work and all AT commands related to the RF function are inaccessible. The following ways can be used to let the module enter airplane mode.

AT+CFUN=<fun> provides the choice of the functionality level through setting **<fun>** into **0**, **1** or **4**.

- **AT+CFUN=0**: Minimum functionality mode (disable (U)SIM and RF functions).
- **AT+CFUN=1**: Full functionality mode (by default).

- **AT+CFUN=4**: Airplane mode (disable RF function).

3.4. Power Supply

3.4.1. Power Supply Interface

The module provides four VBAT pins for connection with the external power supply:

There are two separate voltage domains:

- Two VBAT_RF pins for RF part.
- Two VBAT_BB pins for baseband part.

Table 8: Pin Definition of Power Supply Pins

Pin Name	Pin No.	I/O	Description	Comment
VBAT_BB	38, 39	PI	Power supply for the module's BB part	External power supply must be able to provide sufficient current of at least 1.5 A. A test point is recommended to be reserved.
VBAT_RF	62, 63	PI	Power supply for the module's RF part	External power supply must be able to provide sufficient current of at least 2.0 A. A test point is recommended to be reserved.
VDD_EXT	15	PO	Provide 1.8 V for external circuit	Power supply for external GPIO's pull-up circuits. A test point is recommended to be reserved.

3.4.2. Reference Design for Power Supply

The performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of 2.8 A at least. If the voltage difference between input voltage and the supply voltage is small, it is suggested to use an LDO; if the voltage difference is big, a buck converter is recommended. The figure below is a reference design for a 5 V supply circuit.

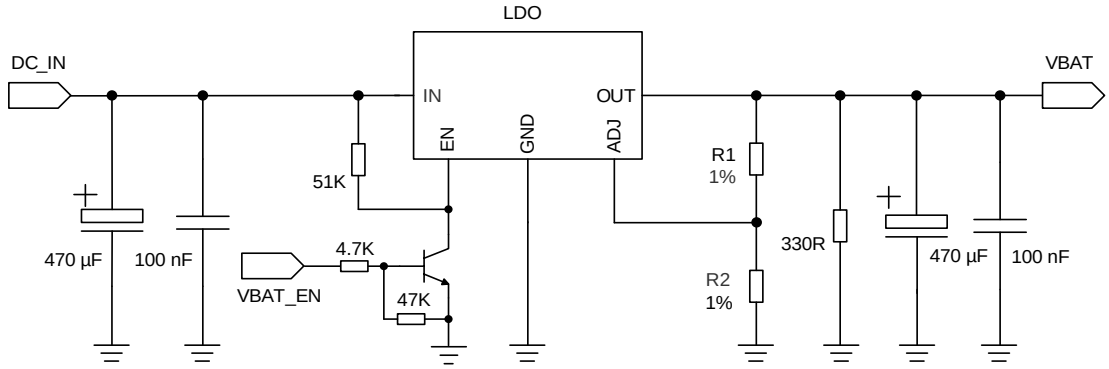


Figure 6: Reference Design of Power Input

NOTE

It is recommended to design a switch-controlled circuit at the power supply.

3.4.3. Requirements for Voltage Stability

The power supply range of the module is from 3.4 V to 4.3 V. Ensure the input voltage never drops below 3.4 V.

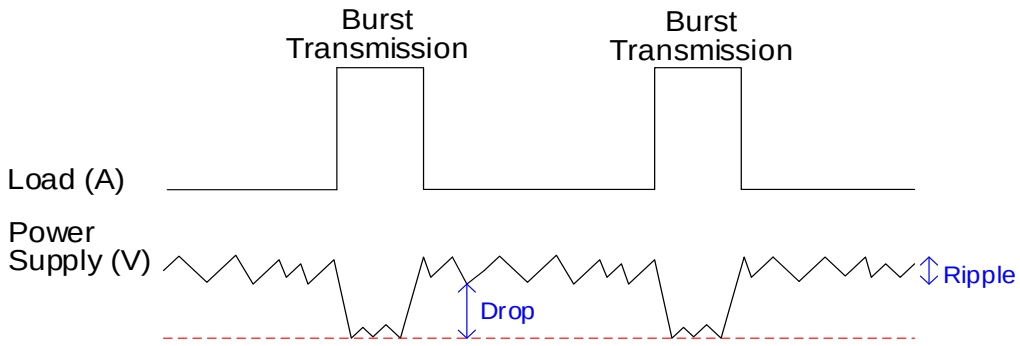


Figure 7: Power Supply Limits During Burst Transmission

To decrease the voltage drop, use a filter capacitor of about 100 µF with low ESR (ESR ≤ 0.7 Ω). and reserve a multi-layer ceramic chip (MLCC) capacitor array with ultra-low ESR. Use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to the VBAT_BB and VBAT_RF pins respectively. The main power supply from an external application should be a single voltage source and can be expanded to two sub paths routed as the star configuration. The width of VBAT_BB trace and VBAT_RF trace should be at least 1.5 mm and 2 mm respectively. As per design rules, the longer the VBAT trace is, the wider it should be.

To ensure the stability of the power supply to the module, add a TVS with V_{RWM} = 4.7 V, P_{PP} = 2550 W near the power supply. The reference design is as follows:

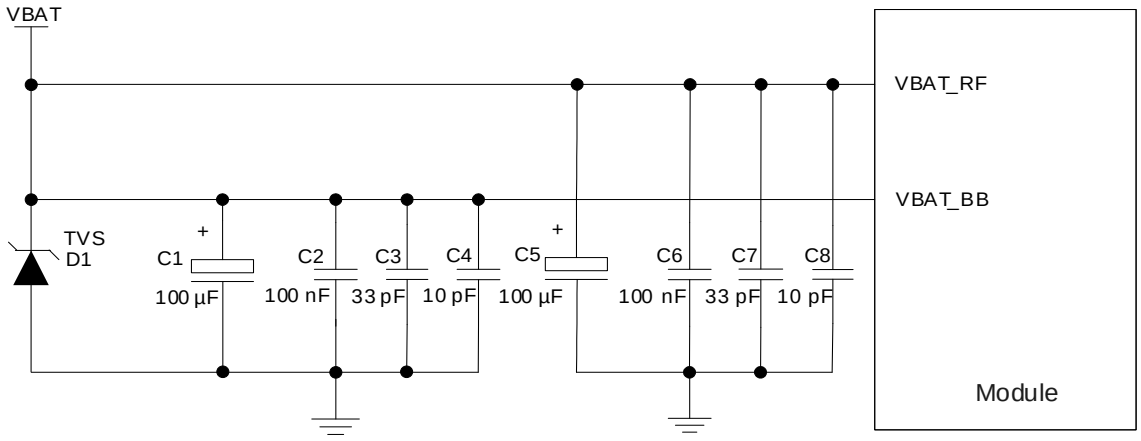


Figure 8: Reference Design of Power Supply

3.5. Turn On

3.5.1. Turn On with PWRKEY

Table 9: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	3	DI	Turn on/off the module	VBAT power domain. Active low. A test point is recommended to be reserved.

When the module is in turn-off state, it can be turned on by driving PWRKEY low for at least 3 s. It is recommended to use an open drain/collector driver to control the PWRKEY. The reference design is as follows:

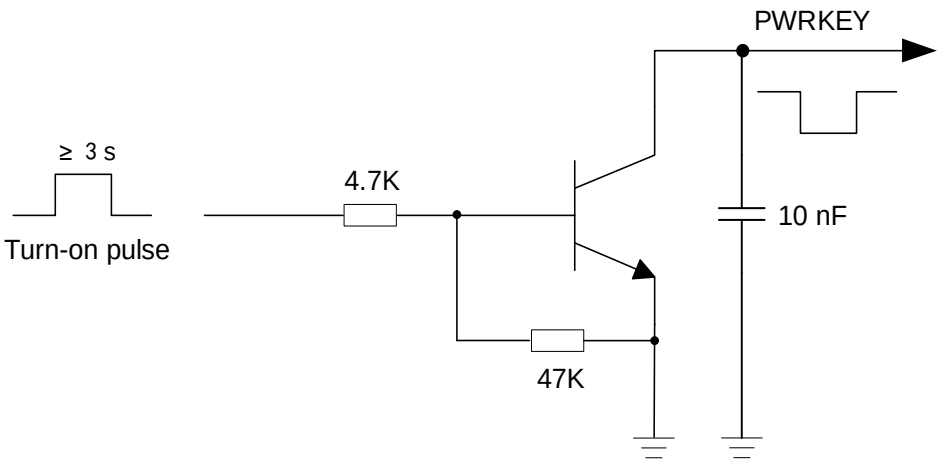


Figure 9: Reference Design of Turn-on with Driving Circuit

The module can also be turned on by pressing the PWRKEY button. A ESD protection component should be placed near the button for protection against ESD, since static electricity may be generated by the finger touching. The reference design is as follows:

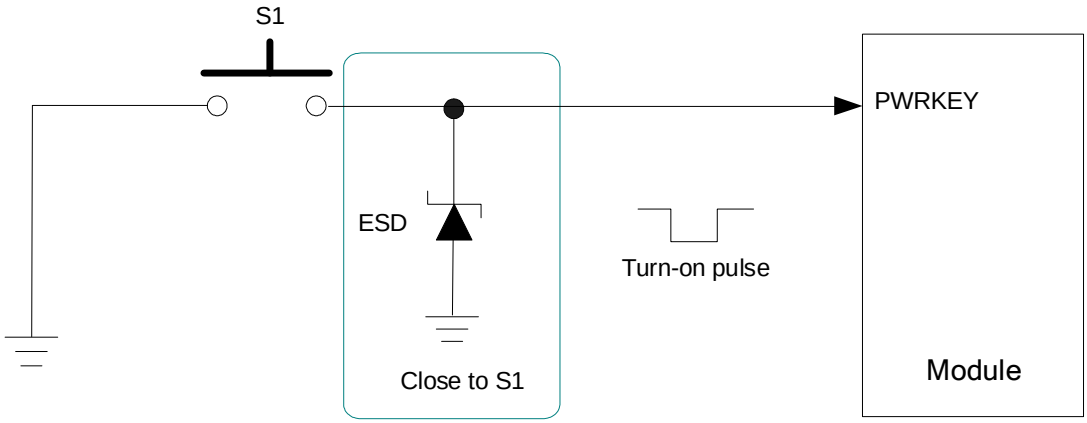


Figure 10: Reference Design of Turn-on with Button

The turn-on scenario is illustrated in the following figure.

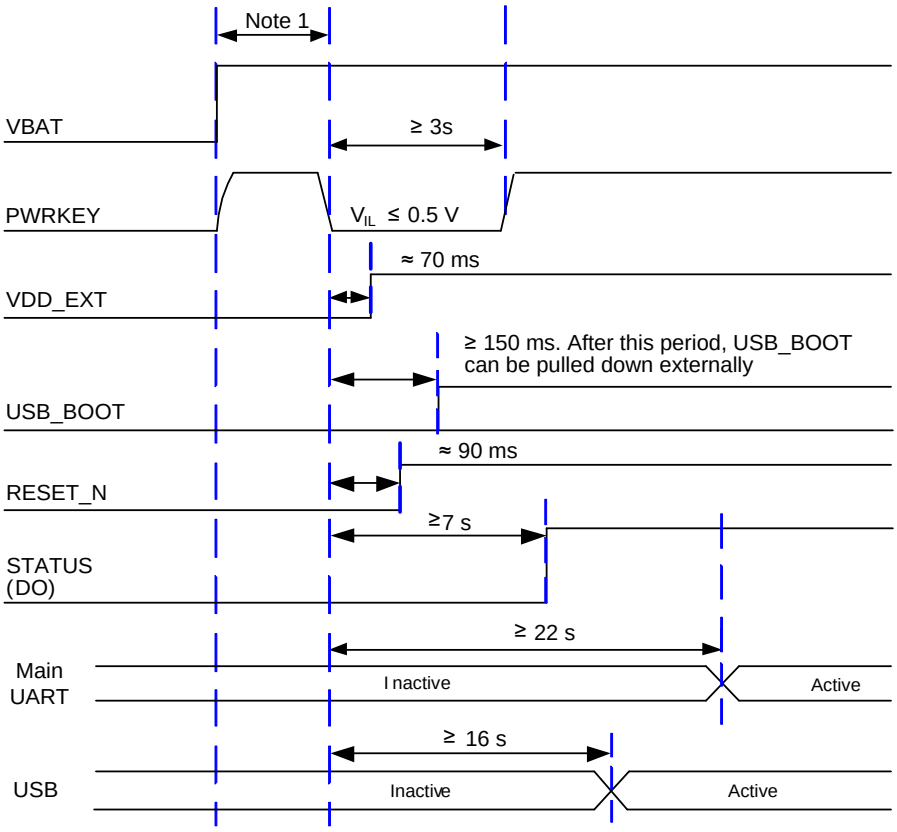


Figure 11: Timing of Turn-on with PWRKEY

NOTE

1. Ensure the voltage of VBAT is stable for at least 30 ms before driving the PWRKEY low.
2. If the module needs to turn on automatically but does not need turn-off function, PWRKEY can be driven low directly to ground with a recommended 4.7 kΩ resistor.

3.6. Turn Off

The following procedures can be used to turn off the module:

3.6.1. Turn Off with PWRKEY

Drive PWRKEY low for at least 650 ms and then release it, and the module will execute power-down procedure. The reference design is as follows:

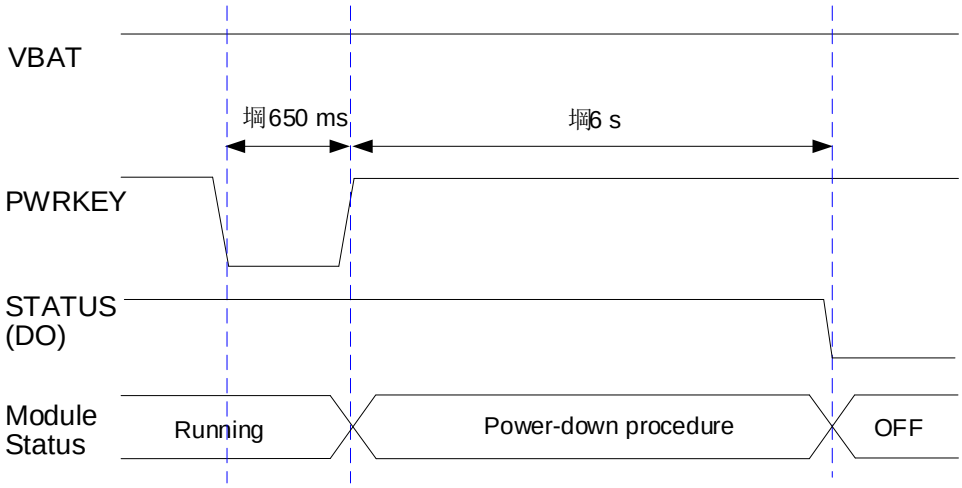


Figure 12: Timing of Turn-off with PWRKEY

3.6.2. Turn Off with AT Command

For proper shutdown procedure, execute **AT+QPOWD**, which has similar timing and effect as turning off the module through driving PWRKEY low.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.
2. When turning off the module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on automatically again after successful turn-off.

3.7. Reset

Driving RESET_N low for at least 300 ms and then releasing it can reset the module. RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 10: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	4	DI	Reset the module	1.8 V power domain. Active low. A test point is recommended to be reserved if unused.

The recommended circuit for reset function is similar to the PWRKEY control circuit. You can use an open drain/collector driver or a button to control RESET_N.

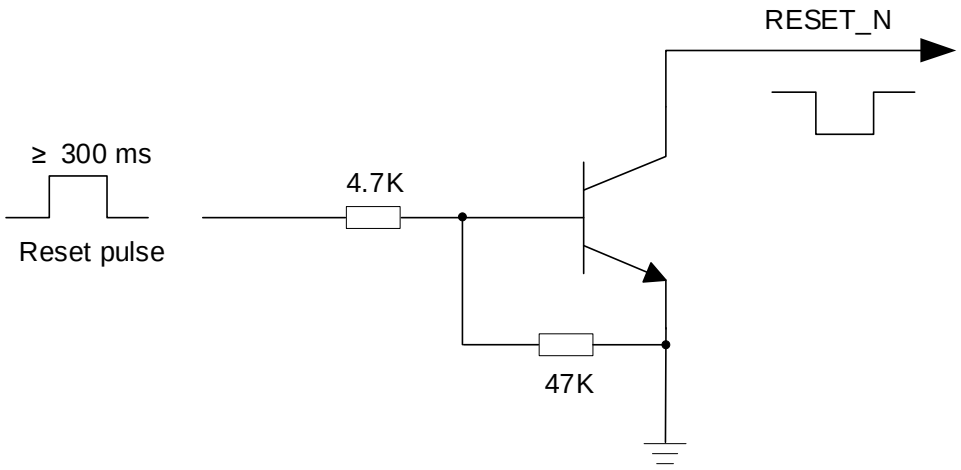


Figure 13: Reference Design of Reset with Driving Circuit

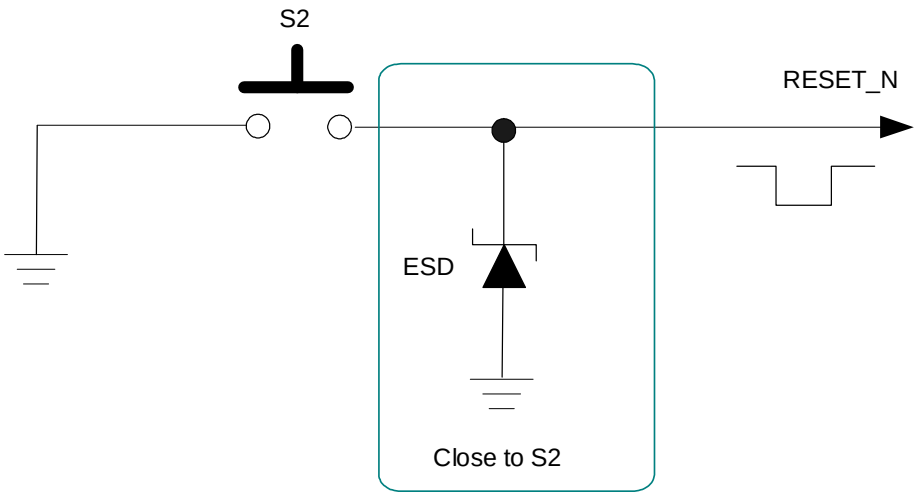


Figure 14: Reference Design of Reset with Button

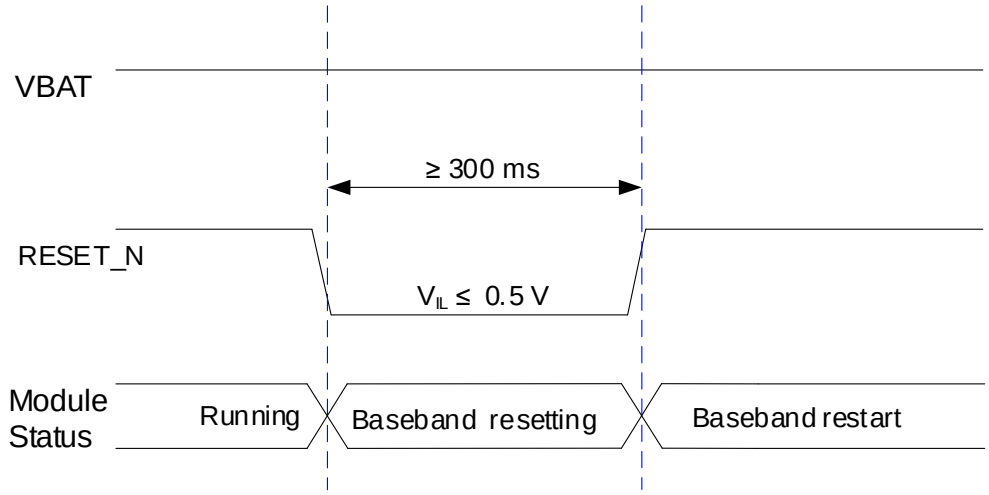


Figure 15: Timing of Reset

NOTE

1. Ensure the capacitance on PWRKEY and RESET_N never exceeds 10 nF.
2. The RESET_N pin only resets the internal baseband chip, not the power supply management chip.

4 Application Interfaces

4.1. USB Interface

The module provides one USB interface which complies with the USB 2.0 specification and supports high-speed (12 Mbps) and full-speed (480 Mbps) for USB 2.0. The USB interface supports master mode* and slave mode, and can be used for AT command communication, data transmission, software debugging and firmware upgrade.

Table 11: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	11	AI	USB connection detect	A test point must be reserved.
USB_DP	13	AIO	USB 2.0 differential data (+)	90 Ω differential impedance is required. Test points must be reserved.
USB_DM	12	AIO	USB 2.0 differential data (-)	
USB_ID*	16	DI	USD ID detect	Used for OTG function only. Compliant with USB 2.0 specification. If unused, keep it open.

For more details about the USB 2.0 specifications, visit http://www.usb.org/home.

4.1.1. Reference Design of USB Interface

Test points must be reserved for software debugging and firmware upgrade in your designs.

The following is the reference design of USB interface.

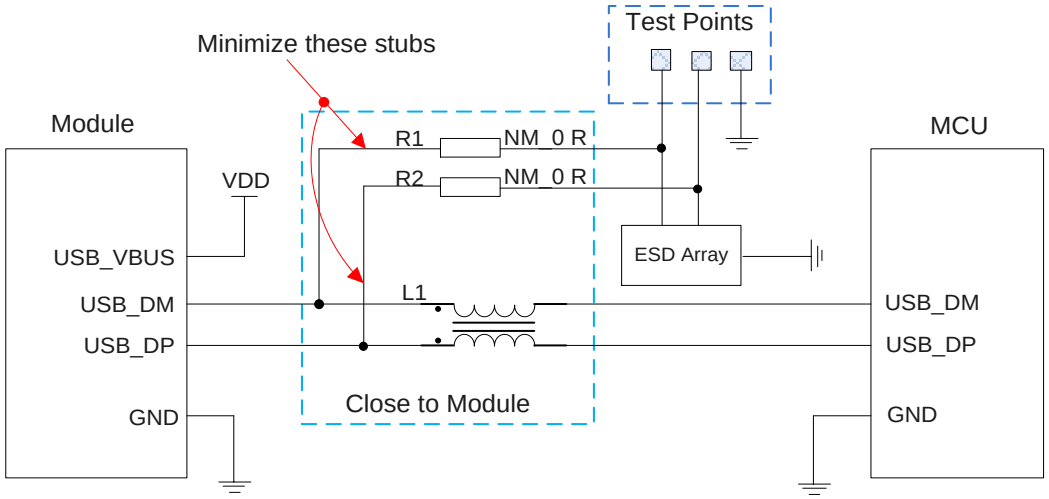


Figure 16: Reference Design of USB Interface

It is recommended to add a common-mode choke L1 in series between MCU and the module to suppress EMI. Meanwhile, it is also suggested to add R1 and R2 in series between the module and test points for debugging. These resistors are not mounted by default. To ensure the signal integrity of USB 2.0 data transmission, you should place L1, R1 and R2 close to the module, and keep these resistors close to each other. Moreover, keep extra stubs of trace as short as possible.

To ensure performance, you should follow the following principles when designing USB interface:

- Route USB signal traces as differential pairs with surrounded ground. The impedance of USB 2.0 differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below.
- Pay attention to the impact caused by stray capacitance of the ESD protection component on USB data lines. Typically, the stray capacitance should be less than 2 pF for USB 2.0.
- If possible, reserve one 0 Ω resistors on USB_DP and USB_DM traces respectively.

4.1.2. USB_ID Interface*

The module supports OTG function, but USB_VBUS cannot provide 5.0 power supply to peripherals, thus, you need to provide (5.0 V) power supply to USB device externally.

The OTG circuit diagram is shown below. This action is detected and completed automatically by USB_ID, and does not require you to send AT command externally. The following is the reference design of USB_ID interface:

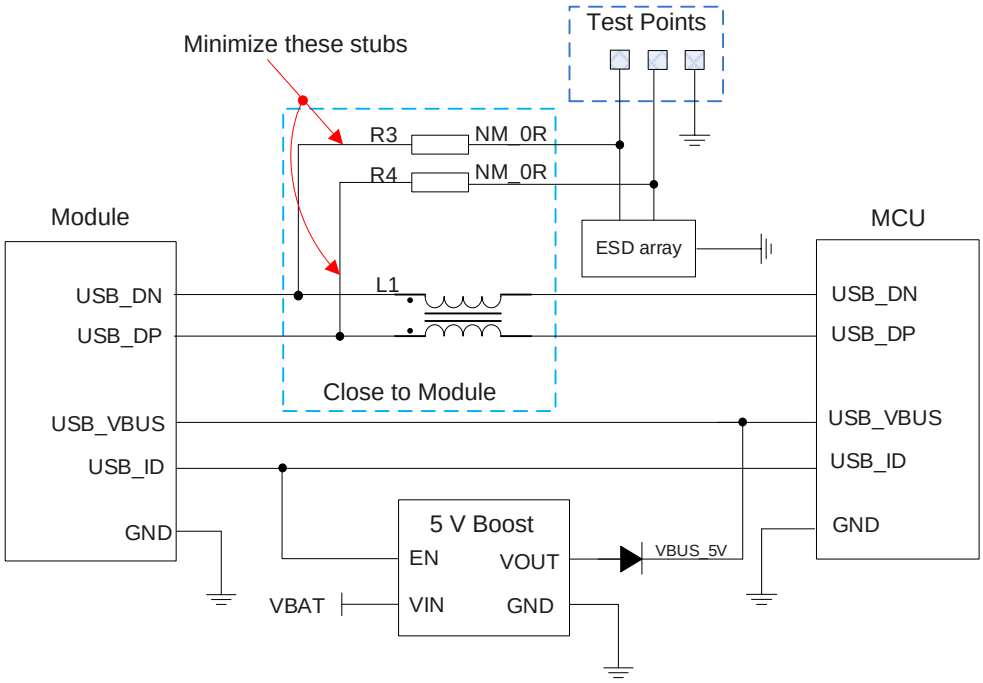


Figure 17: Reference Design of USB OTG

4.2. USB_BOOT

The module supports USB_BOOT function. Pulling down USB_BOOT to GND before turning on the module, and then the module will enter forced download mode. In this mode, the module supports firmware upgrade over USB 2.0 interface.

Table 12: Pin Definition of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	85	DI	Force the module into download mode	Active low. Do not pull it down to a low level before the module starts up successfully. It can be multiplexed as GPIO after the module starts up successfully. A test point is recommended to be reserved.

The reference design is as follows:

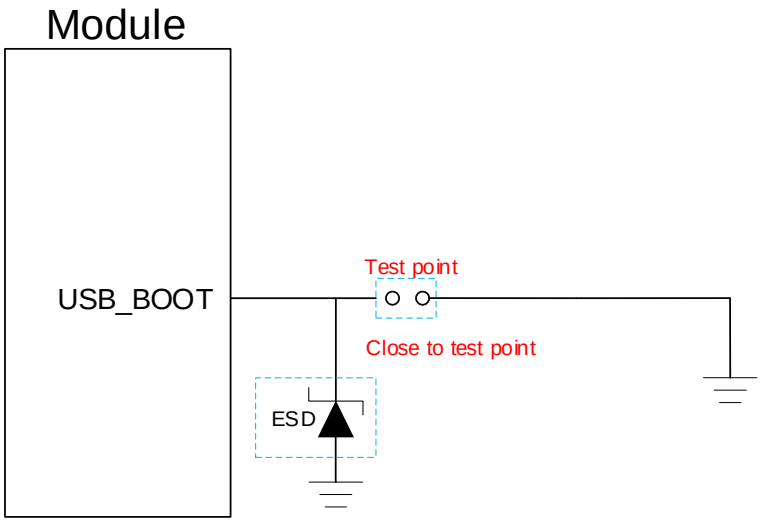


Figure 18: Reference Design of USB_BOOT

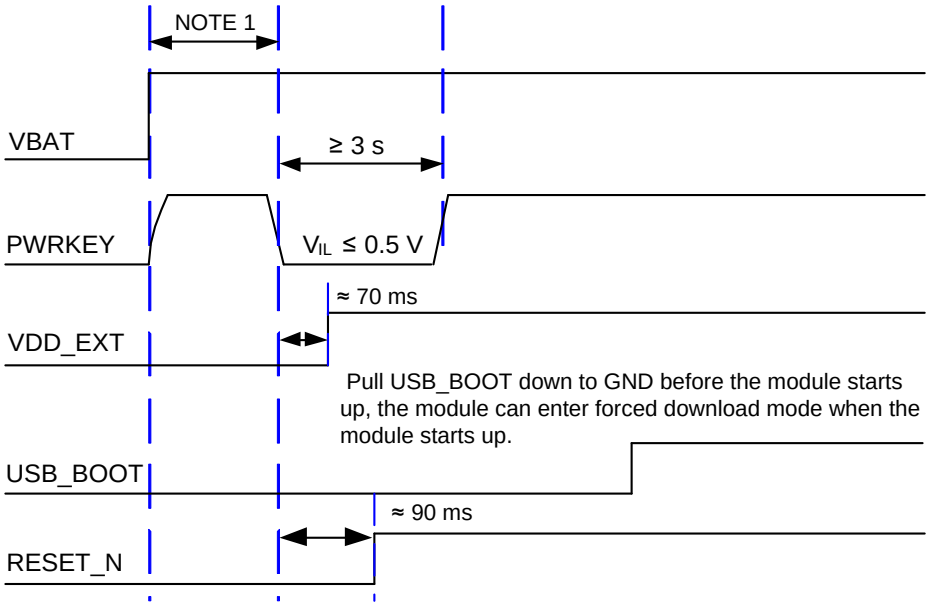


Figure 19: Timing of Entering Forced Download Mode

NOTE

1. Ensure VBAT is stable before driving PWRKEY low. The time period between powering VBAT up and driving PWRKEY low shall be at least 30 ms.
2. Follow the above timing when using MCU to control module to enter the forced download mode. If you need to manually force the module to enter download mode, directly connect the test points shown in ***Figure 18***.

3. If the module needs to start up normally, do not pull USB_BOOT down to a low level before the module starts up successfully.

4.3. (U)SIM Interfaces

The module provides two (U)SIM interfaces, which meet ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V (U)SIM card is supported, and Dual SIM Single Standby function is supported.

Table 13: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	20	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_DATA	17	DIO	(U)SIM1 card data	
USIM1_CLK	19	DO	(U)SIM1 card clock	
USIM1_RST	18	DO	(U)SIM1 card reset	
USIM1_DET	53	DI	(U)SIM1 card hot-plug detect	If unused, keep it open.
USIM2_VDD*	156	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM2_DATA*	155	DIO	(U)SIM2 card data	
USIM2_CLK*	153	DO	(U)SIM2 card clock	
USIM2_RST*	154	DO	(U)SIM2 card reset	

Only (U)SIM1 interface supports hot-plug function. The module supports (U)SIM card hot-plug via the USIM1_DET, and both high-level and low-level detections are supported. Hot-plug function is disabled by default and you can use **AT+QSIMDET** to configure this function.

The reference circuit of the (U)SIM interface with an 8-pin (U)SIM card connector is as follows.

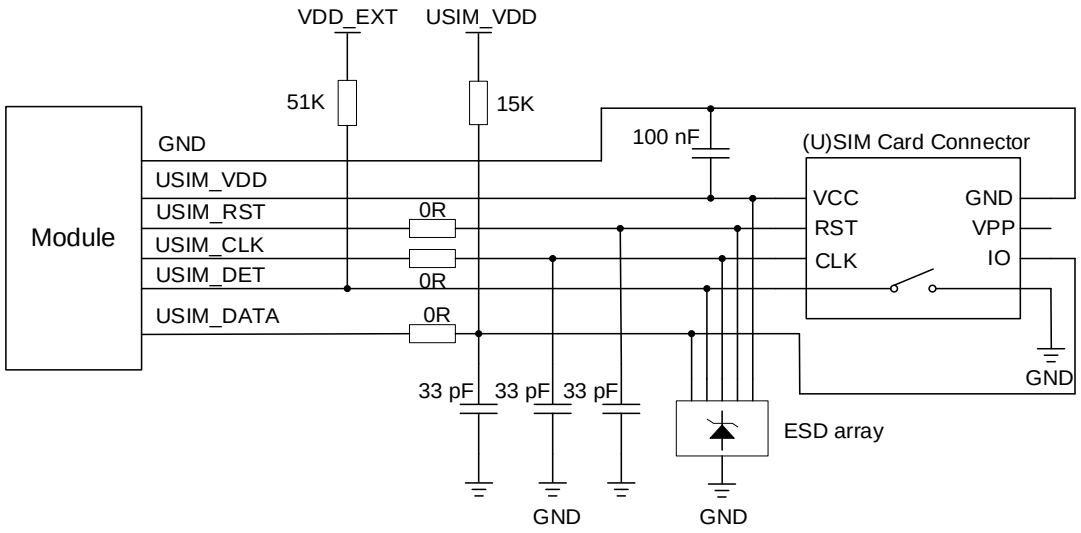


Figure 20: Reference Design of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If the (U)SIM card hot-plug detect function is not needed, keep USIM_DET open. The reference circuit of the (U)SIM interface with a 6-pin (U)SIM card connector is as follows.

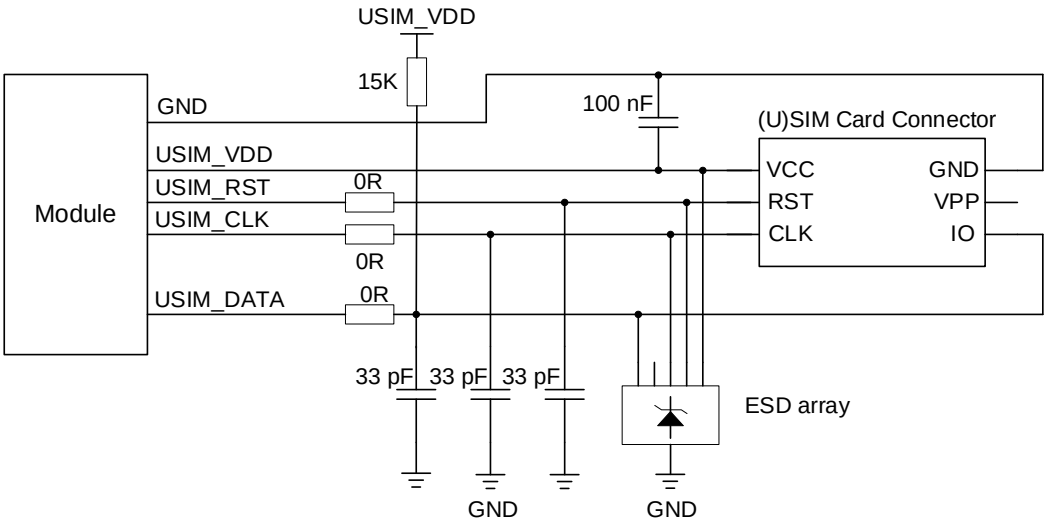


Figure 21: Reference Design of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To ensure performance and reliability, follow the principles below in(U)SIM interface design:

- Place the (U)SIM card connector close to the module. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and power supply traces.
- The bypass capacitor of USIM_VDD cannot exceed 1 μF.

- To avoid cross-talk between USIM_DATA and USIM_CLK, keep the traces away from each other and shield them with surrounded ground.
- To offer better ESD protection, you can add a ESD array of which the parasitic capacitance should not exceed 15 pF. Add 0 Ω resistors in series between the module and the (U)SIM card connector to facilitate debugging. Additionally, add 33 pF capacitors in parallel among USIM_DATA, USIM_CLK and USIM_RST signal traces to filter out RF interference. The peripheral components of the (U)SIM card should be placed as close as possible to the (U)SIM card connector.
- For USIM_DATA, it is recommended to add a pull-up resistor near the (U)SIM card connector to improve the anti-jamming capability of the (U）SIM card. When the routing trace of (U)SIM card is too long or there is a relatively close interference source, it is recommended to add a pull-up resistor near the card connector.

4.4. PCM Interface

The module provides one PCM interface, and it supports short frame synchronization mode: the module can work as both master or slave* device.

In short frame synchronization, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

The module supports 16-bit liner data format. The reference design is illustrated as follows:

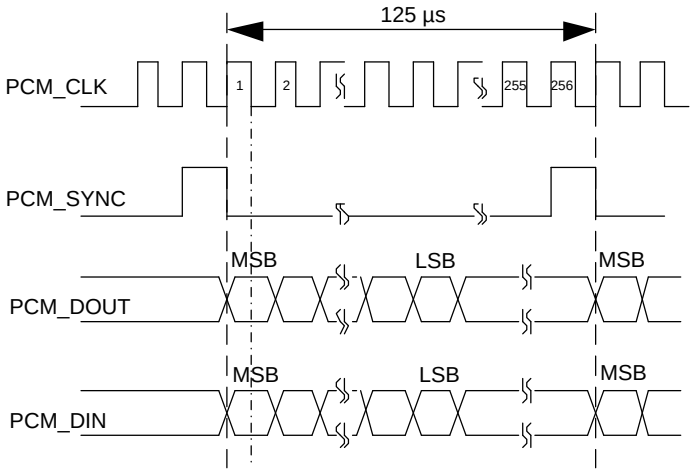


Figure 22: Timing of Short Frame Synchronization Mode

Table 14: Pin Definition of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_SYNC	75	DIO	PCM data frame sync	When the module serves as the master device, the pin is in output state; When the module serves as the slave device*, the pin is in input state. If unused, keep them open.
PCM_CLK	76	DIO	PCM clock	
PCM_DIN	74	DI	PCM data input	If unused, keep them open.
PCM_DOUT	73	DO	PCM data output	

The default configuration is PCM_CLK = 2048 kHz, PCM_SYNC = 8 kHz.

The following figure shows the reference design of PCM and I2C interfaces with external codec chip:

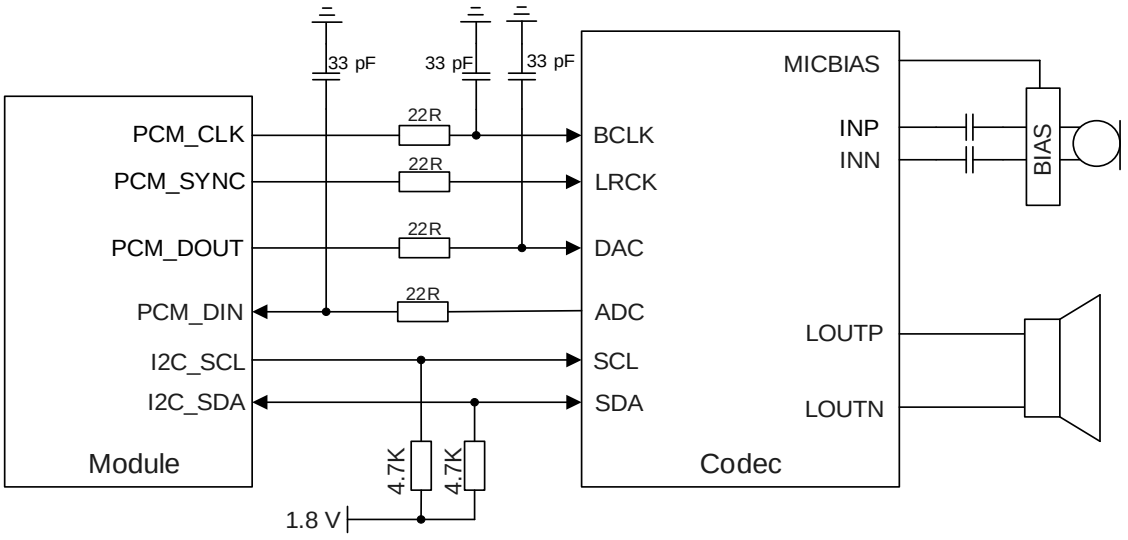


Figure 23: Reference Design of PCM Interface

NOTE

1. It is recommended to reserve an RC (R = 22 Ω, C = 33 pF) circuit on the PCM traces, especially for PCM_CLK.
2. The external codec chip usually requires I2C1 to configure the register, and should be used with the I2C1 interface when using the PCM interface.

4.5. I2C Interfaces

The module has three I2C interfaces, among which two are used by default, and one is multiplexed from other interfaces. The module can only be used as a master device in applications related to the I2C interfaces and does not support multi-master mode. It complies with *The I2C-bus Specification* (100/400 kHz mode). All I2C interfaces are drain open outputs.

Table 15: Pin Definition of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C1_SCL	55	OD	I2C1 serial clock	Used for external codec. An external 1.8 V pull-up resistor is needed. If unused, keep them open.
I2C1_SDA	56	OD	I2C1 serial data	
I2C2_SCL	98	OD	I2C2 serial clock	An external 1.8 V pull-up resistor is needed. If unused, keep them open.
I2C2_SDA	97	OD	I2C2 serial data	

4.6. Analog Audio Interface

The module has one analog audio input channel and one analog audio output channel. Pin definition is shown in the following table.

Table 16: Pin Definition of Analog Audio Interface

Channel	Pin Name	Pin No.	I/O	Description
AIN	MIC_BIAS	157	PO	Bias voltage output for microphone
	MIC_P	158	AI	Microphone analog input (+)
	MIC_N	159		Microphone analog input (-)
AOUT	SPK_P	161	AO	Analog audio differential output channel (+)
	SPK_N	160		Analog audio differential output channel (-)

- AIN channels are differential input channels, which can be applied for input of microphone (usually an electret microphone is used).
- AOUT channel is a differential output channel, typically used for earpiece.

4.6.1. Analog Interface Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g., 10 pF and 33 pF) to filter out RF interference, thus reducing TDD noise. Without this capacitor, TDD noise could be heard during the call. Note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you need to discuss with your capacitor vendors to choose the most suitable capacitor to filter out high-frequency noises.

The severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. Therefore, a suitable capacitor can be selected based on the test results. Sometimes, even no RF filtering capacitor is required. The filter capacitor on the PCB should be placed near the audio device or audio interface as close as possible, and the trace should be as short as possible. The filter capacitor should be passed before reaching other connection points.

To decrease signal interferences, RF antennas should be placed away from audio interfaces and audio traces. Power traces and audio traces should not be parallel, and they should be far away from each other.

The differential audio traces must be routed according to the differential signal layout rule.

4.6.2. Microphone Interface Reference Design

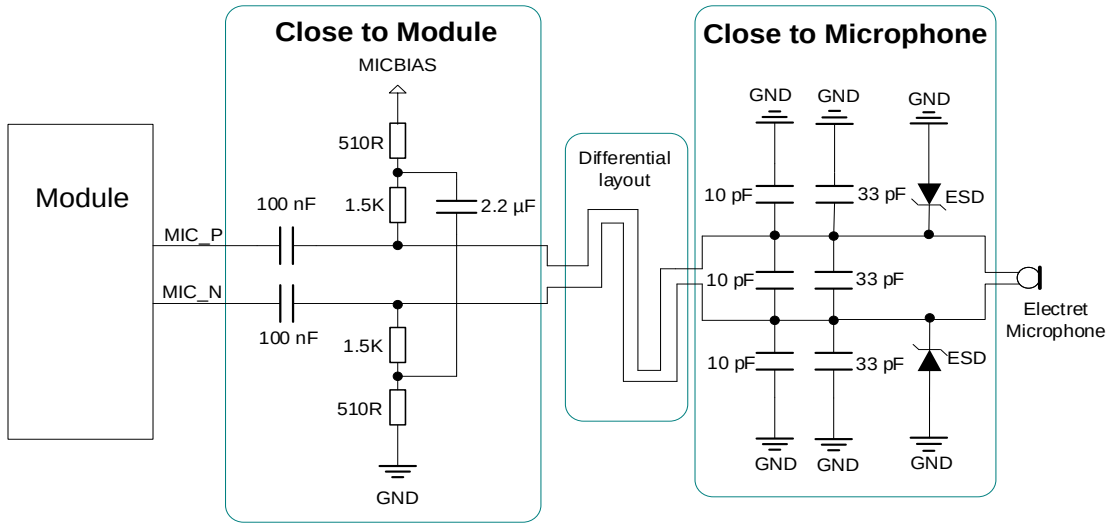


Figure 24: Reference Design of Microphone Interface

NOTE

MIC channel is sensitive to ESD, so it is recommended to use ESD protection components.

4.6.3. Earpiece Interface Reference Design

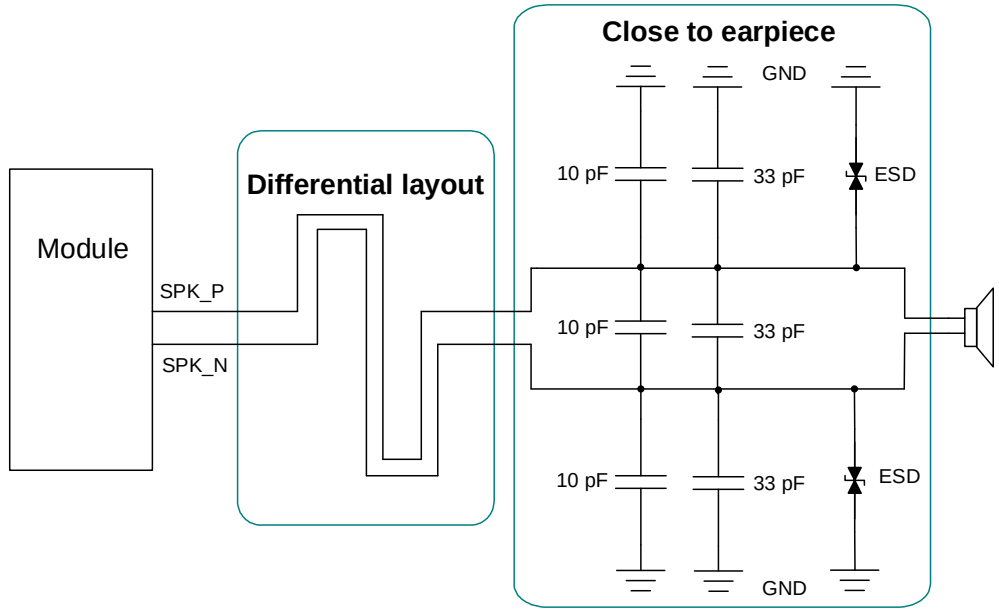


Figure 25: Reference Design of Earpiece Interface

4.7. MIPI DSI Interface

The video output interface of the module is based on MIPI DSI standard and supports one 2-lane MIPI DSI high-speed differential data transmission. It supports up to WVGA (480 × 854) resolution.

Table 17: Pin Definition of MIPI DSI Interface

Pin Name	Pin No.	I/O	Description	Comment
DSI_CLK_N	146	AO	LCD MIPI clock (-)	100 Ω differential impedance is required. If unused, keep them open.
DSI_CLK_P	147	AO	LCD MIPI clock (+)	
DSI_LN0_N	150	AIO	LCD MIPI data 0 (-)	
DSI_LN0_P	151	AIO	LCD MIPI data 0 (+)	

DSI_LN1_N	148	AO	LCD MIPI data 1 (-)
DSI_LN1_P	149	AO	LCD MIPI data 1 (+)

MIPI are high-speed signal traces, to enhance the reliability and availability of application designs, follow the criteria below:

- It is important to route the MIPI signal traces with ground surrounded. The impedance of MIPI data trace is 100 Ω ±10 %.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is recommended to route the MIPI traces in inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below.
- In order to offer good ESD protection, it is recommended to add a TVS array on the MIPI interface with junction capacitance less than 1 pF.
- Keep the MIPI traces at the equal length. The intra-lane length difference of should be kept within 0.5 mm, and the inter-lane length difference should be kept within 1.3 mm, and the total length should be less than 75 mm.
- The spacing between MIPI signal traces should be kept at 1.5 times of the trace width.

NOTE

1. The frame synchronization signal of MIPI DSI interface can be achieved by multiplexing.
2. If MIPI DSI and RGMII/RMII interfaces are used simultaneously, LCD that supports DSI video mode should be used and SYNC signal is not needed.

4.8. Camera Interface

The module provides one camera interface supporting cameras up to 0.3 MP, and the single- or dual-line data transmission of SPI is supported.

Table 18: Pin Definition of Camera Interface

Pin Name	Pin No.	I/O	Description	Comment
CAM_MCLK	100	DO	Camera master clock	1.8 V power domain. If unused, keep them open.
CAM_SPI_CLK	101	DI	Camera SPI clock	
CAM_SPI_DATA0	102	DI	Camera SPI data bit 0	
CAM_SPI_DATA1	103	DI	Camera SPI data bit 1	

NOTE

Keep the impedance of CAM_MCLK signal trace at 50 Ω ±10 %.

4.9. UARTs

The module supports four UARTs, among which main UART and debug UART are used by default, and other two UARTs can be multiplexed from other interfaces. The main features of main UART and debug UART are described as follows:

- Main UART supports 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, 921600 bps baud rates. The default baud rate is 115200 bps. It is used for AT command communication and data transmission. Also, it supports RTS and CTS hardware flow control.
- Debug UART supports 115200 bps baud rates. It is used for partial log output.

The pin definition is as follows:

Table 19: Pin Definition of Main UART

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	67	DI	Clear to send signal to the module	If unused, keep them open.
MAIN_RTS	66	DO	Request to send signal from the module	
MAIN_RXD	112	DI	Main UART receive	Test points are recommended to be reserved.
MAIN_TXD	113	DO	Main UART transmit	
MAIN_DTR	72	DI	Main UART data terminal ready	If unused, keep it open.

Table 20: Pin Definition of Debug UART

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	106	DI	Debug UART receive	Test points must be reserved.
DBG_TXD	42	DO	Debug UART transmit	

The module provides 1.8 V UART. You can use a level-shifting circuit between the module and MCU's UART if the MCU is equipped with a 3.3 V UART. The following figure shows a reference design:

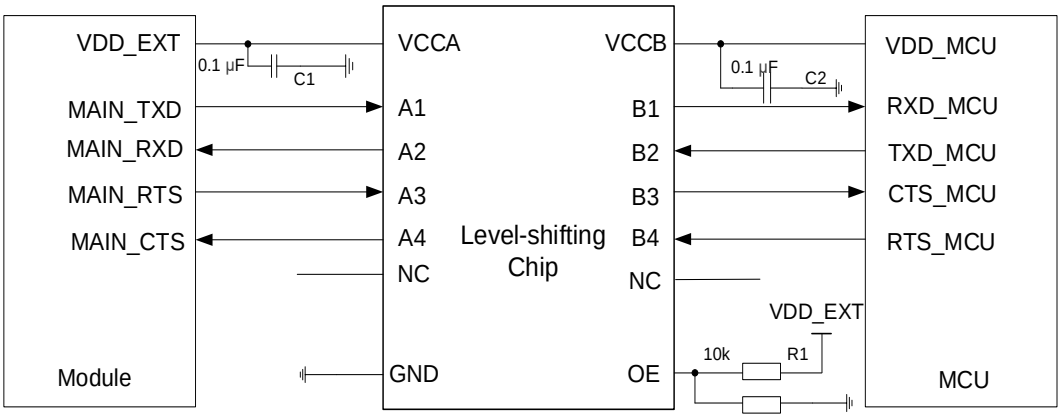


Figure 26: Reference Design of UART with Level-shifting Chip

Another example of level-shifting circuit is shown as below. For the design shown in dotted lines, see that shown in solid lines, but pay attention to the direction of the connection.

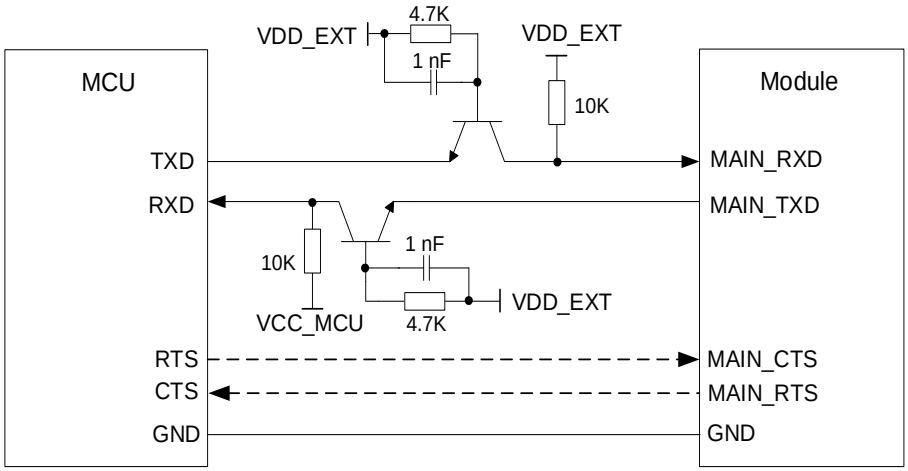


Figure 27: Reference Design of UART with Transistor Circuit

NOTE

1. Transistor circuit above is not suitable for applications with baud rates exceeding 460 kbps.
2. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

4.10. SDIO Interfaces

4.10.1. SD Card Application

The module provides one SD application interface compliant with SD 3.0 specification.

Table 21: Pin Definition of SD Card Application Interface

Pin Name	Pin No.	I/O	Description	Comment
SDIO_CLK	26	DO	SDIO clock	If unused, keep them open.
SDIO_CMD	21	DIO	SDIO command	
SDIO_DATA0	22	DIO	SDIO data bit 0	
SDIO_DATA1	23	DIO	SDIO data bit 1	
SDIO_DATA2	24	DIO	SDIO data bit 2	
SDIO_DATA3	25	DIO	SDIO data bit 3	
SDIO_VDD	144	PO	SDIO power supply	Provides a pull-up power supply for external SDIO interface. It cannot be used as a power supply. If unused, keep it open.
SD_DET*	48	DI	SD card hot-plug detect	If unused, keep it open.

The following figure shows the reference design of SD card application interface.

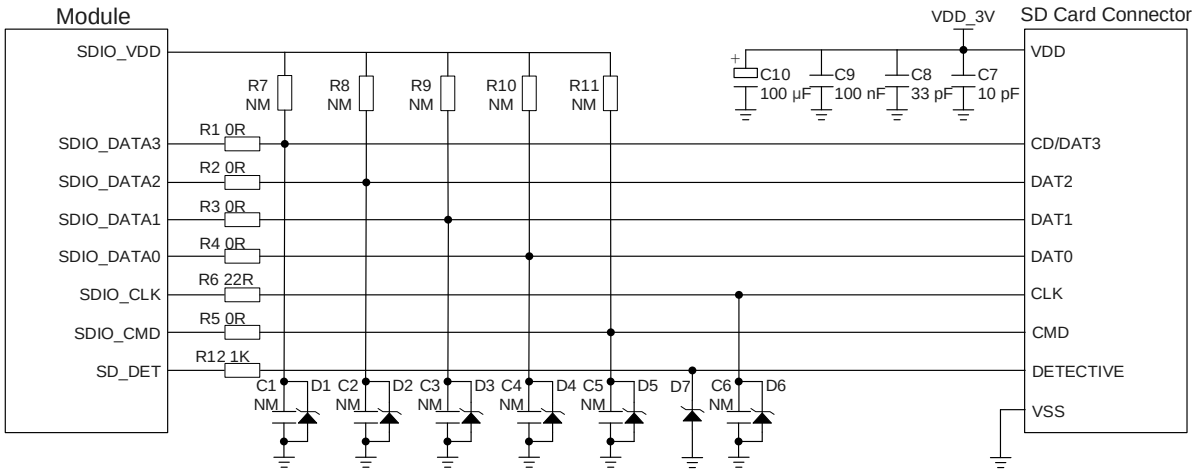


Figure 28: Reference Design of SD Card Application Interface

To ensure better performance and reliability, the following conditions should be taken into considerations when designing SD card application interface:

- The voltage range of VDD_3V is 2.7–3.6 V and it should provide a current of 200–800 mA, which is defined by the type of SD card. SDIO_VDD can provide up to 50 mA current which can only be used for SDIO pull-up resistors. VDD_3V is provided externally.
- To avoid the impact of jitter, reserve pull-up resistors (R7–R11) on SDIO signal traces. The resistance of these resistors can be 10–100 kΩ, the recommended value is 100 kΩ, and they are not mounted by default. SDIO_VDD should be used as the pull-up power supply.
- To enhance signal quality, add 0 Ω resistors (R1–R5) in series, and add 15–24 Ω resistor on SDIO_CLK, keep the trace length matching between SDIO_CLK and the resistor less than 5 mm. Add bypass capacitors C1–C6 (not mounted by default) between the module and the SD card connector. All resistors and bypass capacitors should be placed close to the connector.
- Add an ESD component with capacitance value of less than 8 pF on each SD card pin for better ESD protection.
- It is important to route SDIO signal traces at the inner-layer of the PCB and with surrounded ground. The impedance is 50 Ω ±10 %.
- Keep SDIO signal traces far away from sensitive signals and signals like RF signals, analog signals, and noise signals generated by clock and DC-DC.
- Keep the trace length matching between SDIO_CLK and SDIO_DATA[0:3]/SDIO_CMD less than 1 mm and the total routing length less than 50 mm.
- Keep the adjacent trace clearance twice the trace width and the load capacitance of SDIO bus less than 15 pF.

4.10.2. WLAN Application Interface

The module provides one low-power SDIO 3.0 WLAN application interface and one control interface.

Table 22: Pin Definition of WLAN Application Interface

Pin Name	Pin No.	I/O	Description	Comment
WLAN_SLP_CLK	34	DO	WLAN sleep clock	If unused, keep them open.
WLAN_PWR_EN	33	DO	WLAN power supply enable control	
WLAN_SDIO_DATA3	31	DIO	WLAN SDIO data bit 3	
WLAN_SDIO_DATA2	28	DIO	WLAN SDIO data bit 2	
WLAN_SDIO_DATA1	27	DIO	WLAN SDIO data bit 1	
WLAN_SDIO_DATA0	30	DIO	WLAN SDIO data bit 0	
WLAN_SDO_CLK	32	DO	WLAN SDIO clock	
WLAN_SDIO_CMD	29	DIO	WLAN SDIO command	
WLAN_WAKE	84	DI	WLAN wake up the module	
WLAN_EN	83	DO	WLAN enable control	

In WLAN application interface design, in order to ensure good performance, the following design principles should be complied with:

- To avoid the impact of jitter, reserve pull-up resistors on SDIO signal traces Resistance of these resistors can be 10–100 kΩ and they are not mounted by default. VDD_EXT should be used as the pull-up power supply.
- It is important to route SDIO signal traces at the inner-layer of the PCB and with surrounded ground. The impedance is 50 Ω ±10 %.
- Keep SDIO signal traces far away from sensitive signals and signals like RF signals, analog signals, and noise signals generated by clock and DC-DC.
- It is recommended to keep the trace length difference between WLAN_SDIO_CLK, WLAN_SDIO_DATA[0:3] and WLAN_SDIO_CMD less than 1 mm and the total routing length less than 50 mm.
- Keep series resistors within 15–24 Ω on WLAN_SDIO_CLK traces near the module and keep the distance from the WLAN_SDIO_CLK to these resistors less than 5 mm.
- The spacing between SDIO signals and other signals needs to be greater than twice the trace width, and the load capacitance of SDIO bus is less than 15 pF.

4.11. ADC Interfaces

The module supports three ADC interfaces. To improve the accuracy of ADC, the trace of ADC interface should be surrounded by ground.

Table 23: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	121	AI	General-purpose ADC interface	If unused, keep them open.
ADC1	47	AI		
ADC2	46	AI		

You can use the *ql_adc_read()* to read the voltage of ADC interfaces.

The following table describes the characteristics of ADC interfaces.

Table 24: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC0 input voltage range	0	-	VBAT_BB	V
ADC1 input voltage range	0	-	VBAT_BB	V
ADC2 input voltage range	0	-	1.2	V
ADC resolution	-	12	-	bits

NOTE

1. The input voltage of each ADC interface should not exceed its corresponding voltage range.
2. It is prohibited to directly supply any voltage to ADC[0:1] interfaces when the module is not powered by the VBAT.
3. It is prohibited to directly supply any voltage to ADC2 interface before the module starts up successfully.
4. If use resistor divider circuit for ADC interface application, resistance of the external resistor divider should not exceed 100 kΩ.

4.12. SPI

The module supports three SPIs, which support master and slave* modes with a maximum clock frequency of 52 MHz. One SPI is used by default, and other two are multiplexed from other interfaces.

Table 25: Pin Definition of SPI

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	7	DIO	SPI clock	When the module serves as the master device, the pin is in output state; When the module serves as the slave device*, the pin is in input state. If unused, keep them open.
SPI_CS	8	DIO	SPI chip select	
SPI_DIN	93	DI	SPI data input	If unused, keep them open.
SPI_DOUT	94	DO	SPI data output	

Refer to the following figures.

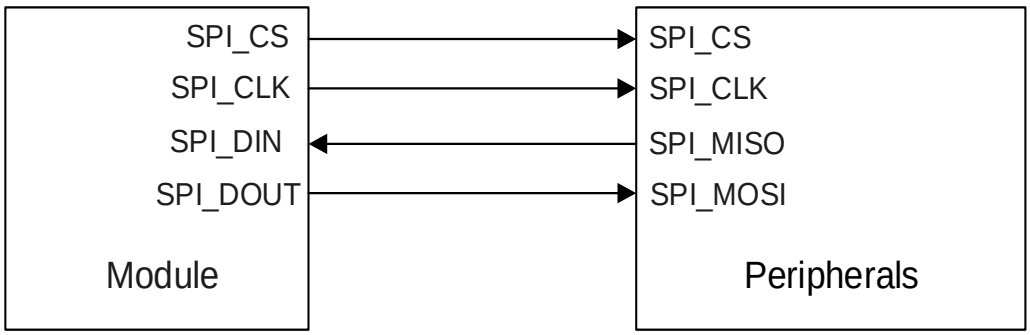


Figure 29: Reference Design of SPI (Module as Master)

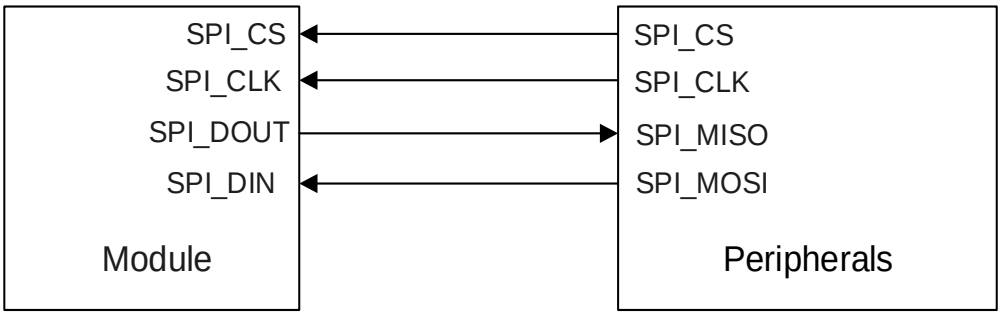


Figure 30: Reference Design of SPI (Module as Slave*)

4.13. RGMII*/RMII Interface

The module provides one RGMII/RMII interface, which can be connected with 100 MB or 1,000 MB PHY chip.

Table 26: Pin Definition of RGMII/RMII Interface

Pin Name	Pin No.	I/O	Description	Comment
RGMII/RMII_RX0	88	DI	RGMII/RMII receive data bit 0	RGMII supports 1.8 V power domain. RMII supports 1.8/3.3 V power domain. If unused, keep them open.
RGMII/RMII_RX1	120	DI	RGMII/RMII receive data bit 1	
RGMII/RMII_RXC	89	DI	RGMII/RMII receive clock	
RGMII/RMII_RX_CTL	90	DI	RGMII/RMII receive control	
RGMII/RMII_TX0	68	DO	RGMII/RMII transmit data bit 0	
RGMII/RMII_TX1	69	DO	RGMII/RMII transmit data bit 1	
RGMII/RMII_TX_CTL	86	DO	RGMII/RMII transmit control	
RGMII/RMII_INT_N	109	DI	RGMII/RMII interrupt	
RGMII/RMII_MDC	117	DO	RGMII/RMII management data clock	
RGMII/RMII_MDIO	116	DIO	RGMII/RMII management data input/output	
RGMII_RX2	127	DI	RGMII receive data bit 2	
RGMII_RX3	119	DI	RGMII receive data bit 3	
RGMII_TX2	114	DO	RGMII transmit data bit 2	

RGMII_TX3	115	DO	RGMII transmit data bit 3	
RGMII_TXC	126	DO	RGMII transmit clock	
RGMII/RMII_RST_N	108	DO	RGMII/RMII external PHY reset	If unused, keep it open.

The following is a reference circuit of the connection between RMII and 100 MB PHY chip (the voltage domain is 3.3 V), where the RMII voltage domain is 3.3 V by default.

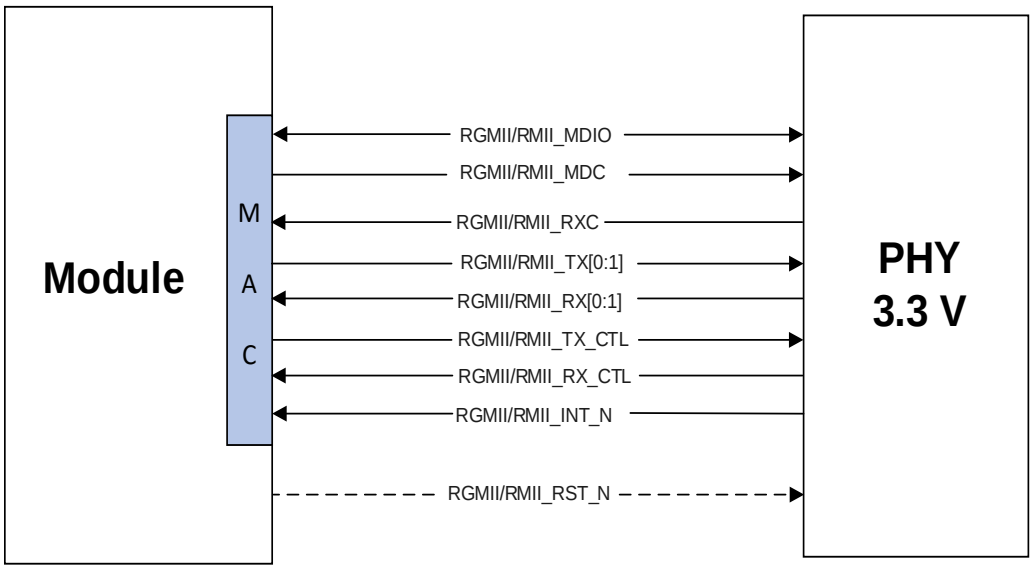


Figure 31: Reference Design of RMII Connected with 100 MB PHY

The following is a reference circuit of the connection between RGMII and 1,000 MB PHY chip (the voltage domain is 1.8 V), where the RGMII voltage domain is 1.8 V by default.

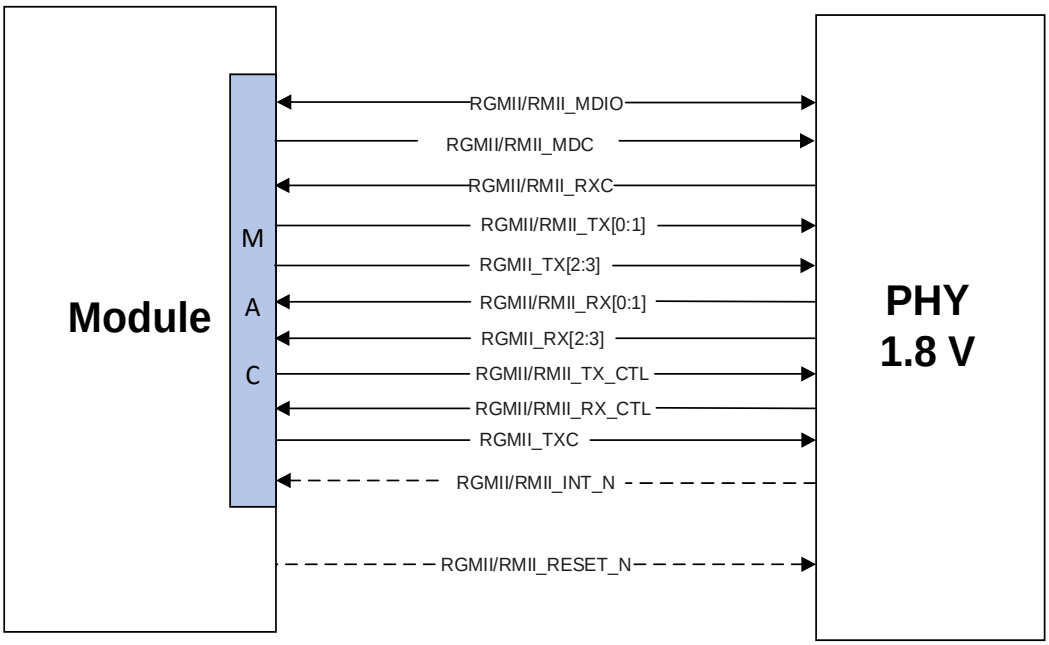


Figure 32: Reference Design of RGMII Connected with 1,000 MB PHY

To ensure performance, you should follow the following principles when designing RGMII/RMII interface:

- Keep data signal and control signal traces of RGMII/RMII interface far away from VBAT power supply traces, crystal, oscillator, magnetic devices and sensitive signals like RF signals, analog signals, and noise signals generated by clock and DC-DC.
- The single-ended impedance of RGMII/RMII data traces is 50 Ω ±10 %.
- The length difference of RGMII/RMII_TX[0:1], RGMII_TX[2:3], RGMII/RMII_TX_CTL, RGMII_TXC should be less than 0.25 mm, and the space between the signal traces should be larger than twice of trace width. Similarly, the length difference of RGMII/RMII_RX[0:1], RGMII_RX[2:3], RGMII/RMII_RX_CTL, RGMII/RMII_RXC should be less than 0.25 mm, and the space between the signal traces should be larger than twice of trace width.
- Spacing between Tx bus and Rx bus should be larger than 2.5 times of the trace width.
- Spacing between Tx bus or Rx bus should be larger than 3 times of the trace width.

NOTE

1. Pin 108 (RGMII/RMII_RST_N) is connected to PHY chip as a GPIO. Other GPIOs can also be used as RGMII/RMII_RST_N to reset PHY chip.
2. Pay attention to the level match shown in the dotted line between the module and the host.
3. If RMII interface is used, the length difference of RGMII/RMII_TX[0:1] and RGMII/RMII_TX_CTL should be less than 2 mm, and the length difference of RGMII/RMII_RX[0:1], RGMII/RMII_RX_CTL and RGMII/RMII_RXC should be less than 2 mm.

4.14. Indication Signal

The following table shows the indication signal interfaces:

Table 27: Pin Definition of Indication Signal

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	51	DO	Indicate the module's network activity status	If unused, keep them open.
STATUS	49	DO	Indicate the module's operation status	

4.14.1. Network Status Indication

The module provides one network status indication pin: the NET_STATUS for the module's network operation status indication, which can drive corresponding LEDs.

Table 28: Network Status Indication Pin Level and Module Network Status

Pin Name	Level Status	Description
NET_STATUS	Blink slowly (200 ms high/1800 ms low)	Network searching
	Blink slowly (1800 ms high/200 ms low)	Idle
	Blink quickly (125 ms high/125 ms low)	Data transmission is ongoing
	High-level input voltage	Voice calling

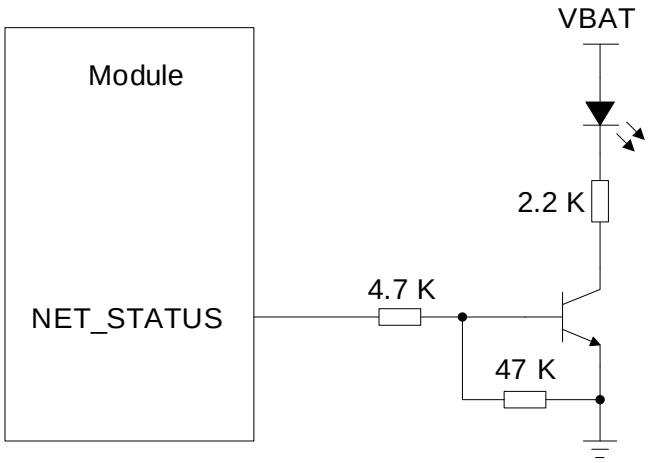


Figure 33: Reference Design of Network Status Indication

4.14.2. STATUS

The STATUS is used for indicating module's operation status. It will output high level when the module is turned on normally.

The following figure shows the reference design of STATUS.

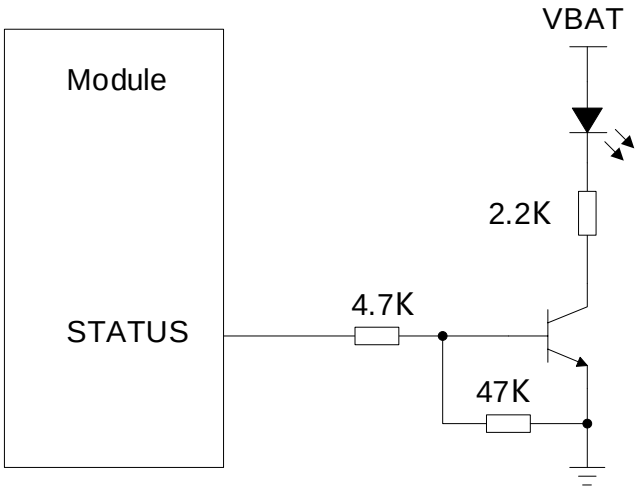


Figure 34: Reference Design of STATUS

NOTE

The status pin cannot be used as an indication of module shutdown status when VBAT is not available.

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Cellular Network

5.1.1. Antenna Interface & Frequency Bands

The cellular network antenna interfaces of the module are defined as follows:

Table 29: Pin Definition of Cellular Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_DRX	82	AI	Rx-diversity antenna interface	50 Ω characteristic impedance.
ANT_MAIN	59	AIO	Main antenna interface	

Table 30: Operating Frequency

Operating Frequency	Transmit (MHz)	Receive (MHz)
GSM850	824–849	869–894
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
PCS1900	1850–1910	1930–1990
WCDMA B1	1922–1978	2112–2168
WCDMA B2	1852–1908	1932–1988
WCDMA B4	1712–1753	2112–2153

WCDMA B5	826–847	871–892
WCDMA B8	882–913	927–958
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B2	1850–1910	1930–1990
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B4	1710–1755	2110–2155
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960
LTE-FDD B28	703–748	758–803
LTE-FDD B66	1710–1780	2110–2180

5.1.2. Antenna Tuner Control Interfaces

The module can control an external antenna tuner via the GRFC interfaces.

Table 31: Pin Definition of GRFC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GRFC1	35	DO	Generic RF controller	1.8 V power domain. If unused, keep them open.
GRFC2	36	DO		

Table 32: Truth Table of GRFC Interfaces (Unit: MHz)

GRFC1 Level	GRFC2 Level	Band Range (MHz)	Frequency Band
Low	Low	703–747.9	B28
Low	High	824–861.9	B5
High	Low	880–914.9	B8
High	High	1710–2674.9	B1/B2/B3/B4/B7/B66

5.1.3. Transmitting Power

Transmitting power is shown in the following table:

Table 33: RF Transmitting Power

Frequency Band	Max.	Min.
GSM850	33 dBm ±2 dB	5 dBm ±5 dB
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
GSM850 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
GSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
PCS1900 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
WCDMA B1/B2/B4/B5/B8	23 dBm ±2 dB	< -49 dBm
LTE-FDD B1/B2/B3/B4/B5/B7/B8/B28/B66	23 dBm ±2 dB	< -39 dBm

NOTE

For GPRS transmission on 4 uplink timeslots, the maximum output power reduction is 4.0 dB. The design conforms to *3GPP TS 51.010-1* ***subclause 13.16***.

5.1.4. Receiver Sensitivity

Receiver sensitivity is shown in the following table:

Table 34: Conducted RF Receiver Sensitivity (Unit: dBm)

Frequency Band	Receiver Sensitivity (Typ.)			3GPP Requirement (SIMO)
	Primary	Diversity	SIMO	
GSM850	-108.6	-	-	-102.4
EGSM900	-108.4	-	-	-102.4
DCS1800	-108	-	-	-102.4
PCS1900	-107.9	-	-	-102.4
WCDMA B1	-109.7	-	-	-106.7
WCDMA B2	-108.8	-	-	-104.7
WCDMA B4	-109.1	-	-	-106.7
WCDMA B5	-109.4	-	-	-104.7
WCDMA B8	-108.8	-	-	-103.7
LTE-FDD B1	-97.7	-97.8	-100.9	-96.3
LTE-FDD B2	-97.1	-98	-100.6	-94.3
LTE-FDD B3	-97.3	-98	-100.3	-93.3
LTE-FDD B4	-97.1	-97.4	-100.3	-96.3
LTE-FDD B5	-98.1	-98.2	-100.6	-94.3
LTE-FDD B7	-95.2	-96.8	-99.7	-94.3
LTE-FDD B8	-97.2	-98.3	-99.9	-93.3
LTE-FDD B28	-98.3	-98.2	-100.1	-94.8
LTE-FDD B66	-96.6	-96.8	-100.3	-96.5

5.1.5. Reference Design

The module provides two RF antenna for antenna connection.

Use a π-type matching circuit for the antenna interfaces for better RF performance. Capacitors are not mounted by default.

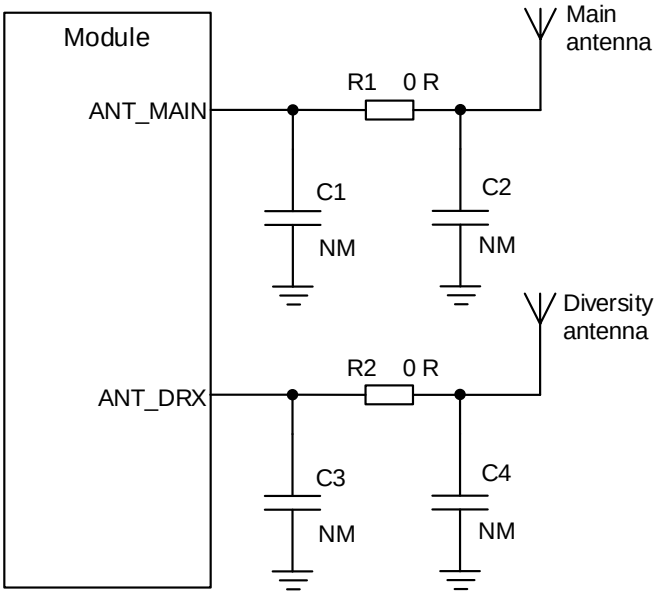


Figure 35: Reference Design of Antenna Interfaces

5.2. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

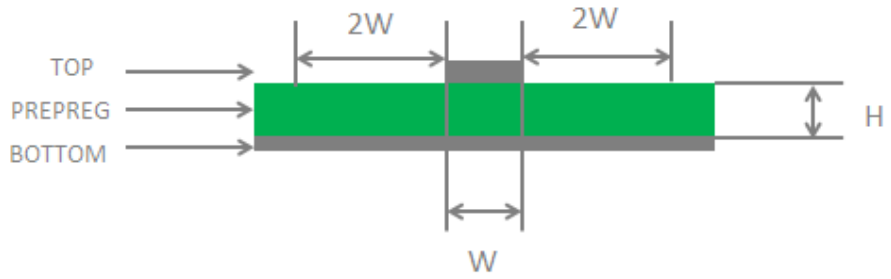


Figure 36: Microstrip Design on a 2-layer PCB

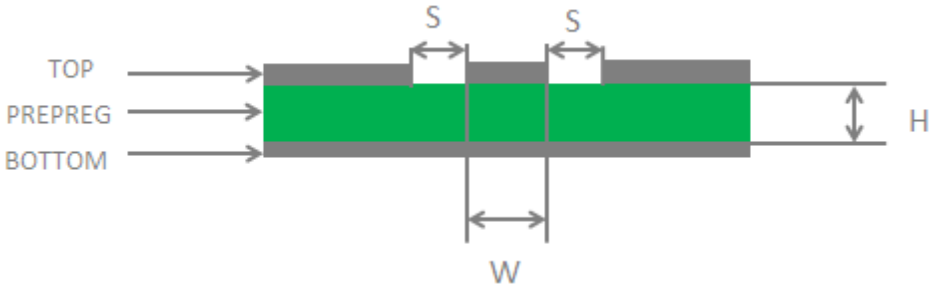


Figure 37: Coplanar Waveguide Design on a 2-layer PCB

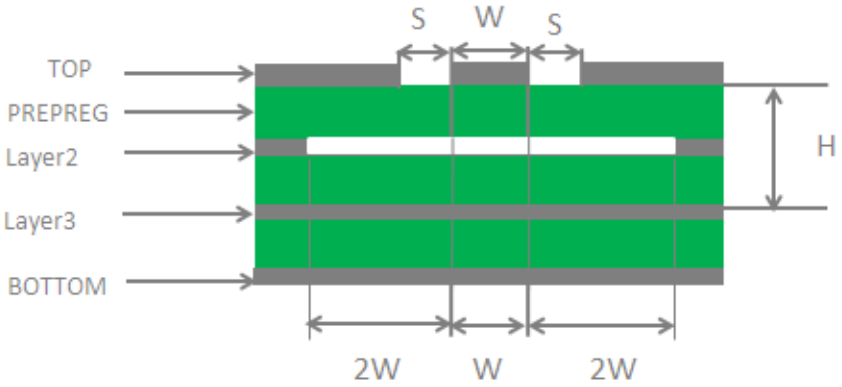


Figure 38: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

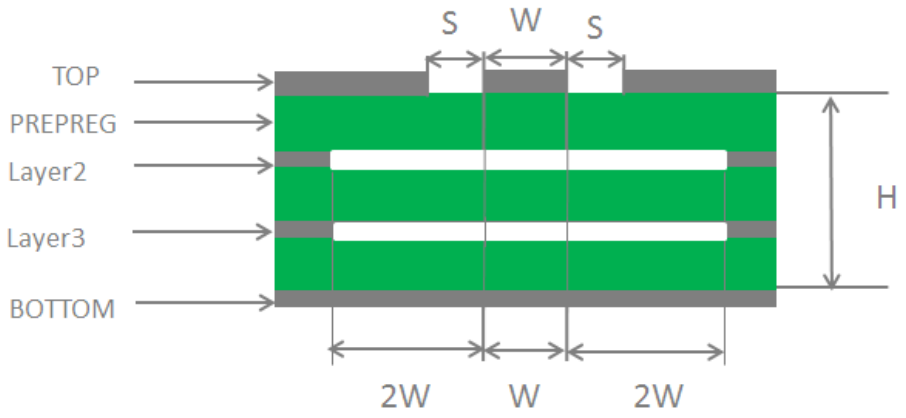


Figure 39: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

5.3. Antenna Design Requirements

The following is antenna design requirements:

Table 35: Antenna Design Requirements

Antenna Type	Requirement
Celluar	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Passive antenna gain: 3 dBi(max) ● Max input power: 50 W ● Input impedance: 50 Ω ● Vertical polarization ● Cable insertion loss: **< 1 dB**: LB (> 1 GHz) **< 1.5 dB**: MB (1–2.3 GHz) **< 2 dB**: HB (> 2.3 GHz)

5.4. RF Connector Recommendation

If the RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT receptacle provided by Hirose.

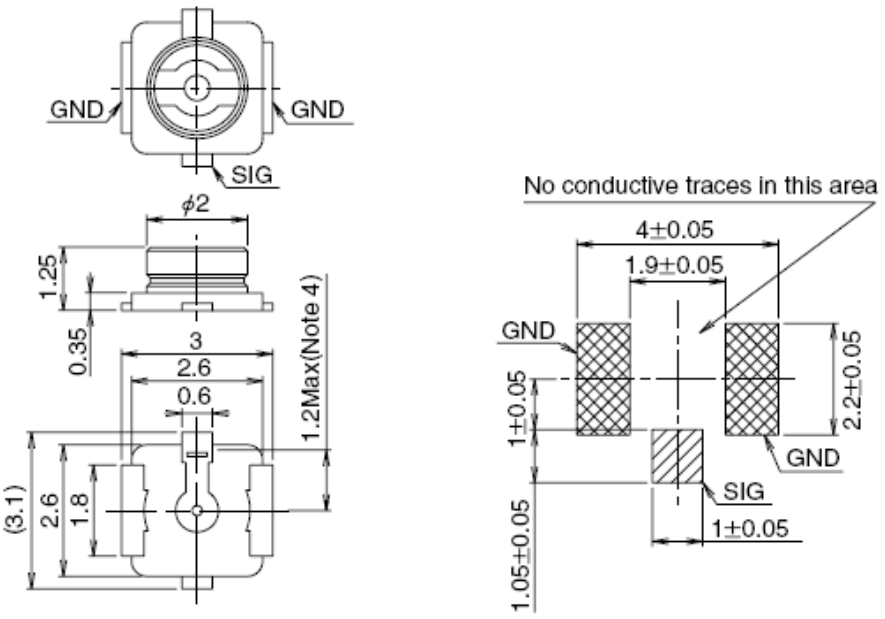


Figure 40: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

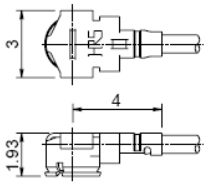
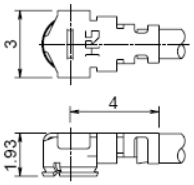
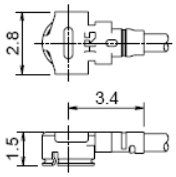
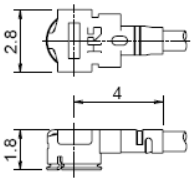
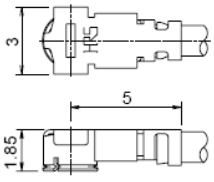
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 41: Specifications of Mated Plugs (Unit: mm)

The following figure describes the space factor of the mated connector.

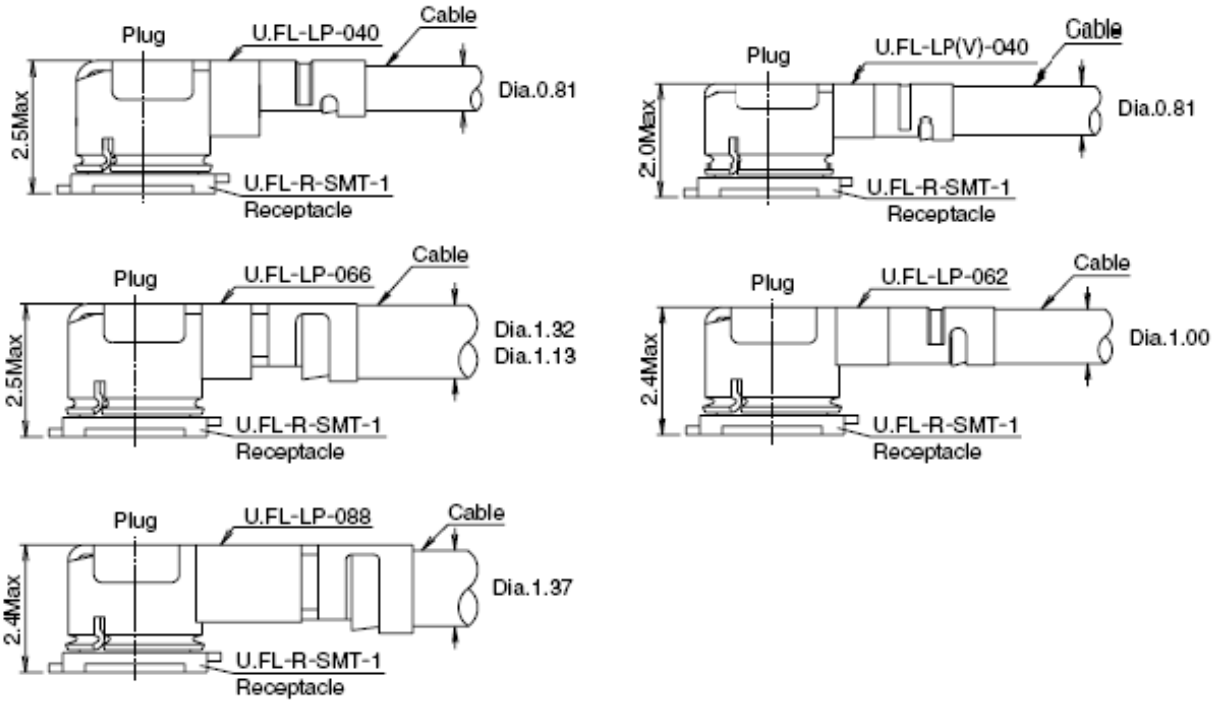


Figure 42: Space Factor of the Mated Connectors (Unit: mm)

For more details, visit http://hirose.com.

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

The table below shows the pin voltage or the maximum tolerance value of current.

Table 36: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	5.5	V
USB_VBUS	-0.3	5.5	V
Current at VBAT_BB	-	1.5	A
Current at VBAT_RF	-	2.0	A
Voltage at digital pins	-0.3	2.3	V
Input voltage at ADC[0:1]	0	VBAT_BB	V
Input voltage at ADC2	0	1.2	V

6.2. Power Supply Ratings

Table 37: Module's Power Supply Ratings

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.4	3.8	4.3	V
	Voltage drops during burst	At maximum power control level	-	-	400	mV

	transmission					
I_{VBAT_RF}	Peak supply power consumption	At maximum power control level	-	-	2.0	A
USB_VBUS	USB connection detect	-	3.0	5.0	5.25	V

6.3. Power Consumption

Table 38: Power Consumption

Description	Condition	Typ.	Unit
Shutdown Mode	Power off	11	μA
Sleep Mode	Minimum Functionality Mode (USB disconnected)	1.54	mA
	EGSM900 @ DRX = 2 (USB disconnected)	2.32	mA
	EGSM900 @ DRX = 5 (USB disconnected)	1.88	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.73	mA
	DCS1800 @ DRX = 2 (USB disconnected)	2.29	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.83	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.70	mA
	WCDMA @ PF = 64 (USB disconnected)	3.18	mA
	WCDMA @ PF = 128 (USB disconnected)	2.45	mA
	WCDMA @ PF = 256 (USB disconnected)	2.09	mA
	WCDMA @ PF = 512 (USB disconnected)	1.88	mA
	LTE-FDD @ PF = 32 (USB disconnected)	3.11	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.42	mA
	LTE-FDD @ PF = 128 (USB disconnected)	2.09	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.87	mA

	LTE-TDD @ PF = 32 (USB disconnected)	3.03	mA
	LTE-TDD @ PF = 64 (USB disconnected)	2.42	mA
	LTE-TDD @ PF = 128 (USB disconnected)	2.07	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.88	mA
Idle Mode	EGSM900 @ DRX = 5 (USB disconnected)	22.70	mA
	EGSM900 @ DRX = 5 (USB connected)	36.72	mA
	DCS1800 @ DRX = 5 (USB disconnected)	22.59	mA
	DCS1800 @ DRX = 5 (USB connected)	35.62	mA
	WCDMA @ PF = 64 (USB disconnected)	23.03	mA
	WCDMA @ PF = 64 (USB connected)	36.07	mA
	LTE-FDD @ PF = 64 (USB disconnected)	23.45	mA
	LTE-FDD @ PF = 64 (USB connected)	35.54	mA
	LTE-TDD @ PF = 64 (USB disconnected)	22.72	mA
	LTE-TDD @ PF = 64 (USB connected)	35.56	mA
GPRS data transmission	GSM850 4DL/1UL @ 32.74 dBm	265	mA
	GSM850 3DL/2UL @ 32.76 dBm	455	mA
	GSM850 2DL/3UL @ 30.96 dBm	542	mA
	GSM850 1DL/4UL @ 29.16 dBm	587	mA
	EGSM900 4DL/1UL @ 32.67 dBm	265	mA
	EGSM900 3DL/2UL @ 32.67 dBm	455	mA
	EGSM900 2DL/3UL @ 31.07 dBm	549	mA
	EGSM900 1DL/4UL @ 29.31 dBm	600	mA
	DCS1800 4DL/1UL @ 29.53 dBm	188	mA
	DCS1800 3DL/2UL @ 29.53 dBm	302	mA
	DCS1800 2DL/3UL @ 28.25 dBm	360	mA

	DCS1800 1DL/4UL @ 26.23 dBm	376	mA
	PCS1900 4DL/1UL @ 29.79 dBm	186	mA
	PCS1900 3DL/2UL @ 29.78 dBm	297	mA
	PCS1900 2DL/3UL @ 28.45 dBm	358	mA
	PCS1900 1DL/4UL @ 26.57 dBm	378	mA
EDGE data transmission	GSM850 4DL/1UL @ 26.81 dBm	185	mA
	GSM850 3DL/2UL @ 27.18 dBm	291	mA
	GSM850 2DL/3UL @ 24.71 dBm	348	mA
	GSM850 1DL/4UL @ 22.65 dBm	395	mA
	EGSM900 4DL/1UL @ 27.11 dBm	193	mA
	EGSM900 3DL/2UL @ 27.01 dBm	303	mA
	EGSM900 2DL/3UL @ 25.21 dBm	353	mA
	EGSM900 1DL/4UL @ 22.76 dBm	393	mA
	DCS1800 4DL/1UL @ 26.04 dBm	169	mA
	DCS1800 3DL/2UL @ 25.89 dBm	263	mA
	DCS1800 2DL/3UL @ 23.73 dBm	328	mA
	DCS1800 1DL/4UL @ 21.84 dBm	397	mA
	PCS1900 4DL/1UL @ 26.24 dBm	168	mA
	PCS1900 3DL/2UL @ 26.22 dBm	260	mA
	PCS1900 2DL/3UL @ 24.06 dBm	332	mA
	PCS1900 1DL/4UL @ 21.74 dBm	401	mA
WCDMA data transmission	WCDMA B1 HSDPA @ 22.39 dBm	571	mA
	WCDMA B2 HSDPA @ 21.91 dBm	641	mA
	WCDMA B4 HSDPA @ 21.57 dBm	618	mA
	WCDMA B5 HSDPA @ 21.87 dBm	594	mA

	WCDMA B8 HSDPA @ 21.77 dBm	620	mA
	WCDMA B1 HSUPA @ 21.72 dBm	571	mA
	WCDMA B2 HSUPA @ 21.57 dBm	641	mA
	WCDMA B4 HSUPA @ 20.82 dBm	569	mA
	WCDMA B5 HSUPA @ 21.31 dBm	581	mA
	WCDMA B8 HSUPA @ 21.36 dBm	668	mA
LTE data transmission	LTE-FDD B1 @ 22.68 dBm	713	mA
	LTE-FDD B2 @ 23.01 dBm	724	mA
	LTE-FDD B3 @ 22.54 dBm	622	mA
	LTE-FDD B4 @ 22.64 dBm	702	mA
	LTE-FDD B5 @ 22.79 dBm	686	mA
	LTE-FDD B7 @ 22.65 dBm	768	mA
	LTE-FDD B8 @ 22.48 dBm	734	mA
	LTE-FDD B28 @ 22.86 dBm	640	mA
	LTE-FDD B66 @ 22.59 dBm	715	mA
GSM voice call	GSM850 PCL = 5 @ 32.69 dBm	271	mA
	GSM850 PCL = 12 @ 19.63 dBm	124	mA
	GSM850 PCL = 19 @ 5.71 dBm	96	mA
	EGSM900 PCL = 5 @ 32.64 dBm	272	mA
	EGSM900 PCL = 12 @ 19.81 dBm	130	mA
	EGSM900 PCL = 19 @ 6.11 dBm	96	mA
	DCS1800 PCL = 0 @ 29.37 dBm	192	mA
	DCS1800 PCL = 7 @ 16.22 dBm	109	mA
	DCS1800 PCL = 15 @ 0.99 dBm	95	mA
	PCS1900 PCL = 0 @ 29.74 dBm	190	mA

	PCS1900 PCL = 7 @ 16.51 dBm	109	mA
	PCS1900 PCL = 15 @ 1.12 dBm	94	mA
WCDMA voice call	WCDMA B1 @ 22.78 dBm	669	mA
	WCDMA B2 @ 22.34 dBm	652	mA
	WCDMA B4 @ 22.46 dBm	654	mA
	WCDMA B5 @ 22.56 dBm	612	mA
	WCDMA B8 @ 22.49 dBm	648	mA

6.4. Digital I/O Characteristics

Table 39: GPIO 1.8 V Characteristics

Parameter	Description	Min.	Max.	Unit
VDD_EXT	I/O power supply	1.67	1.93	V
V_{IH}	High-level input voltage	0.7 × VDD_EXT	VDD_EXT + 0.2	V
V_{IL}	Low-level input voltage	-0.3	0.3 × VDD_EXT	V
V_{OH}	High-level output voltage	VDD_EXT - 0.2	VDD_EXT	V
V_{OL}	Low-level output voltage	0	0.2	V

Table 40: (U)SIM Interface Low-Voltage I/O Charactersitics

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.67	1.93	V
V_{IH}	High-level input voltage	0.8 × USIM_VDD	USIM_VDD	V
V_{IL}	Low-level input voltage	-0.3	0.12 × USIM_VDD	V
V_{OH}	High-level output voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{OL}	Low-level output voltage	0	0.15 × USIM_VDD	V

Table 41: (U)SIM Interface High-Voltage I/O Characteristics

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.3	V
V_{IH}	High-level input voltage	0.8 × USIM_VDD	USIM_VDD	V
V_{IL}	Low-level input voltage	-0.3	0.12 × USIM_VDD	V
V_{OH}	High-level output voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{OL}	Low-level output voltage	0	0.15 × USIM_VDD	V

Table 42: SDIO Interface (SD Card Application) Low-Voltage I/O Characteristics

Parameter	Description	Min.	Max.	Unit
SDIO_VDD	Power supply	1.67	1.93	V
V_{IH}	High-level input voltage	0.7 × SDIO_VDD	SDIO_VDD + 0.2	V
V_{IL}	Low-level input voltage	-0.3	0.3 × SDIO_VDD	V
V_{OH}	High-level output voltage	SDIO_VDD - 0.2	SDIO_VDD	V
V_{OL}	Low-level output voltage	0	0.2	V

Table 43: SDIO Interface (SD Card Application) High-Voltage I/O Characteristics

Parameter	Description	Min.	Max.	Unit
SDIO_VDD	Power supply	2.7	3.05	V
V_{IH}	High-level input voltage	2.0	SDIO_VDD + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.8	V
V_{OH}	High-level output voltage	2.4	SDIO_VDD	V
V_{OL}	Low-level output voltage	0	0.3	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 44: ESD Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Test Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±8	±10	kV
Antenna Interfaces	±8	±10	kV
Other Interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 45: Operating and Storage Temperatures (Unit: °C)

Parameter	Min.	Typ.	Max.	Unit
Normal Operating Temperature [3]	-35	+25	+75	°C
Extended Operating Temperature [4]	-40	-	+85	°C
Storage Temperature	-40	-	+90	°C

[3] Within this range, the module's indicators comply with 3GPP specification requirements.
[4] Within this range, the module retains the ability to establish and maintain functions such as voice, SMS, data transmission and emergency call without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as Pout, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

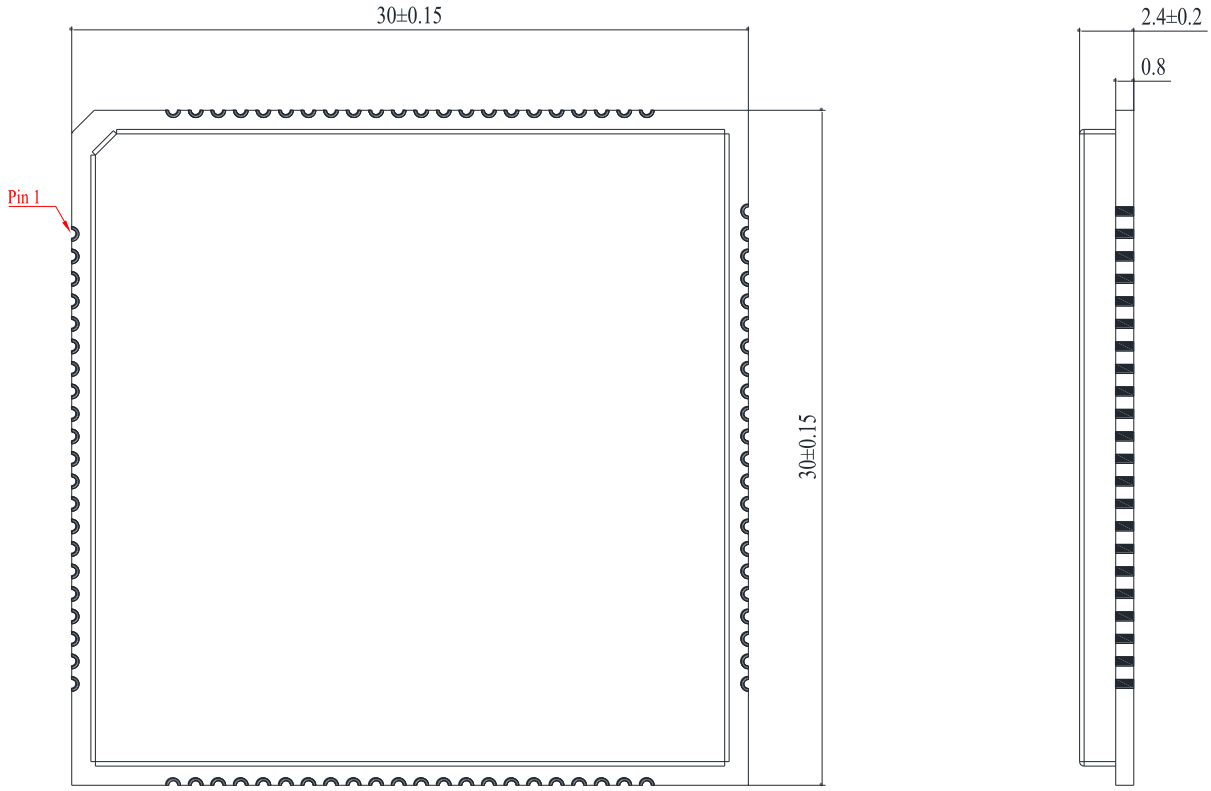


Figure 43: Top and Side Dimensions

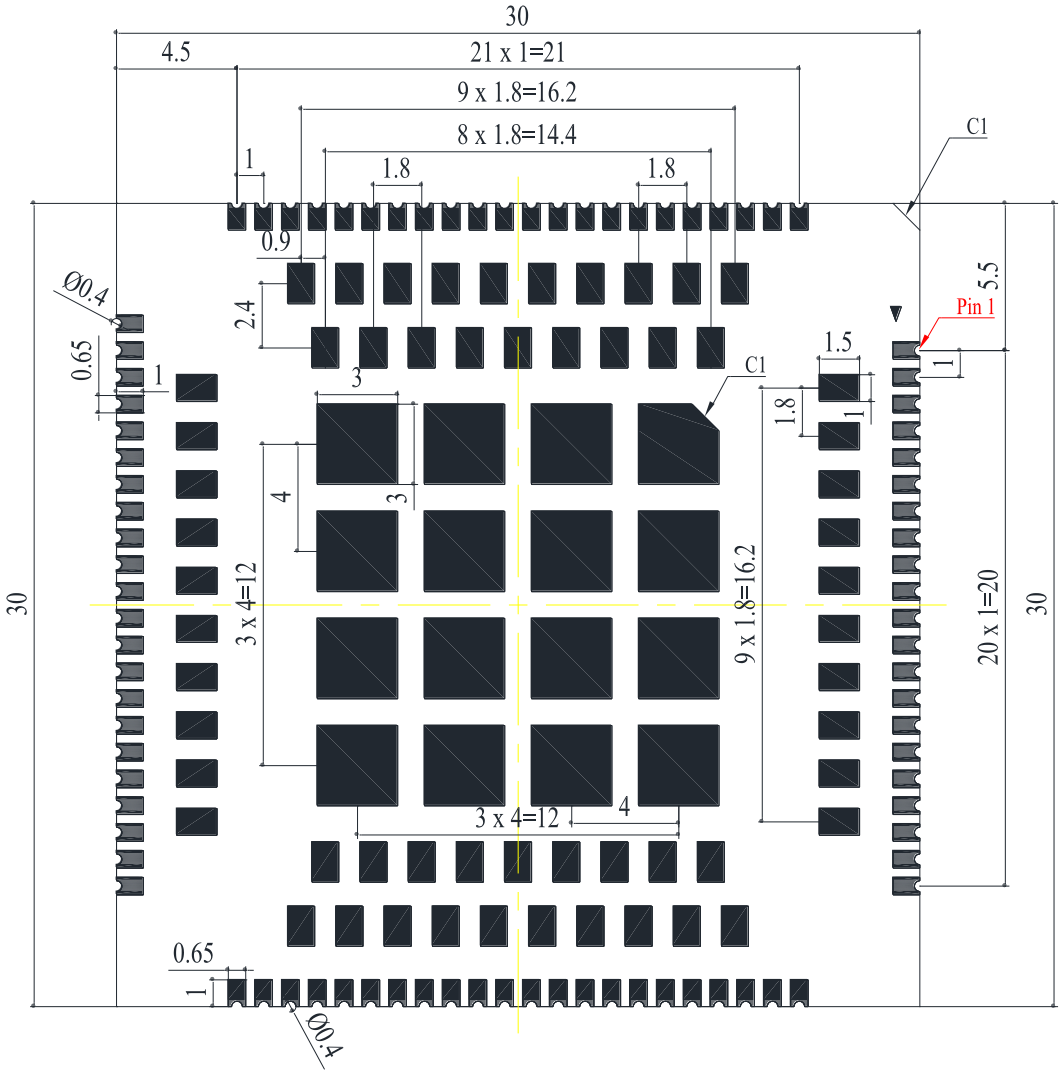


Figure 44: Bottom Dimension

NOTE

The package warpage level of the module refers to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

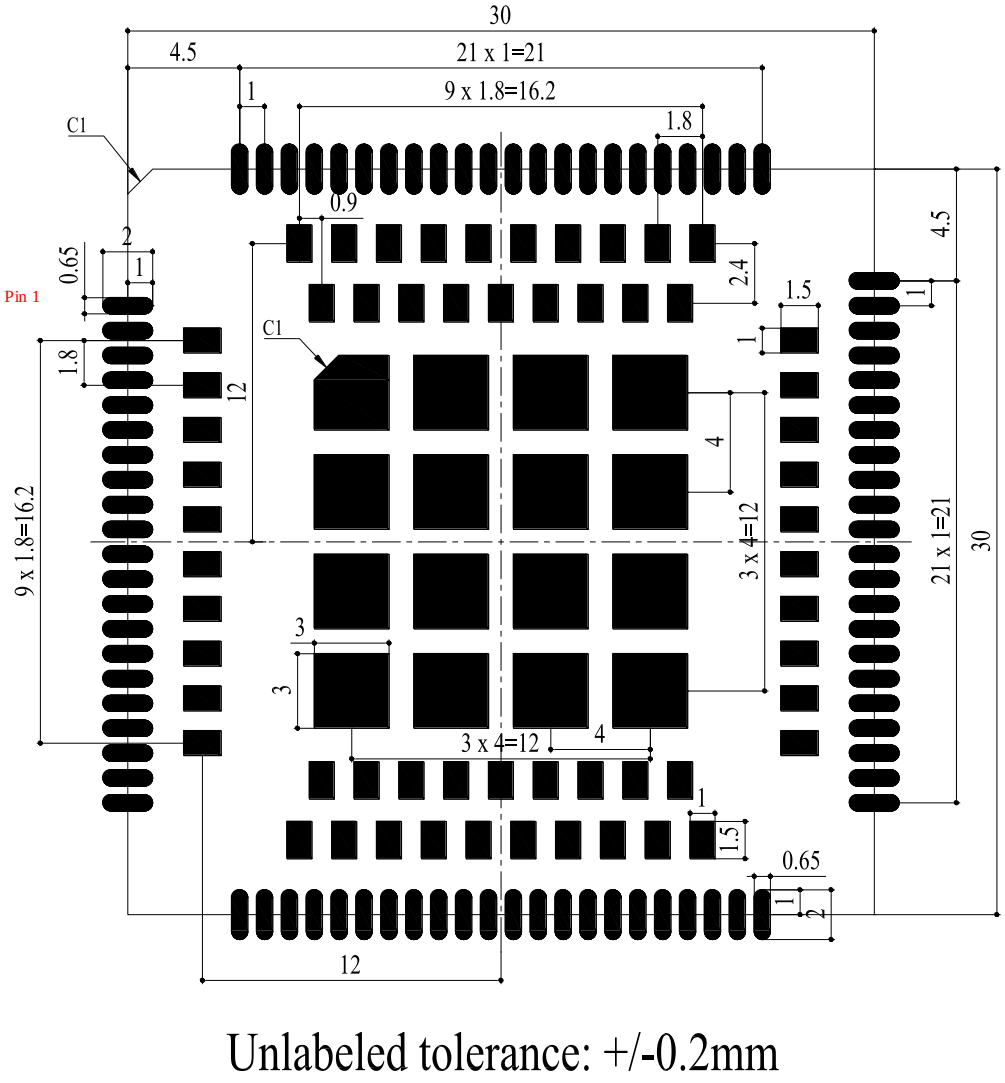


Figure 45: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

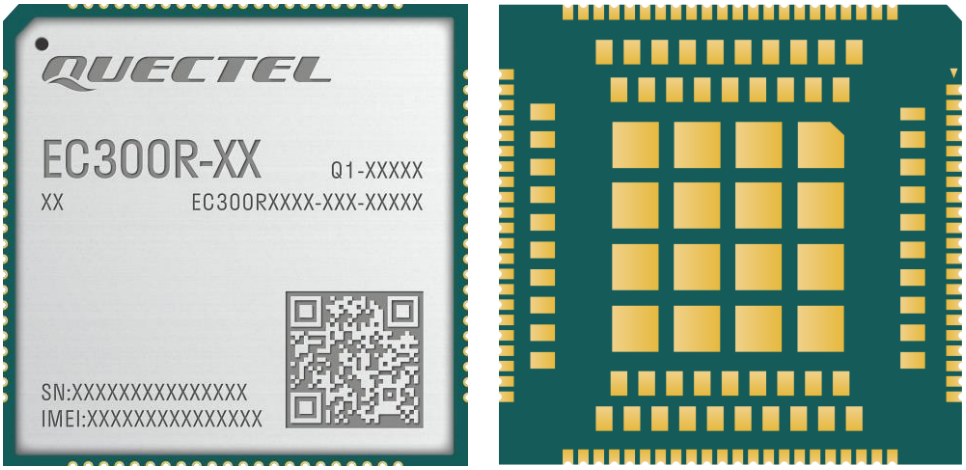


Figure 46: Top & Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 % [5]. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[5] It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to IPC/JEDEC J-STD-033. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.18–0.20 mm.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below:

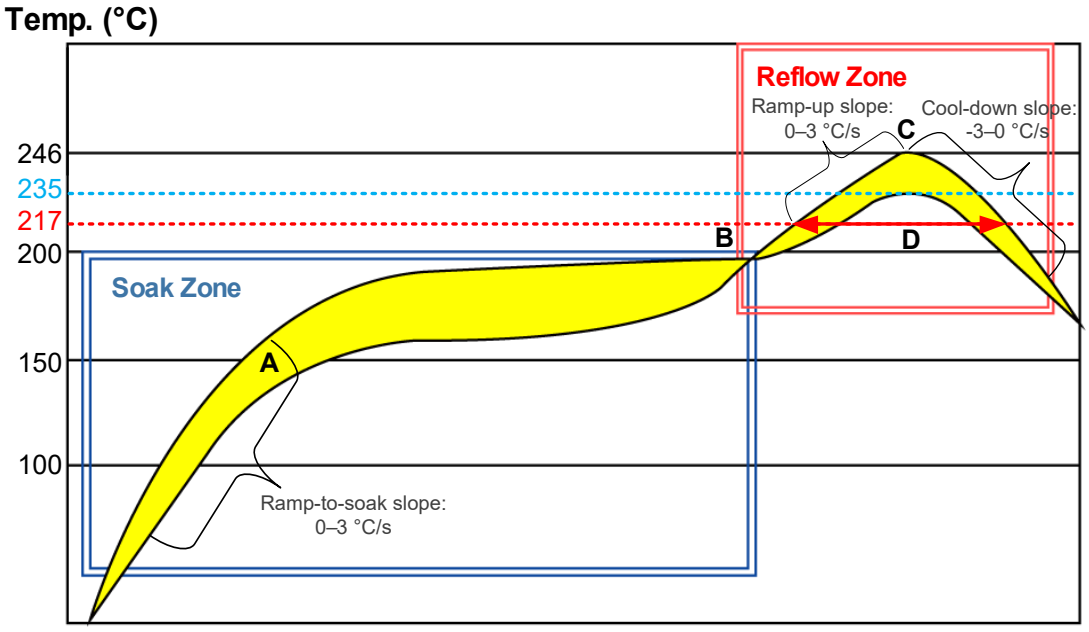


Figure 47: Recommended Reflow Soldering Thermal Profile

Table 46: Recommended Thermal Profile Parameters

Factor	Requirement Value
Soak Zone	
Ramp-up slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic soldering) that is not mentioned in ***document [7]***.

8.3. Packaging Specifications

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

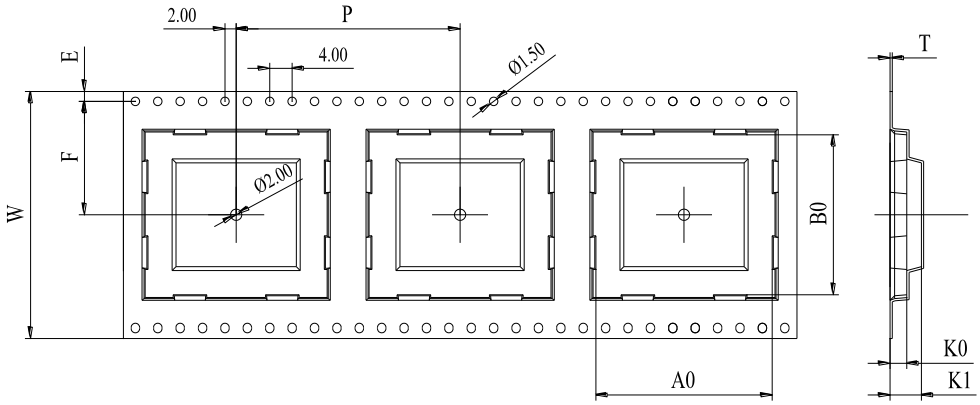


Figure 48: Carrier Tape Dimension Drawing (Unit: mm)

Table 47: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	40	0.35	30.5	30.5	3.0	5.6	20.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

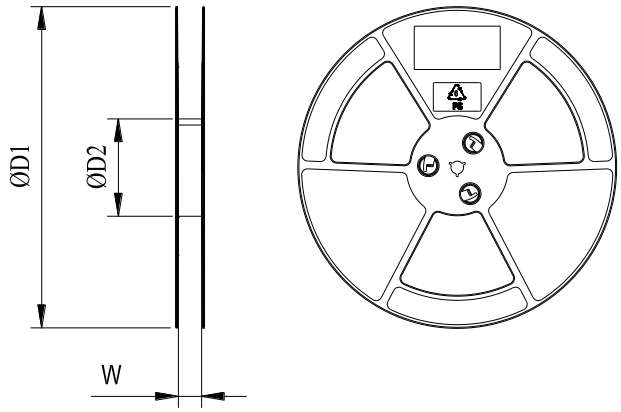


Figure 49: Plastic Reel Dimension Drawing

Table 48: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

8.3.3. Mounting Direction

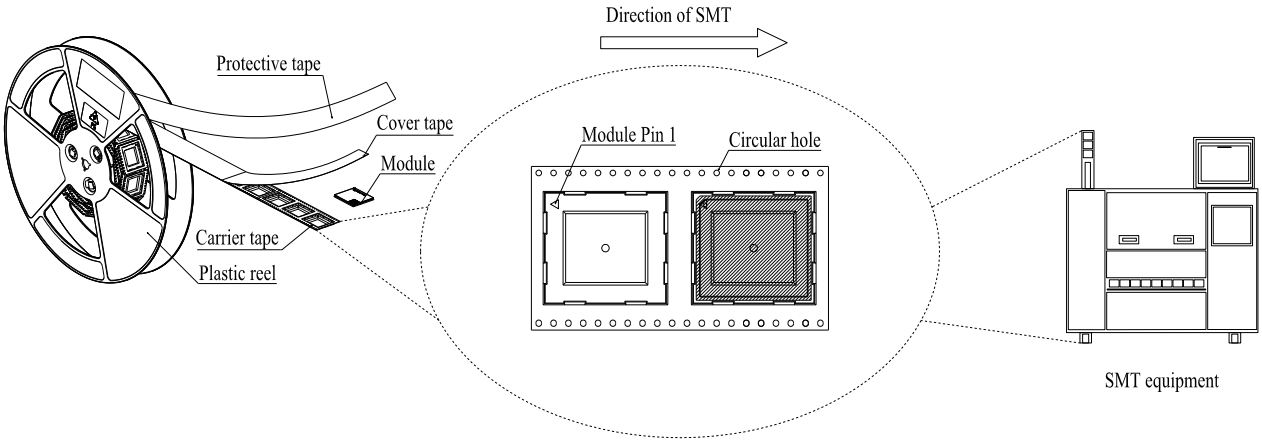
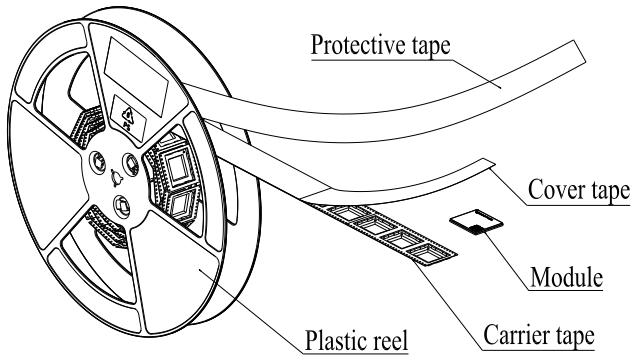


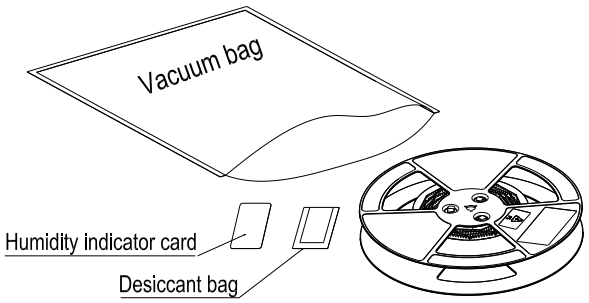
Figure 50: Mounting Direction

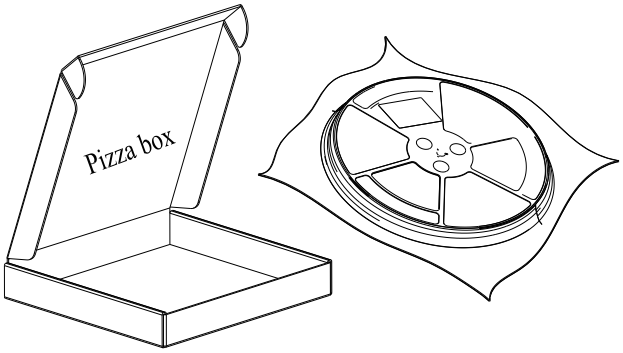
8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 1000 modules.

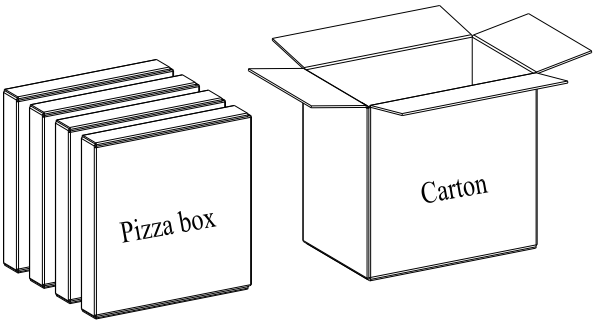


Figure 51: Packaging Process

9 Appendix References

Table 49: Related Documents

Document Name
[1] Quectel_EC300R-LA_QuecOpen_GPIO_Configuration
[2] Quectel_LTE_OPEN_EVB_User_Guide
[3] Quectel_EC200A&ECx00R_Series_QuecOpen(SDK)_AT_Commands_Manual
[4] Quectel_EC200A&ECx00R_Series_QuecOpen(SDK)_Low_Power_Mode_Development_Guide
[5] Quectel_EC200A&ECx00R_Series_QuecOpen(SDK)_Peripheral_Interface_Development_Guide
[6] Quectel_RF_Layout_Application_Note
[7] Quectel_Module_SMT_Application_Note

Table 50: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-Rate
bps	Bytes per second
CDMA	Code Division Multiple Access
CHAP	Challenge Handshake Authentication Protocol
CMUX	Connection Multiplexing
CS	Coding Scheme
CTS	Clear to send
DRX	Discontinuous Reception
EFR	Enhanced Full Rate

EGSM	Enhanced GSM
ESD	Electrostatic Discharge
ETSI	European Telecommunications Standards Institute
EVB	Evaluation Board
FDD	Frequency Division Duplexing
FOTA	Firmware Over-the-Air
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP-SSL: FTP over SSL / FTP Secure
GMSK	Gaussian Filtered Minimum Shift Keying
GND	Ground
GSM	Global System for Mobile Communications
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSPA+	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
IMT-2000	International Mobile Telecommunications 2000
LGA	Land Grid Array
LTE	Long Term Evolution
MCS	Modulation and Coding Scheme
MIPI	Mobile Industry Processor Interface
MMS	Multimedia Messaging Service
MQTT	Message Queuing Telemetry Transport

NITZ	Network Identity and Time Zone
NTP	Network Time Protocol
OTG	On-The-Go
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PING	Packet Internet Groper
PPP	Point-to-Point Protocol
P_{PP}	Peak Pulse Power
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RTS	Request To Send
SDIO	Secure Digital Input and Output Card
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
UDP	User Datagram Protocol
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus

(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-Level Input Voltage
V_{IH}min	Minimum High-Level Input Voltage
V_{IL}max	Maximum Low-Level Input Voltage
V_{IL}min	Minimum Low-Level Input Voltage
V_{OH}min	Minimum High-Level Output Voltage
V_{OL}max	Maximum Low-Level Output Voltage
V_{RWM}	Working Peak Reverse Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part
15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Quectel that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID XMR2024EC300RLA procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: XMR2024EC300RLA”
The FCC ID can be used only when all FCC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.
(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

Antenna Gain	GSM 850:2.13dBi GSM 1900: 1.59dBi WCDMA Band Ⅱ: 1.59dBi WCDMA Band IV: 2.00dBi WCDMA Band V: 2.13dBi	LTE Band 2: 1.59dBi LTE Band 4: 2.00dBi LTE Band 5: 2.13dBi LTE Band 7: 3.00dBi LTE Band 66: 2.00dBi

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, requirements for Modular Approval.
The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01

2.2 List of applicable FCC rules

FCC part 22, part 24, part 27.

2.3 Specific operational use conditions

The module can be used for mobile applications with a maximum 3 dBi antenna. The host manufacturer installing this module into their product must ensure that the final compos it product complies with the FCC requirements by a technical assessment or evaluation to the FCC rules, including the transmitter operation. The host manufacturer has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end

product which integrates this module The end user manual shall include all required regulatory information/warning as show in this manual.

2.4 Limited module procedures

Not applicable The module is a Single module and complies with the requirement of FCC Part 15 212.

2.5 Trace antenna designs

Not applicable The module has its own antenna, and doesn't need a hosts printed board micro strip trace antenna etc.

2.6 RF exposure considerations

The module must be installed in the host equipment such that at least 20cm is maintained between the antenna and users" body; and if RF exposure statement or module layout is changed, then the host product manufacturer required to take responsibility of the module through a change in FCC ID or new application The FCC ID of the module cannot be used on the final product In these circumstances, the host manufacturer will be responsible for reevaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

2.7 Antennas

Antenna Specification are as follows:

Type: External Antenna

Gain: 2.3 dBi Max

This device is intended only for host manufacturers under the following conditions: The transmitter module may not be co-located with any other transmitter or antenna; The module shall be only used with the internal antenna(s) that has been originally tested and certified with this module. The antenna must be either permanently attached or employ a "unique" antenna coupler.

As long as the conditions above are met, further transmitter test will not be required However, the host manufacturer is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc).

2.8 Label and compliance information

Host product manufacturers need to provide a physical or e-label stating "Contains FCC ID: XMR2024EC300RLA" with their finished product.

2.9 Information on test modes and additional testing requirements

Host manufacturer must perform test of radiated & conducted emission and spurious emission, e.t.c according to the actual test modes for a stand-alone modular transmitter in a host, as well as for multiple simultaneously transmitting modules or other transmitters in a host product. Only when all the test results of test modes comply with FCC requirements, then the end product can be sold legally.

2.10 Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only FCC authorized for FCC part 22, part 24, part 27 and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not

covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions:

(For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.