RG620T Series QuecOpen Hardware Design

5G Module Series

Version: 1.0.0

Date: 2023-01-30

Status: Preliminary

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2022-12-10	Dover CAI/ Sam DING/ Ballon SHI	Creation of the document
1.0.0	2023-01-30	Dover CAI/ Sam DING/ Ballon SHI	Preliminary

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1 Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and price-performance ratio

The document defines the RG620T series module itself, its air interfaces and hardware interfaces which are connected to customers' applications. This document can help customers quickly understand interface specifications, RF characteristics, electrical and mechanical details, as well as other information of the module.

NOTE

For conciseness purposes, RG620T-NA and RG620T-EU will hereinafter be referred to collectively as "the module/modules" in parts hereof applicable to both models, and individually as " RG620T-NA " and " RG620T-EU " in parts hereof referring to the differences between them.

1.1. Special Marks

Table 1: Special Marks

Marks	Definitions
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO_DATA pins, SDIO_DATA0, SDIO_DATA1, SDIO_DATA2 and SDIO_DATA3.

2 Product Overview

The module is an SMD module with compact packaging, which is engineered to meet most of the demands of M2M applications, for instance:

- Router
- Home gateway
- STB
- Industrial laptop
- Consumer laptop
- Industrial PDA
- Tablet PC
- Video surveillance

Table 2: Basic Information

RG620T Series	
Packaging type	LGA
Pin counts	570
Dimensions	(44.0 ±0.20) mm × (53.0 ±0.20) mm × (2.95 ±0.20) mm
Weight	TBD
Models	RG620T-NA, RG620T-EU

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

	RG620T-NA	RG620T-EU
5G NR SA	n2/n5/n7/n12/n13/n14/n25/n26/n29/n30/ n38/n41/n48/n66/n70/n71/ n77/n78	n1/n3/n5/n7/n8/n20/n28/n38/ n40/n41/n71 [1]/n75/n77/n78
5G NR NSA	n2/n5/n7/n12/n13/n14/n25/n26/n30/n38/ n41/n48/n66/n70/n71/n77/n78	n1/n3/n5/n7/n8/n20/n28/n38/ n40/n41/n71 [1]/n75/n77/n78
LTE-FDD	B2/B4/B5/B7/B12/B13/B14/B17/ B25/B26/B29/B30/B66/B71	B1/B3/B5/B7/B8/B20/B28/B32/B71 [1]
LTE-TDD	B38/B41/B42/B43/B48/B46	B38/B40/B41/B42/B43/B46
WCDMA	-	B1/B5/B8
GNSS	L1+L5	L1+L5

2.2. Key Features

Table 4: Key Features

Category	Description
Supply Voltage	● 3.3–4.4 V ● Typ.: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: (U)SIM card by default
(U)SIM Interface	1.8 V and 3.0 V
Audio Features	● Two digital audio interfaces: PCM
PCM Interface	● Two PCM interfaces ● Used for audio data transmission between the module and the external codec ● Long and short frame synchronization ● Master and slave modes (but must be in master mode for long frame

[1] This band is optional.

	synchronization)
SPI	● Three SPIs ● Master and slave modes ● 1.8 V voltage domain ● Clock rate: up to 52 MHz
I2C Interface	● Four I2C interfaces
USXGMII Interface	● 100 Mbps, 1000 Mbps, 2500 Mbps, 5000 Mbps and 10000 Mbps Ethernet connection in full duplex mode ● IEEE 802.3x compliant ● Max. data rates: - DL: 10 Gbps - UL: 10 Gbps
USB Interface	● Complies with USB 3.1 Gen 2 specification ● Data rates: – USB 3.1 Gen 2: up to 10 Gbps – USB 2.0: up to 480 Mbps ● Use: AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB ● USB serial drivers for USB drivers under Windows 7/8/8.1/10.
SDIO Interface	● Use: SD card application, Wi-Fi application and wireless connection ● Complies with SD 3.0 protocol
UART	**Main UART:** ● Use: AT command communication and data transmission ● Baud rate: 115200 bps ● RTS and CTS hardware flow control **Debug UART:** ● Use: Linux console and log output ● Baud rate: 921600 bps **Bluetooth UART*:** ● Use: Bluetooth communication ● Baud rate: 115200 bps **Coexistence UART*:** ● Use: WWAN/WLAN coexistence mechanism
PCIe Interface	● **PCIe1**: Complies with PCIe 4.0 specification, supports 2 lanes, 16 Gbps/lane ● **PCIe2/3**: Complies with PCIe 3.0 specification, supports 2 lanes, 8 Gbps/lane ● RC mode ● Use: connect to an external Wi-Fi IC and used for Wi-Fi communication by default
Network Indication	**NET_MODE:** ● Use: network registration status indication

	NET_STATUS: ● Use: network connectivity status indication
AT Commands	Compliant with 3GPP TS 27.007, 27.005 and Quectel enhanced AT commands
Rx-diversity	5G NR, LTE and WCDMA (EU only) Rx-diversity
Antenna Interfaces	● Cellular antenna interfaces (ANT0–7) ● GNSS antenna interface (ANT_GNSS) ● 50 Ω characteristic impedance
Transmitting Power	● 5G NR n41/77/78 for HPUE: Class 2 (26 dBm +2/-3dB) ● 5G NR: Class 3 (23 dBm ±2 dB) ● LTE B41 for HPUE [2]: Class 2 (26 dBm +2/-3 dB) ● LTE-TDD: Class 3 (23 dBm ±2 dB) ● LTE-FDD: Class 3 (23 dBm ±2 dB) ● WCDMA: Class 3 (23 dBm ±2 dB) (RG620T-EU only)
5G NR Features	● The module complies with 3GPP Rel-16 specification ● DL modulations: QPSK, 16QAM, 64QAM and 256QAM ● UL modulations: π/2-BPSK, QPSK, 16QAM, 64QAM and 256QAM ● DL 4 × 4 MIMO: RG620T-NA: n2/n5/n7/n12/n13/n14/n25/n26/n30/n38/n41/ n48/n66/n70/n71/n77/n78 RG620T-EU: n1/n3/n5/n7/n8/n20/n28/n38/n40/n41/n71/n77/n78 ● UL 2 × 2 MIMO: RG620T-NA: n38, n41, n48, n77, n78 RG620T-EU: n38, n40, n41, n77, n78 ● SCS: – FDD: 15 kHz – TDD: 30 kHz **NSA and SA:** ● Option 3x, Option 3a, Option 3 and Option 2 ● NSA max. data rates: – DL: 5.67 Gbps – UL: 1.46 Gbps ● SA max. data rates: – DL: 7.01 Gbps – UL: 2.5 Gbps
LTE Features	● The module complies with 3GPP Rel-16 FDD and TDD ● Max. LTE category: Cat 19 **RG620T-NA:** – DL: Cat 19 – UL: Cat 18 **RG620T-EU:** – DL: Cat 19

[2] HPUE is only for single carrier.

	– UL: Cat 18 ● 1.4 MHz, 3 MHz, 5 MHz, 10 MHz, 15 MHz and 20 MHz RF bandwidths ● DL modulations: QPSK, 16QAM, 64QAM and 256QAM ● UL modulations: QPSK, 16QAM, 64QAM and 256QAM ● DL 4 × 4 MIMO: **RG620T-NA**: B2/B4/B5/B7/B12/B13/B14/B17/B25/B26/B30/B38/B41/B42/B43/B48/B66/B71 **RG620T-EU**: B1/B3/B5/B7/B8/B20/B28/B38/B40/B41/B42/B43/B71 ● LTE max. data rates: – DL: 1.6 Gbps – UL: 211 Mbps
UMTS Features	● The module complies with 3GPP Rel-8 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA ● Modulations: QPSK, 16QAM and 64QAM ● DC-HSDPA max. data rate: 42.2 Mbps (DL) ● HSUPA max. data rate: 11.5 Mbps (UL) ● WCDMA max. data rates: – DL: 384 kbps – UL: 384 kbps
GNSS Features	● Supports GPS/BDS/GLONASS/Galileo/QZSS ● Dual-band GNSS: L1 and L5 ● The module complies with NMEA 0183 protocol ● The data update rate is 1 Hz by default and can support a max. value of 5 Hz
Internet Protocol Features	● The module complies with TCP, UDP, PPP, NTP, NITZ, FTP, HTTP, PING, HTTPS, FTPS, SSL, SMTP, SMTPS protocols ● The module complies with PPP protocol's PAP and CHAP authentication
Temperature Ranges	● Normal operating temperature [3]: -30 °C to +70 °C ● Extended operating temperature [4]: -40 °C to +85 °C ● Storage temperature: -40 °C to +90 °C
Firmware Upgrade	● USB 2.0 interface ● DFOTA
RoHS	All hardware components are fully complying with EU RoHS directive

[3] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module's indicators comply with 3GPP specification requirements.

[4] To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module retains the ability to establish and maintain functions such as voice, SMS, emergency call, etc., without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

2.3. Functional Diagram

The functional diagram illustrates the following major functional parts:

- Power management
- Baseband part
- LPDDR4X+EMMC
- Radio frequency part
- Peripheral interfaces

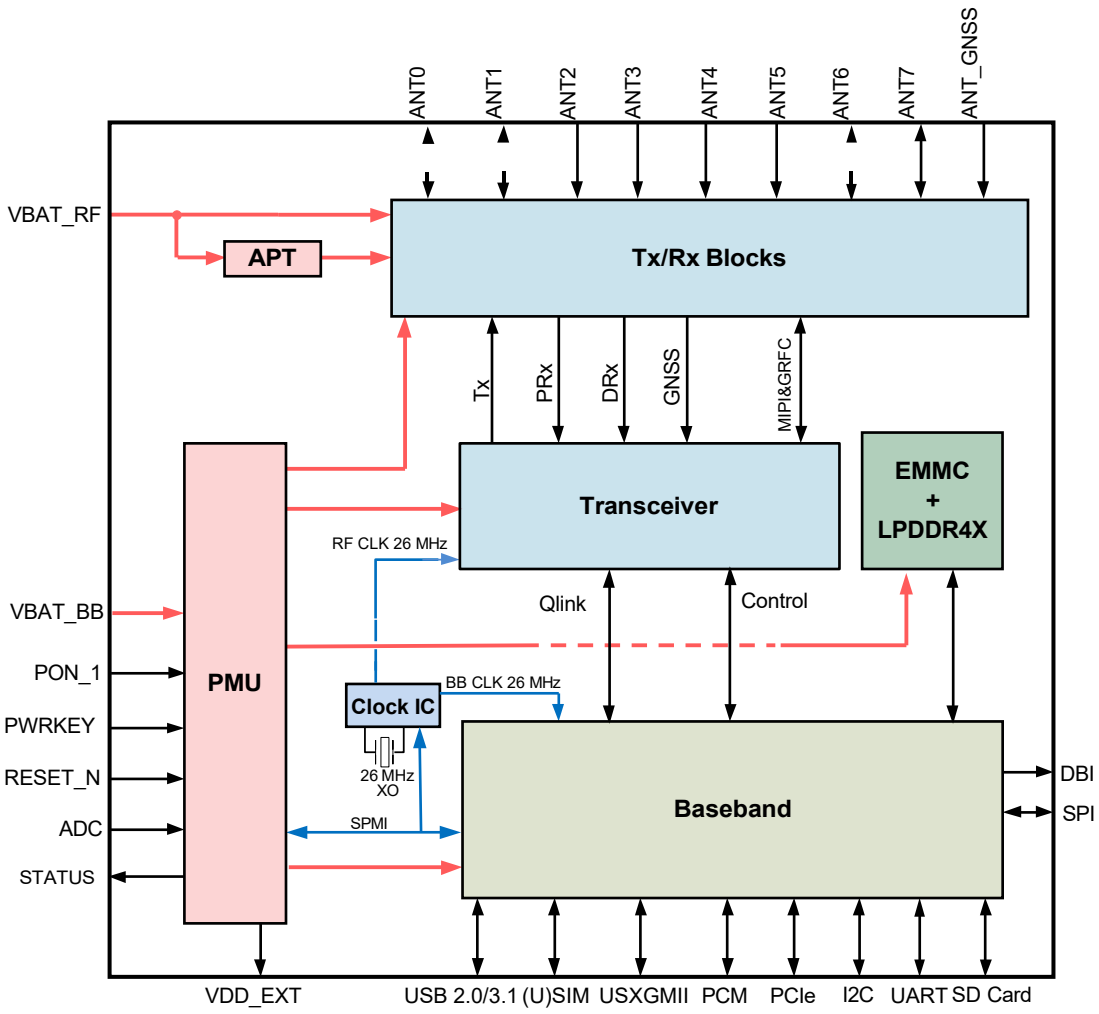


Figure 1: Functional Diagram

2.4. Pin Assignment

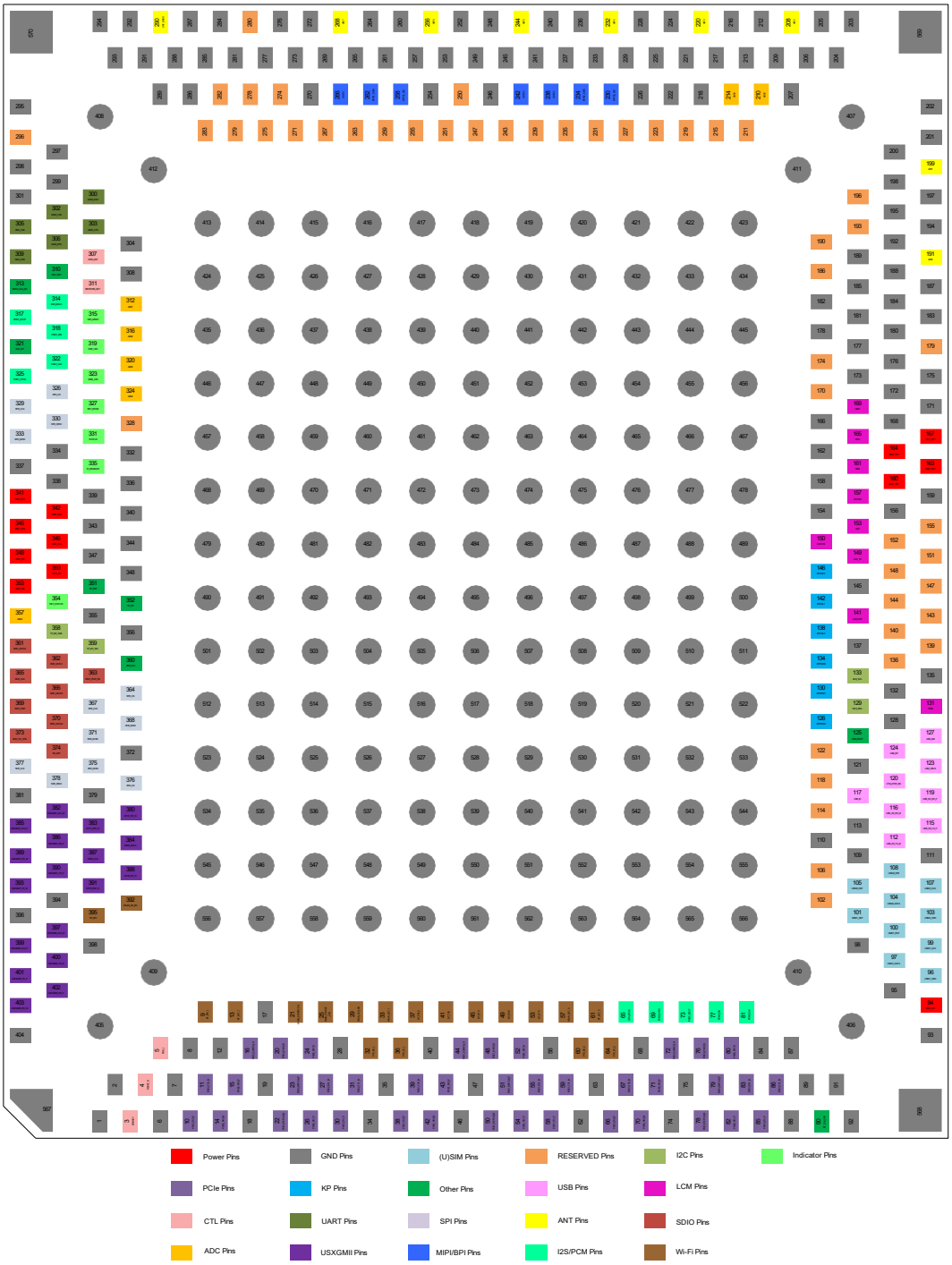


Figure 2: Pin Assignment (Top View)

NOTE

Keep all RESERVED pins unconnected.

2.5. Pin Description

Table 5: Parameter Definition

Parameter	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rate current etc.

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	349,350, 353	PI	Power supply for the module's baseband part	Vmax = 4.4 V Vmin = 3.3 V Vnom = 3.8 V	
VBAT_RF1	160,163, 164,167	PI	Power supply for the module's RF part	Vmax = 4.4 V Vmin = 3.3 V Vnom = 3.8 V	
VBAT_RF2	341,342, 345,346	PI	Power supply for the module's RF part	Vmax = 4.4 V Vmin = 3.3 V Vnom = 3.8 V	
VDD_EXT	94	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. Test point is

					recommended to be reserved.
Turn On/Off & Other Control Signals					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	3	DI	Turn on/off the module	V_{IH}min = 1.45 V V_{IL}max = 0.3 V	Internally pulled up to 1.8 V. Active low.
RESET_N	4	DI	Reset the module	V_{IH}min = 1.45 V V_{IL}max = 0.3 V	Internally pulled up to 1.8 V. Active low. Test point is recommended to be reserved.
PON_1	5	DI	Turn on/off the module	VBAT_BB	
RESTORE_KEY	311	DI	Restore the module	VDD_EXT	
WPS_KEY	307	DI	Wi-Fi protected setup	VDD_EXT	
Indication Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	331	OD	Indicate the module's operation status		PMIC_ISINK3
W_DISABLE#	335	OD	Indicate the module's airplane mode		PMIC_ISINK1
NET_STATUS	354	OD	Indicate the module's network activity status		PMIC_ISINK2
NET_MODE	327	DO	Indicate the module's network registration mode	VDD_EXT	
WIFI_MESH*	315	DO	Indicate the Wi-Fi mesh function status	VDD_EXT	
USIM_LED	323	DO	Indicate the (U)SIM card function status	VDD_EXT	
VOIP_LED*	319	DO	Indicate the VoIP function status	VDD_EXT	
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	123	AI	USB connection detect	Vmax = 15 V Vmin = 4.2 V	Used for USB connection

				Vnom = 5.0 V	detection. Cannot be used for power supply. Test point must be reserved.
USB_DP	124	AIO	USB differential data (+)		Require differential impedance of 90 Ω. Test points must be reserved.
USB_DM	127	AIO	USB differential data (-)		
USB_SS_TX_P	115	AO	USB 3.1 super-speed transmit (+)		Require differential impedance of 90 Ω. If unused, connect RX to GND directly.
USB_SS_TX_M	112	AO	USB 3.1 super-speed transmit (-)		
USB_SS_RX_P	119	AI	USB 3.1 super-speed receive (+)		
USB_SS_RX_M	116	AI	USB 3.1 super-speed receive (-)		
USB_ID	117	DI	USB ID detect	VDD_EXT	
OTG_PWR_EN	120	DO	OTG power control	VDD_EXT	
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	96	PO	(U)SIM1 card power supply	High-voltage: Vmax = 3.1 V Vnom = 3.0 V Vmin = 2.6 V Low-voltage: Vmax = 1.9 V Vnom = 1.8 V Vmin = 1.4 V	
USIM1_DATA	97	DIO	(U)SIM1 card data	USIM1_VDD	
USIM1_CLK	99	DO	(U)SIM1 card clock	USIM1_VDD	
USIM1_RST	100	DO	(U)SIM1 card reset	USIM1_VDD	
USIM1_DET	101	DI	(U)SIM1 card hot-plug detect	VDD_EXT	
USIM2_VDD	103	PO	(U)SIM2 card power supply	High-voltage: Vmax = 3.1 V	

				Vnom = 3.0 V Vmin = 2.6 V Low-voltage: Vmax = 1.9 V Vnom = 1.8 V Vmin = 1.4 V	
USIM2_DATA	104	DIO	(U)SIM2 card data	USIM1_VDD	
USIM2_CLK	107	DO	(U)SIM2 card clock	USIM1_VDD	
USIM2_RST	108	DO	(U)SIM2 card reset	USIM1_VDD	
USIM2_DET	105	DI	(U)SIM2 card hot-plug detect	VDD_EXT	
SDIO Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDIO_CLK	365	DO	SDIO clock	VDD_EXT	Only used for SD card.
SDIO_CMD	369	DIO	SDIO command	VDD_EXT	
SDIO_DATA0	370	DIO	SDIO data bit 0	VDD_EXT	
SDIO_DATA1	362	DIO	SDIO data bit 1	VDD_EXT	
SDIO_DATA2	361	DIO	SDIO data bit 2	VDD_EXT	
SDIO_DATA3	366	DIO	SDIO data bit 3	VDD_EXT	
SD_DET	374	DI	SD card hot-plug detect	VDD_EXT	
SDIO_PWR_EN	363	DO	SDIO power supply enable	VDD_EXT	
SDIO_PU_VDD	373	PO	SD card IO pull-up power supply	High-voltage: Vnom = 3.0 V $I_O$max = 200 mA Low-voltage: Vnom = 1.8 V $I_O$max = 200 mA	
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_CTS	303	DO	DTE clear to send signal from DCE	VDD_EXT	Connect to DTE's CTS.

MAIN_RTS	306	DI	DTE request to send signal to DCE	VDD_EXT	Connect to DTE's RTS.
MAIN_RXD	300	DI	Main UART receive	VDD_EXT	
MAIN_TXD	302	DO	Main UART transmit	VDD_EXT	
Bluetooth UART Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BT_TXD	41	DO	Bluetooth UART transmit	VDD_EXT	
BT_RXD	49	DI	Bluetooth UART receive	VDD_EXT	
BT_RTS	45	DI	DTE request to send signal to DCE	VDD_EXT	Connect to DTE's RTS.
BT_CTS	53	DO	DTE clear to send signal from DCE	VDD_EXT	Connect to DTE's CTS.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	309	DI	Debug UART receive	VDD_EXT	Test points must be reserved.
DBG_TXD	305	DO	Debug UART transmit	VDD_EXT	
I2C Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TP_I2C_SCL	359	OD	TP I2C clock	VDD_EXT	External pull-up resistor is required. 1.8 V only. If unused, keep it open.
TP_I2C_SDA	358	OD	TP I2C data	VDD_EXT	
I2C4_SCL	133	OD	I2C serial clock	VDD_EXT	
I2C4_SDA	129	OD	I2C serial data	VDD_EXT	
PCM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM0_SYNC*	69	DIO	PCM data frame sync	VDD_EXT	In master mode, they are output signals. In slave mode, they are input signals.
PCM0_CLK*	81	DIO	PCM clock	VDD_EXT	
PCM0_DIN*	77	DI	PCM data input	VDD_EXT	If unused, keep

PCM0_DOUT*	73	DO	PCM data output	VDD_EXT	them open.
PCM1_SYNC	325	DIO	PCM data frame sync	VDD_EXT	In master mode, they are output signals. In slave mode, they are input signals.
PCM1_CLK	322	DIO	PCM clock	VDD_EXT	
PCM1_DIN	318	DI	PCM data input	VDD_EXT	If unused, keep them open.
PCM1_DOUT	317	DO	PCM data output	VDD_EXT	
I2S0_MCLK*	314	DO	I2S0 master clock	VDD_EXT	
I2S4_MCLK*	65	DO	I2S4 master clock	VDD_EXT	
PCIe Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE1_REFCLK_M	50	AO	PCIe1 reference clock (-)		The REFCLK requires differential impedance of 100 Ω. The TX/RX requires differential impedance of 85 Ω. PCIe Gen 4 compliant. If unused, connect RX to GND directly.
PCIE1_REFCLK_P	51	AO	PCIe1 reference clock (+)		
PCIE1_RX0_M	42	AI	PCIe1 receive 0 (-)		
PCIE1_RX0_P	43	AI	PCIe1 receive 0 (+)		
PCIE1_TX0_M	39	AO	PCIe1 transmit 0 (-)		
PCIE1_TX0_P	38	AO	PCIe1 transmit 0 (+)		
PCIE1_RX1_M	55	AI	PCIe1 receive 1 (-)		
PCIE1_RX1_P	54	AI	PCIe1 receive 1 (+)		
PCIE1_TX1_M	59	AO	PCIe1 transmit 1 (-)		
PCIE1_TX1_P	58	AO	PCIe1 transmit 1 (+)		
PCIE1_RST_N	52	DO	PCIe1 reset	VDD_EXT	
PCIE1_WAKE_N	48	DI	PCIe1 wake up	VDD_EXT	
PCIE1_CLKREQ_N	44	DI	PCIe1 clock request	VDD_EXT	
PCIE2_REFCLK_M	22	AO	PCIe2 reference clock (-)		The REFCLK requires differential impedance of
PCIE2_REFCLK_P	23	AO	PCIe2 reference clock (+)		

PCIE2_RX0_M	14	AI	PCIe2 receive 0 (-)		100 Ω. The TX/RX requires differential impedance of 85 Ω. PCIe Gen 3 compliant. If unused, connect RX to GND directly.
PCIE2_RX0_P	15	AI	PCIe2 receive 0 (+)		
PCIE2_TX0_M	11	AO	PCIe2 transmit 0 (-)		
PCIE2_TX0_P	10	AO	PCIe2 transmit 0 (+)		
PCIE2_RX1_M	27	AI	PCIe2 receive 1 (-)		
PCIE2_RX1_P	26	AI	PCIe2 receive 1 (+)		
PCIE2_TX1_M	31	AO	PCIe2 transmit 1 (-)		
PCIE2_TX1_P	30	AO	PCIe2 transmit 1 (+)		
PCIE2_RST_N	24	DO	PCIe2 reset	VDD_EXT	
PCIE2_WAKE_N	20	DI	PCIe2 wake up	VDD_EXT	
PCIE2_CLKREQ_N	16	DI	PCIe2 clock request	VDD_EXT	
PCIE3_REFCLK_M*	78	AO	PCIe3 reference clock (-)		The REFCLK requires differential impedance of 100 Ω. The TX/RX requires differential impedance of 85 Ω. PCIe Gen 3 compliant. If unused, connect RX to GND directly.
PCIE3_REFCLK_P*	79	AO	PCIe3 reference clock (+)		
PCIE3_RX0_M*	70	AI	PCIe3 receive 0 (-)		
PCIE3_RX0_P*	71	AI	PCIe3 receive 0 (+)		
PCIE3_TX0_M*	67	AO	PCIe3 transmit 0 (-)		
PCIE3_TX0_P*	66	AO	PCIe3 transmit 0 (+)		
PCIE3_RX1_M*	83	AI	PCIe3 receive 1 (-)		
PCIE3_RX1_P*	82	AI	PCIe3 receive 1 (+)		
PCIE3_TX1_M*	86	AO	PCIe3 transmit 1 (-)		
PCIE3_TX1_P*	85	AO	PCIe3 transmit 1 (+)		
PCIE3_RST_N*	80	DO	PCIe3 reset	VDD_EXT	
PCIE3_WAKE_N*	76	DI	PCIe3 wake up	VDD_EXT	
PCIE3_CLKREQ_N*	72	DI	PCIe3 clock request	VDD_EXT	
LCM Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

LSDI	153	DI	SPI serial input data	VDD_EXT	
LSA0	161	DO	Indicate transmission of data or command	VDD_EXT	
LSCE0B	157	DO	SPI chip select	VDD_EXT	
LSRSTB	150	DO	SPI reset	VDD_EXT	
LSCK	169	DO	SPI serial clock	VDD_EXT	
LSDA	165	DO	SPI serial output data	VDD_EXT	
PWM	131	DO	PWM output	VDD_EXT	For LCD only
LCD_TE	149	DI	LCM tearing effect	VDD_EXT	
LCD_RST	141	DO	LCM reset	VDD_EXT	
USXGMII Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MDIO_DATA	384	DIO	MDIO data	VDD_EXT	
MDIO_CLK	387	DO	MDIO clock	VDD_EXT	
ETH0_INT_N	388	DI	Ethernet PHY 0 interrupt	VDD_EXT	
ETH0_RST_N	391	DO	Ethernet PHY 0 reset	VDD_EXT	
ETH1_INT_N	380	DI	Ethernet PHY 1 interrupt	VDD_EXT	
ETH1_RST_N	383	DO	Ethernet PHY 1 reset	VDD_EXT	
USXGMII0_CLK_M*	397	AO	USXGMII0 clock (-)		
USXGMII0_CLK_P*	399	AO	USXGMII0 clock (+)		
USXGMII0_TX_M	400	AO	USXGMII0 transmit (-)		
USXGMII0_TX_P	401	AO	USXGMII0 transmit (+)		Require differential impedance of 100 Ω. If unused, connect RX to GND directly.
USXGMII0_RX_P	402	AI	USXGMII0 receive (+)		
USXGMII0_RX_M	403	AI	USXGMII0 receive (-)		
USXGMII1_CLK_M*	382	AO	USXGMII1 clock (-)		
USXGMII1_CLK_P*	385	AO	USXGMII1 clock (+)		

USXGMII1_RX_P	386	AI	USXGMII1 receive (+)		
USXGMII1_RX_M	389	AI	USXGMII1 receive (-)		
USXGMII1_TX_P	390	AO	USXGMII1 transmit (+)		
USXGMII1_TX_M	393	AO	USXGMII1 transmit (-)		
WWAN/WLAN Control Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_SYSRST_5G	21	DO	WLAN 5 GHz system reset	VDD_EXT	
WLAN_2.4G_EN*	29	DO	WLAN 2.4 GHz function enable control	VDD_EXT	
WLAN_SYSRST_2.4G	25	DO	WLAN 2.4 GHz system reset	VDD_EXT	
WLAN_5G_EN*	392	DO	WLAN 5 GHz function enable control	VDD_EXT	
BT_ACT_0*	61	DO	Coexistence interface for WWAN and WLAN	VDD_EXT	Used for WWAN/WLAN coexistence by default.
BT_PRI_0*	37	DO	Coexistence interface for WWAN and WLAN	VDD_EXT	
WLAN_ACT_0*	57	DI	Coexistence interface for WWAN and WLAN	VDD_EXT	
PTA_TX_0*	64	DO	Coexistence interface for WWAN and WLAN	VDD_EXT	
PTA_RX_0*	60	DO	Coexistence interface for WWAN and WLAN	VDD_EXT	
BT_ACT_1*	13	DO	Coexistence interface for WWAN and WLAN	VDD_EXT	
BT_PRI_1*	9	DO	Coexistence interface for WWAN and WLAN	VDD_EXT	
WLAN_ACT_1*	33	DI	Coexistence interface for WWAN and WLAN	VDD_EXT	

PTA_TX_1*	36	DO	Coexistence interface for WWAN and WLAN	VDD_EXT	
PTA_RX_1*	32	DO	Coexistence interface for WWAN and WLAN	VDD_EXT	
RF Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT0	191	AIO	Antenna0 interface		50 Ω impedance.
ANT1	199	AIO	Antenna1 interface		
ANT2	208	AI	Antenna2 interface		
ANT3	220	AI	Antenna3 interface		
ANT4	232	AI	Antenna4 interface		
ANT5	244	AI	Antenna5 interface		
ANT6	256	AIO	Antenna6 interface		
ANT7	268	AIO	Antenna7 interface		
ANT_GNSS	290	AI	GNSS antenna interface		
Antenna Tuner Control Interfaces*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC1	266	DO	Generic RF Controller	VDD_EXT	
GRFC2	238	DO	Generic RF Controller	VDD_EXT	
GRFC3	242	DO	Generic RF Controller	VDD_EXT	
RFFE1_DATA	262	DIO	Used for external MIPI IC control	VDD_EXT	
RFFE1_CLK	258	DO	Used for external MIPI IC control	VDD_EXT	
RFFE2_DATA	234	DIO	Used for external MIPI IC control	VDD_EXT	
RFFE2_CLK	230	DO	Used for external MIPI IC control	VDD_EXT	
SPI Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

SPI0_CS*	364	DO	SPI0 chip select	VDD_EXT	
SPI0_CLK*	367	DO	SPI0 clock	VDD_EXT	
SPI0_MOSI*	371	DO	SPI0 master-out slave-in	VDD_EXT	
SPI0_MISO*	368	DI	SPI0 master-in salve-out	VDD_EXT	
SPI2_CS*	376	DO	SPI2 chip select	VDD_EXT	
SPI2_CLK*	377	DO	SPI2 clock	VDD_EXT	
SPI2_MOSI*	375	DO	SPI2 master-out slave-in	VDD_EXT	
SPI2_MISO*	378	DI	SPI2 master-in salve-out	VDD_EXT	
SPI3_CS	326	DO	SPI3 chip select	VDD_EXT	Recommended for SLIC IC communication.
SPI3_CLK	329	DO	SPI3 clock	VDD_EXT	
SPI3_MOSI	333	DO	SPI3 master-out slave-in	VDD_EXT	
SPI3_MISO	330	DI	SPI3 master-in salve-out	VDD_EXT	
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	357	AI	General-purpose ADC interface	0.04–1.78 V	If unused, connect it to GND directly.
ADC1	312	AI	General-purpose ADC interface	0.04–1.78 V	
ADC2	316	AI	General-purpose ADC interface	0.04–1.78 V	
ADC3	320	AI	General-purpose ADC interface	0.04–1.78 V	
ADC4	324	AI	General-purpose ADC interface	0.04–1.78 V	
ADC5	210	AI	General-purpose ADC interface	0.04–1.78 V	
ADC6	214	AI	General-purpose ADC interface	0.04–1.78 V	
Matrix Keypad Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

KPCOL0	146	DIO	Matrix keypad column0	VDD_EXT	Do not pull it low before startup, otherwise it will force the module into emergency download mode.
KPCOL1	142	DIO	Matrix keypad column1	VDD_EXT	
KPCOL2	138	DIO	Matrix keypad column2	VDD_EXT	
KPROW0	134	DIO	Matrix keypad row0	VDD_EXT	
KPROW1	130	DIO	Matrix keypad row1	VDD_EXT	
KPROW2	126	DIO	Matrix keypad row2	VDD_EXT	
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	125	DI	Force the module into emergency download mode	VDD_EXT	Test point is recommended to be reserved.
SLIC_RST	310	DO	SLIC reset	VDD_EXT	
SLIC_INT	321	DI	SLIC interrupt	VDD_EXT	
TP_RST*	351	DO	TP reset	VDD_EXT	
TP_INT*	352	DI	TP interrupt	VDD_EXT	
BT_EN*	395	DO	Bluetooth enable control	VDD_EXT	
GNSS_LNA_EN*	313	DO	GNSS LNA enable control; 1PPS pulse output and frame synchronization	VDD_EXT	
BT_CLK_32K*	90	DO	32 kHz clock for WLAN/Bluetooth	VDD_EXT	
26M_CLK*	360	DO	26 MHz clock for others		
Reserved Pins					
Pin Name	**Pin No.**				
RESERVED	102, 106, 114, 118, 122, 136, 139, 140, 143, 144, 147, 148, 151, 152, 155, 170, 174, 179, 186, 190, 193, 196, 211, 215, 219, 223, 227, 231, 235, 239, 243, 247 250, 251, 255, 259, 263, 267, 271, 274, 275, 278, 279, 280, 282, 283, 296, 328				

GND	
Pin Name	**Pin No.**
GND	1, 2, 6-8, 12, 17-19, 28, 34, 35, 40, 46, 47, 56, 62, 63, 68, 74, 75, 84, 87-89, 91-93, 95, 98, 109-111, 113, 121, 128, 132, 135, 137, 145, 154, 156, 158, 159, 162, 166, 168, 171, 172, 173, 175-178, 180-185, 187-189, 192, 194, 195, 197, 198, 200-207, 209, 212, 213, 216, 217, 218, 221, 222, 224-226, 228, 229, 233, 236, 237, 240, 241, 245, 246, 248, 249, 252-254, 257, 260, 261, 264, 265, 269, 270, 272, 273, 276, 277, 281, 284-289, 291-295, 297-299, 301, 304, 308, 332, 334, 336-340, 343, 344, 347, 348, 355, 356, 372, 379, 381, 394, 396, 398, 404-570

2.6. EVB Kit

Quectel supplies a RG500L-EVB with accessories to control or test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Operating Modes

Table 7: Operating Modes Overview

Mode	Description	
Full Functionality Mode	Idle	The module remains registered on the network but has no data interaction with the network. Software is active.
	Voice/Data	The module is connected to the network. Power consumption is decided by network settings and data rate.
Minimum Functionality Mode	**AT+CFUN=0** can set the module to the minimum functionality mode without removing the power supply. In this mode, both the RF function and the (U)SIM card is invalid.	
Airplane Mode	**AT+CFUN=4** command can set the module to airplane mode. In this case, RF function is invalid.	
Sleep Mode	In this mode, current consumption of the module will be reduced to the minimal level. In this mode, the module can still receive paging, SMS, voice call and TCP/UDP data from network.	
Shutdown Mode	PMU shuts down the power supply. Software is inactive and UART are inaccessible. However, the voltage supply (for VBAT_RF and VBAT_BB) remains connected.	

NOTE

For more details about **AT+CFUN**, see ***Chapter 9.1***.

3.2. Sleep Mode

DRX of the module is able to reduce the current consumption to a minimum value during sleep mode, and DRX cycle index values are broadcasted by the wireless network. The diagram below illustrates the relationship between the DRX run time and the current consumption of the module in this mode. The longer the DRX cycle is, the lower the current consumption will be.

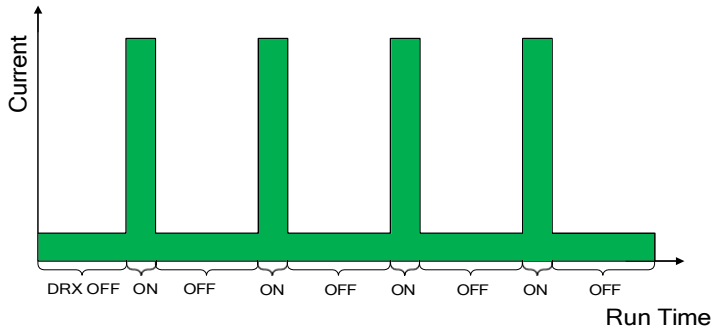


Figure 3: DRX Run Time and Current Consumption in Sleep Mode

3.2.1. UART Application Scenario

If the host communicates with the module via UART interface, the following precondition should be met to set the module into sleep mode:

- Execute **AT+QSCLK=1** command to enable sleep mode. For more details about **AT+QSCLK**, see ***Chapter 9.2***.

3.2.2. USB Application Scenario

If the host communicates with the module via USB interface, the following precondition should be met to set the module into sleep mode:

- Execute **AT+QSCLK=1** command to enable sleep mode. For more details about **AT+QSCLK**, see ***Chapter 9.2***.

3.3. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via **AT+CFUN**.

AT+CFUN=<fun> command provides choices of the functionality level by setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality (Disable RF function and (U)SIM function).
- **AT+CFUN=1:** Full functionality (Default).
- **AT+CFUN=4:** Airplane mode (Disable RF function).

NOTE

The execution of **AT+CFUN** command will not affect GNSS function. For more details about **AT+CFUN**, see ***Chapter 9.1***.

3.4. Power Supply

3.4.1. Power Supply Interface

The module provides 11 VBAT pins dedicate to connecting with the external power supply:

Table 8: VBAT and GND Pins

Pin Name	Pin No.	I/O	Description	Comment
VBAT_BB	349, 350, 353	PI	Power supply for the module's baseband part	
VBAT_RF1	160, 163, 164, 167	PI	Power supply for the module's RF part	
VBAT_RF2	341, 342, 345, 346	PI	Power supply for the module's RF part	
VDD_EXT	94	PO	Provide 1.8 V for external circuit	Power supply for external GPIO's pull-up circuits. Test point is recommended to be reserved.
GND	1, 2, 6-8, 12, 17-19, 28, 34, 35, 40, 46, 47, 56, 62, 63, 68, 74, 75, 84, 87-89, 91-93, 95, 98, 109-111, 113, 121, 128, 132, 135, 137, 145, 154, 156, 158, 159, 162, 166, 168, 171, 172, 173, 175-178, 180-185, 187-189, 192, 194, 195, 197, 198, 200-207, 209, 212, 213, 216, 217, 218, 221, 222, 224-226, 228, 229, 233, 236, 237, 240, 241, 245, 246, 248, 249, 252-254, 257, 260, 261, 264, 265, 269, 270, 272, 273, 276, 277, 281, 284-289, 291-295, 297-299, 301, 304, 308, 332, 334, 336-340, 343, 344, 347, 348, 355, 356, 372, 379, 381, 394, 396, 398, 404-570			

3.4.2. Reference Design for Power Supply

Power design for the module is essential. The power supply of the module should be able to provide sufficient current of 4.5 A at least. If the voltage difference between input voltage and the supply voltage is small, it is suggested to use an LDO; if the voltage difference is big, a buck converter is recommended.

The following figure shows a reference design for 12 V input power supply. The designed output of the power supply is about 3.8 V and the rated current is 4.5 A.

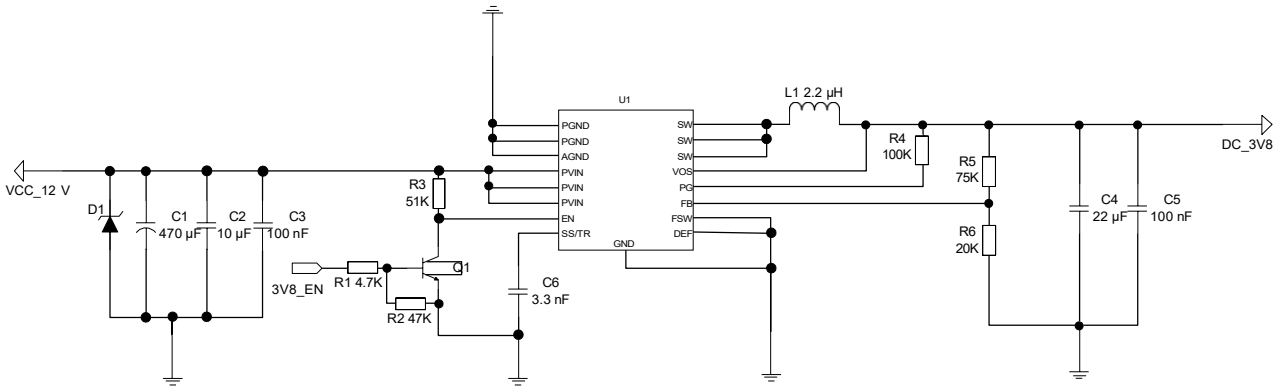


Figure 4: Reference Design of Power Input

NOTE

To avoid corrupting the data in the internal flash, do not switch off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.

3.4.3. Requirements for Voltage Stability

The power supply range of the module is from 3.3 V to 4.4 V. Ensure the input voltage never drops below 3.3 V.

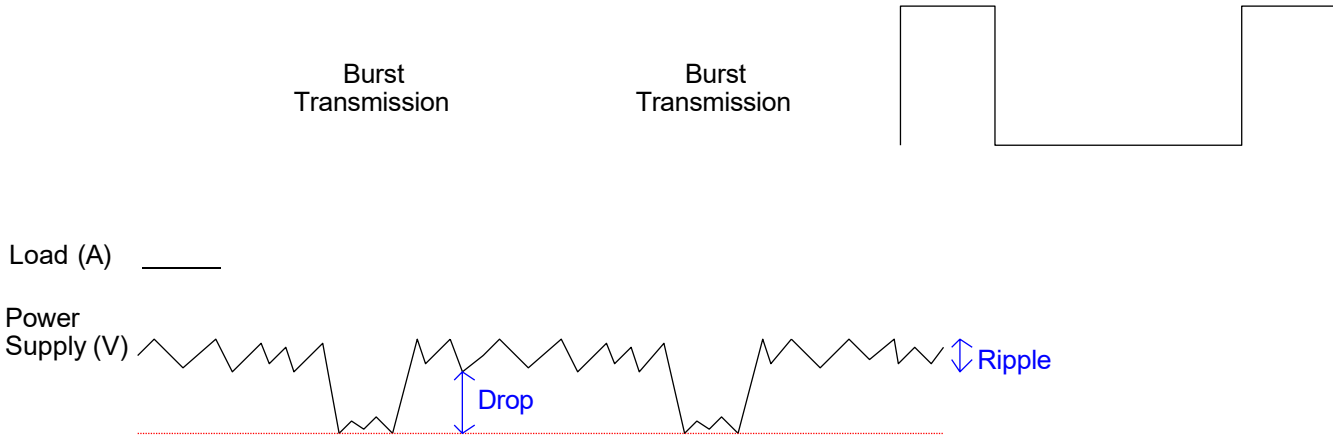


Figure 5: Power Supply Limits During Burst Transmission

To decrease the voltage drop, bypass capacitors of about 470 µF with low ESR (ESR ≤ 0.7 Ω) and a multi-layer ceramic chip (MLCC) capacitor array with ultra-low ESR should be used for VBAT_BB/RF. It is recommended to use 4 ceramic capacitors (100 nF, 6.8 nF, 220 pF, 68 pF) for composing the MLCC array for VABT_BB and 6 ceramic capacitors (100 nF, 220 pF, 68 pF, 15 pF, 9.1 pF, 4.7 pF) for composing the MLCC array for VABT_RF, and place these capacitors close to VBAT pins. The main power supply from an external application must be a single voltage source which can supply power along two sub paths with star topology. The width of VBAT_BB trace should be not less than 2 mm. The width of VBAT_RF trace should be not less than 2.5 mm. In principle, the longer the VBAT trace is, the wider it should be.

To avoid the ripple and surge and to ensure the stability of the power supply to the module, add a high-power rated TVS component at the front end of the power supply.

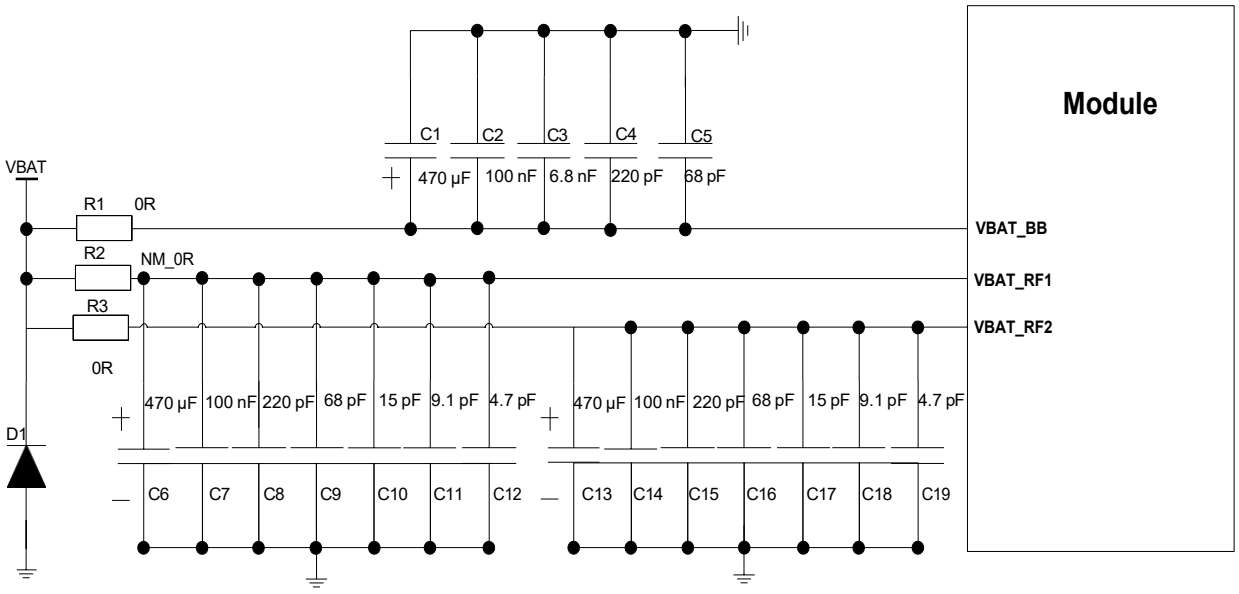


Figure 6: Reference Design of Power Supply

3.5. Turn On

3.5.1. Turn On with PWRKEY

Table 9: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	3	DI	Turn on/off the module	Internally pulled up to 1.8 V. Active low.

When the module is in turn off state, it can be turned on by driving PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY.

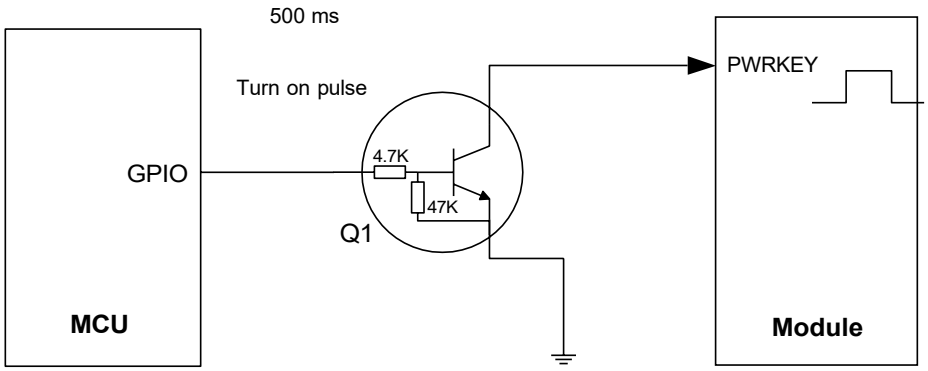


Figure 7: Reference Design of Turn On with Driving Circuit

Another way to control the PWRKEY is using a keystroke directly. When pressing the keystroke, an electrostatic strike may be generated from finger. Therefore, you should place a TVS component near the keystroke for ESD protection.

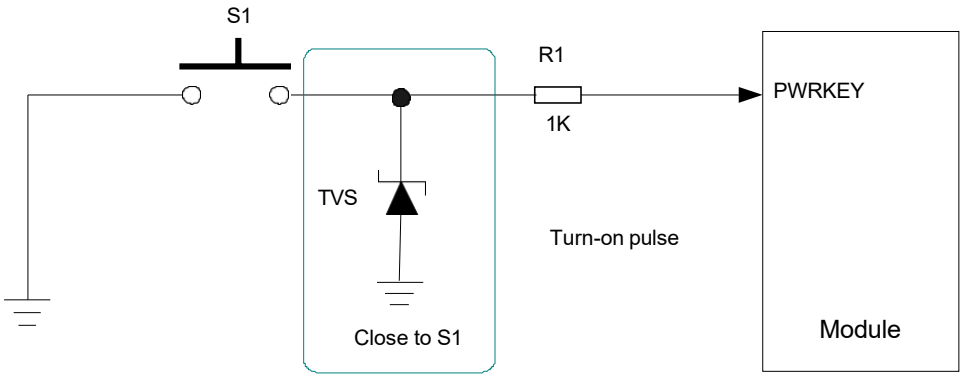


Figure 8: Reference Design of Turn On with Keystroke

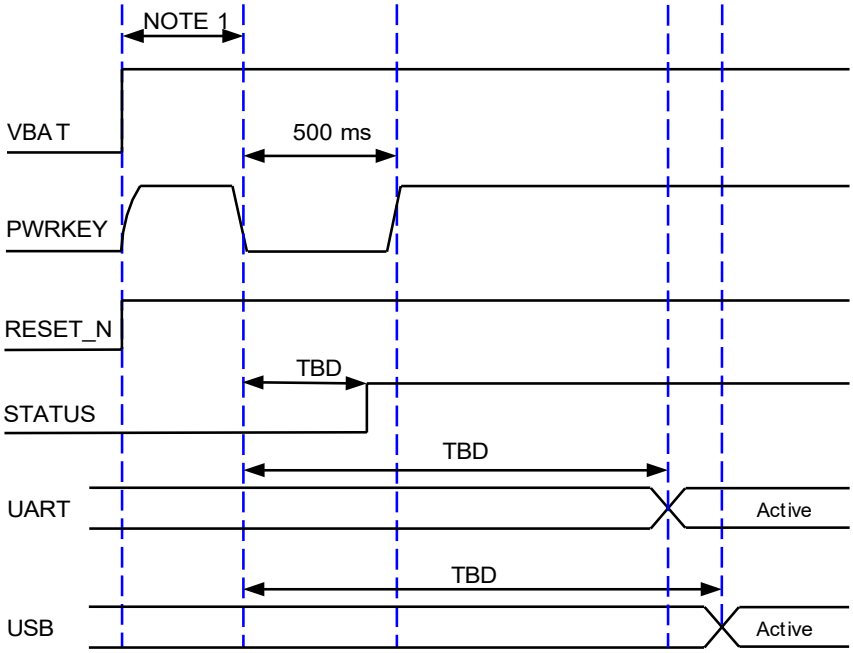


Figure 9: Timing of Turn On with PWRKEY

NOTE

1. Ensure the voltage of VBAT is stable for at least 30 ms before driving the PWRKEY low.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

3.5.2. Turn On with PON_1

Table 10: Pin Description of PON_1

Pin Name	Pin No.	I/O	Description	Comment
PON_1	5	DI	Turn on/off the module	

When the module is in turn-off state, it can be turned on by driving PON_1 high.

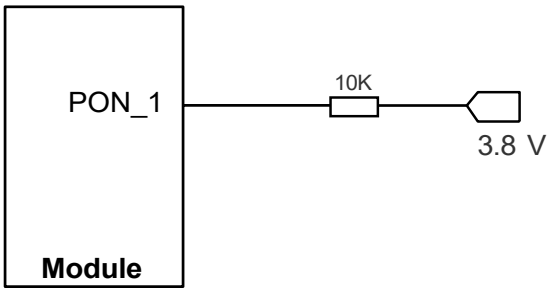


Figure 10: Reference Design of Turn On with PON_1

NOTE

If PON_1 is not used, duly connect it to ground.

3.6. Turn Off

3.6.1. Turn Off with PWRKEY

Drive PWRKEY low for at least 800 ms and then release it. Then, the module will execute turn-off procedure.

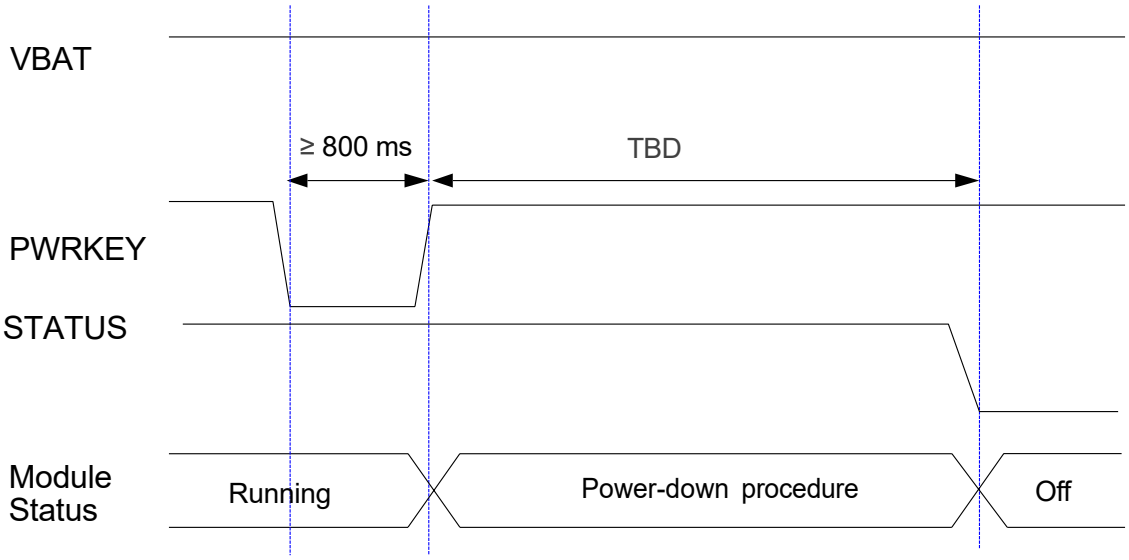


Figure 11: Timing of Turn Off with PWRKEY

3.6.2. Turn Off with PON_1

You can turn off the module by driving PON_1 low.

NOTE

1. When turning off the module with PON_1, please keep PWRKEY at a high level after the execution of power-off. Otherwise, the module will be turned on again after power-off.
2. When USB_VBUS is in place, the module always remains in the power-on state.
3. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or PON_1, can you cut off the power supply.

3.7. RESET_N

Driving RESET_N low for at least 250–550 ms and then releasing it can reset the module. RESET_N signal is sensitive to interference, consequently it is recommended to route the trace as short as possible and surround it with ground.

Table 11: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	4	DI	Reset the module	Internally pulled up to 1.8 V. Active low. Test point is recommended to be reserved.

The recommended circuit for reset function is similar to the PWRKEY control circuit. You can use an open drain/collector driver or a button to control RESET_N.

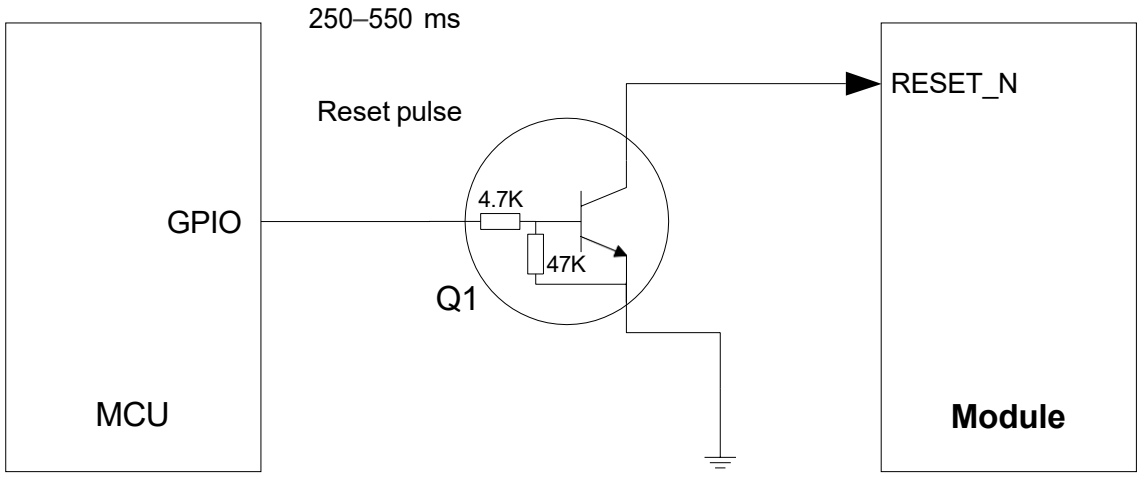


Figure 12: Reference Design of Reset with Driving Circuit

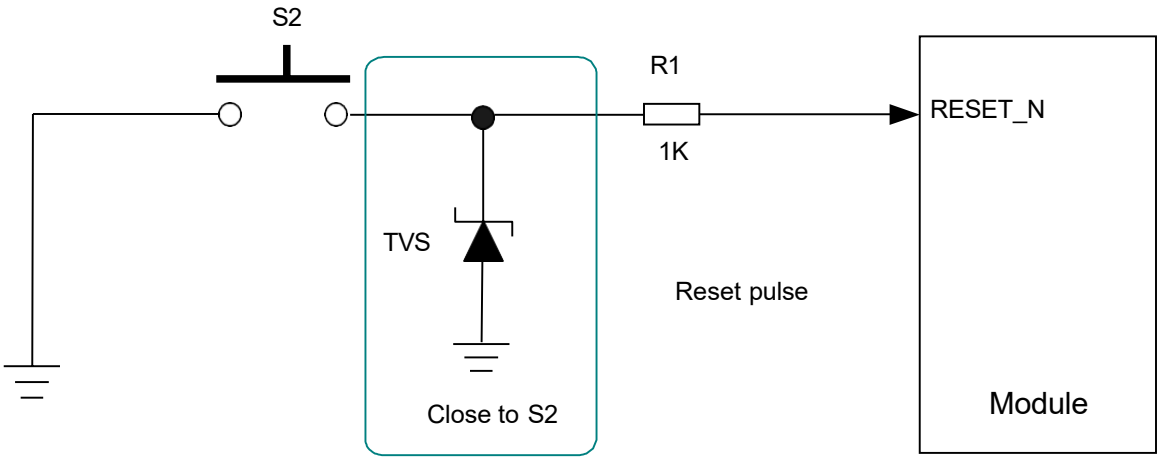


Figure 13: Reference Design of Reset with Button

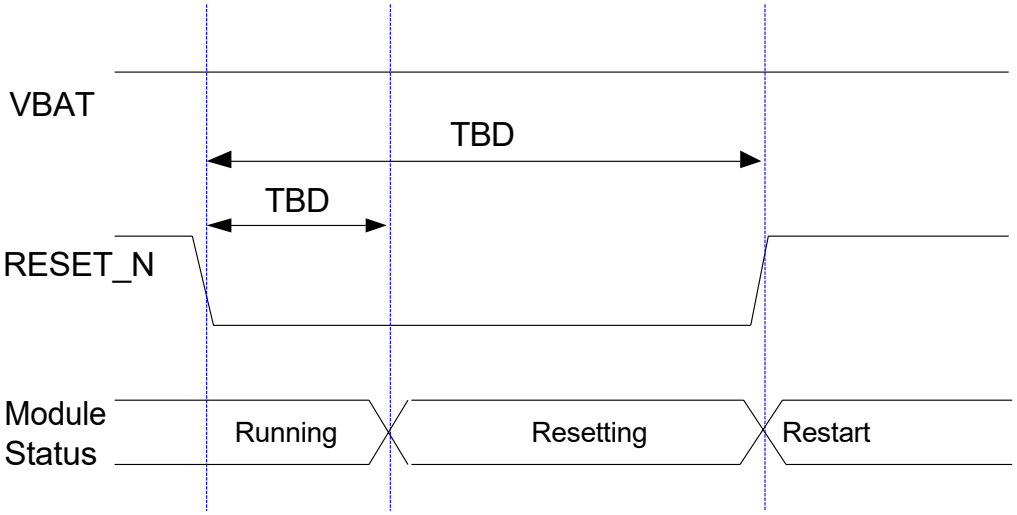


Figure 14: Timing of Reset

NOTE

Ensure there is no large capacitance on PWRKEY and RESET_N.

4 Application Interfaces

4.1. USB Interface

The module provides one USB interface which complies with the USB 3.1 Gen 2 and USB 2.0 specifications and supports SuperSpeed (10 Gbps) for USB 3.1 Gen 2, high-speed (480 Mbps) and full-speed (12 Mbps) for USB 2.0. The USB interface can be used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB.

Table 12: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	123	AI	USB connection detect	Used for USB connection detection Cannot be used for power supply. Test point must be reserved.
USB_DP	124	AIO	USB differential data (+)	Require differential impedance of 90 Ω. Test points must be reserved.
USB_DM	127	AIO	USB differential data (-)	
USB_SS_TX_P	115	AO	USB 3.1 super-speed transmit (+)	Require differential impedance of 90 Ω. If unused, connect RX to GND directly.
USB_SS_TX_M	112	AO	USB 3.1 super-speed transmit (-)	
USB_SS_RX_P	119	AI	USB 3.1 super-speed receive (+)	
USB_SS_RX_M	116	AI	USB 3.1 super-speed receive (-)	
USB_ID	117	DI	USB ID detect	
OTG_PWR_EN	120	DO	OTG power control	

It is recommended to use USB 2.0 interface for firmware upgrading and reserve test points for debugging in your designs.

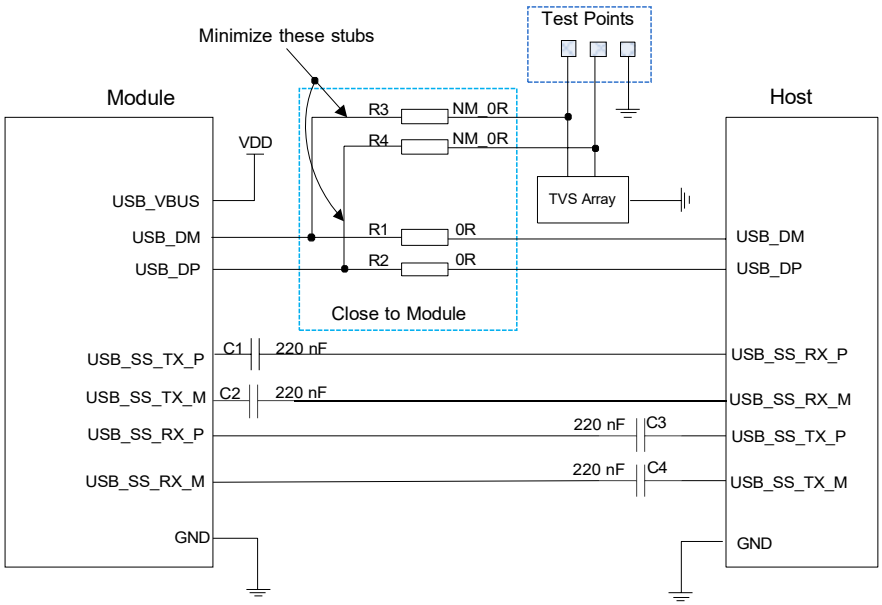


Figure 15: Reference Design of USB 2.0 Interface

To ensure the signal integrity of USB 2.0 data transmission, you should place C1 and C2 close to the module, place C3, C4 close to the host, and place resistors R1 to R4 close to each other. Moreover, keep extra stubs of trace as short as possible.

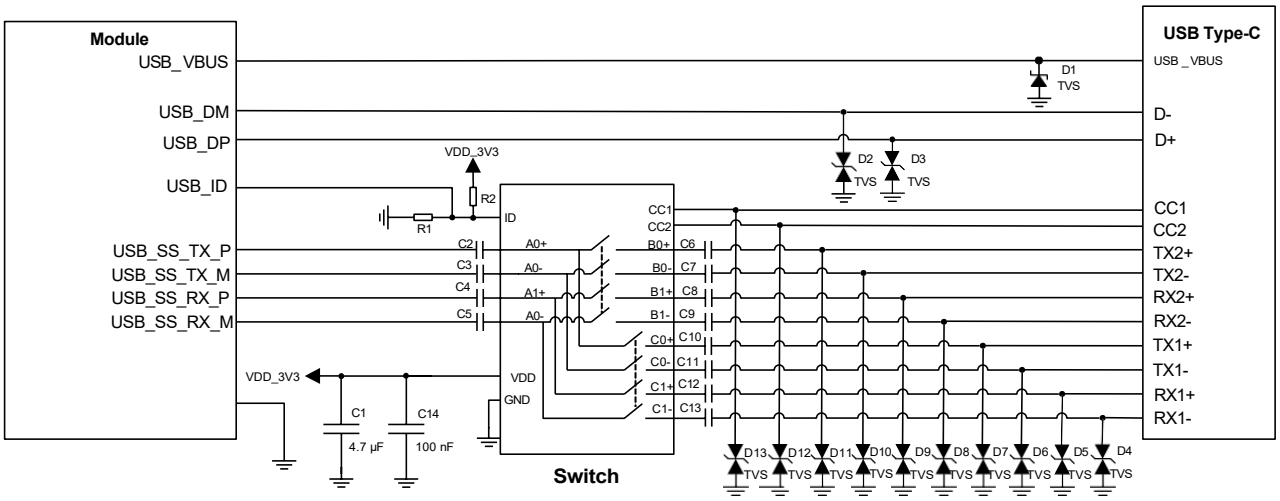


Figure 16: Reference Design of USB Type-C Interface

Type-C interface USB_VBUS can charge the battery through the external charging circuit, and can also be used for module's USB insertion detection. Input voltage of the USB_VBUS power supply ranges from 4.2 V to 15 V. The voltage should be adjusted for high-voltage charging through divider circuit and the recommended value is 5.0 V. The module supports charging management of a single Li-ion battery.

Different charging parameters need to be set for batteries with different capacities. Meanwhile, the module also supports USB OTG mode. When USB_ID is held at high level by default, the module acts as USB slave device. When USB_ID is grounded, the module acts as USB master device. USB_VBUS pin of the charging IC is the OTG power output.

To ensure performance, you should follow the following principles when designing USB interface:

- Route USB signal traces as differential pairs with surrounded ground. The impedance of USB 2.0/3.1 differential trace is 90 Ω.
- For USB 3.1 Gen 2 signal traces, the trace length should be less than 80 mm, and the length matching of each differential data pair (Tx/Rx) should be less than 0.125 mm.
- For USB 2.0 signal traces, the trace length should be less than 150 mm, and the differential data pair matching (P/M) should be less than 0.5 mm.
- Route USB differential traces at the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below. For signal traces, provide clearance from power supply traces, crystal-oscillators, magnetic devices, sensitive signals like RF signals, analog signals, and noise signals generated by clock, DC-DC, etc.
- Pay attention to the impact caused by stray capacitance of the ESD protection component on USB data lines. Typically, the stray capacitance should be less than 3.0 pF for USB 2.0, and less than 0.5 pF for USB 3.1 Gen 2.
- If possible, reserve one 0 Ω resistor on USB_DP and USB_DM traces respectively.

For more details about the USB specifications, visit http://www.usb.org/home.

Table 13: USB Interface Trace Length Inside the Module (Unit: mm)

Pin Name.	Pin No.	Length	Length Matching
USB_DM	127	27.48	-0.05
USB_DP	124	27.53	
USB_SS_RX_M	116	26.31	-0.08
USB_SS_RX_P	119	26.39	
USB_SS_TX_M	112	25.12	0.11
USB_SS_TX_P	115	25.01	

4.2. USB_BOOT

The module provides a USB_BOOT for emergency download. Pulling up USB_BOOT to VDD_EXT before turning on the module, and then the module will enter emergency download mode. In this mode, the module supports firmware upgrade over USB 2.0 interface.

Table 14: Pin Description of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	125	DI	Force the module into emergency download mode	Test point is recommended to be reserved.

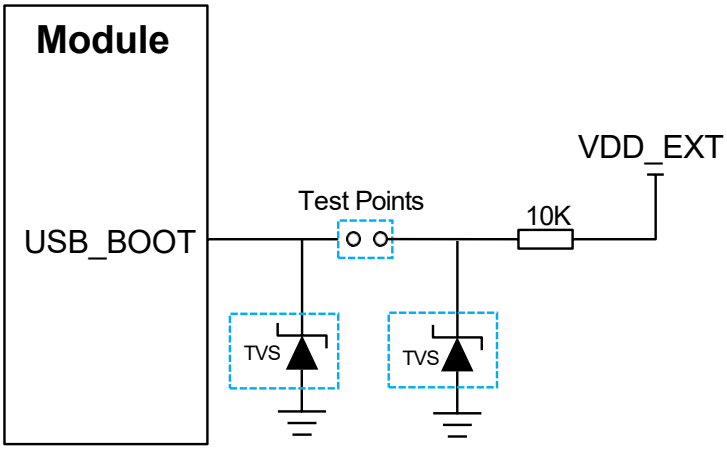


Figure 17: Reference Design of USB_BOOT

NOTE

Follow the above timing when using MCU control the module to enter the emergency download mode. Do not pull up USB_BOOT to 1.8 V before powering up VBAT.

4.3. (U)SIM Interface

The (U)SIM interface meets ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V (U)SIM card is supported, and Dual SIM Single Standby function is supported.

Table 15: Pin Description of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	96	PO	(U)SIM1 card power supply	
USIM1_DATA	97	DIO	(U)SIM1 card data	
USIM1_CLK	99	DO	(U)SIM1 card clock	
USIM1_RST	100	DO	(U)SIM1 card reset	
USIM1_DET	101	DI	(U)SIM1 card hot-plug detect	
USIM2_VDD	103	PO	(U)SIM2 card power supply	
USIM2_DATA	104	DIO	(U)SIM2 card data	
USIM2_CLK	107	DO	(U)SIM2 card clock	
USIM2_RST	108	DO	(U)SIM2 card reset	
USIM2_DET	105	DI	(U)SIM2 card hot-plug detect	

The module supports (U)SIM card hot-plug via the USIM_DET pin, which is a level-triggered pin.

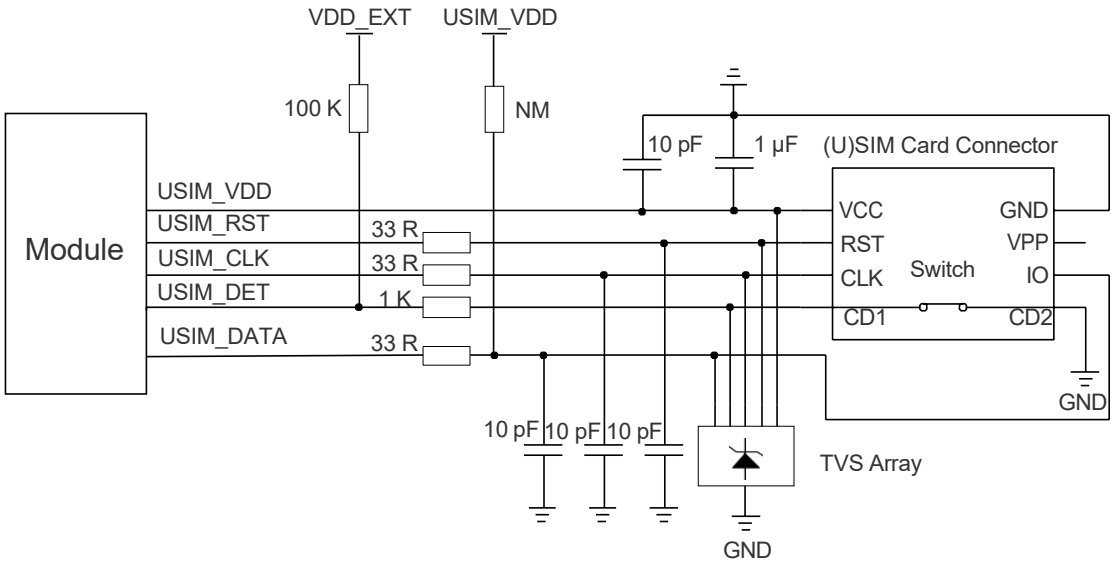


Figure 18: Reference Design of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If the function of (U)SIM card hot-swap is not needed, keep USIM_DET disconnected.

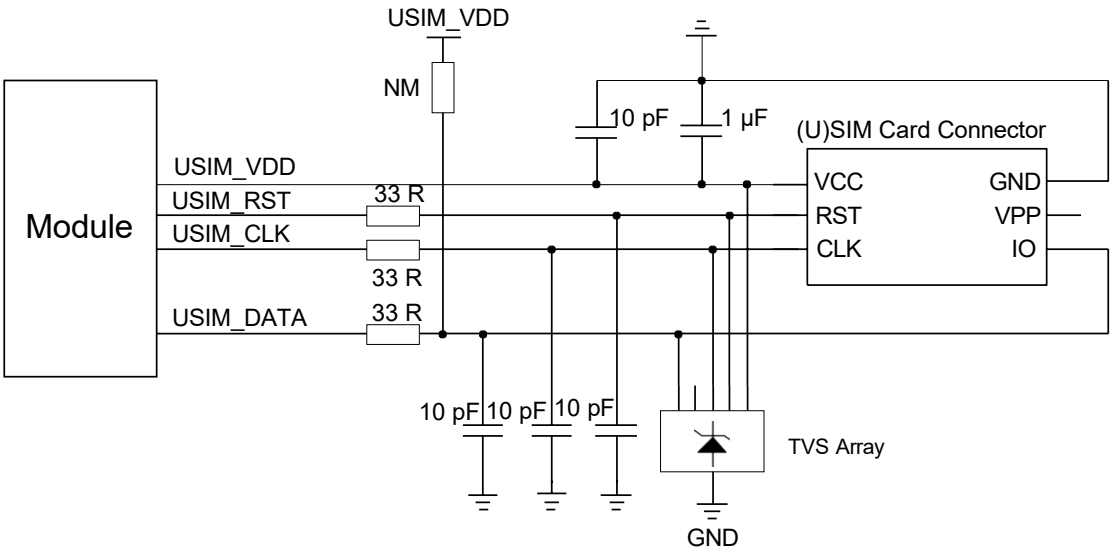


Figure 19: Reference Design of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, you should follow the principles below in the (U)SIM circuit design:

- Place the (U)SIM card connector close to the module. Keep the trace length less than 200 mm if possible.
- Route (U)SIM card traces at the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below. For signal traces, provide clearance from power supply traces, crystal-oscillators, magnetic devices, sensitive signals like RF signals, analog signals, and noise signals generated by clock, DC-DC, etc.
- Ensure the tracing between the (U)SIM card connector and the module is short and wide. Keep the trace width of ground and USIM_VDD at least 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep the traces away from each other and shield them with surrounded ground.
- To offer better ESD protection, you can add a TVS array of which the parasitic capacitance should be less than 45 pF. Add 33 Ω resistors in series between the module and the (U)SIM card connector to facilitate debugging. Additionally, add 10 pF capacitors in parallel among USIM_DATA, USIM_CLK and USIM_RST signal traces to filter out RF interference.

4.4. SDIO Interface

The module provides one SDIO interface which supports SD 3.0 protocol.

Table 16: Pin Description of SDIO Interface

Pin Name	Pin No.	I/O	Description	Comment
SDIO_CLK	365	DO	SDIO clock	Only used for SD card.
SDIO_CMD	369	DIO	SDIO command	
SDIO_DATA0	370	DIO	SDIO data bit 0	
SDIO_DATA1	362	DIO	SDIO data bit 1	
SDIO_DATA2	361	DIO	SDIO data bit 2	
SDIO_DATA3	366	DIO	SDIO data bit 3	
SD_DET	374	DI	SD card hot-plug detect	
SDIO_PWR_EN	363	DO	SDIO power supply enable	
SDIO_PU_VDD	373	PO	SD card IO pull-up power supply	

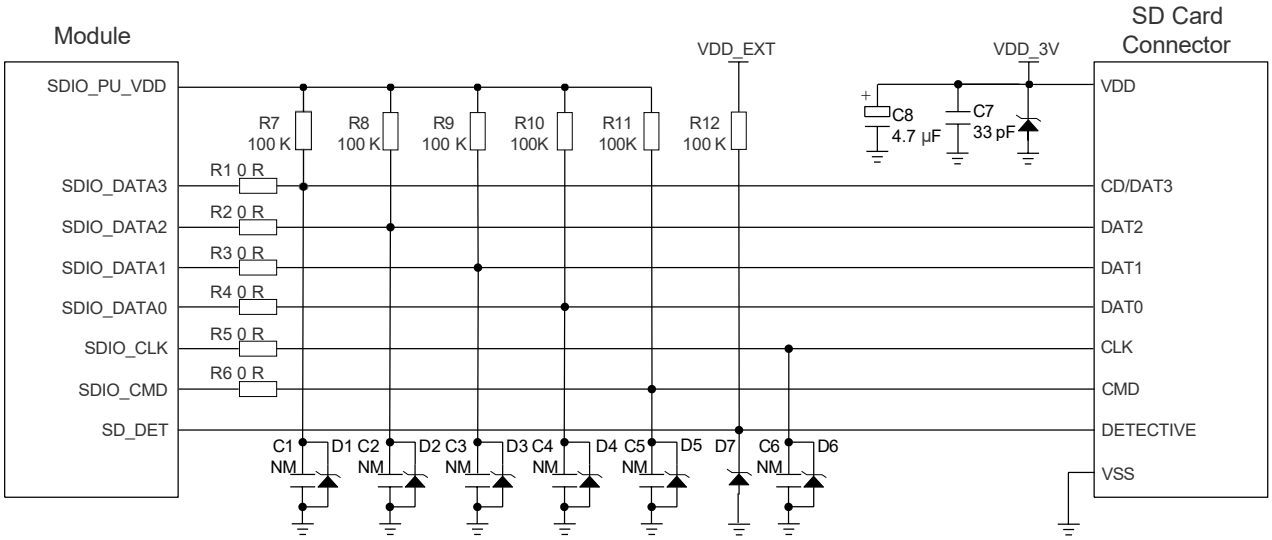


Figure 20: Reference Design of SDIO Interface

To ensure communication performance, the following conditions should be taken into considerations when designing SDIO interface:

- The voltage range of VDD_3V is 2.7–3.6 V and it should provide a current up to 800 mA. SDIO_PU_VDD can provide up to 200 mA current.
- To avoid the impact of jitter, pull up SDIO_CMD and SDIO_DATA[0:3] to SDIO_VDD with R7–R11. Resistance of these resistors can be 10–100 kΩ and the recommended value is 100 kΩ.
- To enhance signal quality, add 0 Ω resistors R1–R6 in series and bypass capacitors C1–C6 (not mounted by default) between the module and the SD card connector. All resistors and bypass capacitors should be placed close to the connector.
- Add a TVS component with capacitance value of less than 3 pF on each SD card pin for better ESD protection.
- It is important to route SDIO signal traces at the inner-layer of the PCB and with surrounded ground. The impedance of SDIO signal trace is 50 Ω ±10 %.
- Keep SDIO signal traces far away from power supply traces, crystal-oscillators, magnetic devices, sensitive signals and signals like RF signals, analog signals, and noise signals generated by clock, DC-DC, etc.
- Keep the trace length matching between SDIO_CLK and SDIO_DATA[0:3]/SDIO_CMD less than 7.6 mm and the total routing length less than 104 mm. The total trace length inside the module is 41 mm, so the exterior total trace length should be less than 63 mm.
- Keep the adjacent trace clearance twice the trace width and the load capacitance of SDIO bus less than 5 pF.

NOTE

For SD 3.0 SDR104 mode, a sufficient current of up to 800 mA and a 4.7 μF capacitor for the power supply is necessary.

4.5. UART Interfaces

The module provides four UARTs:

Table 17: UART Information

UART Type	Baud Rate (Typ.)	Functions
Main UART	115200 bps	Data transmission and AT command communication
Debug UART	921600 bps	Linux console and log output
Bluetooth UART*	115200 bps	Bluetooth communication
Coexistence UART*	115200 bps	Wi-Fi Coexistence communication

Table 18: Pin Description of UART

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	303	DO	DTE clear to send signal from DCE	Connect to DTE's CTS.
MAIN_RTS	306	DI	DTE request to send signal to DCE	Connect to DTE's RTS.
MAIN_RXD	300	DI	Main UART receive	
MAIN_TXD	302	DO	Main UART transmit	
BT_TXD	41	DO	Bluetooth UART transmit	
BT_RXD	49	DI	Bluetooth UART receive	
BT_RTS	45	DI	DTE request to send signal to DCE	Connect to DTE's RTS.
BT_CTS	53	DO	DTE clear to send signal from DCE	Connect to DTE's CTS.
DBG_RXD	309	DI	Debug UART receive	Test points must be reserved.
DBG_TXD	305	DO	Debug UART transmit	

The module provides 1.8 V UART. You can use a level-shifting chip between the module and host's UART if the host is equipped with a 3.3 V UART.

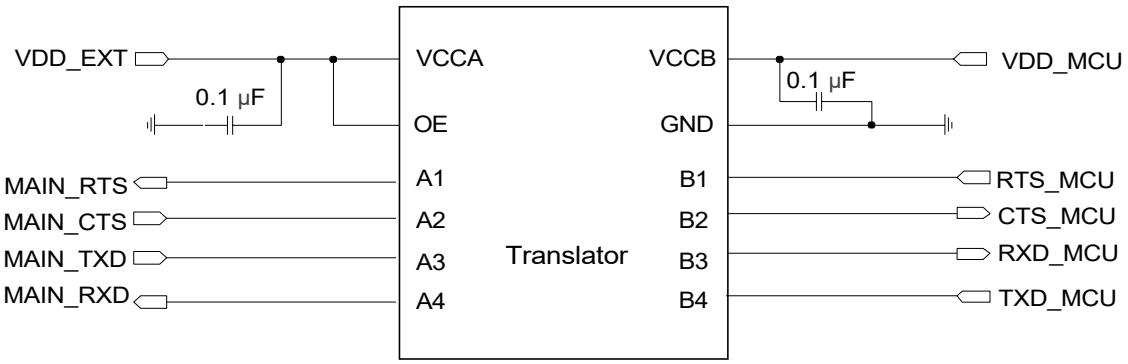


Figure 21: Reference Design of UART with Level-shifting Chip

The following figure illustrates the reference design for Bluetooth UART interface connection between RG620T series and Wi-Fi/Bluetooth module.

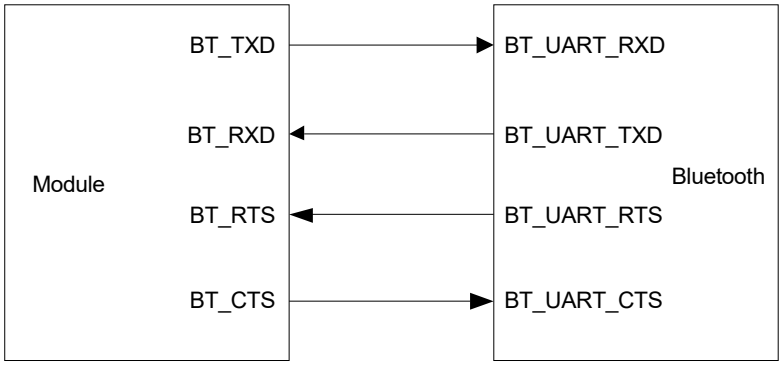


Figure 22: Bluetooth UART Interface Connection

Another example of level-shifting circuit is shown as below. For the design of input/output circuits in dotted lines, see that shown in solid lines, but pay attention to the direction of the connection.

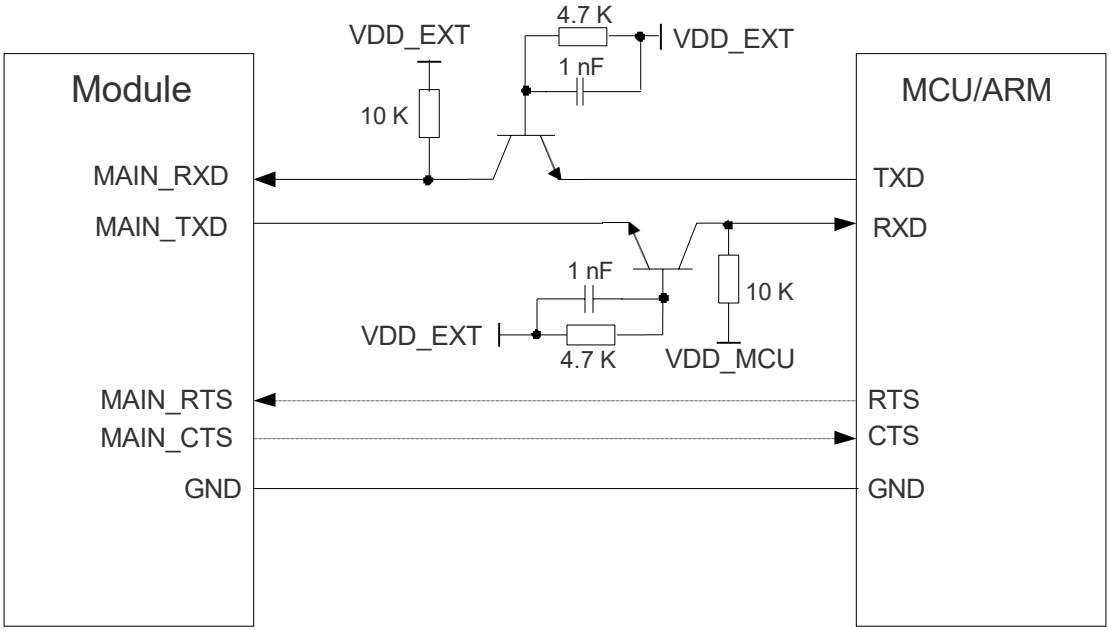


Figure 23: Reference Design of UART with Transistor Level-shifting Circuit

NOTE

1. Transistor level-shifting circuit above is not suitable for applications with baud rates exceeding 460 kbps.
2. Note that the module's CTS is connected to the host's CTS, and the module's RTS is connected to the host's RTS.

4.6. I2C Interface*

The module provides four I2C interfaces:

Table 19: Pin Description of I2C Interface

Pin Name	Pin No.	Alternate Function	I/O	Description	Comment
TP_I2C_SCL	359	-	OD	TP I2C clock	External pull-up resistor is required. 1.8 V only. If unused, keep it open.
TP_I2C_SDA	358	-	OD	TP I2C data	
I2C4_SCL	133	-	OD	I2C serial clock	
I2C4_SDA	129	-	OD	I2C serial data	
SPI0_CS	364	I2C_SDA2	OD	I2C serial data	External pull-up resistor is required. 1.8 V only. If unused, keep it open.
SPI0_CLK	367	I2C_SCL2	OD	I2C serial clock	
SPI0_MOSI	371	I2C_SCL3	OD	I2C serial data	
SPI0_MISO	368	I2C_SDA3	OD	I2C serial clock	

NOTE

For more details about pin multiplexing, see ***document [5]***.

4.7. PCM Interface

The module provides two PCM interface:

Table 20: Pin Description of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM0_SYNC*	69	DIO	PCM data frame sync	In master mode, they are output signals. In slave mode, they are input signals.
PCM0_CLK*	81	DIO	PCM clock	

PCM0_DIN*	77	DI	PCM data input	If unused, keep them open.
PCM0_DOUT*	73	DO	PCM data output	
PCM1_SYNC	325	DIO	PCM data frame sync	In master mode, they are output signals. In slave mode, they are input signals.
PCM1_CLK	322	DIO	PCM clock	
PCM1_DIN	318	DI	PCM data input	If unused, keep them open.
PCM1_DOUT	317	DO	PCM data output	
I2S0_MCLK*	314	DO	I2S0 master clock	If unused, keep them open.
I2S4_MCLK*	65	DO	I2S4 master clock	

NOTE

PCM1 is used for SLIC by default.

4.8. ADC Interface

The module provides 7 ADC interface. To improve the accuracy of ADC, the trace of ADC interface should be surrounded by ground.

Table 21: Pin Description of ADC Interface

Pin Name	Pin No.	I/O	Description	Comment
ADC0	357	AI	General-purpose ADC interface	Max input 1.78 V. If unused, connect it to GND directly.
ADC1	312	AI	General-purpose ADC interface	
ADC2	316	AI	General-purpose ADC interface	
ADC3	320	AI	General-purpose ADC interface	
ADC4	324	AI	General-purpose ADC interface	
ADC5	210	AI	General-purpose ADC interface	

ADC6	214	AI	General-purpose ADC interface

With **AT+QADC=<port>**, you can:

- **AT+QADC=0**: read the voltage value on ADC0
- **AT+QADC=1**: read the voltage value on ADC1
- **AT+QADC=2**: read the voltage value on ADC2
- **AT+QADC=3**: read the voltage value on ADC3
- **AT+QADC=4**: read the voltage value on ADC4
- **AT+QADC=5**: read the voltage value on ADC5
- **AT+QADC=6**: read the voltage value on ADC6

For more details about the AT command, see ***Chapter 9.3***.

Table 22: Characteristics of ADC Interface

Parameter	Min.	Typ.	Max.	Unit
ADC0 voltage range	0.04	-	1.78	V
ADC1 voltage range	0.04	-	1.78	V
ADC2 voltage range	0.04	-	1.78	V
ADC3 voltage range	0.04	-	1.78	V
ADC4 voltage range	0.04	-	1.78	V
ADC5 voltage range	0.04	-	1.78	V
ADC6 voltage range	0.04	-	1.78	V
ADC resolution	0	-	12	bits

NOTE

1. The input voltage of every ADC interface should not exceed its corresponding voltage range.
2. It is prohibited to directly supply any voltage to ADC interface when the module is not powered by the VBAT.
3. It is recommended to use resistor divider circuit for ADC interface application.

4.9. USXGMII Interface

The module includes two integrated Ethernet MAC with two USXGMII interfaces and one MDIO management interface. Key features of the USXGMII interfaces are shown below:

- IEEE 802.3x compliant
- Full duplex mode for 100 Mbps, 1000 Mbps, 2500 Mbps, 5000 Mbps and 10000 Mbps.
- Can be connected to an external Ethernet Switch or PHY, such as MT7531AE, RTL8221B and AQR113C.
- The MDIO management interface and USXGMII interrupt/reset signals support 1.8 V power domain

Table 23: Pin Definition of USXGMII Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MDIO_DATA	384	DIO	MDIO data	
MDIO_CLK	387	DO	MDIO clock	
ETH0_INT_N	388	DI	Ethernet PHY 0 interrupt	
ETH0_RST_N	391	DO	Ethernet PHY 0 reset	
ETH1_INT_N	380	DI	Ethernet PHY 1 interrupt	
ETH1_RST_N	383	DO	Ethernet PHY 1 reset	
USXGMII0_CLK_M*	397	AO	USXGMII0 clock (-)	Require differential impedance of 100 Ω. If unused, connect RX to GND directly.
USXGMII0_CLK_P*	399	AO	USXGMII0 clock (+)	
USXGMII0_TX_M	400	AO	USXGMII0 transmit (-)	
USXGMII0_TX_P	401	AO	USXGMII0 transmit (+)	
USXGMII0_RX_P	402	AI	USXGMII0 receive (+)	
USXGMII0_RX_M	403	AI	USXGMII0 receive (-)	
USXGMII1_CLK_M*	382	AO	USXGMII1 clock (-)	
USXGMII1_CLK_P*	385	AO	USXGMII1 clock (+)	
USXGMII1_RX_P	386	AI	USXGMII1 receive (+)	
USXGMII1_RX_M	389	AI	USXGMII1 receive (-)	

USXGMII1_TX_P	390	AO	USXGMII1 transmit (+)
USXGMII1_TX_M	393	AO	USXGMII1 transmit (-)

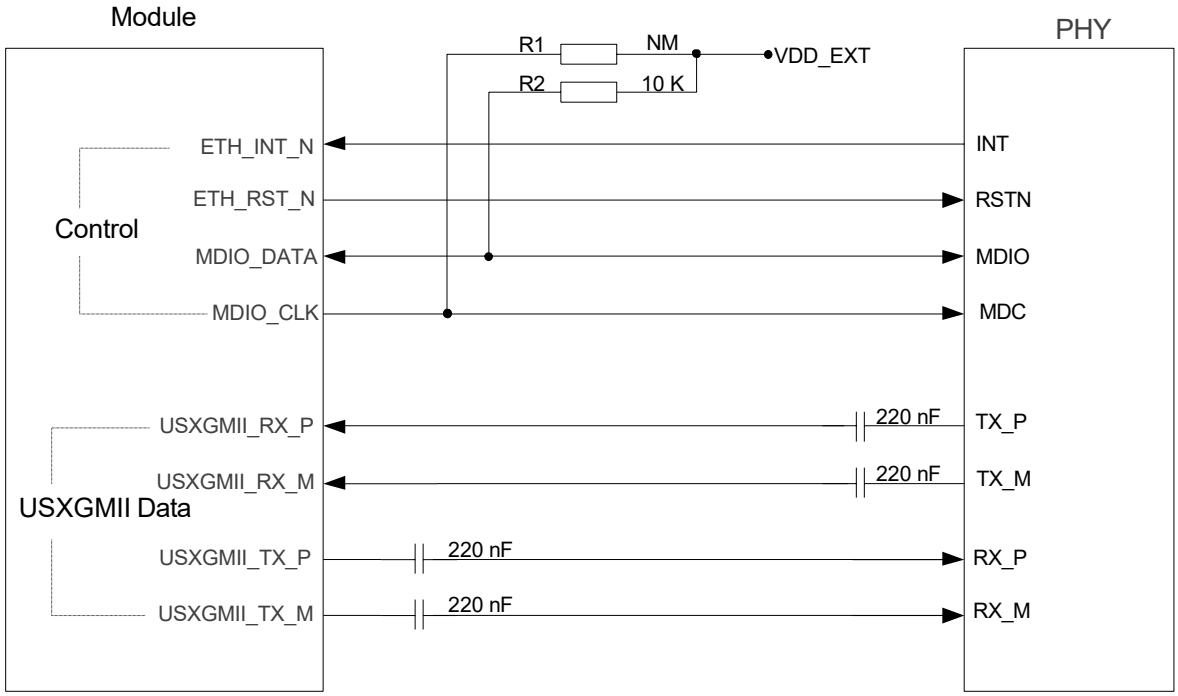


Figure 24: Reference Circuit of USXGMII Interface with PHY Application

To enhance the reliability and availability of your application, please follow the criteria below in the Ethernet PHY circuit design:

- Keep USXGMII data and control signals away from RF and VBAT traces.
- Keep the maximum trace length less than 200 mm and keep length matching within each differential pair less than 0.125 mm.
- The differential impedance of USXGMII data traces is 100 Ω ±10%.
- To minimize crosstalk, the distance between separate adjacent pairs on the same layer must be equal to or larger than 1 mm.
- Less than 2 vias should be designed in each differential pair.
- Reserve enough GND planes between MDC and MDIO to prevent crosstalk.
- 0.22 μF AC coupling capacitors should be placed close to the transmitter source.

Table 24: USXGMII Interface Trace Length Inside the Module (Unit: mm)

Pin Name.	Pin No.	Length (mm)	Length Matching
USXGMII0_CLK_M	397	21.71	-0.07
USXGMII0_CLK_P	399	21.78	
USXGMII0_TX_M	400	21.54	-0.03
USXGMII0_TX_P	401	21.57	
USXGMII0_RX_P	402	22.86	-0.02
USXGMII0_RX_M	403	22.84	
USXGMII1_CLK_M	382	27.70	0.06
USXGMII1_CLK_P	385	27.64	
USXGMII1_RX_P	386	25.02	-0.03
USXGMII1_RX_M	389	24.99	
USXGMII1_TX_P	390	24.49	0.08
USXGMII1_TX_M	393	24.57	

4.10. LCM Interface*

The module provides an LCM interface and also supports 4-lane SPI communication. LCM interface of the module has a multiplexing relationship, and the function can be realized through DBI and other interfaces.

Table 25: Pin Description of LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
LSDI	153	DI	SPI serial input data	
LSA0	161	DO	Indicate transmission of data or command	
LSCE0B	157	DO	SPI chip select	

LSRSTB	150	DO	SPI reset	
LSCK	169	DO	SPI serial clock	
LSDA	165	DO	SPI serial output data	
PWM	131	DO	PWM output	For LCD only
LCD_TE	149	DI	LCM tearing effect	
LCD_RST	141	DO	LCM reset	

The following figures show the reference design for LCM interface.

Figure 25: Reference Circuit Design for LCM Interface

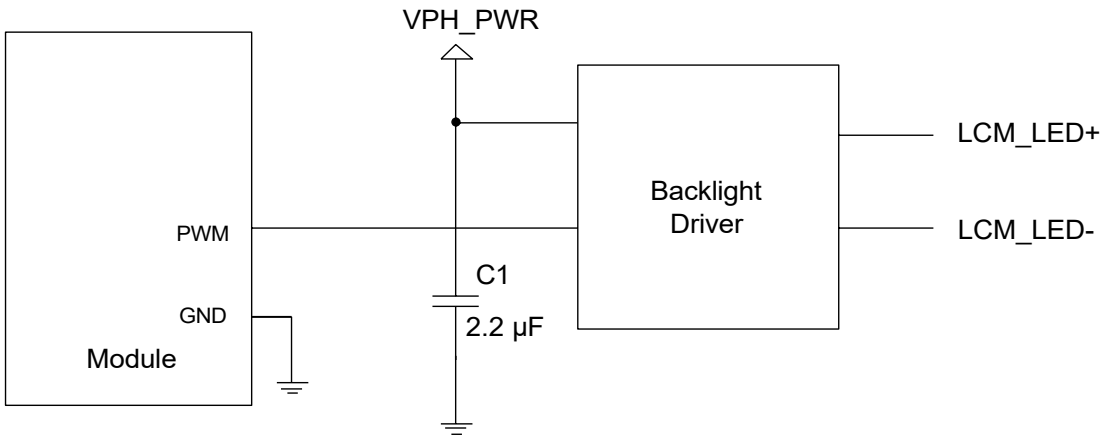


Figure 26: Reference Circuit of LCM External Backlight Driver

4.11. Touch Panel Interface

The module provides one group of I2C interface for connection with touch panel (TP) by default. Also, reset pin and interrupt pin are provided.

Table 26: Pin Description of Touch Panel Interface

Pin Name	Pin No.	I/O	Description	Comment
TP_I2C_SCL	359	OD	TP I2C clock	External pull-up resistor is required. 1.8 V only. If unused, keep it open.
TP_I2C_SDA	358	OD	TP I2C data	
TP_RST*	351	DO	TP reset	
TP_INT*	352	DI	TP interrupt	

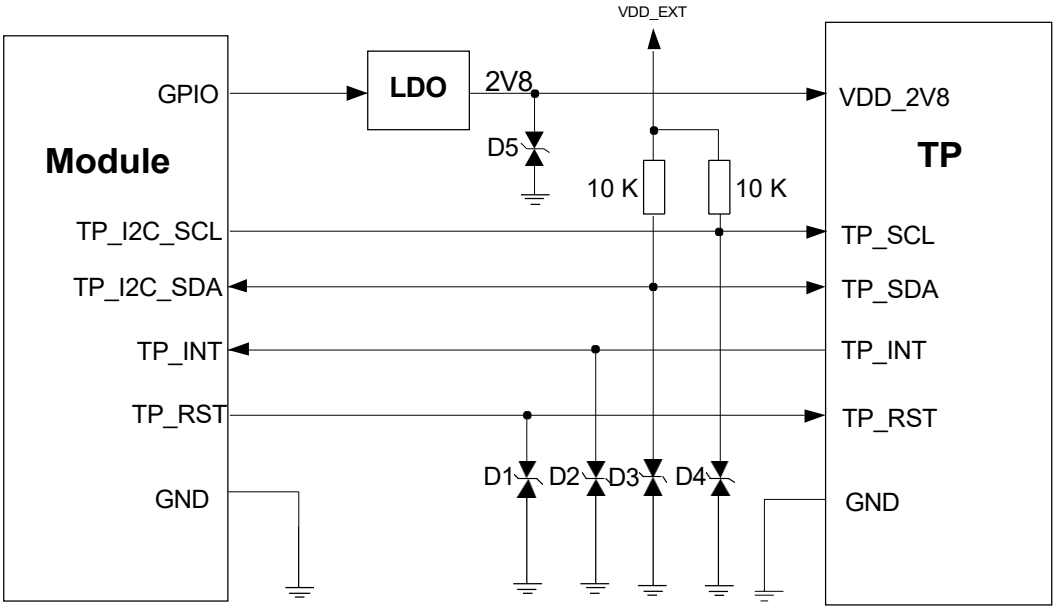


Figure 27: Reference Design of Touch Panel Interface

4.12. Matrix Keypad Interface*

The matrix keypad interfaces support 3 × 3 of nine keypads. They can be used as general GPIOs.

Table 27: Pin Description of Matrix Keypad Interface

Pin Name	Pin No.	I/O	Description	Comment
KPCOL0	146	DIO	Matrix keypad column0	Do not pull it low before startup, otherwise it will force the module into emergency download mode.
KPCOL1	142	DIO	Matrix keypad column1	
KPCOL2	138	DIO	Matrix keypad column2	
KPROW0	134	DIO	Matrix keypad row0	
KPROW1	130	DIO	Matrix keypad row1	
KPROW2	126	DIO	Matrix keypad row2	

4.13. PCIe Interface

The module provides three PCIe interfaces. PCIe1 is in compliance with *PCI Express Base Specification Revision 4.0*. PCIe2 and PCIe3 are in compliance with *PCI Express Base Specification Revision 3.0*. Key features of the PCIe interface are as below:

- Data rate: PCIe1 16 Gbps/lane，PCIe2/3 8 Gbps/lane.
- Can be used to connect to an external Ethernet IC (MAC and PHY) or Wi-Fi IC

Table 28: Pin Description of PCIe Interface

Pin Name	Pin No.	I/O	Description	Comment
PCIE1_REFCLK_M	50	AO	PCIe1 reference clock (-)	The REFCLK requires differential impedance of 100 Ω. The TX/RX requires differential impedance of 85 Ω. PCIe Gen 4 compliant. If unused, connect RX to
PCIE1_REFCLK_P	51	AO	PCIe1 reference clock (+)	
PCIE1_RX0_M	42	AI	PCIe1 receive 0 (-)	
PCIE1_RX0_P	43	AI	PCIe1 receive 0 (+)	
PCIE1_TX0_M	39	AO	PCIe1 transmit 0 (-)	
PCIE1_TX0_P	38	AO	PCIe1 transmit 0 (+)	

PCIE1_RX1_M	55	AI	PCIe1 receive 1 (-)	GND directly.
PCIE1_RX1_P	54	AI	PCIe1 receive 1 (+)	
PCIE1_TX1_M	59	AO	PCIe1 transmit 1 (-)	
PCIE1_TX1_P	58	AO	PCIe1 transmit 1 (+)	
PCIE1_RST_N	52	DO	PCIe1 reset	
PCIE1_WAKE_N	48	DI	PCIe1 wake up	
PCIE1_CLKREQ_N	44	DI	PCIe1 clock request	
PCIE2_REFCLK_M	22	AO	PCIe2 reference clock (-)	The REFCLK requires differential impedance of 100 Ω. The TX/RX requires differential impedance of 85 Ω. PCIe Gen 3 compliant. If unused, connect RX to GND directly.
PCIE2_REFCLK_P	23	AO	PCIe2 reference clock (+)	
PCIE2_RX0_M	14	AI	PCIe2 receive 0 (-)	
PCIE2_RX0_P	15	AI	PCIe2 receive 0 (+)	
PCIE2_TX0_M	11	AO	PCIe2 transmit 0 (-)	
PCIE2_TX0_P	10	AO	PCIe2 transmit 0 (+)	
PCIE2_RX1_M	27	AI	PCIe2 receive 1 (-)	
PCIE2_RX1_P	26	AI	PCIe2 receive 1 (+)	
PCIE2_TX1_M	31	AO	PCIe2 transmit 1 (-)	
PCIE2_TX1_P	30	AO	PCIe2 transmit 1 (+)	
PCIE2_RST_N	24	DO	PCIe2 reset	
PCIE2_WAKE_N	20	DI	PCIe2 wake up	
PCIE2_CLKREQ_N	16	DI	PCIe2 clock request	
PCIE3_REFCLK_M*	78	AO	PCIe3 reference clock (-)	The REFCLK requires differential impedance of 100 Ω. The TX/RX require differential impedance of 85 Ω. PCIe Gen 3 compliant. If unused, connect RX to
PCIE3_REFCLK_P*	79	AO	PCIe3 reference clock (+)	
PCIE3_RX0_M*	70	AI	PCIe3 receive 0 (-)	
PCIE3_RX0_P*	71	AI	PCIe3 receive 0 (+)	
PCIE3_TX0_M*	67	AO	PCIe3 transmit 0 (-)	
PCIE3_TX0_P*	66	AO	PCIe3 transmit 0 (+)	

PCIE3_RX1_M*	83	AI	PCIe3 receive 1 (-)	GND directly.
PCIE3_RX1_P*	82	AI	PCIe3 receive 1 (+)	
PCIE3_TX1_M*	86	AO	PCIe3 transmit 1 (-)	
PCIE3_TX1_P*	85	AO	PCIe3 transmit 1 (+)	
PCIE3_RST_N*	80	DO	PCIe3 reset	
PCIE3_WAKE_N*	76	DI	PCIe3 wake up	
PCIE3_CLKREQ_N*	72	DI	PCIe3 clock request	

The following figure illustrates the PCIe interface connection.

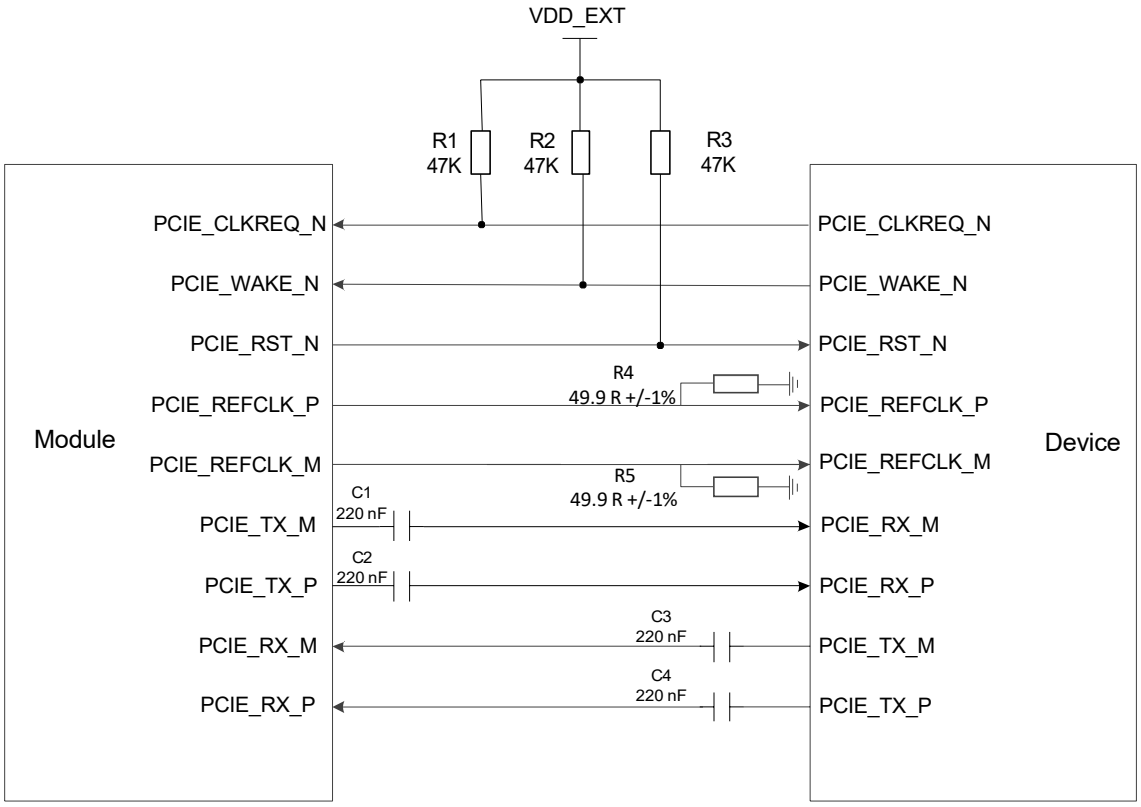


Figure 28: Reference Design of PCIe Interface Connection

To ensure the signal integrity of the PCIe interface, place C1 and C2 near the module and place C3 and C4 near the PCIe device. Keep the traces as short as possible.

To ensure the PCIe interface design meets PCIe specifications, you should follow the principles below:

- Route PCIe signal traces (Tx/Rx/REFCLK) as differential pairs with surrounded ground. The differential impedance should be 85 Ω ±10 % of Tx/Rx and 100 Ω ±10 % of REFCLK.
- For PCIe signal traces, the recommended maximum length for Tx and Rx differential data pairs should be less than 200 mm, and the intra-lane length matching of Tx and Rx differential data pairs should be less than 0.125 mm.
- Clearance between Tx and Rx signal traces and that among Tx, Rx and all other signal traces should be wider than 3 and 4 times of the trace width respectively.
- Add capacitors in series on Tx/Rx traces to immune from leakage current.
- Route PCIe differential signal traces at the inner-layer of PCB, and surround the traces with ground on that layer and with ground planes above and below. Meanwhile, protect them from interferences such as crystal-oscillators, VBAT traces, RF signal traces, etc.
- For the PCIE_REFCLK pair, add resistors near the slot (EP) side and the recommended resister value is 49.9 Ω +/-1 %.

Table 29: PCIe Interface Trace Length Inside the Module (Unit: mm)

Pin Name	Pin No.	Length (mm)	Length Matching
PCIE1_REFCLK_M	50	12.68	-0.12
PCIE1_REFCLK_P	51	12.80	
PCIE1_RX0_M	42	13.20	0.09
PCIE1_RX0_P	43	13.11	
PCIE1_TX0_M	39	12.67	0.04
PCIE1_TX0_P	38	12.63	
PCIE1_RX1_M	55	12.66	0.00
PCIE1_RX1_P	54	12.66	
PCIE1_TX1_M	59	12.62	-0.01
PCIE1_TX1_P	58	12.63	
PCIE2_REFCLK_M	22	13.83	-0.04
PCIE2_REFCLK_P	23	13.87	
PCIE2_RX0_M	14	14.08	0.10
PCIE2_RX0_P	15	13.98	
PCIE2_TX0_M	11	14.22	-0.10

PCIE2_TX0_P	10	14.32	
PCIE2_RX1_M	27	13.87	-0.05
PCIE2_RX1_P	26	13.92	
PCIE2_TX1_M	31	13.84	-0.01
PCIE2_TX1_P	30	13.85	
PCIE3_REFCLK_M	78	18.67	0.00
PCIE3_REFCLK_P	79	18.67	
PCIE3_RX0_M	70	18.61	0.00
PCIE3_RX0_P	71	18.61	
PCIE3_TX0_M	67	18.59	0.03
PCIE3_TX0_P	66	18.56	
PCIE3_RX1_M	83	19.01	-0.01
PCIE3_RX1_P	82	19.02	
PCIE3_TX1_M	86	19.08	0.04
PCIE3_TX1_P	85	19.04	

4.14. SPI Interface

The module provides three SPI which supports both master and slave modes with a maximum clock frequency up to 52 MHz.

Table 30: Pin Description of SPI

Pin Name	Pin No.	I/O	Description	Comment
SPI0_CS*	364	DO	SPI0 chip select	
SPI0_CLK*	367	DO	SPI0 clock	
SPI0_MOSI*	371	DO	SPI0 master-out slave-in	
SPI0_MISO*	368	DI	SPI0 master-in salve-out	

SPI2_CS*	376	DO	SPI2 chip select	
SPI2_CLK*	377	DO	SPI2 clock	
SPI2_MOSI*	375	DO	SPI2 master-out slave-in	
SPI2_MISO*	378	DI	SPI2 master-in salve-out	
SPI3_CS	326	DO	SPI3 chip select	Recommended for SLIC IC communication.
SPI3_CLK	329	DO	SPI3 clock	
SPI3_MOSI	333	DO	SPI3 master-out slave-in	
SPI3_MISO	330	DI	SPI3 master-in salve-out	

The module provides 1.8 V SPI interfaces. A voltage-level translator should be used between the module and the host if the application is equipped with a 3.3 V processor or device interface. The following figure shows a reference design:

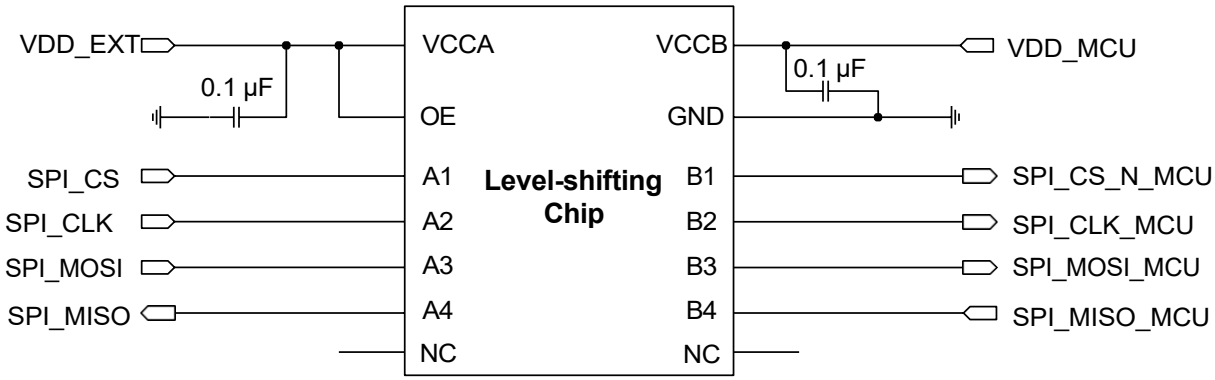


Figure 29: Reference Design of SPI with a Level-Shifting Chip

4.15. Time Service and Repeater Interface

'Time service' means to provide time information for other devices or systems through standard or customized interfaces and protocols. Basic channels include shortwave, TV signals, cables, networks, satellites, base stations, etc.

'Repeater' is a kind of wireless signal relay device, which can amplify the base station signal and then transmits it to areas with weak signal coverage, to expand the network coverage.

With GNSS time service and repeater functions, the module can provide 1PPS pulse output and execute

time service through AT commands based on baseline SIB9 system messages.

Table 31: Pin Description of Time Service and Repeater Interface

Pin Name	Pin No.	I/O	Description	Comment
GNSS_LNA_EN*	313	DO	GNSS LNA enable control; 1PPS pulse output and frame synchronization	

4.16. Control Signal

Table 32: Pin Description of Control Signal

Pin Name	Pin No.	I/O	Description	Comment
RESTORE_KEY	311	DI	Restore the module	
WPS_KEY	307	DI	Wi-Fi protected setup	

Reference circuit is shown as below.

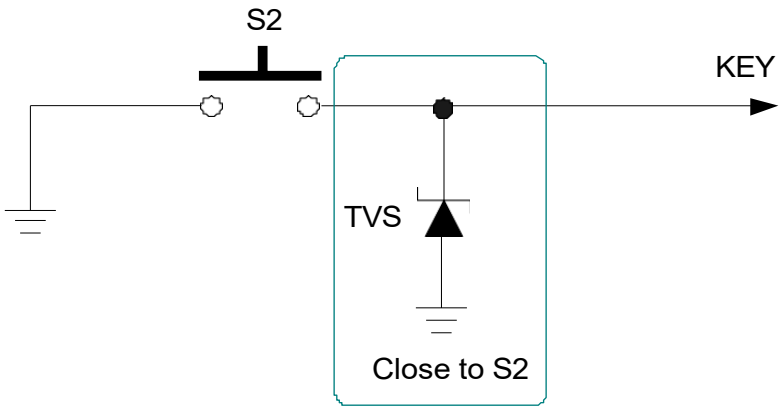


Figure 30: Reference Circuit of Control KEY

4.16.1. WWAN/WLAN Control Interface

The module provides some WWAN/WLAN control interfaces for WLAN function.

Table 33: Pin Description of WWAN/WLAN Control Interface

Pin Name	Pin No.	I/O	Description	Comment
WLAN_SYSRST_5G	21	DO	WLAN 5 GHz system reset	
WLAN_2.4G_EN*	29	DO	WLAN 2.4 GHz function enable control	
WLAN_SYSRST_2.4G	25	DO	WLAN 2.4 GHz system reset	
WLAN_5G_EN*	392	DO	WLAN 5 GHz function enable control	
BT_ACT_0*	61	DO	Coexistence interface for WWAN and WLAN	Used for WWAN/WLAN coexistence by default.
BT_PRI_0*	37	DO	Coexistence interface for WWAN and WLAN	
WLAN_ACT_0*	57	DI	Coexistence interface for WWAN and WLAN	
PTA_TX_0*	64	DO	Coexistence interface for WWAN and WLAN	
PTA_RX_0*	60	DO	Coexistence interface for WWAN and WLAN	
BT_ACT_1*	13	DO	Coexistence interface for WWAN and WLAN	
BT_PRI_1*	9	DO	Coexistence interface for WWAN and WLAN	
WLAN_ACT_1*	33	DI	Coexistence interface for WWAN and WLAN	
PTA_TX_1*	36	DO	Coexistence interface for WWAN and WLAN	
PTA_RX_1*	32	DO	Coexistence interface for WWAN and WLAN	

4.17. Indication Signal

Table 34: Pin Description of Indication Signal

Pin Name	Pin No.	I/O	Description	Comment
STATUS	331	OD	Indicate the module's operation status	PMIC_ISINK3
W_DISABLE#	335	OD	Indicate the module's airplane mode	PMIC_ISINK1
NET_STATUS	354	OD	Indicate the module's network activity status	PMIC_ISINK2
NET_MODE	327	DO	Indicate the module's network registration mode	
WIFI_MESH*	315	DO	Indicate the Wi-Fi mesh function status	
USIM_LED	323	DO	Indicate the (U)SIM card function status	
VOIP_LED*	319	DO	Indicate the VoIP function status	

4.17.1. Network Status Indication

The module provides two network status indication pins: the NET_MODE for the module's network registration status indication and the NET_STATUS for the module's network operation status indication. Both can drive corresponding LEDs.

Table 35: Network Status Indication Pin Level and Module Network Status

Pin Name	NET_MODE/NET_STATUS Level Status	Module Network Status
NET_MODE	Always high	Registered on 5G network [5]
	Always low	Others
NET_STATUS	Flicker slowly (200 ms high/1800 ms low)	Network searching
	Flicker slowly (1800 ms high/200ms low)	Idle
	Flicker quickly (125 ms high/125 ms low)	Data transmission is ongoing

[5] At 'Always high' status, whether the module is 'Registered on LTE network' or 'Registered on 5G network' depends on specific modules.

	Always high	Voice calling
	Always low	Minimum functionality mode

Reference circuit is shown as below.

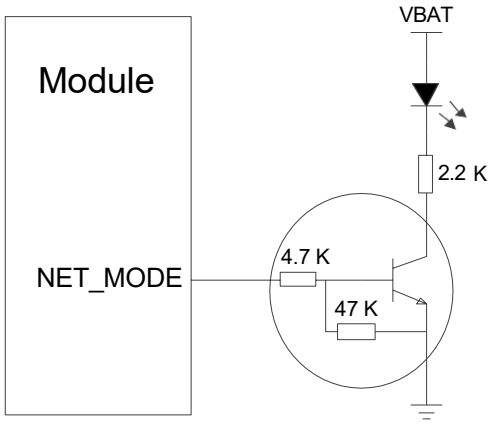


Figure 31: Reference Circuit of NET_MODE Indicator

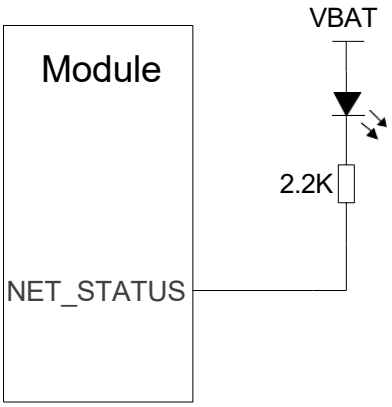


Figure 32: Reference Circuit of NET_STATUS Indicator

4.17.2. STATUS

The STATUS is used for indicating module's operation status. It will output high level when the module is turned on.

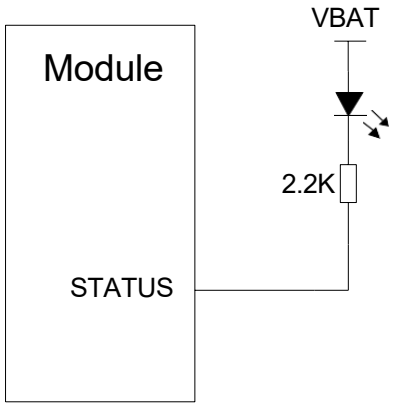


Figure 33: Reference Design of STATUS

4.17.3. W_DISABLE#

The W_DISABLE# pin is an open drain output for indicating the module's airplane mode status. It will output low level when the module enters airplane mode successfully.

A reference circuit is shown as below.

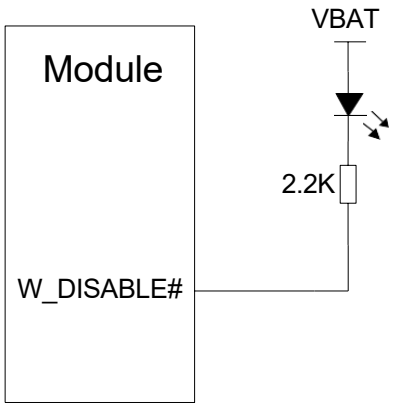


Figure 34: Reference Circuit of W_DISABLE# Indicator

4.17.4. Other Indication Signals

The WIFI_MESH*, USIM_LED and VOIP_LED* pins are output signals for indicating the functional state of the module. A reference circuit is shown as below.

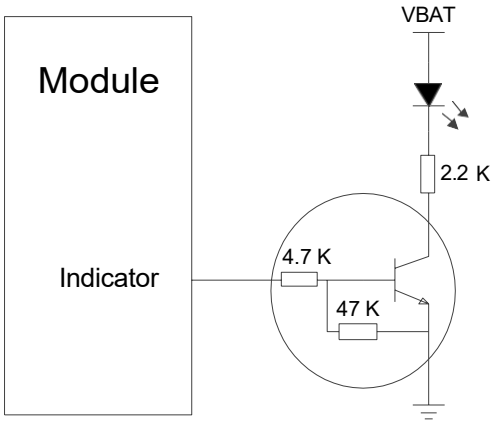


Figure 35: Reference Circuit of Other Indicators

5 RF Specifications

5.1. Cellular Network

5.1.1. Antenna Interface & Frequency Bands

Table 36: Pin Description of Cellular Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT0	191	AIO	Antenna 0 interface	50 Ω characteristic impedance
ANT1	199	AIO	Antenna 1 interface	
ANT2	208	AI	Antenna 2 interface	
ANT3	220	AI	Antenna 3 interface	
ANT4	232	AI	Antenna 4 interface	
ANT5	244	AI	Antenna 5 interface	
ANT6	256	AIO	Antenna 6 interface	
ANT7	268	AIO	Antenna 7 interface	

Table 37: RG620T-NA Cellular Antenna Interface Mapping

Pin Name	WCDMA	LTE	5G NR			LB (MHz)	MHB (MHz)	n77/n78 (MHz)	LAA (MHz)
			Refarming	n41	n77/n78				
ANT0	-	LTE_UHB_TX1/PRX	-	-	TRX0	-	-	3300–4200	-
ANT1	-	LTE_MHB+B5/B26_TX1 LTE_LMHB_DRX	MHB/n5_TX0 LMHB_DRX	TX0/DRX	MIMO5 (HW Ready)	617-894	1695–2690	3300–4200	-
ANT2	-	LTE_UHB_PRX1 LAA_PRX	-	-	PRX1	-	-	3300–4200	5150–5925
ANT3	-	LTE_LMHB_DRX1 B29 DRX	LMHB_DRX1 n29 DRX	DRX1	MIMO4 (HW Ready)	617–894	1695–2690	3300–4200	-
ANT4	-	LTE_UHB_DRX1 LAA_DRX	-	-	DRX1	-	-	3300–4200	5150–5925
ANT5	-	LTE_LMHB_PRX1 B29_PRX	LMHB_PRX1 n29 PRX	PRX1	MIMO6 (HW Ready)	617–894	1695–2690	3300–4200	-
ANT6	-	LTE_UHB_TX0/DRX	-	-	TX1/DRX	-	-	3300–4200	-
ANT7	-	LTE_LMHB_TRX0	LB_TX0 (Except n5) n5_TX1 MHB_TX1 LMHB_PRX	TX1/PRX	MIMO7 (HW Ready)	617–894	1695–2690	3300–4200	-

Table 38: RG620T-EU Cellular Antenna Interface Mapping

Pin Name	WCDMA	LTE	5G NR			LB (MHz)	MHB (MHz)	n77/n78 (MHz)	LAA (MHz)
			Reframing	n41	n77/n78				
ANT0	-	LTE_UHB_TX1/PRX	-	-	TRX0	-	-	3300–4200	-
ANT1	B1/B5/B8_DRX	LTE_MHB+B28_TX1 LTE_LMHB_DRX	MHB_TX0/n28_TX0 LMHB_DRX	TX0/DRX	MIMO5 (HW Ready)	617–960	1695–2690	3300–4200	-
ANT2	-	LTE_UHB_PRX1 LAA_PRX	-	-	PRX1	-	-	3300–4200	5150–5925
ANT3	-	LTE_LMHB_DRX1 B32_DRX	LMHB_DRX1/ n75_DRX	DRX1	MIMO4 (HW Ready)	617–960	1432–2690	3300–4200	-
ANT4	-	LTE_UHB_DRX1 LAA_DRX	-	-	DRX1	-	-	3300–4200	5150–5925
ANT5	-	LTE_LMHB_PRX1 B32_PRX	LMHB_PRX1/ n75_PRX	PRX1	MIMO6 (HW Ready)	617–960	1432–2690	3300–4200	-
ANT6	-	LTE_UHB_TX0/DRX	-	-	TX1/DRX	-	-	3300–4200	-
ANT7	B1/B5/B8_TRX0	LTE_LMHB_TRX0	LB_TX0 (Except n28) n28 TX1 MHB_TX1 LMHB_PRX	TX1/PRX	MIMO7 (HW Ready)	617–960	1695–2690	3300–4200	-

NOTE

1. Only passive antennas are supported.
2. LTE L/M/H/UHB_TRX1 is activated when 5G NR FDD low/middle/high bands are supported in NSA mode.
3. UHB frequency range: 3400–4200 MHz.
4. TRX0/1 = TX0/1 + PRX/DRX.

5.1.2. Antenna Tuner Control Interface

The module can use GRFC (generic RF control) interface to control external antenna tuner.

Table 39: Pin Description of GRFC Interface

Pin Name	Pin No.	I/O	Description	Comment
GRFC1	266	DO	Generic RF Controller	
GRFC2	238	DO	Generic RF Controller	
GRFC3	242	DO	Generic RF Controller	

5.1.3. Transmitting Power

Table 40: RF Transmitting Power

Mode	Frequency Band	Max.	Min.	Power Class
WCDMA	B1/B5/B8 (RG620T-EU only)	23 dBm ±2 dB	<-50 dBm	PC3
LTE	LTE bands	23 dBm ±2 dB	<-40 dBm	PC3
	LTE HPUE bands (B41)	26 dBm +2/-3 dB	<-40 dBm	PC2
5G NR	5G NR bands	23 dBm ±2 dB	<-40 dBm	PC3
	5G NR HPUE bands (n41/n77/n78)	26 dBm +2/-3 dB	<-40 dBm	PC2

5.1.4. Receiver Sensitivity

Table 41: Conducted RF Receiver Sensitivity of RG620T-NA (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)			3GPP Requirements (SIMO)
	Primary	Diversity	SIMO [6]	
LTE-FDD B2 (10 MHz)	TBD	TBD	TBD	-94.3

[6] SIMO is a smart antenna technology that uses a single antenna at the transmitter side and multiple antennas at the receiver side, which improves Rx performance.

LTE-FDD B4 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B5 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B7 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B12 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B13 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B14 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B17 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B25 (10 MHz)	TBD	TBD	TBD	-92.8
LTE-FDD B26 (10 MHz)	TBD	TBD	TBD	-93.8
LTE-FDD B29 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B30 (10 MHz)	TBD	TBD	TBD	-95.3
LTE-TDD B38 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-TDD B41 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-TDD B42 (10 MHz)	TBD	TBD	TBD	-95
LTE-TDD B43 (10 MHz)	TBD	TBD	TBD	-95
LTE LAA B46 (10 MHz)	TBD	TBD	TBD	-95
LTE-TDD B48 (10 MHz)	TBD	TBD	TBD	-95
LTE-FDD B66 (10 MHz)	TBD	TBD	TBD	-95.8
LTE-FDD B71 (10 MHz)	TBD	TBD	TBD	-93.5
5G NR-FDD n2 (10 MHz) (SCS: 15 kHz)	TBD	TBD	TBD	-94.8
5G NR-FDD n5 (10 MHz) (SCS: 15 kHz)	TBD	TBD	TBD	-94.8
5G NR-FDD n7 (10 MHz) (SCS: 15 kHz)	TBD	TBD	TBD	-94.8
5G NR-FDD n12 (10 MHz) (SCS: 15 kHz)	TBD	TBD	TBD	-93.8
5G NR-FDD n25 (10 MHz) (SCS: 15 kHz)	TBD	TBD	TBD	-93.3
5G NR-TDD n38 (10 MHz) (SCS: 30 kHz)	TBD	TBD	TBD	-97.1

5G NR-TDD n41 (100 MHz) (SCS: 30 kHz)	TBD	TBD	TBD	-84.7
5G NR-TDD n48 (100 MHz) (SCS: 30 kHz)	TBD	TBD	TBD	-86.7
5G NR-FDD n66 (10 MHz) (SCS: 15 kHz)	TBD	TBD	TBD	-96.3
5G NR-FDD n70 (10 MHz) (SCS: 15 kHz)	TBD	TBD	TBD	-96.8
5G NR-FDD n71 (10 MHz) (SCS: 15 kHz)	TBD	TBD	TBD	-94
5G NR-TDD n77 (100 MHz) (SCS: 30 kHz)	TBD	TBD	TBD	-85.1
5G NR-TDD n78 (100 MHz) (SCS: 30 kHz)	TBD	TBD	TBD	-85.6

Table 42: Conducted RF Receiver Sensitivity of RG620T-EU (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)			3GPP Requirements (SIMO)
	Primary	Diversity	SIMO	
WCDMA-FDD B1 (5 MHz)	TBD	TBD	TBD	-106.7
WCDMA-FDD B5 (5 MHz)	TBD	TBD	TBD	-104.7
WCDMA-FDD B8 (5 MHz)	TBD	TBD	TBD	-103.7
LTE-FDD B1 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-FDD B3 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B5 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-FDD B7 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-FDD B8 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B20 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B28 (10 MHz)	TBD	TBD	TBD	-94.8
LTE-FDD B32 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-TDD B38 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-TDD B40 (10 MHz)	TBD	TBD	TBD	-96.3
LTE-TDD B41 (10 MHz)	TBD	TBD	TBD	-94.3

LTE-TDD B42 (10 MHz)	TBD	TBD	TBD	-95
LTE-TDD B43 (10 MHz)	TBD	TBD	TBD	-95
LTE-TDD B46 (10 MHz)	TBD	TBD	TBD	-95
LTE-FDD B71 (10 MHz)	TBD	TBD	TBD	-93.5
5G NR-FDD n1 (10 MHz) (SCS: 15 kHz)	TBD	TBD	TBD	-96.8
5G NR-FDD n3 (10 MHz) (SCS: 15 kHz)	TBD	TBD	TBD	-93.8
5G NR-FDD n5 (10 MHz) (SCS: 15 kHz)	TBD	TBD	TBD	-94.8
5G NR-FDD n7 (10 MHz) (SCS: 15 kHz)	TBD	TBD	TBD	-94.8
5G NR-FDD n8 (10 MHz) (SCS: 15 kHz)	TBD	TBD	TBD	-93.8
5G NR-FDD n20 (10 MHz) (SCS: 15 kHz)	TBD	TBD	TBD	-93.8
5G NR-FDD n28 (10 MHz) (SCS: 15 kHz)	TBD	TBD	TBD	-95.5
5G NR-TDD n38 (10 MHz) (SCS: 30 kHz)	TBD	TBD	TBD	-97.1
5G NR-TDD n40 (10 MHz) (SCS: 30 kHz)	TBD	TBD	TBD	-97.1
5G NR-TDD n41 (100 MHz) (SCS: 30 kHz)	TBD	TBD	TBD	-84.7
5G NR-FDD n71 (10 MHz) (SCS: 15 kHz)	TBD	TBD	TBD	-94
5G NR-SDL n75 (10 MHz) (SCS: 15 kHz)	TBD	TBD	TBD	-96.8
5G NR-TDD n77 (100 MHz) (SCS: 30 kHz)	TBD	TBD	TBD	-85.1
5G NR-TDD n78 (100 MHz) (SCS: 30 kHz)	TBD	TBD	TBD	-85.6

5.1.5. Reference Design

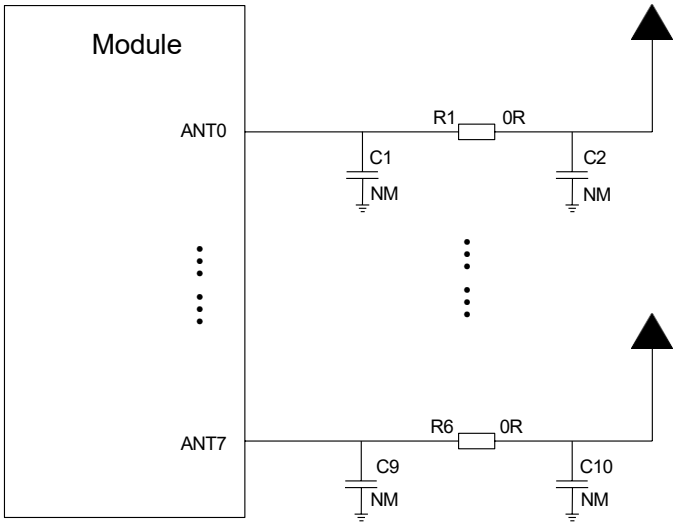


Figure 36: Reference Design of Cellular Antenna

NOTE

1. Use a π-type matching circuit for all the antenna interfaces for better RF performance and for the ease of debugging.
2. Capacitors are not mounted by default.
3. Place the π-type matching components to antennas as close as possible.
4. Keep the characteristic impedance of cellular antenna (ANT0–ANT7, ANT_GNSS) traces as 50 Ω when routing.
5. Keep at least 15 dB isolation between RF antennas on PCB to improve the receiver sensitivity, and at least 20 dB isolation between 5G NR UL MIMO antennas.
6. The isolation between each two antenna traces on PCB is recommended to be over 75 dB.
7. Keep digital signals such as (U)SIM interface, USB interface, camera module, SDIO and display module away from the antenna traces.

5.2. GNSS

GNSS information of the module is as follows:

- Supports GPS, GLONASS, BDS, Galileo, QZSS positioning system.
- Supports NMEA 0183 protocol and outputs NMEA sentences via USB interface (data update rate for positioning: 1–5 Hz, 1 Hz by default).
- The module's GNSS function is OFF by default. It must be ON via AT commands.

For more details about GNSS technology and configurations, see ***document [2]***.

5.2.1. Antenna Interface & Frequency Bands

Table 43: Pin Description of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	290	AI	GNSS antenna interface	50 Ω impedance.

Table 44: GNSS Frequency (Unit: MHz)

Antenna Type	Frequency
GPS	1575.42 ±1.023 (L1) 1176.45 ±10.23 (L5)
GLONASS	1597.5–1605.8 (L1)
BDS	1561.098 ±2.046 (B1I)
Galileo	1575.42 ±2.046 (E1) 1176.45 ±10.23 (E5a)
QZSS	1575.42 ±1.023 (L1) 1176.45 ±10.23 (L5)

5.2.2. GNSS Performance

Table 45: GNSS Performance

Parameter	Mode	Condition	Typ.	Unit
Sensitivity	Acquisition	Autonomous	TBD	dBm
	Reacquisition		TBD	
	Tracking		TBD	
TTFF	Cold start @ open sky	Autonomous	TBD	s
	Warm start @ open sky	Autonomous	TBD	
	Hot start @ open sky	Autonomous	TBD	
Accuracy	CEP-50	Autonomous @ open sky	TBD	m

NOTE

1. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position of navigation signals successfully within 3 minutes after executing cold start command.
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock of navigation signals within 3 minutes after loss of lock.
3. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock of navigation signals (keep positioning for at least 3 minutes continuously).

5.2.3. Reference Design

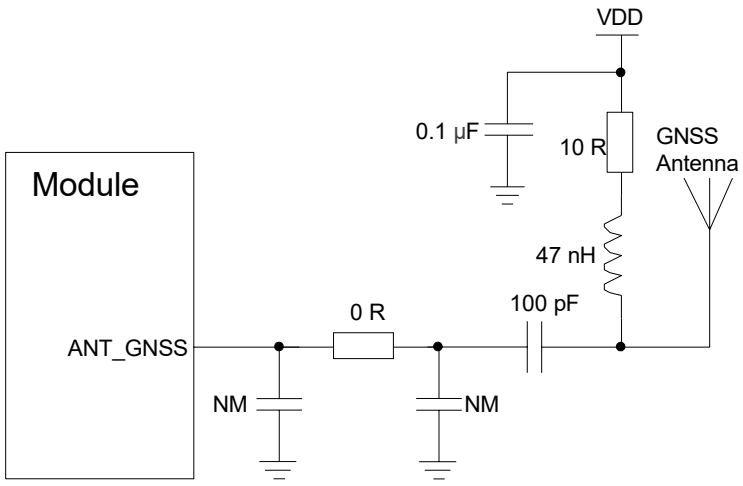


Figure 37: Reference Design of GNSS Antenna

NOTE

1. You can select an external LDO according to the active antenna types. If you design the module with a passive antenna, you will not need the VDD circuit.
2. Junction capacitance of ESD protection components on the antenna interface should not exceed 0.05 pF.
3. Keep the characteristic impedance for ANT_GNSS trace as 50 Ω when routing.
4. Place the π-type matching components as close to the antenna as possible.
5. Keep digital circuits such as switch-mode power supply, (U)SIM interface, USB interface, camera module, display connector and SD card interface away from the antenna traces.
6. Keep 75 dB isolation between GNSS and cellular antenna traces on PCB.
7. Keep 15 dB isolation between GNSS and cellular antennas on PCB to improve receiver sensitivity.
8. It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.3. RF Routing Guidelines

When designing PCB, characteristic impedance of all RF traces should be controlled to 50 Ω. Generally, the impedance of RF traces is determined by materials' dielectric constant, trace width (W), space between RF traces and grounds (S) and height from the reference ground to the signal layer (H). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures when characteristic impedance of RF traces is controlled to 50 Ω.

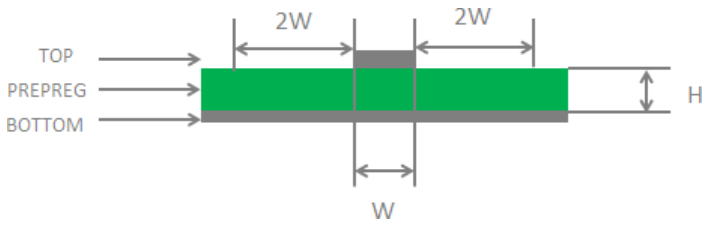


Figure 38: Microstrip Design on a 2-layer PCB

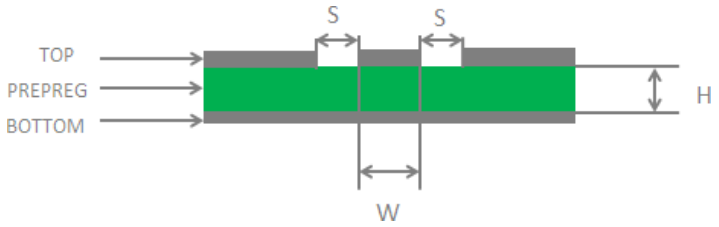


Figure 39: Coplanar Waveguide Design on a 2-layer PCB

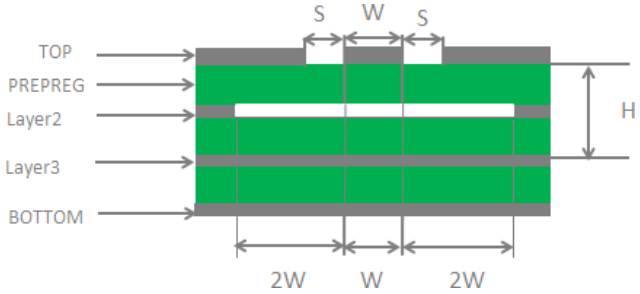


Figure 40: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

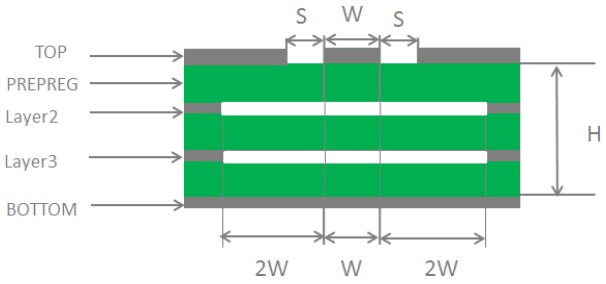


Figure 41: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure better RF performance and reliability, the following conditions should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- Clearance between RF pins and RF connector should be as short as possible, and all right-angle (90°) traces should be changed to the ones with the angle of 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, ground vias around RF traces and the reference ground can improve RF performance. The clearance between ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between any traces on adjacent layers.

For more details about RF layout, see ***document [3]***.

5.4. Requirements for Antenna Design

Table 46: Requirements for Antenna Design

Antenna Type	Requirements
GNSS	**Frequency range:** ● L1: 1559–1609 MHz ● L5: 1166–1187 MHz RHCP or linear polarization VSWR: ≤ 2 (Typ.)
	For passive antenna application:

	Passive antenna gain: > 0 dBi
	For active antenna application: Active antenna noise coefficient: < 1.5 dB Active antenna embedded LNA gain: < 17 dB
UMTS, LTE, 5G NR [7]	VSWR: ≤ 2 Efficiency: > 30 % Gain: > 0 dBi Max input power: 50 W Input impedance: 50 Ω Vertical polarization **Cable insertion loss:** ● < 1 dB: LB (< 1 GHz) ● < 1.5 dB: MB (1–2.3 GHz) ● < 2 dB: HB (> 2.3 GHz)

5.5. RF Connector Recommendation

If the RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT receptacle provided by Hirose.

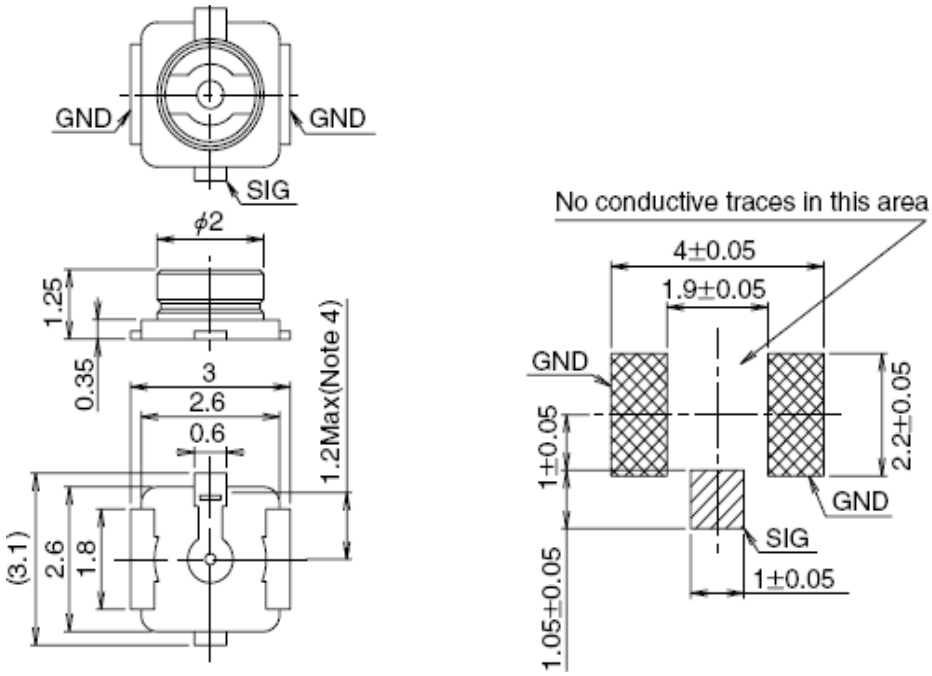


Figure 42: Dimensions of the Receptacle (Unit: mm)

[7] The performance parameters are Quectel recommended and you are advised to confirm these parameters with antenna suppliers and adjust them according to the actual products, test results and certification requirements to ensure the overall wireless performance for your terminals.

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

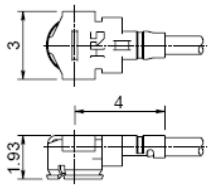
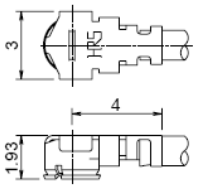
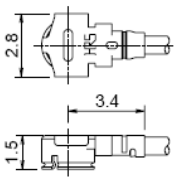
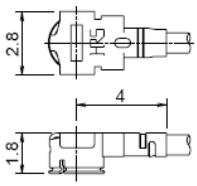
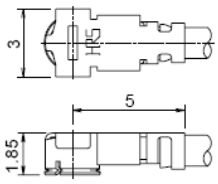
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 43: Specifications of Mated Plugs (Unit: mm)

The following figure describes the space factor of the mated connector.

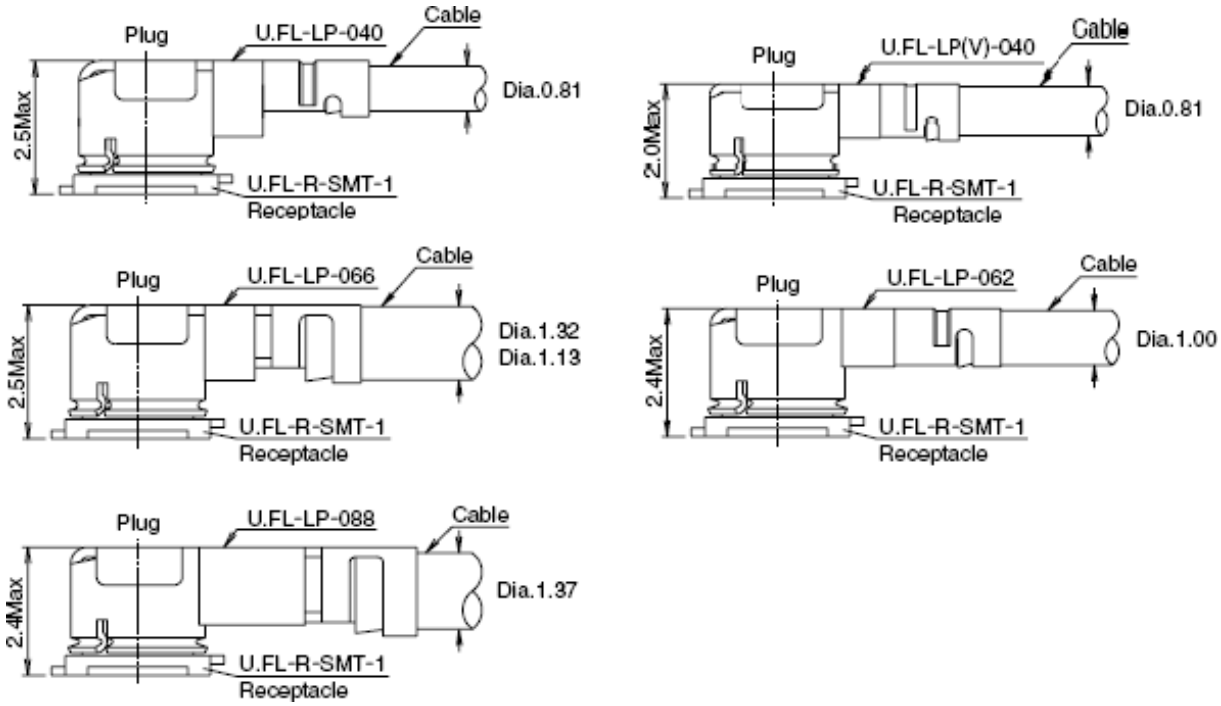


Figure 44: Space Factor of the Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Table 47: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Voltage at VBAT_RF & VBAT_BB	-0.5	5	V
Voltage at USB_VBUS	0	21	V
Voltage at digital pins	-0.5	2.48	V
Voltage at ADC0	-0.5	2.48	V
Voltage at ADC1	-0.5	2.48	V
Voltage at ADC2	-0.5	2.48	V
Voltage at ADC3	-0.5	2.48	V
Voltage at ADC4	-0.5	2.48	V
Voltage at ADC5	-0.5	2.48	V
Voltage at ADC6	-0.5	2.48	V
Current at VBAT_BB	-	TBD	A
Current at VBAT_RF	-	TBD	A

6.2. Power Supply Ratings

Table 48: Module's Power Supply Ratings

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB & VBAT_RF	The actual input voltage must be within this range	3.3	3.8	4.4	V
	Voltage drops during burst transmission	Maximum power control level on n41	-	-	TBD	mV
I_{VBAT}	Peak supply current	Maximum power control level on n41	-	TBD	TBD	A
USB_VBUS	USB connection detection		4.2	5.0	15	V

6.3. Power Consumption

Table 49: RG620T-NA Power Consumption

Mode	Condition	Band/Combination	Typ.	Unit
Turn off	Power off	-	TBD	μA
RF disabled	**AT+CFUN=0** (USB 3.1 disabled)	-	TBD	mA
	AT+CFUN=4 (USB 3.1 disabled)	-	TBD	mA
Sleep mode	SA FDD PF = 64 (USB 3.1 disabled)	-	TBD	mA
	SA TDD PF = 64 (USB 3.1 disabled)	-	TBD	mA
Idle mode	SA PF = 64 (USB 2.0 active)	-	TBD	mA
	SA PF = 64 (USB 3.1 active)	-	TBD	mA
LTE	LTE LB @ 23 dBm	B5	TBD	mA
	LTE MB @ 23 dBm	B2	TBD	mA
	LTE HB @ 23 dBm	B7	TBD	mA

LTE CA	DL 3CA, 256QAM	CA_2A-66A-30A	TBD	mA
	UL 1CA, 256QAM			
	Tx power @ 23 dBm			
5G SA FR1 (1 Tx)	5G NR LB @ 23 dBm	n5	TBD	mA
	5G NR, MB @ 23 dBm	n2	TBD	mA
	5G NR HB @ 23 dBm	n7	TBD	mA
	5G NR UHB @ 26 dBm	n78	TBD	mA
5G SA FR1 (2 Tx)	5G NR UL 2 × 2 MIMO @ 26 dBm	n78	TBD	mA
5G SA FR1 CA	DL 2CA, 256QAM	n78C	TBD	mA
	UL 1CA, 256QAM			
	Tx power @ 26 dBm			
LTE + 5G FR1 EN-DC	LTE DL, 256QAM	DC_2A_n78A	TBD	mA
	LTE UL, QPSK			
	NR DL, 256QAM			
	NR UL, QPSK			
	LTE Tx Power @ 23 dBm			
	NR Tx Power @ 26 dBm			

Table 50: RG620T-EU Power Consumption

Mode	Condition	Band/Combination	Typ.	Unit
Turn off	Power off	-	TBD	μA
RF disabled	**AT+CFUN=0** (USB 3.1 disabled)	-	TBD	mA
	AT+CFUN=4 (USB 3.1 disabled)	-	TBD	mA
Sleep mode	SA FDD PF = 64 (USB 3.1 disabled)	-	TBD	mA

	SA TDD PF = 64 (USB 3.1 disabled)	-	TBD	mA
Idle mode	SA PF = 64 (USB 2.0 active)	-	TBD	mA
	SA PF = 64 (USB 3.1 active)	-	TBD	mA
LTE	LTE LB @ 23 dBm	B5	TBD	mA
	LTE MB @ 23 dBm	B1	TBD	mA
	LTE HB @ 23 dBm	B7	TBD	mA
LTE CA	DL 3CA, 256QAM	CA_1A-3A-7A	TBD	mA
	UL 1CA, 256QAM			
	Tx power @ 23 dBm			
5G SA FR1 (1 Tx)	5G NR LB @ 23 dBm	n5	TBD	mA
	5G NR, MB @ 23 dBm	n1	TBD	mA
	5G NR HB @ 23 dBm	n7	TBD	mA
	5G NR UHB @ 26 dBm	n78	TBD	mA
5G SA FR1 (2 Tx)	5G NR UL 2 × 2 MIMO @ 26 dBm	n78	TBD	mA
5G SA FR1 CA	DL 2CA, 256QAM	n78C	TBD	mA
	UL 1CA, 256QAM			
	Tx power @ 26 dBm			
LTE + 5G FR1 EN-DC	LTE DL, 256QAM	DC_3A_n78A	TBD	mA
	LTE UL, QPSK			
	NR DL, 256QAM			
	NR UL, QPSK			
	LTE Tx Power @ 23 dBm			
	NR Tx Power @ 26 dBm			

NOTE

1. Power consumption test is carried out under 3.8 V, 25 °C with EVB and thermal dissipation measures.
2. The power consumption data above is for reference only, which may vary among different modules. For detailed information, contact Quectel Technical Support for the power consumption test report of the specific module.

6.4. Digital I/O Characteristics

Table 51: VDD_EXT V I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	0.65 × VDD_EXT	VDD_EXT + 0.3
V_{IL}	Low-level input voltage	-0.3	0.35 × VDD_EXT
V_{OH}	High-level output voltage	0.75 × VDD_EXT	-
V_{OL}	Low-level output voltage	-	0.25 × VDD_EXT

Table 52: SDIO I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	0.65 × VDD_EXT	VDD_EXT + 0.3
V_{IL}	Low-level input voltage	-0.3	0.35 × VDD_EXT
V_{OH}	High-level output voltage	VDD_EXT - 0.45	-
V_{OL}	Low-level output voltage	-	VDD_EXT

Table 53: (U)SIM Low-voltage I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	Input high voltage	1.17	-

V_{IL}	Input low voltage	-	0.63
V_{OH}	Output high voltage	1.4	1.9
V_{OL}	Output low voltage	-	0.27

Table 54: (U)SIM High-voltage I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	Input high voltage	1.875	-
V_{IL}	Input low voltage	-	0.75
V_{OH}	Output high voltage	2.7	3.1
V_{OL}	Output low voltage	-	0.4

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 55: ESD Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %; Unit: kV)

Test Point	Contact Discharge	Air Discharge
VBAT & GND	±5	±10
All antenna interfaces	±4	±8
Other interfaces	±0.25	±1

6.6. Operating and Storage Temperatures

Table 56: Operating and Storage Temperatures (Unit: °C)

Parameter	Min.	Typ.	Max.
Normal Operating Temperature [8]	-30	+25	+70
Extended Operating Temperature [9]	-40	+25	+85
Storage Temperature	-40	-	+90

6.7. Thermal Dissipation

The module offers the best performance when all internal IC chips are working within their operating temperatures. When the IC chip reaches or exceeds the maximum junction temperature, the module may still work but the performance and functions (such as RF output power, data rate, etc.) will be affected to a certain extent. Therefore, the thermal design should be maximally optimized to ensure all internal IC chips always work within the recommended operating temperature range. The following principles for thermal consideration are provided for reference:

- Keep the module away from heat sources on your PCB, especially high-power components such as processor, power amplifier, and power supply.
- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Follow the principles below when the heatsink is necessary:
  - Do not place large size components in the area where the module is mounted on your PCB to reserve enough place for heatsink installation.
  - Attach the heatsink to the shielding cover of the module; In general, the base plate area of the heatsink should be larger than the module area to cover the module completely;
  - Choose the heatsink with adequate fins to dissipate heat;
  - Choose a TIM (Thermal Interface Material) with high thermal conductivity, good softness and good wettability and place it between the heatsink and the module;
  - Fasten the heatsink with four screws to ensure that it is in close contact with the module to prevent the heatsink from falling off during the drop, vibration test, or transportation.

[8] To meet this operating temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module's related indicators can meet 3GPP specifications.

[9] To meet this extended temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module remains the ability to establish and maintain functions such as voice, SMS, emergency call, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module's related indicators will meet 3GPP specifications again.

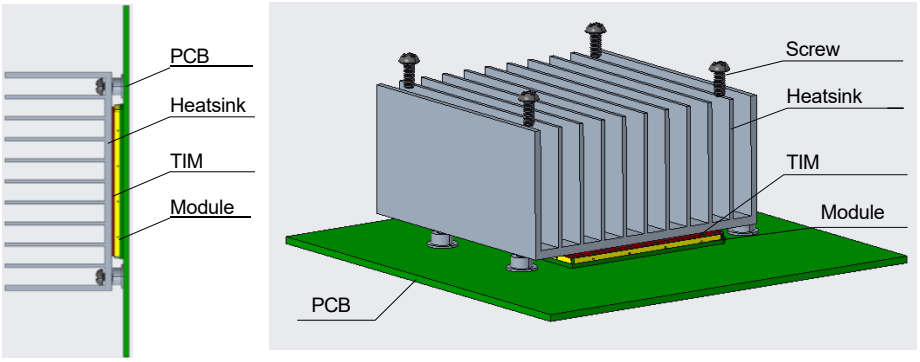


Figure 45: Placement and Fixing of the Heatsink

Table 57: Recommended Junction Operating Temperature Range for Main Chips (Unit: °C)

BB	PMU	APT	MCP	WTR	PA-1	PA-2
-20 to +105	-30 to +125	-20 to +125	-25 to +85	-20 to +115	-20 to +85	-20 to +85

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

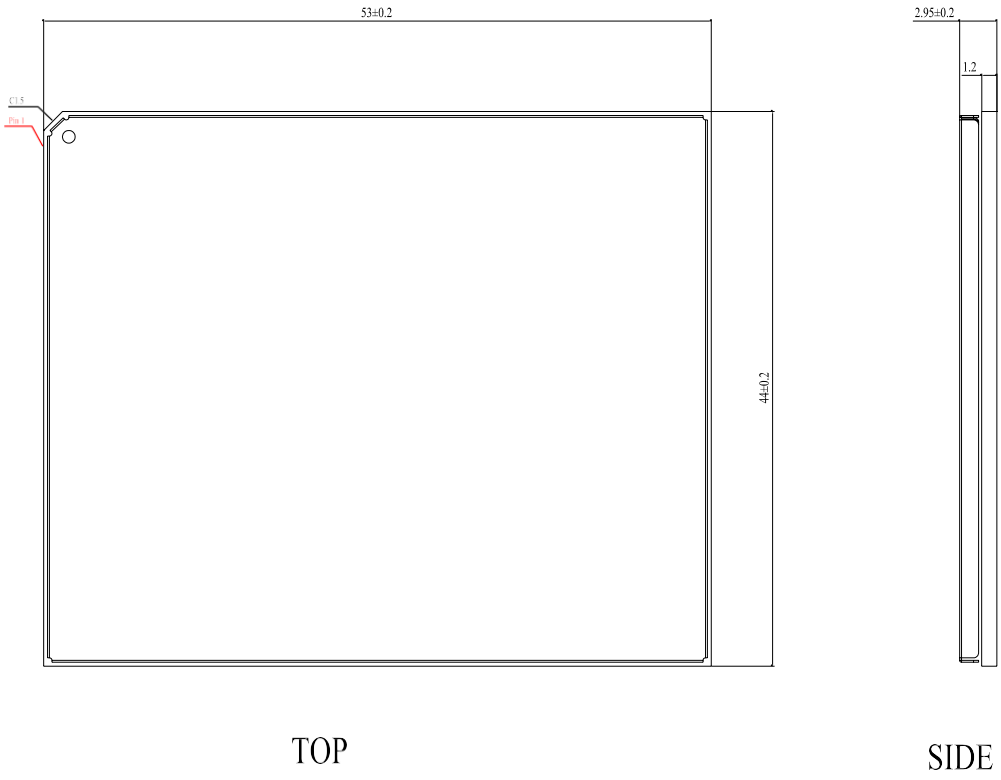


Figure 46: Top and Side Dimensions

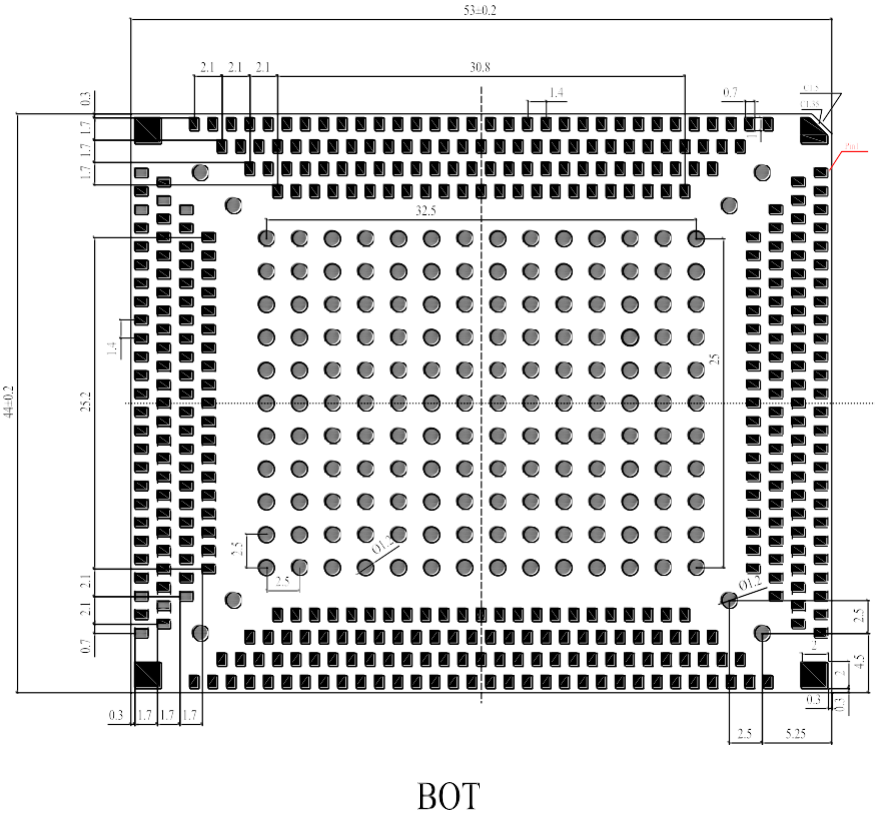


Figure 47: Bottom Dimensions

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

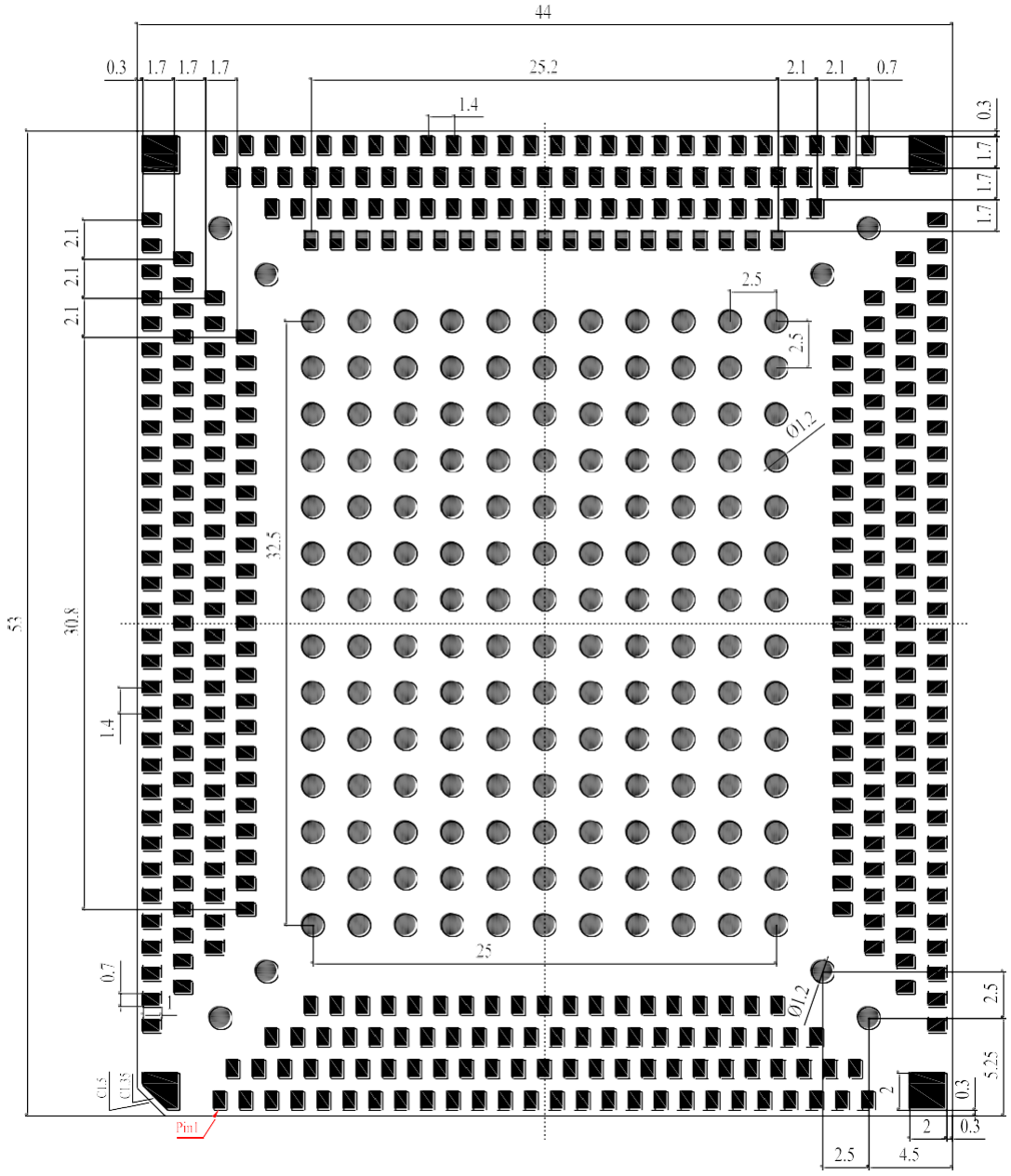


Figure 48: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

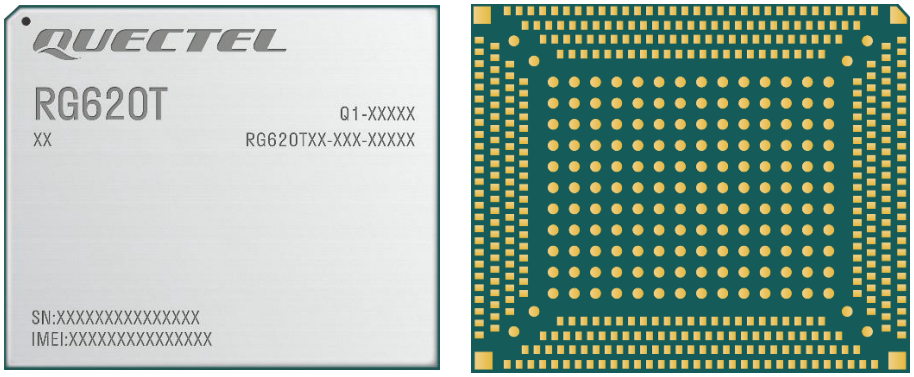


Figure 49: Top & Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [10] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[10] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18mm. For more details, see ***document [4]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below:

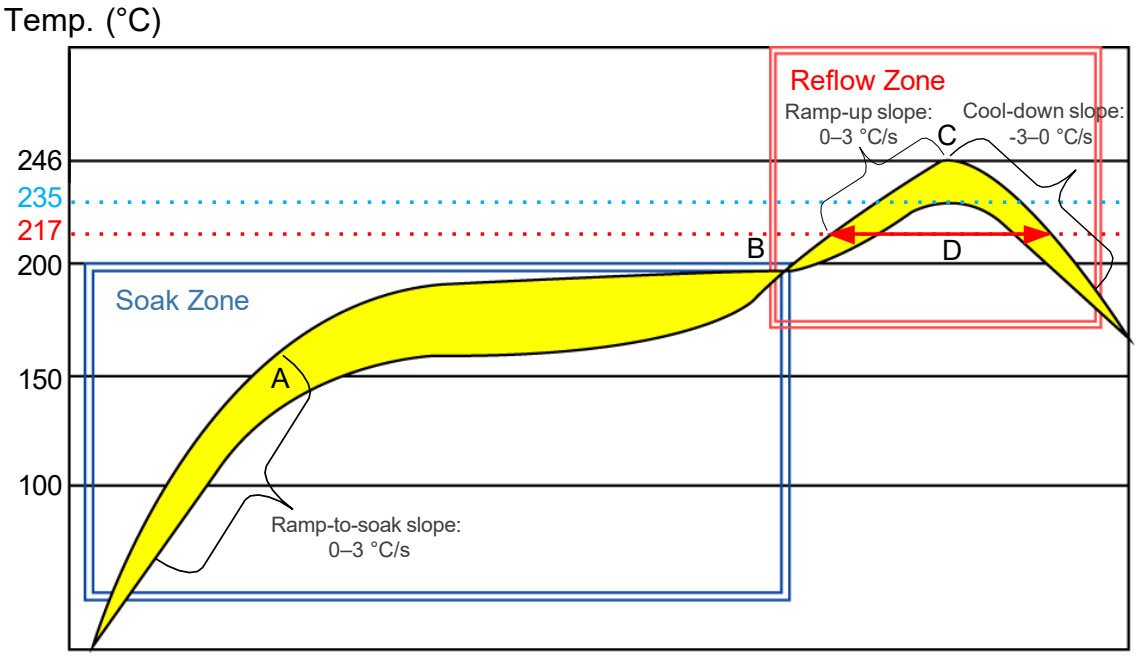


Figure 50: Recommended Reflow Soldering Thermal Profile

Table 58: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. If a conformal coating is necessary for the module, do not use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
3. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
4. Due to the complexity of the SMT process, contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective wave soldering, ultrasonic soldering) that is not mentioned in ***document [4]***.

8.3. Packaging Specification

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

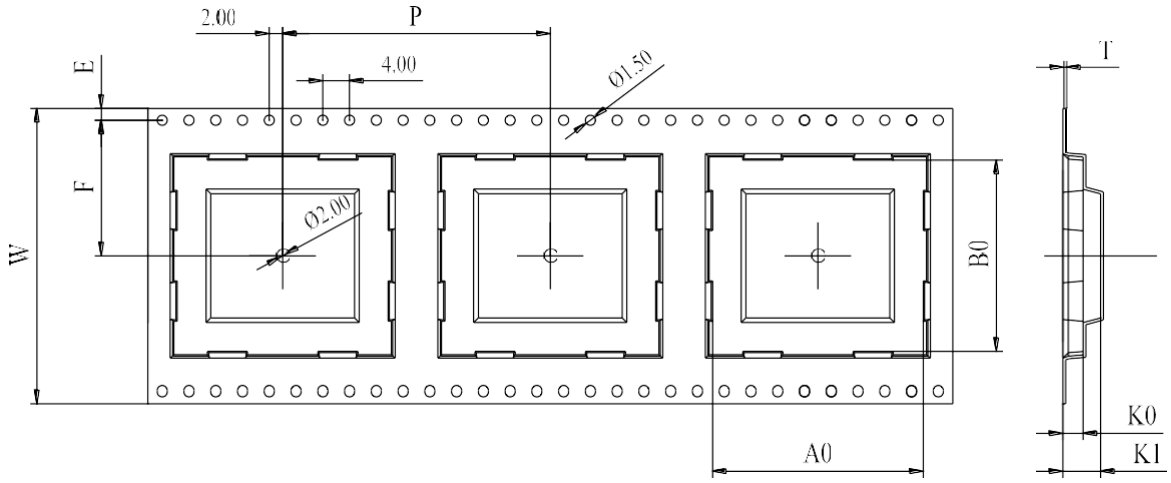


Figure 51: Carrier Tape Dimension Drawing

Table 59: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
72	72	0.5	53.6	44.6	4.25	7.6	34.2	1.75

8.3.2. Plastic Reel

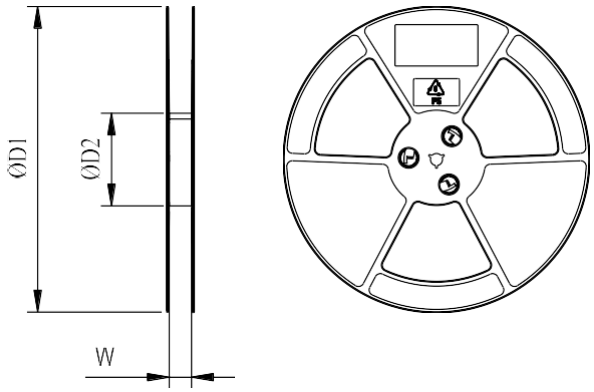


Figure 52: Plastic Reel Dimension Drawing

Table 60: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
380	180	72.5

8.3.3. Mounting Direction

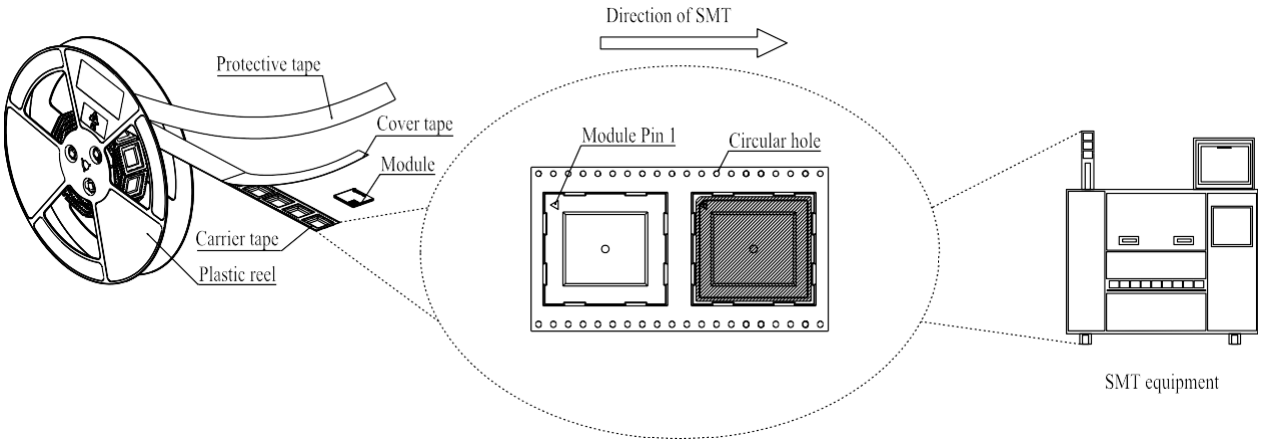
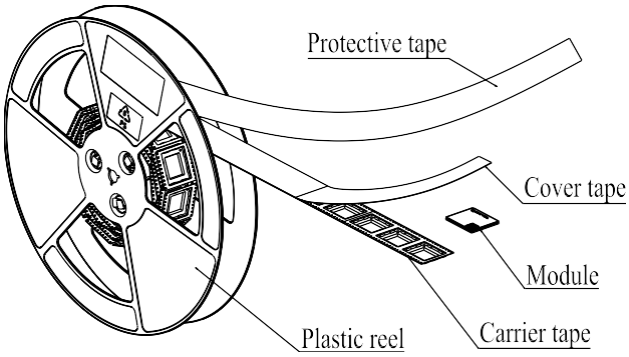


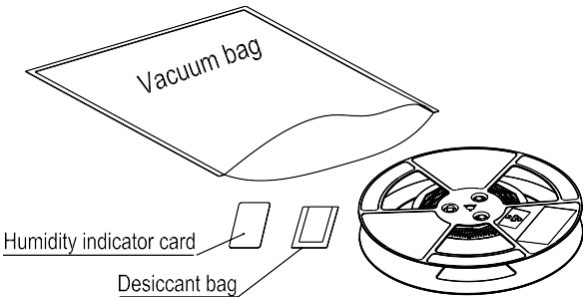
Figure 53: Mounting Direction

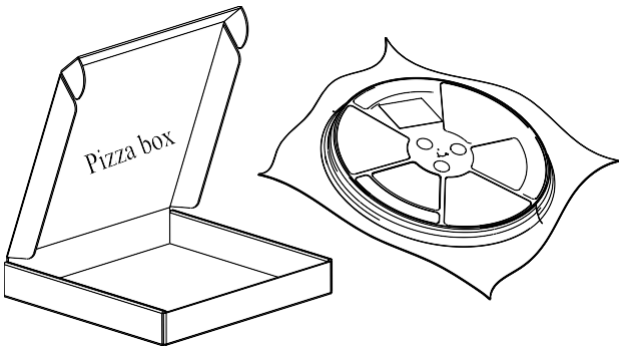
8.3.4. Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 100 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 carton box and seal it. 1 carton box can pack 400 modules.

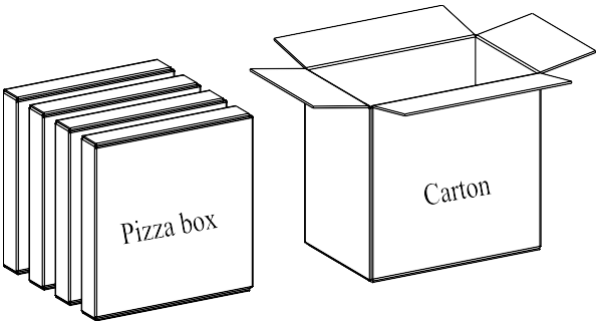


Figure 54: Packaging Process

9 Related AT Commands

9.1. AT+CFUN Set UE Functionality

This command controls the functionality level. It can also be used to reset the UE.

- **AT+CFUN=0** turns off radio and (U)SIM power.
- **AT+CFUN=1,1** or **AT+CFUN=4,1** can reset the UE.
- **AT+CFUN=1** enters full functionality mode.
- **AT+CFUN=4** enters airplane mode.

AT+CFUN Set UE Functionality	
Test Command **AT+CFUN=?**	Response **+CFUN: (**list of supported **<fun>**s**),(**list of supported **<rst>**s**)** **OK**
Read Command **AT+CFUN?**	Response **+CFUN: <fun>** **OK**
Write Command **AT+CFUN=<fun>[,<rst>]**	Response **OK** If there is any error related to MT functionality: **+CME ERROR: <err>** Or **ERROR**
Maximum Response Time	15 s, determined by the network.
Characteristics	/
Reference	*3GPP TS 27.007*

Parameter

<fun>	Integer type. Functionality level.	
	0	Minimum functionality (Disable RF function and (U)SIM function)
	1	Full functionality
	4	Airplane mode (Disable RF function)
	15	Reboot the modem and AP synchronously
<rst>	Integer type.	
	0	Do not reset the UE before setting it to **<fun>** power level (Default value when **<rst>** is omitted)
	1	Reset the UE before setting it to **<fun>** power level
<err>	Error code.	

Example

```
AT+CFUN=0                    //Switch UE to minimum functionality.
OK
AT+CFUN=1                    //Switch UE to full functionality.
OK
```

NOTE

1. **AT+CFUN=1,1** or **AT+CFUN=4,1** can only reset the UE, which is not fully compliable with *3GPP TS 27.007*.
2. The execution of **AT+CFUN** command will not affect GNSS function.

9.2. AT+QSCLK Enable/Disable Sleep Mode

This command controls whether MT enters sleep mode. When entering into sleep mode is enabled, the MT can directly enter sleep mode.

AT+QSCLK Enable/Disable Sleep Mode	
Test Command **AT+QSCLK=?**	Response **+QSCLK: (**list of supported **<n>**s**)** **OK**
Read Command **AT+QSCLK?**	Response **+QSCLK: <n>** **OK**
Write Command	Response

AT+QSCLK=<n>	OK
Maximum Response Time	300 ms
Characteristics	/

Parameter

<n>	Integer type. Enable/disable sleep mode. 0 Disable 1 Enable

NOTE

1. **AT+QSCLK=1** enables the module to enter sleep mode. At this time, the USB is powered down and the module's modem part enters airplane mode.
2. **AT+QSCLK=0** disables the module to enter sleep mode. At this time, the USB is powered up and the module's modem part is in normal operating mode. Under such condition, the module will never go into sleep mode.

9.3. AT+QADC Read ADC Value

This command reads the voltage value of specified ADC channel.

AT+QADC Read ADC Value	
Test Command **AT+QADC=?**	Response **+QADC: (**range of supported **<port>**s**)** **OK**
Read Command **AT+QADC=<port>**	Response **+QADC: <status>,<value>** **OK**
Maximum Response Time	300 ms
Characteristics	/

Parameter

<port>	Integer type. Channel number of the ADC. 0 ADC channel 0 1 ADC channel 1 2 ADC channel 2
<status>	Integer type. Indicates whether the ADC value read is successful. 0 Failed 1 Successful
<value>	Integer type. The voltage of specified ADC channel. Unit: mV.

10 Appendix A References

Table 61: Related Documents

Document Name
[1] Quectel_RG500L_EVB_User_Guide
[2] Quectel_RG620T_Series_Quecopen_GNSS_Application_Note
[3] Quectel_RF_Layout_Application_Note
[4] Quectel_Module_Secondary_SMT_Application_Note
[5] Quectel_RG620T_Series_QuecOpen_GPIO_Configuration

Table 62: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AP	Application Processor
bps	Bits Per Second
BPSK	Binary Phase Shift Keying
BW	Bandwidth
CA	Carrier Aggregation
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear to Send
DAI	Digital Audio Interface
DCE	Data Communications Equipment

DC-HSDPA	Dual-carrier High Speed Downlink Packet Access
DFOTA	Delta Firmware Upgrade Over-The-Air
DL	Downlink
DRX	Discontinuous Reception
DRX	Diversity Receive
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate
GLONASS	Global Navigation Satellite System (Russia)
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GRFC	General RF Control
HB	High Band
HPUE	High Power User Equipment
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
IC	Integrated Circuit
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
I/O	Input/Output
Inom	Normal Current

LAA	License Assisted Access
LB	Low Band
LED	Light Emitting Diode
LGA	Land Grid Array
LMHB	Low/Middle/High Band
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MAC	Media Access Control
MB	Middle Band
MCU	Microcontroller Unit
MDC	Management Data Clock
MDIO	Management Data Input/Output
MHB	Middle/High Band
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MT	Mobile Terminated
NR	New Radio
NSA	Non-Stand Alone
PA	Power Amplifier
PAP	Password Authentication Protocol
PC	Personal Computer
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
PDA	Personal Digital Assistant

PDU	Protocol Data Unit
PHY	Physical Layer
PMIC	Power Management Integrated Circuit
PRX	Primary Receive
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RI	Ring Indicator
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SA	Stand Alone
SCS	Sub-Carrier Space
SD	Secure Digital
SIMO	Single Input Multiple Output
SMD	Surface Mount Device
SMS	Short Message Service
SPI	Serial Peripheral Interface
STB	Set Top Box
TDD	Time Division Duplexing
TDMA	Time Division Multiple Access
TRX	Transmit & Receive
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UHB	Ultra High Band

UL	Uplink
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
USXGMII	The Universal Serial 10 Gigabit Media Independent Interface
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
V_{I}max	Absolute Maximum Input Voltage
V_{I}min	Absolute Minimum Input Voltage
V_{OH}max	Maximum High-level Output Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
V_{OL}min	Minimum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
WWAN	Wireless Wide Area Network

11 Appendix B Operating Frequency

Table 63: Operating Frequencies (5G)

5G	Duplex Mode	Uplink Operating Band	Downlink Operating Band	Unit
n1	FDD	1920–1980	2110–2170	MHz
n2	FDD	1850–1910	1930–1990	MHz
n3	FDD	1710–1785	1805–1880	MHz
n5	FDD	824–849	869–894	MHz
n7	FDD	2500–2570	2620–2690	MHz
n8	FDD	880–915	925–960	MHz
n12	FDD	699–716	729–746	MHz
n13	FDD	777–787	746–756	MHz
n14	FDD	788–798	758–768	MHz
n18	FDD	815–830	860–875	MHz
n20	FDD	832–862	791–821	MHz
n24	FDD	1626.5–1660.5	1525–1559	MHz
n25	FDD	1850–1915	1930–1995	MHz
n26	FDD	814–849	859–894	MHz
n28	FDD	703–748	758–803	MHz
n29	SDL	-	717–728	MHz
n30	FDD	2305–2315	2350–2360	MHz
n34	TDD	2010–2025	2010–2025	MHz
n38	TDD	2570–2620	2570–2620	MHz

n39	TDD	1880–1920	1880–1920	MHz
n40	TDD	2300–2400	2300–2400	MHz
n41	TDD	2496–2690	2496–2690	MHz
n46	TDD	5150–5925	5150–5925	MHz
n47	TDD	5855–5925	5855–5925	MHz
n48	TDD	3550–3700	3550–3700	MHz
n50	TDD	1432–1517	1432–1517	MHz
n51	TDD	1427–1432	1427–1432	MHz
n53	TDD	2483.5–2495	2483.5–2495	MHz
n65	FDD	1920–2010	2110–2200	MHz
n66	FDD	1710–1780	2110–2200	MHz
n67	SDL	-	738–758	MHz
n70	FDD	1695–1710	1995–2020	MHz
n71	FDD	663–698	617–652	MHz
n74	FDD	1427–1470	1475–1518	MHz
n75	SDL	-	1432–1517	MHz
n76	SDL	-	1427–1432	MHz
n77	TDD	3300–4200	3300–4200	MHz
n78	TDD	3300–3800	3300–3800	MHz
n79	TDD	4400–5000	4400–5000	MHz
n80	SUL	1710–1785	-	MHz
n81	SUL	880–915	-	MHz
n82	SUL	832–862	-	MHz
n83	SUL	703–748	-	MHz
n84	SUL	1920–1980	-	MHz
n85	FDD	698–716	728–746	MHz

n86	SUL	1710–1780	-	MHz
n89	SUL	824–849	-	MHz
n90	TDD	2496–2690	2496–2690	MHz
n91	FDD	832–862	1427–1432	MHz
n92	FDD	832–862	1432–1517	MHz
n93	FDD	880–915	1427–1432	MHz
n94	FDD	880–915	1432–1517	MHz
n95	SUL	2010–2025	-	MHz
n96	TDD	5925–7125	5925–7125	MHz
n97	SUL	2300–2400	-	MHz
n98	SUL	1880–1920	-	MHz
n99	SUL	1626.5–1660.5	-	MHz
n257	-	26.50–29.50	26.50–29.50	GHz
n258	-	24.25–27.50	24.25–27.50	GHz
n260	-	37.00–40.00	37.00–40.00	GHz
n261	-	27.50–28.35	27.50–28.35	GHz

Table 64: Operating Frequencies (2G + 3G + 4G; Unit: MHz)

2G	3G	4G	Duplex Mode	Uplink Operating Band	Downlink Operating Band
-	B1	B1	FDD	1920–1980	2110–2170
PCS1900	B2/BC1	B2	FDD	1850–1910	1930–1990
DCS1800	B3	B3	FDD	1710–1785	1805–1880
-	B4	B4	FDD	1710–1755	2110–2155
GSM850	B5/BC0	B5	FDD	824–849	869–894
-	B6	-	FDD	830–840	875–885
-	B7	B7	FDD	2500–2570	2620–2690

EGSM900	B8	B8	FDD	880–915	925–960
-	B9	B9	FDD	1749.9–1784.9	1844.9–1879.9
-	B10	B10	FDD	1710–1770	2110–2170
-	B11	B11	FDD	1427.9–1447.9	1475.9–1495.9
-	B12	B12	FDD	699–716	729–746
-	B13	B13	FDD	777–787	746–756
-	B14	B14	FDD	788–798	758–768
-	-	B17	FDD	704–716	734–746
-	-	B18	FDD	815–830	860–875
-	B19	B19	FDD	830–845	875–890
-	B20	B20	FDD	832–862	791–821
-	B21	B21	FDD	1447.9–1462.9	1495.9–1510.9
-	B22	B22	FDD	3410–3490	3510–3590
-	-	B24	FDD	1626.5–1660.5	1525–1559
-	B25	B25	FDD	1850–1915	1930–1995
-	B26	B26	FDD	814–849	859–894
-	-	B27	FDD	807–824	852–869
-	-	B28	FDD	703–748	758–803
-	-	B29	FDD [11]	-	717–728
-	-	B30	FDD	2305–2315	2350–2360
-	-	B31	FDD	452.5–457.5	462.5–467.5
-	-	B32	FDD [11]	-	1452–1496
-	B33	B33	TDD	1900–1920	1900–1920
-	B34	B34	TDD	2010–2025	2010–2025
-	B35	B35	TDD	1850–1910	1850–1910

[11] Restricted to E-UTRA operation when carrier aggregation is configured. The downlink operating band is paired with the uplink operating band (external) of the carrier aggregation configuration that is supporting the configured Pcell.

-	B36	B36	TDD	1930–1990	1930–1990
	B37	B37	TDD	1910–1930	1910–1930
-	B38	B38	TDD	2570–2620	2570–2620
-	B39	B39	TDD	1880–1920	1880–1920
-	B40	B40	TDD	2300–2400	2300–2400
-	-	B41	TDD	2496–2690	2496–2690
-	-	B42	TDD	3400–3600	3400–3600
-	-	B43	TDD	3600–3800	3600–3800
-	-	B44	TDD	703–803	703–803
-	-	B45	TDD	1447–1467	1447–1467
-	-	B46	TDD	5150–5925	5150–5925
-	-	B47	TDD	5855–5925	5855–5925
-	-	B48	TDD	3550–3700	3550–3700
-	-	B50	TDD	1432–1517	1432–1517
-	-	B51	TDD	1427–1432	1427–1432
-	-	B52	TDD	3300–3400	3300–3400
-	-	B65	FDD	1920–2010	2110–2200
-	-	B66	FDD	1710–1780	2110–2200 [12]
-	-	B67	FDD [11]	-	738–758
-	-	B68	FDD	698–728	753–783
-	-	B69	FDD [11]	-	2570–2620
-	-	B70	FDD [13]	1695–1710	1995–2020
-	-	B71	FDD	663–698	617–652
-	-	B72	FDD	451–456	461–466

[12] The range 2180–2200 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured.
[13] The range 2010–2020 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured and TX-RX separation is 300 MHz. The range 2005–2020 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured and TX-RX separation is 295 MHz.

-	-	B73	FDD	450–455	460–465
-	-	B74	FDD	1427–1470	1475–1518
-	-	B75	FDD [11]	-	1432–1517
-	-	B76	FDD [11]	-	1427–1432
-	-	B85	FDD	698–716	728–746
-	-	B87	FDD	410–415	420–425
-	-	B88	FDD	412–417	422–427

Product Marketing Name:Quectel RG620T-NA

FCC Certification Requirements.

According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.

And the following conditions must be met:

1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based timeaveraging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.
2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.
3. A label with the following statements must be attached to the host end product: This device contains FCC ID: XMR2023RG620TNA
4. To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

radiation, maximum antenna gain (including cable loss) must not exceed: Operating Band	FCC Max Antenna Gain（dBi）
LTE Band 2/N2	8.00
LTE Band 4	5.00
LTE Band 5/LTE CA_5B	9.41
LTE Band 7/LTE CA_7C/N7	8.00
LTE Band 12	8.70
LTE Band 13	9.16
LTE Band 14/N14	9.23
LTE Band 17	8.74
LTE Band 25/N25	8.00
LTE Band 26(814-824)	9.36
LTE Band 26(824-849)	9.41
LTE Band 30/N30	-1.02
LTE Band 38/LTE CA_38C/N38/N38 MIMO	5.00
LTE Band 41/LTE CA_41C/N41/N41MIMO	5.00
LTE Band 42(3450-3550) /LTE CA_42C	5.00
LTE Band 42(3550-3600) /LTE CA_42C	5.00
LTE Band 43(3600-3700)	5.00
LTE Band 43(3700-3800)	5.00
LTE Band 48/LTE CA_48C/N48	-2.00
LTE Band 66/LTE CA_66B/LTE CA_66C/N66	5.00
LTE Band71/N71	8.48
NR Band n5	9.42
NR Band n12	8.71
NR Band n13	8.99
NR Band n26(814-824)	9.37
NR Band n26(824-849)	9.42
NR Band n48(MIMO)	-4.00
NR Band n70	5.00
NR Band n77 (3450-3550)	2.00
NR Band n77 (3450-3550)(MIMO)	2.00
NR Band n77 (3550-3700)	-4.00
NR Band n77 (3550-3700)(MIMO)	-4.00
NR Band n77 (3700-3980)	2.00

NR Band n77 (3700-3980)(MIMO)	2.00
NR Band n78 (3450-3550)	2.00
NR Band n78 (3450-3550)(MIMO)	2.00
NR Band n78 (3550-3700)	-4.00
NR Band n78 (3550-3700)(MIMO)	-4.00
NR Band n78 (3700-3800)	2.00
NR Band n78 (3700-3800)(MIMO)	2.00

5. This module must not transmit simultaneously with any other antenna or transmitter
6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.
For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093
If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.
For this device, OEM integrators must be provided with labeling instructions of finished products.
Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:
A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2

Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module FCC ID: XMR2023RG620TNA" or "Contains FCC ID: XMR2023RG620TNA" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Supplier's Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

IC Statement

IRSS-GEN

"This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device." or "Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

1) l'appareil ne doit pas produire de brouillage; 2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Déclaration sur l'exposition aux rayonnements RF

L'autre utilisé pour l'émetteur doit être installé pour fournir une distance de séparation d'au moins 20 cm

de toutes les personnes et ne doit pas être colocalisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.
The host product shall be properly labeled to identify the modules within the host product.
The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word “Contains” or similar wording expressing the same meaning, as follows: “Contains IC: 10224A-023RG620TNA” or “where: 10224A-023RG620TNA is the module’s certification number”.
Le produit hôte doit être correctement étiqueté pour identifier les modules dans le produit hôte.
L'étiquette de certification d'Innovation, Sciences et Développement économique Canada d'un module doit être clairement visible en tout temps lorsqu'il est installédans le produit hôte; sinon, le produit hôte doit porter une étiquette indiquant le numéro de certification d'Innovation, Sciences et Développement économique Canada pour le module, précédé du mot «Contient» ou d'un libellé semblable exprimant la même signification, comme suit:
"Contient IC: 10224A-023RG620TNA " ou "où: 10224A-023RG620TNA est le numéro de certification du module".