SG865W Series

Hardware Design

Smart Module Series

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Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

Or our local offices. For more information, please visit:
http://www.quectel.com/support/sales.htm.

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

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-	2022-04-30	Glenn GE/ Joshua PAN	Creation of the document
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1 Introduction

This document defines SG865W series module and describes its air interfaces and hardware interfaces which are connected with your applications.

It can help you quickly understand interface specifications, electrical and mechanical details as well as other related information of the module. Associated with application notes and user guides, you can use this module to design and to set up mobile applications easily.
changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.
If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
-- Reorient or relocate the receiving antenna.
-- Increase the separation between the equipment and receiver.
-- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
-- Consult the dealer or an experienced radio/TV technician for help.

This device complies with FCC radiation exposure limits set forth for an uncontrolled environment. In order to avoid the possibility of exceeding the FCC radio frequency exposure limits, human proximity to the antenna shall not be less than 20cm (8 inches) during normal operation.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations

4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part

15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).

The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Quectel Wireless Solutions Co., Ltd that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: XMR2022SG865WWF”

The FCC ID can be used only when all FCC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,

(2) The transmitter module may not be co-located with any other transmitter or antenna.

(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

(4) The max allowed antenna gain is 0dBi for external antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This device complies with ISED’s licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Le présent appareil est conforme aux CNR d' ISED applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) le dispositif ne doit pas produire de brouillage préjudiciable, et (2) ce dispositif doit accepter tout brouillage reçu, y compris un brouillage susceptible de provoquer un fonctionnement indésirable.

Radiation Exposure Statement:
This equipment complies with ISED radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

Déclaration d'exposition aux radiations:
Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)
1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:
In the event that these conditions can not be met (for example certain laptop configurations or co- location with another transmitter), then the Canada authorization is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:
Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances,

l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 10224A-2022SG865W”.

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 10224A-2022SG865W ".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.

Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

RSS-247 Section 6.4 (5) (6) (for local area network devices, 5GHz)

The device could automatically discontinue transmission in case of absence of information to transmit, or operational failure. Note that this is not intended to prohibit transmission of control or signaling information or the use of repetitive codes where required by the technology.

Caution:

i) The device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems;

ii) where applicable, antenna type(s), antenna models(s), and worst-case tilt angle(s) necessary to remain compliant with the e.i.r.p. elevation mask requirement set forth in section 6.2.2.3 shall be clearly indicated.

L'appareil peut interrompre automatiquement la transmission en cas d'absence d'informations à transmettre ou de panne opérationnelle. Notez que ceci n'est pas destiné à interdire la transmission d'informations de contrôle ou de signalisation ou l'utilisation de codes répétitifs lorsque cela est requis par la technologie.

Avertissement:

i) Le dispositif utilisé dans la bande 5150-5250 MHz est réservé à une utilisation en intérieur afin de réduire le risque de brouillage préjudiciable aux systèmes mobiles par satellite dans le même canal;

ii) lorsqu’il y a lieu, les types d’antennes (s’il y en a plusieurs), les numéros de modèle de l’antenne et les pires angles

d’inclinaison nécessaires pour rester conforme à l’exigence de la
p.i.r.e. applicable au masque d’élévation, énoncée à la section 6.2.2.3, doivent être clairement indiqués.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SD_DATA[0:3] refers to all four SDIO pins: SD_DATA0, SD_DATA1, SD_DATA2, and SD_DATA3.

2 Product Overview

SG865W series is a series of smart modules based on Android operating system, and provides industrial grade performance. Its general features are listed below:

- Supports built-in high performance Kryo™ 585 CPU, Adreno™ 650 GPU, Adreno 995 DPU, Adreno 665 VPU, Hexagon™ DSP, and Spectra™ 480 ISP
- Provides multiple audio and video input/output interfaces as well as abundant GPIO interfaces.
- Supports multiple video codecs

The module is engineered to meet the demanding requirements in high computing power, AI and multimedia functions. Its general features are listed below:

Table 2: Brief Introduction of the Module

Categories	
Packaging and pins number	LGA; 571
Dimensions	46.0 × 42.0 × 2.95 mm
Weight	14 g
Wi-Fi & Bluetooth functions	● 2.4 GHz, 5 GHz ● BLE 5.1 (BR/EDR + BLE)
Variants	SG865W-WF, SG865W-AP [1]

[1] Compared to SG865W-WF, SG865W-AP does not support Wi-Fi and Bluetooth function.

2.1. Frequency Bands and Functions

Table 3: Wireless Network Type of the Module

Mode	Frequency Bands
Wi-Fi 802.11a/b/g/n/ac/ax	2402–2482 MHz 5170–5835 MHz
BLE 5.1 (BR/EDR + BLE)	2402–2480 MHz

2.2. Key Features

Table 4: Key Features

Features	Details
Application Processors	● 64-bit applications processor (Kryo 585) with 4 MB L3 cache ● 1 × Kryo 585 Gold prime core with a 512 KB L2 cache, Fmax at 2.842 GHz ● 3 × Kryo 585 Gold cores with 256 KB L2 cache per core, Fmax at 2.419 GHz ● 4 × low-power Kryo 585 Silver cores with 128 KB L2 cache per core, Fmax at 1.805 GHz
DSP	Hexagon™ DSP with 4 Hexagon Vector eXtensions (HVX) processor
GPU	● Adreno™ 650
Memory	● 64 GB UFS + 8 GB LPDDR5 (default) ● 256 GB UFS + 12GB LPDDR5 (optional)
Operating System	● Android 10
Power Supply	● Supply voltage: 3.55–4.4 V ● Typical supply voltage: 3.8 V
LCM Interfaces	● Supports 2 groups of 4-lane MIPI DSI, up to 2.5 Gbps/lane
Camera Interfaces	● Support 6 groups of 4-lane MIPI CSI, up to 2.5 Gbps/lane ● Support 7 concurrent camera usages ● Max. 64 MP @ 30 fps ZSL @ 2 × ISP
Video Codec	● Adreno 665 VPU ● Video decode up to 4K @ 240 fps; 8K @ 60 fps ● Video encode up to 4K @ 120 fps; 8K @ 30 fps

Audio Interfaces	● Digital MIC ● SWR ● MI2S ● TDM/PCM
SPI Interfaces	● 5 × SPI interfaces, only supports master mode ● 1.8 V operating voltage with clock rates up to 50 MHz
I2C Interfaces	● Supports up to 9 × I2C interfaces 4 × I2C interfaces dedicated for the camera control interface 1 × I2C interface dedicated for communication with the sensors 2 × I2C interfaces for TP interface 1 × I2C interface for NFC interface 1 × I2C interface for general purpose interface ● Multi-master mode is not supported
ADC Interfaces	4 × General purpose ADC interfaces
Vibrator Drive Interface	1 × Drive ERM/LRA vibrator
I2S Interfaces	3 × I2S interfaces
Flashlight Interfaces	3 × High-current Flash LED drivers, which support both flash and torch modes ● Up to 1.5 A for LED1 and LED2 in flash mode ● Up to 0.75 A for LED3 in flash mode
Wireless Charging Interface	Used for battery voltage detection, fuel gauge, battery temperature detection
Real Time Clock	Supported
USB Interfaces	2 × USB interfaces ● Compliant with USB 2.0 and 3.1 Gen 2 specifications, with transmission rates up to 480 Mbps on USB 2.0 and 10 Gbps on USB 3.1 Gen 2 ● USB0 is used for data transmission, software debugging, firmware upgrade ● USB0 supports DisplayPort V1.4 over Type-C ● USB0 supports USB OTG function ● USB1 supports host mode only ● USB1 supports USB hub expansion
PCIe Interfaces	2 × 2-lane PCIe Gen 3
SDIO Interface	● Supports SD 3.0 protocol ● Supports SD card hot-plug ● Supports 1.8 V or 2.95 V SD card
UART Interfaces	4 × UART interfaces: UART5, UART16, UART17 and debug UART ● **UART5/UART16/UART17:** − Four-wire UART interface − Supports RTS and CTS hardware flow control ● **Debug UART:**

	– Two-wire UART interface – Used for debugging by default – Baud rate: 115200 bps by default
Bluetooth Features (SG865W-WF only)	● BLE 5.1
Antenna Interfaces	● ANT1 ● ANT2 ● ANT_BT* 50 Ω impedance
Wi-Fi Features (SG865W-WF only)	● 2.4 GHz and 5 GHz ● Supports 802.11a/b/g/n/ac/ax (20/40/80 MHz), up to 1774.5 Mbps (2 × 2 + 2 × 2 11ax DBS) ● Supports MIMO and DBS ● Supports AP and STA modes
Temperature Range	● Operating temperature range [2]: -35 to +75 °C ● Storage temperature range: -40 to +90 °C
Firmware Upgrade	● Use USB interface or OTA to upgrade
RoHS	● All hardware components are fully compliant with EU RoHS directive

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- LPDDR5 + UFS flash
- Radio frequency
- Peripheral interfaces
  -- USB interfaces
  -- UART interfaces
  -- SD card interface
  -- GPIOs
  -- I2C interfaces
  -- ADC interfaces
  -- PCIe interfaces
  -- Vibrator Drive interface
  -- Wireless Charging interface
  -- RGB interfaces
  -- Keypad interfaces

[2] Within operating temperature range, the module is IEEE compliant.

-- LCM interfaces
-- Touch panel interfaces
-- Camera interfaces
-- Sensor interfaces
-- Audio interfaces
-- I2S interfaces
-- SPI interfaces
-- Emergency Download interface

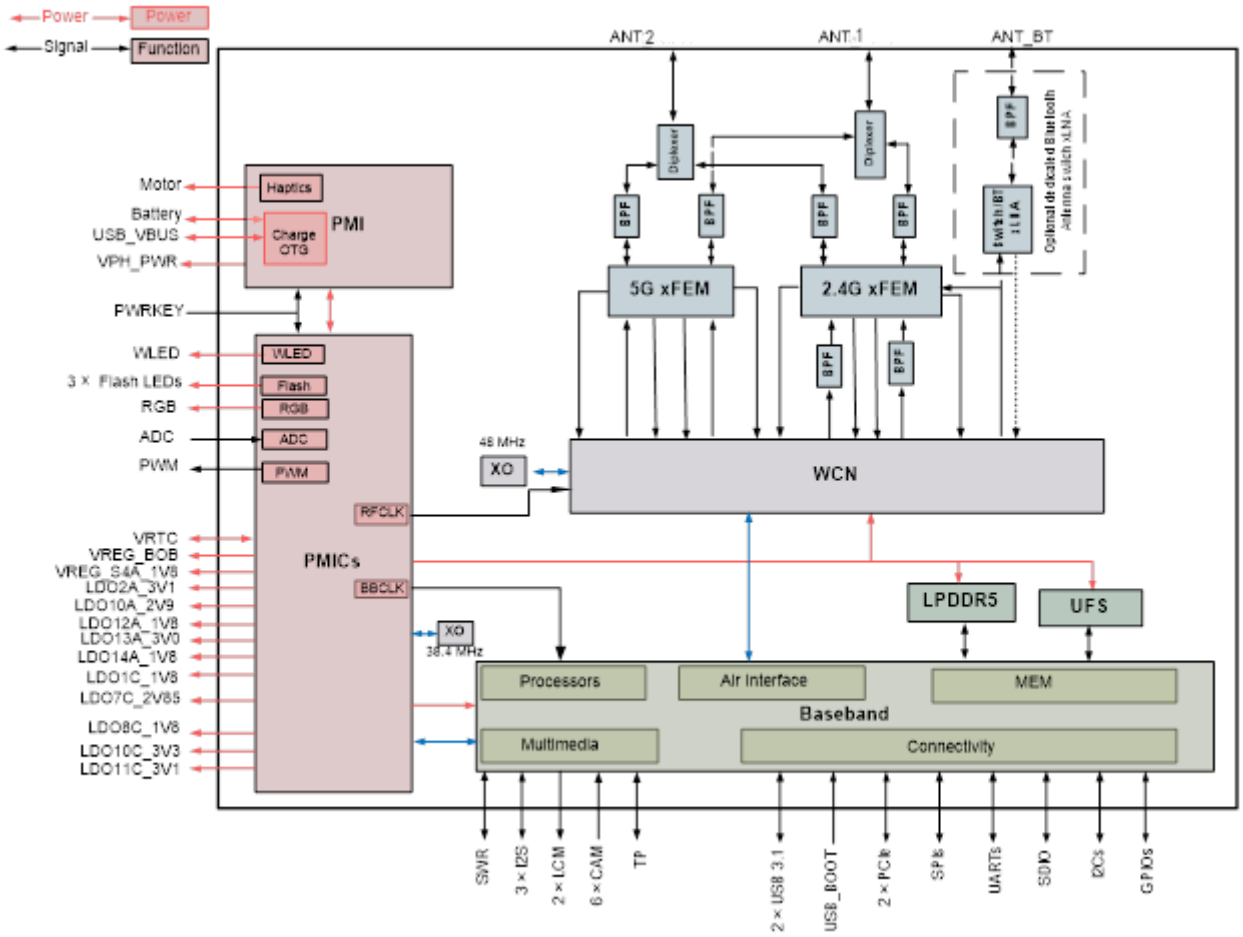

Figure 1: Functional Diagram

2.4. Pin Assignment

The following figure illustrates the pin assignment of the module.

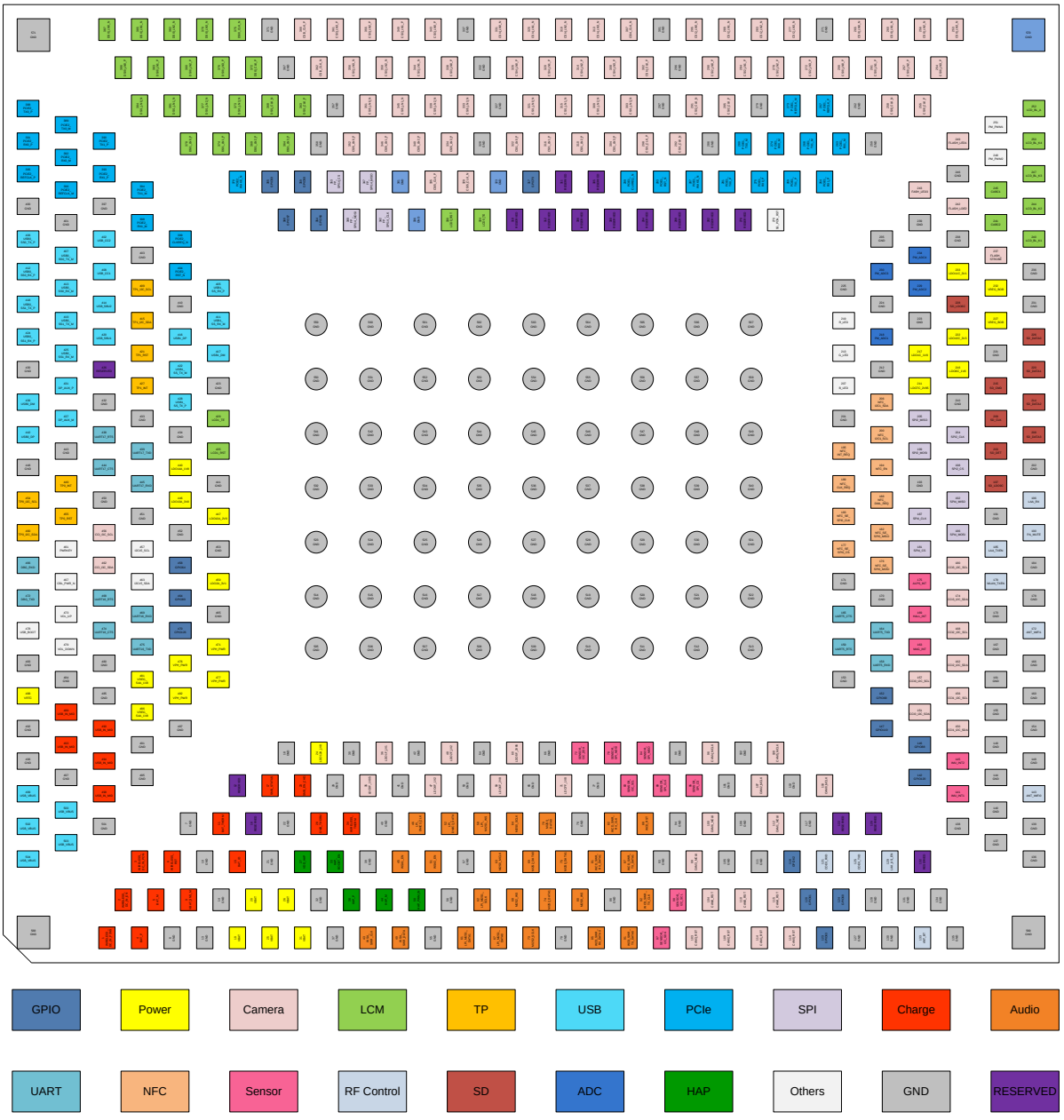

Figure 2: Pin Assignment (Top View)

NOTE

Keep all RESERVED pins unconnected.

2.5. Pin Description

The following table shows the DC characteristics and pin descriptions.

Table 5: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output
PIO	Power Input/Output

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	19, 20, 25, 26, 31	PIO	Power supply for the module	Vmax = 4.4 V Vmin = 3.55 V Vnom = 3.8 V	It must be provided with sufficient current up to 5.0 A. It is recommended to use a TVS to increase voltage surge withstand capability.
LDO2A_3V1	459	PO	3.1 V output	Vnom = 3.1 V $I_O$max = 150 mA	Power supply for DP's pull-up circuits. Reserve a 1.0 μF bypass capacitor if used. If unused, keep this pin open.
LDO10A_2V9	447	PO	2.9 V output	Vnom = 2.9 V $I_O$max = 600 mA	Power supply for digital MIC circuits.

					Add a 4.7 μF bypass capacitor if used. If unused, keep this pin open.
LDO12A_1V8	24	PO	1.8 V output	Vnom = 1.8 V $I_O$max = 300 mA	Power supply for the pull-up of the forced shutdown pin of SMB1390 battery charger. Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open.
LDO13A_3V0	446	PO	3.0 V output	Vnom = 3.0 V $I_O$max = 150 mA	Power supply for VDD of TPs. Add a 2.2 μF bypass capacitor if used. If unused, keep this pin open.
LDO14A_1V8	440	PO	1.8 V output	Vnom = 1.8 V $I_O$max = 300 mA	Power supply for IOVDD of LCDs. Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open.
LDO1C_1V8	217	PO	1.8 V output	Vnom = 1.8 V $I_O$max = 150 mA	Power supply for IOVDD of TPs. Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open.
LDO7C_2V85	211	PO	2.85 V output	Vnom = 2.85 V $I_O$max = 600 mA	Power supply for motor of cameras. Add a 4.7 μF bypass capacitor if used. If unused, keep this pin open.
LDO8C_1V8	216	PO	1.8 V output	Vnom = 1.8 V $I_O$max = 150 mA	Power supply for IOVDD or VDD of sensors. Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open
LDO10C_3V3	222	PO	3.3 V output	Vnom = 3.3 V $I_O$max = 600 mA	Power supply for LED of ALPS sensors. Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open
LDO11C_3V1	233	PO	3.1 V output	Vnom = 3.1 V $I_O$max = 600 mA	Power supply for VDD of LCDs. Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open
VREG_BOB	227, 232	PO	BOB output	Vnom = 3.3 V $I_O$max = 2000 mA	Power supply for external LDOs

VREG_S4A_1V8	481, 486	PO	1.8 V output of buck 4	Vnom = 1.8 V $I_O$max = 500 mA	Power supply for external GPIO's pull up circuits and level shifting circuit.
VPH_PWR	471, 476, 477, 482	PO	Power supply for peripherals	Vnom = VBAT $I_O$max = 2000 mA	
VRTC	488	PIO	Power supply for RTC	Vmin = 2.5 V Vnom = 3.0 V Vmax = 3.25 V	
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO56	354	DIO	General-purpose input/output		
GPIO57	360	DIO	General-purpose input/output		
GPIO58	359	DIO	General-purpose input/output		
GPIO59	365	DIO	General-purpose input/output		
GPIO60	124	DIO	General-purpose input/output		
GPIO61	120	DIO	General-purpose input/output		
GPIO62	116	DIO	General-purpose input/output		
GPIO63	123	DIO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V	1.8 V power domain.
GPIO64	458	DIO	General-purpose input/output		
GPIO68	152	DIO	General-purpose input/output		
GPIO70	317	DIO	General-purpose input/output		
GPIO88	146	DIO	General-purpose input/output		
GPIO89	464	DIO	General-purpose input/output		
GPIO119	147	DIO	General-purpose input/output		
GPIO120	142	DIO	General-purpose input/output		
GPIO126	470	DIO	General-purpose input/output		

RGB Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
R_LED	219	AO	Current source for red LED		
G_LED	213	AO	Current source for green LED		
B_LED	207	AO	Current source for blue LED		
USB Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	499, 500, 502, 503, 504	PIO	Charging power input; Power supply for OTG device; USB/adaptor insertion detection	Vmax = 12.6 V Vmin = 4.0 V Vnom = 5.0 V	
USB0_DP	442	AIO	USB0 2.0 differential data (+)		90 Ω differential impedance. USB 2.0 standard compliant.
USB0_DM	436	AIO	USB0 2.0 differential data (-)		
USB0_SS0_RX_P	412	AI	USB0 3.1 channel 0 SuperSpeed receive (+)		90 Ω differential impedance. USB 3.1 standard compliant.
USB0_SS0_RX_M	413	AI	USB0 3.1 channel 0 SuperSpeed receive (-)		
USB0_SS0_TX_P	406	AO	USB0 3.1 channel 0 SuperSpeed transmit (+)		
USB0_SS0_TX_M	407	AO	USB0 3.1 channel 0 SuperSpeed transmit (-)		
USB0_SS1_RX_P	424	AI	USB0 3.1 channel 1 SuperSpeed receive (+)		
USB0_SS1_RX_M	425	AI	USB0 3.1 channel 1 SuperSpeed receive (-)		
USB0_SS1_TX_P	418	AO	USB0 3.1 channel 1 SuperSpeed transmit (+)		

USB0_SS1_TX_M	419	AO	USB0 3.1 channel 1 SuperSpeed transmit (-)		
USB_CC1	408	AI	USB Type-C detect 1		
USB_CC2	402	AI	USB Type-C detect 2		
USB1_DP	416	AIO	USB1 2.0 differential data (+)		90 Ω differential impedance. USB 2.0 standard compliant.
USB1_DM	417	AIO	USB1 2.0 differential data (-)		
USB1_SS_TX_P	428	AO	USB1 3.1 SuperSpeed transmit (+)		90 Ω differential impedance. USB 3.1 standard compliant.
USB1_SS_TX_M	422	AO	USB1 3.1 SuperSpeed transmit (-)		
USB1_SS_RX_P	405	AI	USB1 3.1 SuperSpeed receive (+)		
USB1_SS_RX_M	411	AI	USB1 3.1 SuperSpeed receive (-)		
DP_AUX_P	431	AIO	DisplayPort auxiliary channel (+)		
DP_AUX_M	437	AIO	DisplayPort auxiliary channel (-)		
USB_SBU1	420	DI	USB Type-C side band use 1		
USB_SBU2	414	DI	USB Type-C side band use 2		
Audio Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WSA1_EN	45	DO	WSA enable 1		
WSA2_EN	51	DO	WSA enable 2		
WSA_SWR_CLK	43	DO	WSA SoundWire clock		
WSA_SWR_DATA	49	DIO	WSA SoundWire data		
WCD_RST	88	DO	WCD reset		

WCD_SWR_TX_CLK	92	DO	WCD SoundWire transmit clock		
WCD_SWR_TX_DATA0	91	DIO	WCD SoundWire transmit data 0		
WCD_SWR_TX_DATA1	87	DIO	WCD SoundWire transmit data 1		
WCD_SWR_RX_CLK	82	DO	WCD SoundWire receive clock		
WCD_SWR_RX_DATA0	85	DIO	WCD SoundWire receive data 0		
WCD_SWR_RX_DATA1	81	DIO	WCD SoundWire receive data 1		
LPI_DMIC3_CLK	46	DO	LPI digital MIC3 clock		
LPI_DMIC3_DATA	52	DI	LPI digital MIC3 data		
I2S Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LPI_MI2S1_SCLK	62	DO	LPI MI2S1 bit clock		
LPI_MI2S1_WS	58	DO	LPI MI2S1 word select		
LPI_MI2S1_DATA0	67	DIO	LPI MI2S1 data channel 0		
LPI_MI2S1_DATA1	61	DIO	LPI MI2S1 data channel 1		
MI2S0_MCLK	63	DO	MI2S0 master clock		
MI2S0_SCLK	64	DO	MI2S0 bit clock		
MI2S0_WS	80	DO	MI2S0 word select		
MI2S0_DATA0	70	DIO	MI2S0 data channel 0		
MI2S0_DATA1	75	DIO	MI2S0 data channel 1		
MI2S2_SCLK	73	DO	MI2S2 bit clock		
MI2S2_WS	68	DO	MI2S2 word select		
MI2S2_DATA0	69	DIO	MI2S2 data channel 0		
MI2S2_DATA1	74	DIO	MI2S2 data channel 1		

SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_CLK	209	DO	SD card clock		
SD_CMD	215	DIO	SD card command	**1.8 V SD card:** V_{IL}max = 0.58 V V_{IH}min = 1.27 V V_{OL}max = 0.45 V V_{OH}min = 1.4 V **2.95 V SD card:** V_{IL}max = 0.73 V V_{IH}min = 1.85 V V_{OL}max = 0.36 V V_{OH}min = 2.22 V	
SD_DATA0	226	DIO	SDIO data bit 0		
SD_DATA1	220	DIO	SDIO data bit 1		
SD_DATA2	214	DIO	SDIO data bit 2		
SD_DATA3	208	DIO	SDIO data bit 3		
SD_DET	203	DI	SD card hot-plug detect	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
SD_LDO9C	197	PO	SD card power supply	$I_o$max = 600 mA	Add a 1.0–2.2 µF bypass capacitor if used. If unused, keep this pin open
SD_LDO6C	228	PO	1.8/2.95 V output power for SD card pull-up circuits	$I_o$max = 150 mA	Add a 1.0–4.7 µF bypass capacitor if used. If unused, keep this pin open
PCIe Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE1_REFCLK_P	267	DO	PCIe1 reference clock (+)		85 Ω differential impedance.
PCIE1_REFCLK_M	273	DO	PCIe1 reference clock (-)		
PCIE1_TX0_P	281	DO	PCIe1 transmit 0 (+)		
PCIE1_TX0_M	280	DO	PCIe1 transmit 0 (-)		
PCIE1_RX0_P	275	DI	PCIe1 receive 0 (+)		
PCIE1_RX0_M	274	DI	PCIe1 receive 0 (-)		
PCIE1_TX1_P	269	DO	PCIe1 transmit 1 (+)		
PCIE1_TX1_M	268	DO	PCIe1 transmit 1 (-)		
PCIE1_RX1_P	264	DI	PCIe1 receive 1 (+)		

PCIE1_RX1_M	263	DI	PCIe1 receive 1 (-)		
PCIE1_WAKE_N	287	DI	PCIe1 wake up host		
PCIE1_RST_N	293	DO	PCIe1 reset		
PCIE1_CLKREQ_N	299	DI	PCIe1 clock request		
PCIE2_REFCLK_P	395	DO	PCIe2 reference clock (+)		
PCIE2_REFCLK_M	396	DO	PCIe2 reference clock (-)		
PCIE2_TX0_P	388	DO	PCIe2 transmit 0 (+)		
PCIE2_TX0_M	389	DO	PCIe2 transmit 0 (-)		
PCIE2_RX0_P	391	DI	PCIe2 receive 0 (+)		85 Ω differential impedance.
PCIE2_RX0_M	392	DI	PCIe2 receive 0 (-)		
PCIE2_TX1_P	390	DO	PCIe2 transmit 1 (+)		
PCIE2_TX1_M	394	DO	PCIe2 transmit 1 (-)		
PCIE2_RX1_P	393	DI	PCIe2 receive 1 (+)		
PCIE2_RX1_M	398	DI	PCIe2 receive 1 (-)		
PCIE2_WAKE_N	370	DI	PCIe2 wake up host		
PCIE2_RST_N	404	DO	PCIe2 reset		
PCIE2_CLKREQ_N	399	DI	PCIe2 clock request		
Touch Panel Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TP0_RST	455	DO	TP0 reset		
TP0_INT	449	DI	TP0 interrupt		
TP0_I2C_SCL	454	OD	TP0 I2C clock		
TP0_I2C_SDA	460	OD	TP0 I2C data		1.8 V power domain.
TP1_RST	421	DO	TP1 reset		
TP1_INT	427	DI	TP1 interrupt		
TP1_I2C_SCL	409	OD	TP1 I2C clock		

TP1_I2C_SDA	415	OD	TP1 I2C data		
LCM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LCD_BL_A	252	PO	Current output for LCD backlight		
LCD_BL_K1	240	AI	Current sink for LCD backlight		
LCD_BL_K2	244	AI	Current sink for LCD backlight		
LCD_BL_K3	247	AI	Current sink for LCD backlight		
LCD_BL_K4	250	AI	Current sink for LCD backlight		
CABC1	245	DI	Content adaptive brightness control 1		
CABC2	241	DI	Content adaptive brightness control 2		
LCD0_RST	330	DO	LCD0 reset		
LCD0_TE	324	DI	LCD0 tearing effect		
LCD1_RST	435	DO	LCD1 reset		
LCD1_TE	429	DI	LCD1 tearing effect		
DSI0_CLK_P	372	AO	LCD0 MIPI clock (+)		
DSI0_CLK_N	375	AO	LCD0 MIPI clock (-)		
DSI0_LN0_P	386	AO	LCD0 MIPI lane 0 data (+)		
DSI0_LN0_N	387	AO	LCD0 MIPI lane 0 data (-)		
DSI0_LN1_P	383	AO	LCD0 MIPI lane 1 data (+)		85 Ω differential impedance.
DSI0_LN1_N	385	AO	LCD0 MIPI lane 1 data (-)		
DSI0_LN2_P	380	AO	LCD0 MIPI lane 2 data (+)		
DSI0_LN2_N	382	AO	LCD0 MIPI lane 2 data (-)		
DSI0_LN3_P	376	AO	LCD0 MIPI lane 3 data (+)		

DSI0_LN3_N	379	AO	LCD0 MIPI lane 3 data (-)		
DSI1_CLK_P	363	AO	LCD1 MIPI clock (+)		
DSI1_CLK_N	368	AO	LCD1 MIPI clock (-)		
DSI1_LN0_P	378	AO	LCD1 MIPI lane 0 data (+)		
DSI1_LN0_N	384	AO	LCD1 MIPI lane 0 data (-)		
DSI1_LN1_P	374	AO	LCD1 MIPI lane 1 data (+)		
DSI1_LN1_N	381	AO	LCD1 MIPI lane 1 data (-)		
DSI1_LN2_P	369	AO	LCD1 MIPI lane 2 data (+)		
DSI1_LN2_N	377	AO	LCD1 MIPI lane 2 data (-)		
DSI1_LN3_P	364	AO	LCD1 MIPI lane 3 data (+)		
DSI1_LN3_N	373	AO	LCD1 MIPI lane 3 data (-)		
Camera Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CSI0_CLK_P	255	AI	MIPI clock of camera 0 (+)		
CSI0_CLK_N	258	AI	MIPI clock of camera 0 (-)		
CSI0_LN0_P	266	AI	MIPI lane 0 data of camera 0 (+)		
CSI0_LN0_N	265	AI	MIPI lane 0 data of camera 0 (-)		
CSI0_LN1_P	261	AI	MIPI lane 1 data of camera 0 (+)		85 Ω differential impedance.
CSI0_LN1_N	260	AI	MIPI lane 1 data of camera 0 (-)		
CSI0_LN2_P	257	AI	MIPI lane 2 data of camera 0 (+)		
CSI0_LN2_N	256	AI	MIPI lane 2 data of camera 0 (-)		
CSI0_LN3_P	254	AI	MIPI lane 3 data of camera 0 (+)		

CSI0_LN3_N	253	AI	MIPI lane 3 data of camera 0 (-)
CSI1_CLK_P	298	AI	MIPI clock of camera 1 (+)
CSI1_CLK_N	292	AI	MIPI clock of camera 1 (-)
CSI1_LN0_P	322	AI	MIPI lane 0 data of camera 1 (+)
CSI1_LN0_N	321	AI	MIPI lane 0 data of camera 1 (-)
CSI1_LN1_P	316	AI	MIPI lane 1 data of camera 1 (+)
CSI1_LN1_N	315	AI	MIPI lane 1 data of camera 1 (-)
CSI1_LN2_P	310	AI	MIPI lane 2 data of camera 1 (+)
CSI1_LN2_N	309	AI	MIPI lane 2 data of camera 1 (-)
CSI1_LN3_P	304	AI	MIPI lane 3 data of camera 1 (+)
CSI1_LN3_N	303	AI	MIPI lane 3 data of camera 1 (-)
CSI2_CLK_P	285	AI	MIPI clock of camera 2 (+)
CSI2_CLK_N	291	AI	MIPI clock of camera 2 (-)
CSI2_LN0_P	290	AI	MIPI lane 0 data of camera 2 (+)
CSI2_LN0_N	295	AI	MIPI lane 0 data of camera 2 (-)
CSI2_LN1_P	284	AI	MIPI lane 1 data of camera 2 (+)
CSI2_LN1_N	289	AI	MIPI lane 1 data of camera 2 (-)
CSI2_LN2_P	278	AI	MIPI lane 2 data of camera 2 (+)
CSI2_LN2_N	283	AI	MIPI lane 2 data of camera 2 (-)
CSI2_LN3_P	272	AI	MIPI lane 3 data of camera 2 (+)
CSI2_LN3_N	277	AI	MIPI lane 3 data of camera 2 (-)
CSI3_CLK_P	366	AI	MIPI clock of camera 3 (+)

CSI3_CLK_N	362	AI	MIPI clock of camera 3 (-)
CSI3_LN0_P	343	AI	MIPI lane 0 data of camera 3 (+)
CSI3_LN0_N	338	AI	MIPI lane 0 data of camera 3 (-)
CSI3_LN1_P	349	AI	MIPI lane 1 data of camera 3 (+)
CSI3_LN1_N	344	AI	MIPI lane 1 data of camera 3 (-)
CSI3_LN2_P	355	AI	MIPI lane 2 data of camera 3 (+)
CSI3_LN2_N	350	AI	MIPI lane 2 data of camera 3 (-)
CSI3_LN3_P	361	AI	MIPI lane 3 data of camera 3 (+)
CSI3_LN3_N	356	AI	MIPI lane 3 data of camera 3 (-)
CSI4_CLK_P	302	AI	MIPI clock of camera 4 (+)
CSI4_CLK_N	307	AI	MIPI clock of camera 4 (-)
CSI4_LN0_P	326	AI	MIPI lane 0 data of camera 4 (+)
CSI4_LN0_N	331	AI	MIPI lane 0 data of camera 4 (-)
CSI4_LN1_P	320	AI	MIPI lane 1 data of camera 4 (+)
CSI4_LN1_N	325	AI	MIPI lane 1 data of camera 4 (-)
CSI4_LN2_P	314	AI	MIPI lane 2 data of camera 4 (+)
CSI4_LN2_N	319	AI	MIPI lane 2 data of camera 4 (-)
CSI4_LN3_P	308	AI	MIPI lane 3 data of camera 4 (+)
CSI4_LN3_N	313	AI	MIPI lane 3 data of camera 4 (-)
CSI5_CLK_P	335	AI	MIPI clock of camera 5 (+)
CSI5_CLK_N	329	AI	MIPI clock of camera 5 (-)
CS5_LN0_P	352	AI	MIPI lane 0 data of camera 5 (+)

CSI5_LN0_N	351	AI	MIPI lane 0 data of camera 5 (-)
CSI5_LN1_P	346	AI	MIPI lane 1 data of camera 5 (+)
CSI5_LN1_N	345	AI	MIPI lane 1 data of camera 5 (-)
CSI5_LN2_P	340	AI	MIPI lane 2 data of camera 5 (+)
CSI5_LN2_N	339	AI	MIPI lane 2 data of camera 5 (-)
CSI5_LN3_P	334	AI	MIPI lane 3 data of camera 5 (+)
CSI5_LN3_N	333	AI	MIPI lane 3 data of camera 5 (-)
CAM0_MCLK	118	DO	Master clock of camera 0
CAM1_MCLK	112	DO	Master clock of camera 1
CAM2_MCLK	107	DO	Master clock of camera 2
CAM3_MCLK	99	DO	Master clock of camera 3
CAM4_MCLK	96	DO	Master clock of camera 4
CAM5_MCLK	108	DO	Master clock of camera 5
CAM6_MCLK	100	DO	Master clock of camera 6
CAM0_RST	119	DO	Reset of camera 0
CAM1_RST	114	DO	Reset of camera 1
CAM2_RST	109	DO	Reset of camera 2
CAM3_RST	103	DO	Reset of camera 3
CAM4_RST	115	DO	Reset of camera 4
CAM5_RST	110	DO	Reset of camera 5
CAM6_RST	104	DO	Reset of camera 6
CCI0_I2C_SDA	151	OD	I2C data of CCI0
CCI0_I2C_SCL	157	OD	I2C clock of CCI0

CCI1_I2C_SDA	150	OD	I2C data of CCI1		
CCI1_I2C_SCL	156	OD	I2C clock of CCI1		
CCI2_I2C_SDA	162	OD	I2C data of CCI2		
CCI2_I2C_SCL	168	OD	I2C clock of CCI2		
CCI3_I2C_SDA	174	OD	I2C data of CCI3		
CCI3_I2C_SCL	180	OD	I2C3 clock of CCI3		
CCI_I3C_SDA	462	OD	I3C data of CCI		
CCI_I3C_SCL	456	OD	I3C clock of CCI		
LDO1F_1V1	36	PO	1.1 V output	Vnom = 1.1 V $I_O$max = 1200 mA	Power supply for DVDD of camera. Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open.
LDO2F_1V2	48	PO	1.2 V output	Vnom = 1.2 V $I_O$max = 1200 mA	Power supply for DVDD of camera. Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open.
LDO3F_1V05	35	PO	1.05 V output	Vnom = 1.05 V $I_O$max = 300 mA	Power supply for DVDD of camera. Reserve a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open.
LDO4F_1V2*	47	PO	1.2 V output	Vnom = 1.2 V $I_O$max = 600 mA	Power supply for DVDD of camera. Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open.
LDO5F_2V85	60	PO	2.85 V output	Vnom = 2.85 V $I_O$max = 600 mA	Power supply for AVDD of camera. Add a 4.7 μF bypass capacitor if used. If unused, keep this pin open.
LDO6F_2V8	59	PO	2.8 V output	Vnom = 2.8 V $I_O$max = 600 mA	Power supply for AVDD of camera. Add a 4.7 μF bypass capacitor if used. If unused, keep this pin open.

LDO7F_1V8	71	PO	1.8 V output	Vnom = 1.8 V $I_O$max = 600 mA	Power supply for DOVDD of camera. Add a 4.7 μF bypass capacitor if used. If unused, keep this pin open.
Flashlight Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
FLASH_LED1	249	AO	Flash/torch driver output 1		
FLASH_LED2	242	AO	Flash/torch driver output 2		
FLASH_LED3	243	AO	Flash/torch driver output 3		
FLASH_STROBE	237	DI	Flash LED strobe		If unused, connect it to GND.
Keypad Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	461	DI	Turn on/off the module		PWRKEY pin is pulled to 1.8 V internally.
VOL_UP	473	DI	Volume up		
VOL_DOWN	479	DI	Volume down		
UART Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	472	DO	Debug UART transmit		
DBG_RXD	466	DI	Debug UART receive		
UART5_TXD	164	DO	UART5 transmit		
UART5_RXD	158	DI	UART5 receive		
UART5_CTS	165	DI	DCE clear to send signal from DTE		
UART5_RTS	159	DO	DCE request to send signal to DTE		
UART16_TXD	475	DO	UART16 transmit		
UART16_RXD	469	DI	UART16 receive		
UART16_CTS	474	DI	DCE clear to send signal from DTE		

UART16_RTS	468	DO	DCE request to send signal to DTE		
UART17_TXD	439	DO	UART17 transmit		
UART17_RXD	445	DI	UART17 receive		
UART17_CTS	444	DI	DCE clear to send signal from DTE		
UART17_RTS	438	DO	DCE request to send signal to DTE		
Sensor Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SENSOR_I2C_SDA	97	OD	I2C clock for external sensor		
SENSOR_I2C_SCL	98	OD	I2C data for external sensor		
SENSOR_I3C_SDA	72	OD	I3C data for external sensor		
SENSOR_I3C_SCL	83	OD	I3C clock for external sensor		
SENSOR_SPI_CLK	89	DO	SPI clock for external sensor		
SENSOR_SPI_CS	95	DO	SPI chip select for external sensor		
SENSOR_SPI_MOSI	78	DO	SPI master-out slave-in for external sensor		
SENSOR_SPI_MISO	84	DI	SPI master-in slave-out for external sensor		
MAG_INT	163	DI	MAG interrupt		
HALL_INT	169	DI	HALL interrupt		
ALPS_INT	175	DI	ALPS interrupt		
IMU_INT1	141	DI	IMU interrupt 1		
IMU_INT2	145	DI	IMU interrupt 2		
SPI Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI2_CLK	204	DO	SPI2 clock		

SPI2_CS	198	DO	SPI2 chip select		
SPI2_MISO	205	DI	SPI2 master-in slave-out		
SPI2_MOSI	199	DO	SPI2 master-out slave-in		
SPI4_CLK	187	DO	SPI4 clock		
SPI4_CS	181	DO	SPI4 chip select		
SPI4_MISO	192	DI	SPI4 master-in slave-out		
SPI4_MOSI	186	DO	SPI4 master-out slave-in		
FP_SPI14_CLK	342	DO	FP SPI14 clock		
FP_SPI14_CS	353	DO	FP SPI14 chip select		
FP_SPI14_MISO	347	DI	FP SPI14 master-in slave-out		
FP_SPI14_MOSI	348	DO	FP SPI14 master-out slave-in		
RF Control Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_BT*	133	AIO	Bluetooth antenna interface		Reserved
ANT_WIFI0	143	AIO	Wi-Fi0/Bluetoothantenna interface		
ANT_WIFI1	172	AIO	Wi-Fi1 antenna interface		
PA_MUTE	190	DI	Wi-Fi xFEM control to disable Wi-Fi PA		If unused, connect it to GND.
WLAN_TXEN	179	DO	Wi-Fi xFEM control to enable Wi-Fi transmit		If unused, connect it to GND with a 10 kΩ resistor.
LAA_RX	196	DI	Wi-Fi xFEM control for LAA/n79 receiver		If unused, connect it to GND.
LAA_TXEN	185	DO	Wi-Fi xFEM control to enable LAA/n79 transmit		If unused, connect it to GND.
LAA_AS_EN	129	DI	Allow LAA/n79 to control Wi-Fi xFEM during Wi-Fi sleep mode		If unused, connect it to GND with a 10 kΩ resistor.

COEX_RXD	121	DI	2.4 GHz WWAN & Wi-Fi/Bluetooth coexistence receive		If unused, connect it to GND.
COEX_TXD	125	DO	2.4 GHz WWAN & Wi-Fi/Bluetooth coexistence transmit		If unused, connect it to GND with 10 kΩ resistor.
NFC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NFC_SE_SPI0_CLK	183	DO	NFC SE SPI0 clock		
NFC_SE_SPI0_CS	177	DO	NFC SE SPI0 chip select		
NFC_SE_SPI0_MISO	182	DI	NFC SE SPI0 master-in slave-out		
NFC_SE_SPI0_MOSI	176	DO	NFC SE SPI0 master-out slave-in		
NFC_I2C1_SCL	200	OD	I2C1 clock of NFC		
NFC_I2C1_SDA	206	OD	I2C1 data of NFC		
NFC_DWL_REQ	188	DI	NFC download request		
NFC_EN	194	DO	NFC enable		
NFC_CLK_REQ	189	DI	NFC clock request		
NFC_INT_REQ	195	DI	NFC interrupt request		
I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C15_SCL	457	OD	I2C15 serial clock		
I2C15_SDA	463	OD	I2C15 serial data		
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PM_ADC1	218	AI	General-purpose ADC interface 1		
PM_ADC2	229	AI	General-purpose ADC interface 2		
PM_ADC3	230	AI	General-purpose ADC interface 3		

PM_ADC4	234	AI	General-purpose ADC interface 4		
Charging Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BAT_P	4	AI	Battery voltage detect (+)		Must be connected.
BAT_M	5	AI	Battery voltage detect (-)		Must be connected.
VBAT_SNS_M	9	AI	Sensed battery voltage (-) for charger circuits		Must be connected.
BAT_THERM	11	AI	Battery temperature detect		Must be pull down to GND with a 100 kΩ resistor.
BAT_ID	15	AI	Battery type detect		
SMB_THERM	28	AI	SMB1390 parallel charging temperature detect		Parallel charging is not supported by default. If parallel charging is not needed, keep these pins open.
SMB_STATUS	17	DI	SMB1390 parallel charging status indicator		
SMB_EN_CHG	23	DO	SMB1390 parallel charging enable		
USB_IN_MID	489, 490, 493, 494, 498	PO	Power output for SMB1390 parallel charging		
Wireless Charging Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WIRELESS_DC_IN_PSNS	1	AI	DC and wireless charging input for power sense		
WIRELESS_DC_IN_EN	2	DO	DC and wireless charging output enable and disable		
WIRELESS_DC_IN_PON	3	AI	DC and wireless charging power-on trigger		
WIRELESS_RST	6	DO	Wireless charging reset		
WIRELESS_THERM	34	AI	Wireless charging temperature detect		

Vibration Drive Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
HAP_P	38	AO	Haptics driver output (+)		
HAP_M	44	AO	Haptics driver output (-)		
HAP_PWM_IN	50	DI	Haptics PWM input		If unused, connect it to GND.
VDD_HAP	27	PI	Power supply for haptics		
HAP_BOOST_EN	33	DO	Haptics boost enable		
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
5G_PON_RST	270	DO	PON control signal for 5G		
USB_BOOT	478	DI	Force the module into emergency download mode		
CBL_PWR_N	467	DI	Initiates power-on when grounded		
PM_PWM1	251	DO	PWM output 1		
PM_PWM2	248	DO	PWM output 2		
RESERVED	12, 16, 122, 126, 132, 276, 282, 288, 294, 300, 305, 306, 311, 312, 318, 426				
GND	7, 8, 10, 13, 14, 18, 21, 22, 29, 30, 32, 37, 39, 40, 41, 42, 53, 54, 55, 56, 57, 65, 66, 76, 77, 79, 86, 90, 93, 94, 101, 102, 105, 106, 111, 113, 117, 127, 128, 130, 131, 134, 135, 136, 137, 138, 139, 140, 144, 148, 149, 153, 154, 155, 160, 161, 166, 167, 170, 171, 173, 178, 184, 191, 193, 201, 202, 210, 212, 221, 223, 224, 225, 231, 235, 236, 238, 239, 246, 259, 262, 271, 279, 286, 296, 297, 301, 323, 327, 328, 332, 336, 337, 341, 357, 358, 367, 371, 397, 400, 401, 403, 410, 423, 430, 432, 433, 434, 441, 443, 448, 450, 451, 452, 453, 465, 480, 483, 484, 485, 487, 491, 492, 495, 496, 497, 501, 505–571		

NOTE

1. Keep all RESERVED pins unconnected.
2. All GND pins should be connected to the ground network.

2.6. EVB Kit

To help you develop applications with the module, Quectel supplies an evaluation board with accessories to control or test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Power Supply

3.1.1. Power Supply Pins

The module provides 5 VBAT pins, 4 VPH_PWR pins. VBAT pins must be connected to an external power to supply power to the module. VPH_PWR pins are used to power other devices.

3.1.2. Battery Charge and Management

The module can recharge batteries. The battery charger in the module supports trickle charging, constant current charging and constant voltage charging modes, which optimize the charging procedure for Li-ion batteries.

- **Trickle charging:** There are two steps in this mode. When the battery voltage is below 2.1 V, a 45 mA trickle charging current is applied to the battery. When the battery voltage is charged to between 2.1 V and 3.0 V, the maximum charging current can be set to 1575 mA.
- **Constant current mode (CC mode):** When the battery is increased to between 3.0 V and 4.35 V, the system will switch to CC mode. The maximum charging current is 6 A when an adapter is used for battery charging, and the maximum charging current is 500 mA for USB charging.
- **Constant voltage mode (CV mode):** When the battery voltage reaches the final value 4.35 V, the system will switch to CV mode and the charging current will decrease gradually. When the battery level reaches 100 %, the charging is completed.

Table 7: Pin Definition of Charging Interface

Pin Name	Pin No.	I/O	Description	Comment
BAT_P	4	AI	Battery voltage detect (+)	Must be connected.
BAT_M	5	AI	Battery voltage detect (-)	Must be connected.
VBAT_SNS_M	9	AI	Sensed battery voltage (-) for charger circuits	Must be connected.
BAT_THERM	11	AI	Battery temperature detect	Must be pull down to GND with a 100 kΩ resistor.

BAT_ID	15	AI	Battery type detect	
SMB_THERM	28	AI	SMB1390 parallel charging temperature detect	Parallel charging is not supported by default. If parallel charging is not needed, keep these pins open.
SMB_STATUS	17	DI	SMB1390 parallel charging status indicator	
SMB_EN_CHG	23	DO	SMB1390 parallel charging enable	
USB_IN_MID	489, 490, 493, 494, 498	PO	Power output for SMB1390 parallel charging	

The module supports battery temperature detection in the condition that the battery integrates a thermistor (100 kΩ 1 % NTC thermistor with a B-constant of 4050K by default); and the thermistor is connected to BAT_THERM pin, If the BAT_THERM pin is not connected, there will be malfunctions such as battery charging failure, battery level display error, etc.

A reference design for the battery charging circuit is shown below.

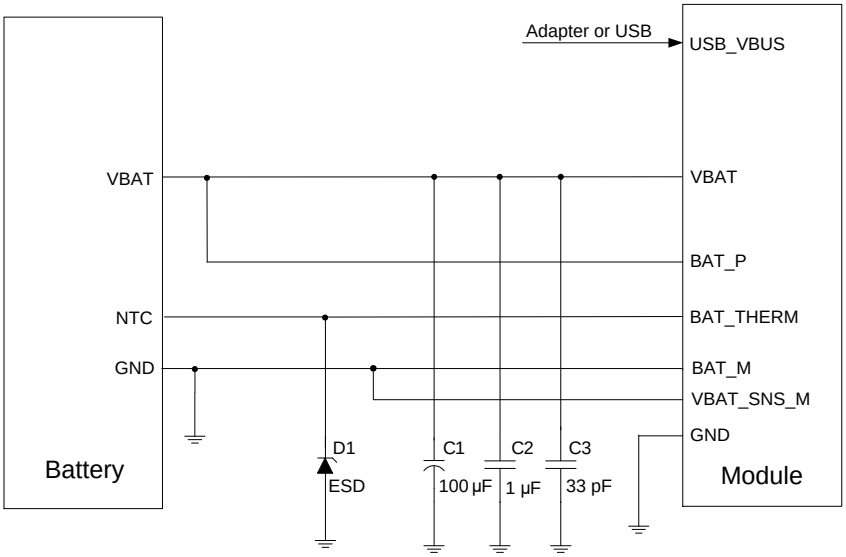

Figure 3: Reference Design for Battery Charging Circuit

Mobile devices such as mobile phones and handheld POS systems are powered by batteries. When different batteries are utilized, the charging and discharging curve must be modified correspondingly to achieve the best effect.

If the thermistor is not available in the battery, or adapter is utilized for powering the module, then there is only a need for VBAT and GND connection. In this case, the system may mistakenly judge that the battery temperature is abnormal, which will cause battery charging failure. In order to avoid this, BAT_THERM should be connected to GND via a 100 kΩ resistor. If BAT_THERM is unconnected, the system will be

unable to detect the battery, making the battery cannot be charged.

BAT_P and BAT_M must be connected, and VBAT_SNS_M pin must be connected. Otherwise, the module will have abnormalities in voltage detection, as well as associated module power on/off and battery charging and discharging issues.

3.1.3. Reference Design for Power Supply

The power design for the module is very important for the performance of the module. The power supply of the module should be able to provide sufficient current up to 5 A at least. If the voltage drop between the input and output is not too high, it is suggested to use an LDO to supply power for the module. If there is a big voltage difference between the input voltage and the desired output (VBAT) voltage, a buck converter is recommended.

The following figure shows a reference design for +12 V input power source:

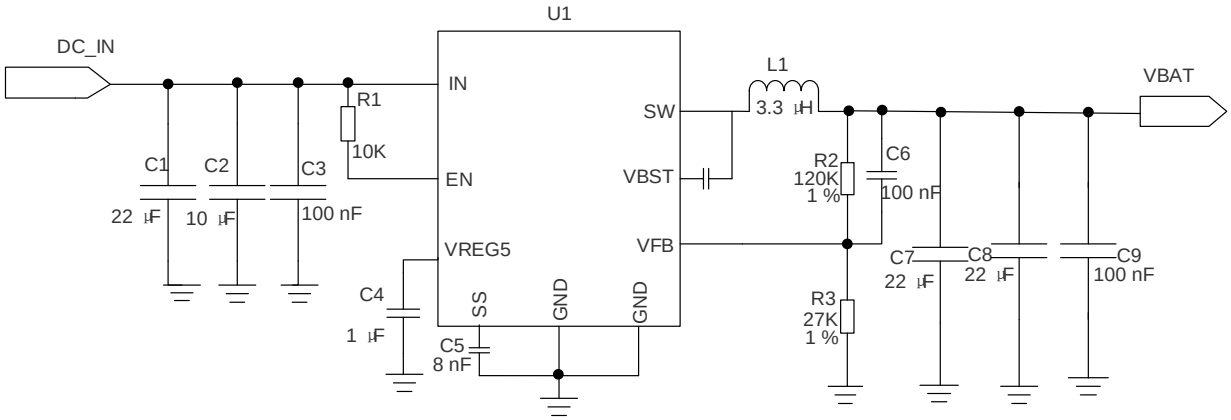

Figure 4: Reference Circuit of Power Supply

3.1.4. Voltage Stability Requirements

The power supply range of the module is from 3.55 V to 4.4 V, and the recommended value is 3.8 V. The power supply performance, such as load capacity, voltage ripple, etc. directly influences the module's performance and stability. Under ultimate conditions, the module may have a transient peak current of up to 3 A. If the power supply capability is not sufficient, there will be voltage drops, and if the voltage drops below 3.1 V, the module will power off automatically. Therefore, make sure the input voltage never drops below 3.1 V.

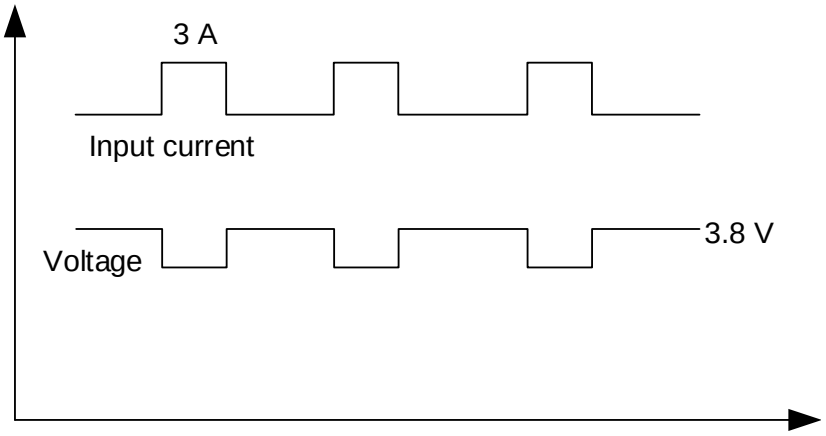

Figure 5: Voltage Drop Sample

To prevent the voltage from dropping below 3.1 V, use a bypass capacitor of about 100 µF with low ESR (ESR = 0.7 Ω), and reserve a multi-layer ceramic chip capacitor (MLCC) array due to its ultra-low ESR. It is recommended to use four ceramic capacitors (10 µF, 100 nF, 33 pF, 10 pF) to compose the MLCC array, and place four capacitors close to VBAT pins. The width of VBAT trace should be no less than 3 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, to get a stable power source, it is suggested to use a 2000 W TVS and place it as close to the VBAT pins as possible to enhance surge protection.

The following figure shows the structure of the power supply.

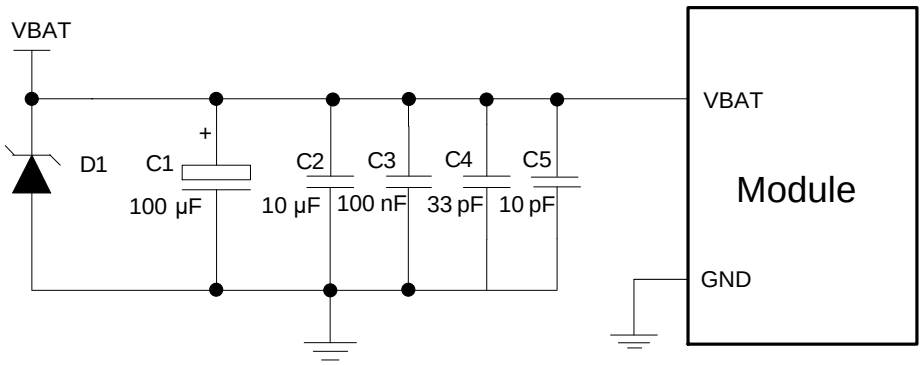

Figure 6: Structure of Power Supply

3.2. Turn On

3.2.1. Turn On with PWRKEY

Table 8: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	461	DI	Turn on/off the module	PWRKEY pin is pulled to 1.8 V internally.

The module can be turned on by driving PWRKEY low for at least 1.6 s.

It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

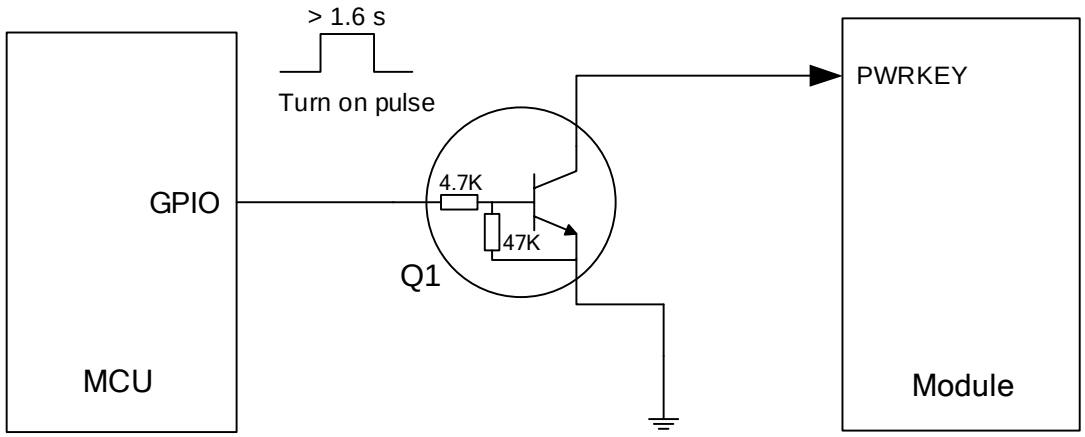

Figure 7: Turn On the Module Using Driving Circuit

The other way to control the PWRKEY is by using a button directly. A TVS component is indispensable to be placed nearby the button for ESD protection. Additionally, a 1 kΩ resistor is connected in series to PWRKEY. A reference circuit is shown in the following figure.

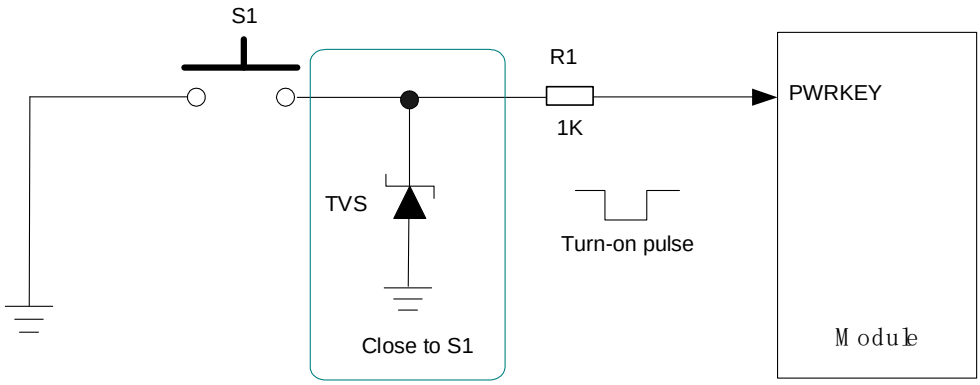

Figure 8: Turn On the Module Using a Button

3.2.2. Turn On Automatically with CBL_PWR_N

Table 9: Pin Definition of CBL_PWR_N

Pin Name	Pin No.	I/O	Description
CBL_PWR_N	467	DI	Initiates power-on when grounded

The module can be turned on automatically by driving CBL_PWR_N pin to GND via a 1 kΩ resistor. CBL_PWR_N pin is pulled up internally. A simple reference circuit is illustrated in the following figure.

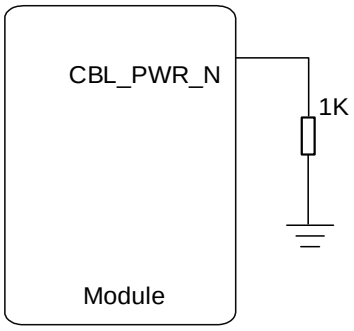

Figure 9: Reference Circuit of Automatic Turn-on

NOTE

If the module turns on automatically through CBL_PWR_N pin, it cannot be turned off manually. In such case, it can be turned off only by cutting off the power supply of system.

The power-up timing is illustrated in the following figure.

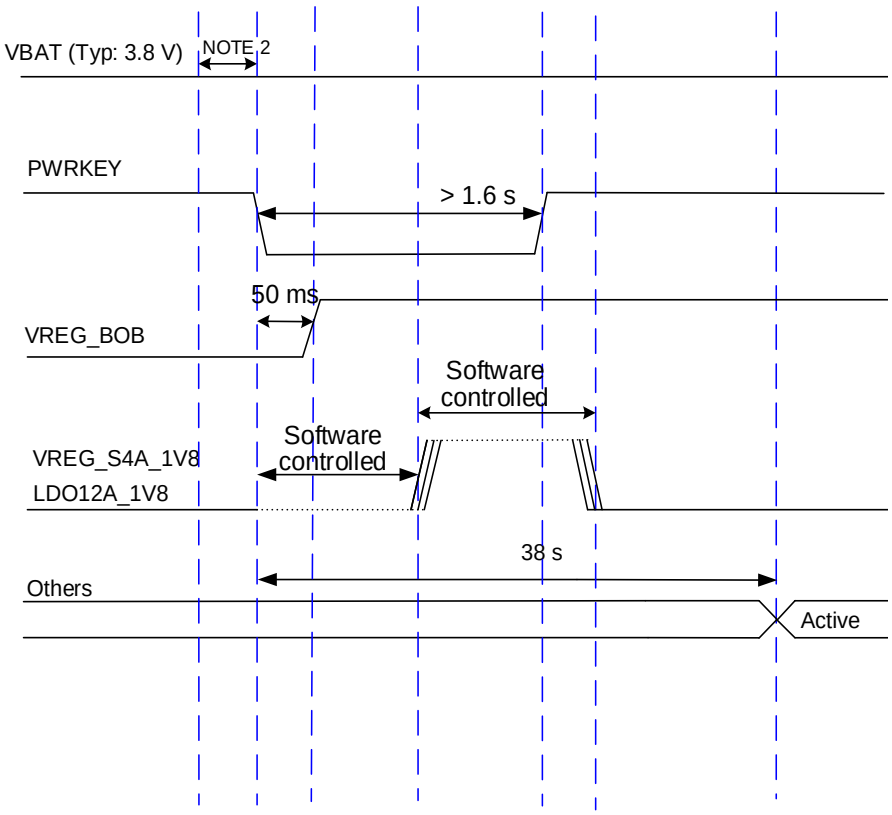

Figure 10: Power-up Timing

NOTE

1. When the module is powered on for the first time, its power-up timing may be different from that shown in the figure above.
2. Make sure that VBAT is stable before pulling down the PWRKEY pin. The recommended time between them is no less than 30 ms. PWRKEY pin cannot be pulled down all the time.

3.3. Turn Off/Restart

The module can be turned off by driving PWRKEY low for at least 1 s. Then the module will detect a turn-off action and a prompt window will pop up on the screen. You can choose to turn off the module in the prompt window.

The other way to turn off the module is by driving PWRKEY low for at least 8 s. The module will execute the forced shutdown. The forced power-down timing is illustrated in the following figure.

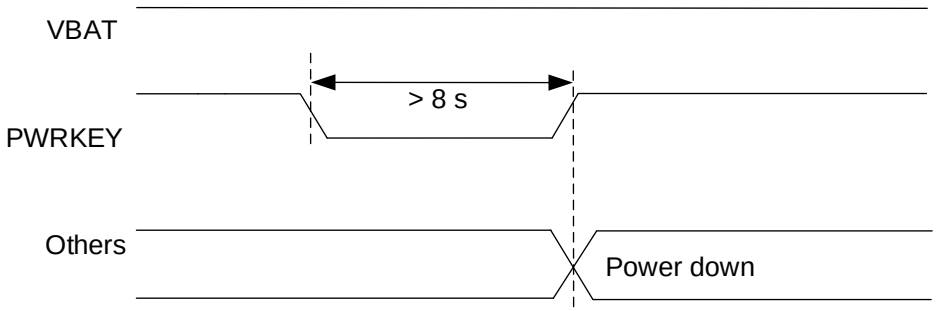

Figure 11: Forced Power-down Timing

3.4. VRTC Interface

The RTC (Real Time Clock) can be powered by an external power source through VRTC when the module is powered down and there is no power supply for the VBAT. The external power source can be a capacitor according to application demands. The following are some reference circuit designs when an external battery is utilized for powering RTC.

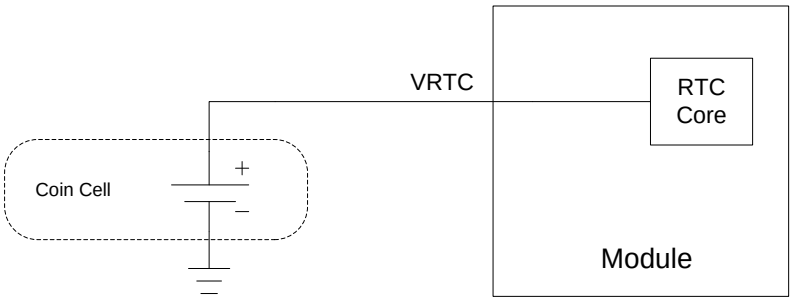

Figure 12: RTC Powered by a Coin Cell

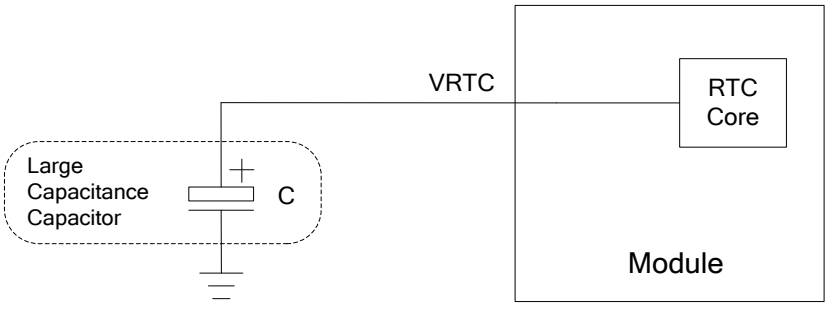

Figure 13: RTC Powered by Capacitor

- When VBAT is disconnected, the recommended input voltage range for VRTC is 2.5–3.25 V and the recommended typical value is 3.0 V.
- When powered by VBAT, the RTC error is 50 ppm. When powered by VRTC, the RTC error is about 200 ppm.
- If a rechargeable battery is used, ESR of the battery should be less than 1 kΩ, and it is recommended to use MS621FE FL11E of SEIKO.

3.5. Power Supply Output

The module supports regulated voltages output for peripheral circuits. During application, it is recommended to use 33 pF and 10 pF capacitors in parallel in the circuit to effectively suppress high-frequency noise.

Table 10: Power Supply Description

Pin Name	Default Voltage (V)	Drive Current (mA)	Standby
LDO2A_3V1	3.1	150	
LDO10A_2V9	1.8	600	
LDO12A_1V8	1.8	300	
LDO13A_3V0	3.0	150	
LDO14A_1V8	1.8	300	
LDO1C_1V8	1.8	150	
LDO7C_2V85	2.85	600	
LDO8C_1V8	1.8	150	
LDO10C_3V3	3.3	600	
LDO11C_3V1	3.1	600	
VREG_BOB	3.3	2000	Keep ON
VREG_S4A_1V8	1.8	500	Keep ON
VPH_PWR	VBAT	2000	Keep ON

NOTE

The actual LDO output voltage can be adjusted according to different application scenarios.

4 Application Interfaces

4.1. USB Interfaces

USB0 interface:

- Compliant with the USB 3.1 Gen 2 and USB 2.0 specifications
- Supports USB OTG function
- Supports host and device modes
- Used for AT command communication, data transmission, software debugging and firmware upgrade
- Supports DisplayPort V1.4 over Type-C

USB1 interface:

- Compliant with the USB 3.1 Gen 2 and USB 2.0 specifications
- Supports host mode only
- Supports USB hub expansion

The following table shows the pin definition of USB0 and USB1 interfaces.

Table 11: Pin Definition of USB0 and USB1 Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	499, 500, 502, 503, 504	PIO	Charging power input; Power supply for OTG device; USB/adaptor insertion detection	
USB0_DP	442	AIO	USB0 2.0 differential data (+)	90 Ω differential impedance. USB 2.0 standard compliant.
USB0_DM	436	AIO	USB0 2.0 differential data (-)	
USB0_SS0_RX_P	412	AI	USB0 3.1 channel 0 SuperSpeed receive (+)	90 Ω differential impedance. USB 3.1 standard compliant.
USB0_SS0_RX_M	413	AI	USB0 3.1 channel 0 SuperSpeed receive (-)	
USB0_SS0_TX_P	406	AO	USB0 3.1 channel 0 SuperSpeed transmit (+)	

USB0_SS0_TX_M	407	AO	USB0 3.1 channel 0 SuperSpeed transmit (-)	
USB0_SS1_RX_P	424	AI	USB0 3.1 channel 1 SuperSpeed receive (+)	
USB0_SS1_RX_M	425	AI	USB0 3.1 channel 1 SuperSpeed receive (-)	
USB0_SS1_TX_P	418	AO	USB0 3.1 channel 1 SuperSpeed transmit (+)	
USB0_SS1_TX_M	419	AO	USB0 3.1 channel 1 SuperSpeed transmit (-)	
USB_CC1	408	AI	USB Type-C detect 1	
USB_CC2	402	AI	USB Type-C detect 2	
DP_AUX_P	431	AIO	DisplayPort auxiliary channel (+)	
DP_AUX_M	437	AIO	DisplayPort auxiliary channel (-)	
USB_SBU1	420	DI	USB Type-C side band use 1	
USB_SBU2	414	DI	USB Type-C side band use 2	
USB1_DP	416	AIO	USB1 2.0 differential data (+)	90 Ω differential impedance. USB 2.0 standard compliant.
USB1_DM	417	AIO	USB1 2.0 differential data (-)	
USB1_SS_TX_P	428	AO	USB1 3.1 SuperSpeed transmit (+)	90 Ω differential impedance. USB 3.1 standard compliant.
USB1_SS_TX_M	422	AO	USB1 3.1 SuperSpeed transmit (-)	
USB1_SS_RX_P	405	AI	USB1 3.1 SuperSpeed receive (+)	
USB1_SS_RX_M	411	AI	USB1 3.1 SuperSpeed receive (-)	

4.1.1. USB0 Type-C

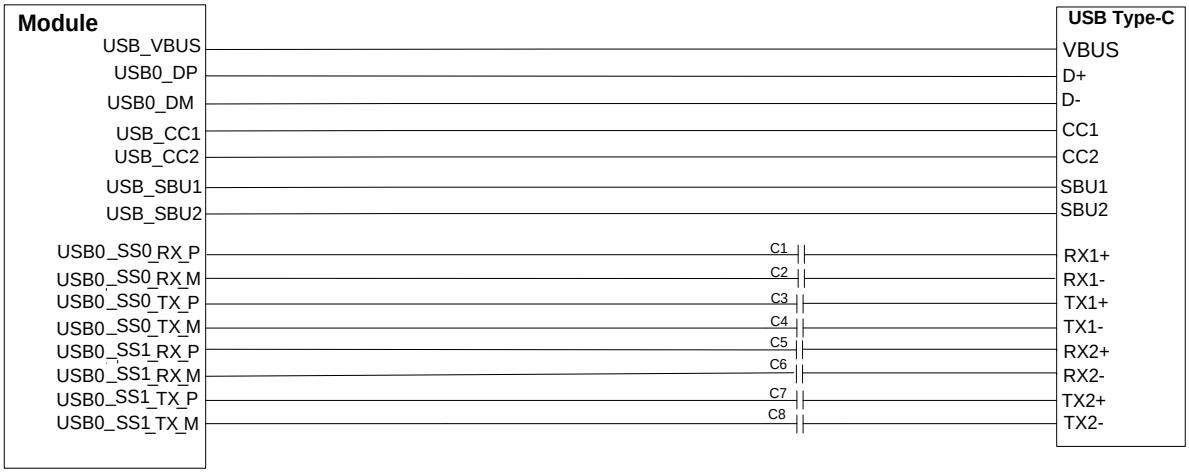

Figure 14: USB Type-C Interface Reference Design

Follow the following principles while designing the USB interfaces to ensure USB performance.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90 Ω.
- Pay attention to the influence of junction capacitance of ESD protection components on USB data traces. Typically, the junction capacitance value should be less than 2 pF for USB 2.0 and less than 0.5 pF for USB 3.1.
- Do not route signal traces under crystals, oscillators, magnetic devices, and RF signal traces. It is important to route the USB differential traces in inner-layer and surround the traces with ground on that layer and with ground planes above and below.
- For USB 2.0, the total trace length of each signal should be less than 250 mm, and the length matching of each differential pair should be less than 2 mm.
- For USB 3.1, intra-pair length matching (USB_SS_TX/RX_P/M) should be less than 0.7 mm, while the inter-pair length matching (USB_SS_Tx/Rx) should be less than 10 mm.
- For DisplayPort, intra-pair length matching (DP_AUX_P/M) should be less than 7 mm.

Table 12: USB Trace Length Inside the Module

Signal	Pin No.	Length (mm)	Length Difference (mm)
USB0_DP	442	53.00	-0.16
USB0_DM	436	53.16	
USB0_SS0_RX_P	412	18.33	-0.30

USB0_SS0_RX_M	413	18.63	
USB0_SS0_TX_P	406	22.72	0.29
USB0_SS0_TX_M	407	22.43	
USB0_SS1_RX_P	424	22.03	-0.22
USB0_SS1_RX_M	425	22.25	
USB0_SS1_TX_P	418	24.18	-0.21
USB0_SS1_TX_M	419	24.39	
DP_AUX_P	431	19.17	-0.42
DP_AUX_M	437	19.59	
USB1_DP	416	18.47	0.3
USB1_DM	417	18.17	
USB1_SS_TX_P	428	20.81	-0.07
USB1_SS_TX_M	422	20.88	
USB1_SS_RX_P	405	14.82	-0.25
USB1_SS_RX_M	411	15.07	

4.1.2. DisplayPort

The module supports 4-lane DisplayPort mode of up to 4K @ 60 fps over Type-C. The pin definition of USB Type-C/DisplayPort mode is listed below:

Table 13: Pin Definition of USB Type-C/DisplayPort Mode

Pin Name	USB Type-C Mode	DisplayPort Mode
USB0_SS1_RX_P/M	USB0_SS1_RX_P/M	DP_LANE0_P/M
USB0_SS1_TX_P/M	USB0_SS1_TX_P/M	DP_LANE1_P/M
USB0_SS0_RX_P/M	USB0_SS0_RX_P/M	DP_LANE3_P/M
USB0_SS0_TX_P/M	USB0_SS0_TX_P/M	DP_LANE2_P/M

DP_AUX_P/M	SBU1/2	DP_AUX_P/N
USB0_DP/M	USB1_DP/M	USB1_DP/M
USB_CC1/CC2	USB_CC1/CC2	HOTPLUG_DET/VCONN
USB_VBUS	USB_VBUS	USB_VBUS
UART5_CTS	-	SBU_SW_OE
UART5_RTS	-	SBU_SW_SEL
GND	GND	GND

The reference design for DisplayPort is shown below:

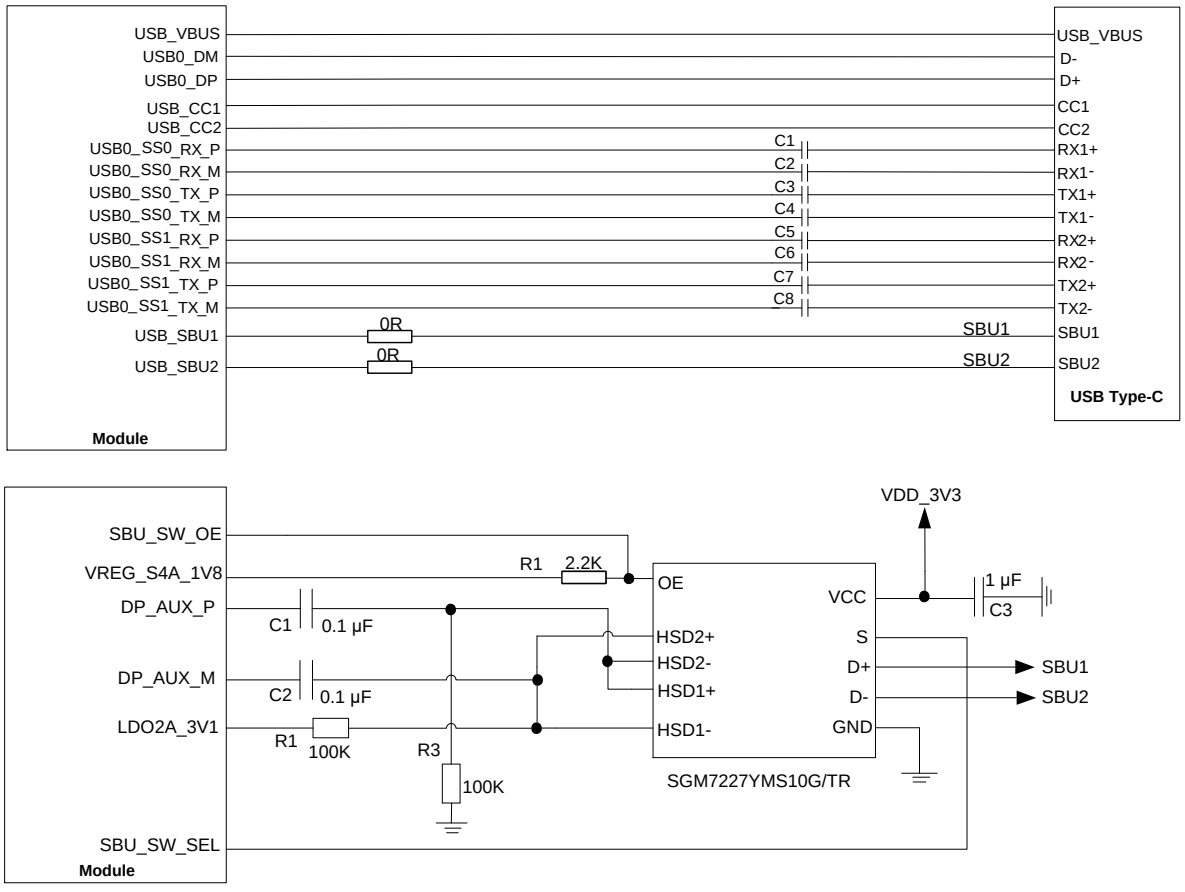

Figure 15: Reference Design for DisplayPort Mode

4.2. UART Interfaces

The module provides 4 UART interfaces:

- **UART5/UART16/UART17:** 4-wire UART interface, supports hardware flow control.
- **Debug UART:** 2-wire UART interface; used for debugging by default, baud rate is 115200 bps by default.

Pin definition of the UART interfaces is here as follows:

Table 14: Pin Definition of UART Interfaces

Pin Name	Pin No.	I/O	Description
DBG_TXD	472	DO	Debug UART transmit
DBG_RXD	466	DI	Debug UART receive
UART5_TXD	164	DO	UART5 transmit
UART5_RXD	158	DI	UART5 receive
UART5_CTS	165	DI	DCE clear to send signal from DTE
UART5_RTS	159	DO	DCE request to send signal to DTE
UART16_TXD	475	DO	UART16 transmit
UART16_RXD	469	DI	UART16 receive
UART16_CTS	474	DI	DCE clear to send signal from DTE
UART16_RTS	468	DO	DCE request to send signal to DTE
UART17_TXD	439	DO	UART17 transmit
UART17_RXD	445	DI	UART17 receive
UART17_CTS	444	DI	DCE clear to send signal from DTE
UART17_RTS	438	DO	DCE request to send signal to DTE

UART5/UART16/UART17 are a 4-wire UART interface with 1.8 V power domain. A voltage-level translator chip should be used if your application is equipped with a 3.3 V UART interface. The following figure shows a reference design.

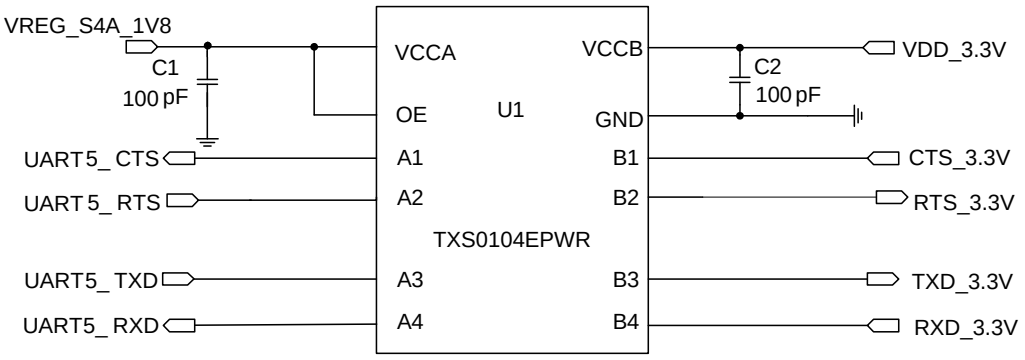

Figure 16: Reference Circuit with Voltage-level Translator Chip (for UART 5)

When the module communicates with PC, voltage-level translator is also required. A voltage-level translator chip and an RS-232 translator chip are recommended to be added. The following figure shows a corresponding reference design.

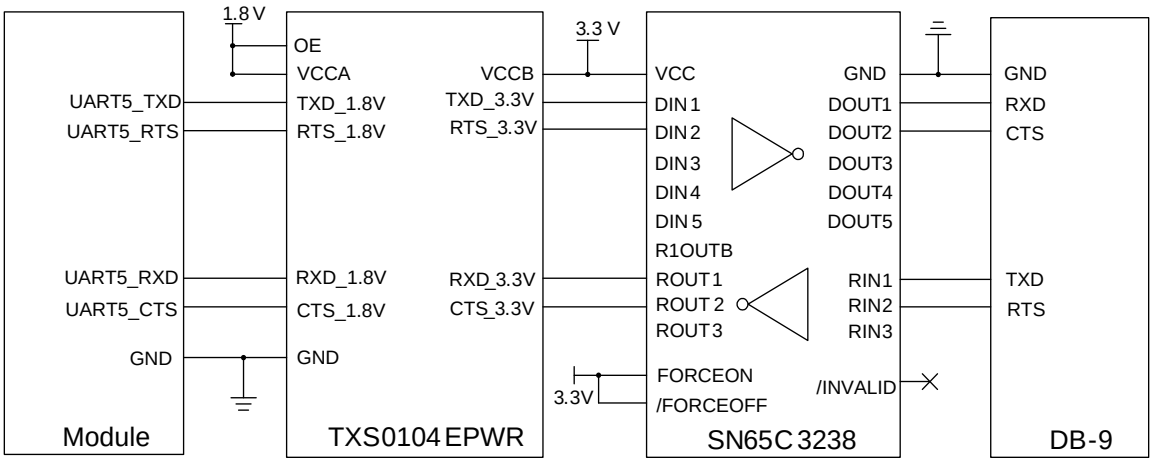

Figure 17: RS-232 Level Matching Circuit (for UART 5)

NOTE

Debug UART, UART16 and UART17 are similar to UART5. For the reference designs, refer to that of UART5.

4.3. SD Card Interface

The module supports SD 3.0 specifications. The pin definition of the SD card interface is shown below.

Table 15: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_CLK	209	DO	SD card clock	-
SD_CMD	215	DIO	SD card command	-
SD_DATA0	226	DIO	SDIO data bit 0	-
SD_DATA1	220	DIO	SDIO data bit 1	-
SD_DATA2	214	DIO	SDIO data bit 2	-
SD_DATA3	208	DIO	SDIO data bit 3	-
SD_DET	203	DI	SD card hot-plug detect	-
SD_LDO9C	197	PO	SD card power supply	$I_O$max = 600 mA Add a 1.0–2.2 μF bypass capacitor if used. If unused, keep this pin open.
SD_LDO6C	228	PO	1.8/2.95 V output power for SD card pull-up circuits	$I_O$max = 150 mA Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open.

A reference circuit for SD card interface is shown below.

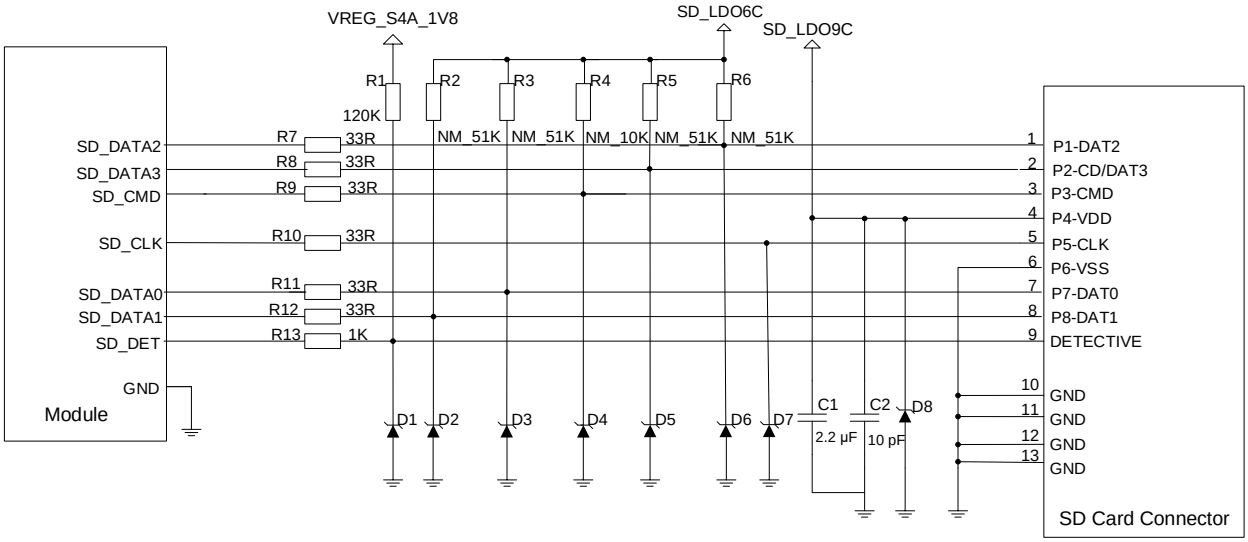

Figure 18: Reference Circuit for SD Card Interface

SD_LDO9C is a peripheral driver power supply for SD card. The maximum drive current is 600 mA. Because of the large drive current, it is recommended that the trace width is 0.6 mm or above. To ensure the stability of drive power, add 2.2 µF and 10 pF capacitors in parallel near the SD card connector.

SD_CMD, SD_CLK, SD_DATA[0:3] are all high-speed signal traces. In PCB design, control the characteristic impedance of them as 45 Ω ±10 %, and do not cross them with other traces. It is recommended to route these traces on the inner layer of PCB, and keep the same trace length for SD_CMD, SD_CLK, SD_DATA[0:3]. Additionally, SD_CLK needs separate ground shielding.

Layout guidelines:

- Control impedance to 45 Ω ±10 %, and add ground shielding for SD_DATA[0:3] traces.
- The total trace length of each signal (except for SD_DET) should be less than 50 mm for SDR 104 mode.
- The trace length difference between SD_CLK and other signal traces like SD_CMD/SD_DATA should not exceed 2 mm for SDR 104 mode.

Table 16: SD Card Signal Trace Length Inside the Module

Signal	Pin No.	Length (mm)	Length Difference (mm)
SD_CLK	209	23.92	1.35
SD_CMD	215	22.83	
SD_DATA0	226	23.23	

SD_DATA1	220	23.82
SD_DATA2	214	23.4
SD_DATA3	208	22.57

4.4. GPIOs

The module has abundant GPIO interfaces with 1.8 V power domain. The pin definition is listed below.

Table 17: Pin Definition of GPIO Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GPIO56	354	DIO	General-purpose input/output	1.8 V power domain.
GPIO57	360	DIO	General-purpose input/output	
GPIO58	359	DIO	General-purpose input/output	
GPIO59	365	DIO	General-purpose input/output	
GPIO60	124	DIO	General-purpose input/output	
GPIO61	120	DIO	General-purpose input/output	
GPIO62	116	DIO	General-purpose input/output	
GPIO63	123	DIO	General-purpose input/output	
GPIO64	458	DIO	General-purpose input/output	
GPIO68	152	DIO	General-purpose input/output	
GPIO70	317	DIO	General-purpose input/output	
GPIO88	146	DIO	General-purpose input/output	
GPIO89	464	DIO	General-purpose input/output	
GPIO119	147	DIO	General-purpose input/output	
GPIO120	142	DIO	General-purpose input/output	
GPIO126	470	DIO	General-purpose input/output	

4.5. I2C Interfaces

The module provides 9 I2C interfaces. All I2C interfaces are open drain signals and therefore you must pull them up externally. The reference power domain is 1.8 V.

Table 18: Pin Definition of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C15_SCL	457	OD	I2C15 serial clock	
I2C15_SDA	463	OD	I2C15 serial data	
TP0_I2C_SCL	454	OD	TP0 I2C clock	
TP0_I2C_SDA	460	OD	TP0 I2C data	
TP1_I2C_SCL	409	OD	TP1 I2C clock	
TP1_I2C_SDA	415	OD	TP1 I2C data	
CCI0_I2C_SDA	151	OD	I2C data of CCI0	
CCI0_I2C_SCL	157	OD	I2C clock of CCI0	
CCI1_I2C_SDA	150	OD	I2C data of CCI1	
CCI1_I2C_SCL	156	OD	I2C clock of CCI1	
CCI2_I2C_SDA	162	OD	I2C data of CCI2	
CCI2_I2C_SCL	168	OD	I2C clock of CCI2	
CCI3_I2C_SDA	174	OD	I2C data of CCI3	
CCI3_I2C_SCL	180	OD	I2C3clock of CCI3	
SENSOR_I2C_SDA	97	OD	I2C clock for external sensor	
SENSOR_I2C_SCL	98	OD	I2C data for external sensor	
NFC_I2C1_SDA	206	OD	I2C data of NFC	
NFC_I2C1_SCL	200	OD	I2C clock of NFC	

4.6. ADC Interfaces

The module provides 4 Analog-to-Digital Converter (ADC) interfaces. To improve the accuracy of ADC, the trace of ADC interfaces should be surrounded by ground.

Table 19: Pin Definition of ADC Interface

Pin Name	Pin No.	I/O	Description	Comment
PM_ADC1	218	AI	General-purpose ADC interface 1	
PM_ADC2	229	AI	General-purpose ADC interface 2	
PM_ADC3	230	AI	General-purpose ADC interface 3	
PM_ADC4	234	AI	General-purpose ADC interface 4	

The accuracy of the ADC is up to 7 mV. The following table describes the characteristic of the ADC interface.

Table 20: Characteristics of ADC Interface

Name	Min.	Typ.	Max.	Unit
ADC1 Voltage Range	0	-	1.8	V
ADC2 Voltage Range	0	-	5.0	V
ADC3 Voltage Range	0	-	1.8	V
ADC4 Voltage Range	0	-	1.8	V
ADC Input Resistance	1	-	-	MΩ
ADC1/ADC3/ADC4 Accuracy (Voltage Range: 0–1.8 V)	-12.5	±7	12.5	mV
ADC2 Accuracy (Voltage Range: 0–5.0 V)	-20	±10	20	mV
ADC Sample Clock	-	4.8	-	MHz

NOTE

1. The input voltage of ADC should not exceed its corresponding voltage range.
2. It is prohibited to supply any voltage to ADC pin when VBAT is removed.

3. It is recommended to use resistor divider circuit for ADC application.

4.7. PCIe Interfaces

The module provides 2 integrated PCIe (Peripheral Component Interconnect Express) interfaces. The key features of the PCIe interfaces are mentioned below:

- *PCI Express Base Specification Revision 3.0* compliance.
- Data rate at 8 Gbps per lane.
- Can be used to connect to an external Ethernet IC (MAC and PHY) or WLAN IC.

Table 21: Pin Definition of PCIe Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCIE1_REFCLK_P	267	DO	PCIe1 reference clock (+)	85 Ω differential impedance.
PCIE1_REFCLK_M	273	DO	PCIe1 reference clock (-)	
PCIE1_TX0_P	281	DO	PCIe1 transmit 0 (+)	
PCIE1_TX0_M	280	DO	PCIe1 transmit 0 (-)	
PCIE1_RX0_P	275	DI	PCIe1 receive 0 (+)	
PCIE1_RX0_M	274	DI	PCIe1 receive 0 (-)	
PCIE1_TX1_P	269	DO	PCIe1 transmit 1 (+)	
PCIE1_TX1_M	268	DO	PCIe1 transmit 1 (-)	
PCIE1_RX1_P	264	DI	PCIe1 receive 1 (+)	
PCIE1_RX1_M	263	DI	PCIe1 receive 1 (-)	
PCIE1_WAKE_N	287	DI	PCIe1 wake up host	
PCIE1_RST_N	293	DO	PCIe1 reset	
PCIE1_CLKREQ_N	299	DI	PCIe1 clock request	
PCIE2_REFCLK_P	395	DO	PCIe2 reference clock (+)	85 Ω differential impedance.
PCIE2_REFCLK_M	396	DO	PCIe2 reference clock (-)	

PCIE2_TX0_P	388	DO	PCIe2 transmit 0 (+)
PCIE2_TX0_M	389	DO	PCIe2 transmit 0 (-)
PCIE2_RX0_P	391	DI	PCIe2 receive 0 (+)
PCIE2_RX0_M	392	DI	PCIe2 receive 0 (-)
PCIE2_TX1_P	390	DO	PCIe2 transmit 1 (+)
PCIE2_TX1_M	394	DO	PCIe2 transmit 1 (-)
PCIE2_RX1_P	393	DI	PCIe2 receive 1 (+)
PCIE2_RX1_M	398	DI	PCIe2 receive 1 (-)
PCIE2_WAKE_N	370	DI	PCIe2 wake up host
PCIE2_RST_N	404	DO	PCIe2 reset
PCIE2_CLKREQ_N	399	DI	PCIe2 clock request

The following figure illustrates the PCIe interface connection.

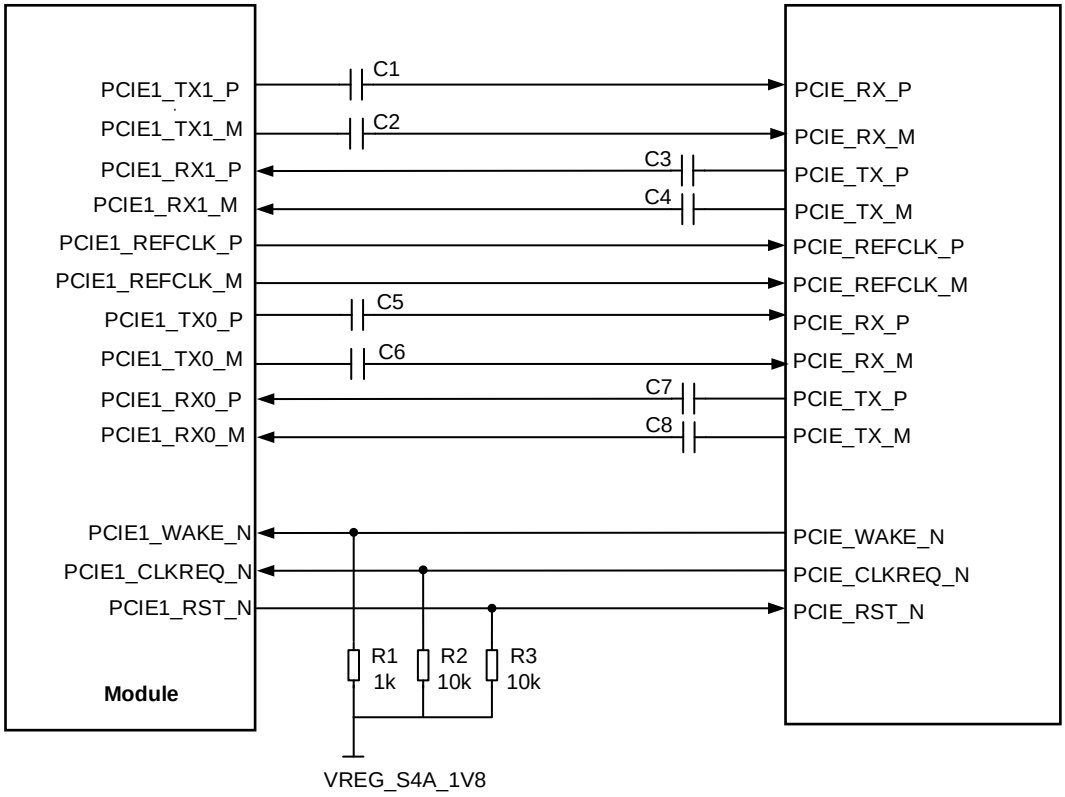

Figure 19: Reference Design of PCIe1 Interfaces

NOTE

The reference design of PCIe2 interface is similar to PCIe1 interface.

The following principles of PCIe interface design should be complied with to meet PCIe specifications.

- It is important to route the PCIe signal traces as differential pairs with ground surrounded. The differential impedance is 70–100 Ω and 85 Ω is recommended.
- PCIe signals must be protected from noisy signals (clocks, DC-DC, RF and so forth). All other sensitive/high-speed signals and circuits must be routed far away from PCIe traces.
- The total trace length of each signal should be less than 300 mm.
- For each differential pair, intra-lane length match (P/M) should be less than 0.7 mm.
- Inter-lane length match, that is, the trace length matching between the reference clock, Tx, and Rx pairs is not required.
- The spacing between Tx and Rx, and the spacing between PCIe lanes and all other signals, should be larger than 4 times of the trace width.
- PCIe Tx AC coupling capacitors can be anywhere along the line, but better to be placed close to source or connector side to keep good SI of main route on PCB.
- Ensure not to stagger the capacitors. This can affect the differential integrity of the design and can create EMI.
- PCIe Tx AC coupling capacitors should be 220 nF for Gen 3, and 100 nF is recommended for Gen 2 application.
- In the case of trace serpentines, one trace of a differential pair must be routed to make up a length delta, then it must be routed at the source (breakout) – this ensures that traces stay differential thereafter.
- To reduce the probability for layer-to-layer manufacturing variation, minimize layer transitions on the main route (in other words, apply layer transitions only at module breakouts and connectors to ensure minimum layer transitions on the main route).

Table 22: PCIe Trace Length Inside the Module

Signal	Pin No.	Length (mm)	Length Difference (mm)
PCIE1_REFCLK_P	267	20.16	-0.26
PCIE1_REFCLK_M	273	20.42	
PCIE1_TX0_P	281	9.26	-0.07
PCIE1_TX0_M	280	9.33	
PCIE1_RX0_P	275	22.55	0.3

PCIE1_RX0_M	274	22.25	
PCIE1_TX1_P	269	17.06	0.09
PCIE1_TX1_M	268	16.97	
PCIE1_RX1_P	264	23.58	-0.24
PCIE1_RX1_M	263	23.82	
PCIE2_REFCLK_P	395	19.38	-0.28
PCIE2_REFCLK_M	396	19.66	
PCIE2_TX0_P	388	22.19	0.35
PCIE2_TX0_M	389	21.84	
PCIE2_RX0_P	391	19.19	-0.24
PCIE2_RX0_M	392	19.43	
PCIE2_TX1_P	390	19.84	0.18
PCIE2_TX1_M	394	19.66	
PCIE2_RX1_P	393	16.49	-0.02
PCIE2_RX1_M	398	16.51	

4.8. Vibrator Drive Interface

The module supports eccentric rotating machines (ERM) and linear resonant actuators (LRA). The pin definition of vibrator drive interface is listed below.

Table 23: Pin Definition of Vibrator Drive Interface

Pin Name	Pin No	I/O	Description	Comment
HAP_P	38	AO	Haptics driver output (+)	
HAP_M	44	AO	Haptics driver output (-)	
HAP_PWM_IN	50	DI	Haptics PWM input	If unused, connect it to GND.

VDD_HAP	27	PI	Power supply for haptics
HAP_BOOST_EN	33	DO	Haptics boost enable

The vibrator is driven by an exclusive circuit, and a reference design is shown below.

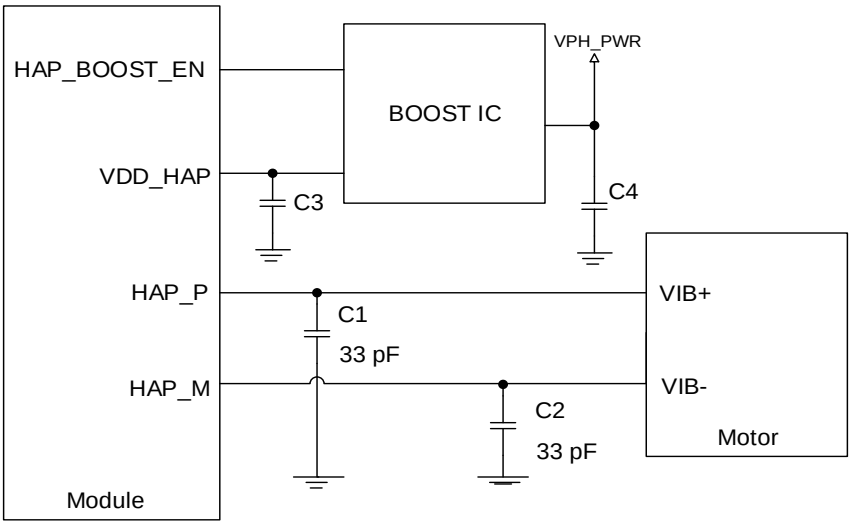

Figure 20: Reference Design for Vibrator Connection

4.9. Wireless Charging Interface

The module provides a wireless charging interface and the Rx integrated circuit of HL6111 is recommended.

Table 24: Pin Definition of Wireless Charging Interface

Pin Name	Pin No.	I/O	Description
WIRELESS_DC_IN_PSNS	1	AI	DC and wireless charging input for power sense
WIRELESS_DC_IN_EN	2	DO	DC and wireless charging output enable and disable
WIRELESS_DC_IN_PON	3	AI	DC and wireless charging power-on trigger
WIRELESS_RST	6	DO	Wireless charging reset.
WIRELESS_THERM	34	AI	Wireless charging temperature detect

4.10. RGB Interfaces

The module provides 3 RGB interfaces, which are with maximal output current up to 12 mA.

Table 25: Pin Definition of RGB Interfaces

Pin Name	Pin No.	I/O	Description
R_LED	219	AO	Current source for red LED
G_LED	213	AO	Current source for green LED
B_LED	207	AO	Current source for blue LED

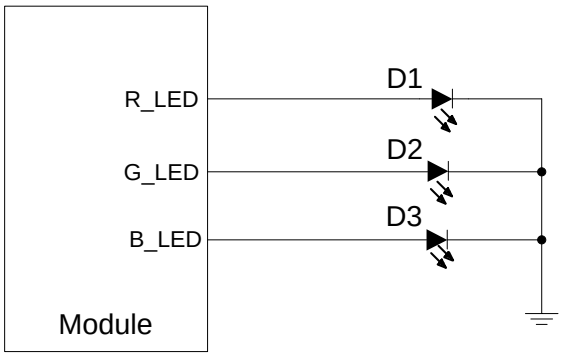

Figure 21: Reference Design for RGB Interfaces

4.11. Keypad Interfaces

The module provides 3 keypad interfaces, which are used for turning on/off the module and adjusting the volume.

Table 26: Pin Definition of Keypad Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	461	DI	Turn on/off the module	PWRKEY pin is pulled to 1.8 V internally.
VOL_UP	473	DI	Volume up	

VOL_DOWN	479	DI	Volume down

4.12. LCM Interfaces

The module provides 2 LCM interfaces, which is MIPI_DSI standard compliant. The interface supports high-speed differential data transmission and supports double 2560 × 1600 @ 60 fps with 4-lane MIPI or 5040 × 2160 @ 60 fps with 8-lane MIPI. The pin definition of the LCM interface is shown below.

Table 27: Pin Definition of LCM Interfaces

Pin Name	Pin No.	I/O	Description
LCD_BL_A	252	PO	Current output for LCD backlight
LCD_BL_K1	240	AI	Current sink for LCD backlight
LCD_BL_K2	244	AI	Current sink for LCD backlight
LCD_BL_K3	247	AI	Current sink for LCD backlight
LCD_BL_K4	250	AI	Current sink for LCD backlight
CABC1	245	DI	Content adaptive brightness control 1
CABC2	241	DI	Content adaptive brightness control 2
LCD0_RST	330	DO	LCD0 reset
LCD0_TE	324	DI	LCD0 tearing effect
LCD1_RST	435	DO	LCD1 reset
LCD1_TE	429	DI	LCD1 tearing effect
DSI0_CLK_P	372	AO	LCD0 MIPI clock (+)
DSI0_CLK_N	375	AO	LCD0 MIPI clock (-)
DSI0_LN0_P	386	AO	LCD0 MIPI lane 0 data (+)
DSI0_LN0_N	387	AO	LCD0 MIPI lane 0 data (-)
DSI0_LN1_P	383	AO	LCD0 MIPI lane 1 data (+)
DSI0_LN1_N	385	AO	LCD0 MIPI lane 1 data (-)

DSI0_LN2_P	380	AO	LCD0 MIPI lane 2 data (+)
DSI0_LN2_N	382	AO	LCD0 MIPI lane 2 data (-)
DSI0_LN3_P	376	AO	LCD0 MIPI lane 3 data (+)
DSI0_LN3_N	379	AO	LCD0 MIPI lane 3 data (-)
DSI1_CLK_P	363	AO	LCD1 MIPI clock (+)
DSI1_CLK_N	368	AO	LCD1 MIPI clock (-)
DSI1_LN0_P	378	AO	LCD1 MIPI lane 0 data (+)
DSI1_LN0_N	384	AO	LCD1 MIPI lane 0 data (-)
DSI1_LN1_P	374	AO	LCD1 MIPI lane 1 data (+)
DSI1_LN1_N	381	AO	LCD1 MIPI lane 1 data (-)
DSI1_LN2_P	369	AO	LCD1 MIPI lane 2 data (+)
DSI1_LN2_N	377	AO	LCD1 MIPI lane 2 data (-)
DSI1_LN3_P	364	AO	LCD1 MIPI lane 3 data (+)
DSI1_LN3_N	373	AO	LCD1 MIPI lane 3 data (-)

The following figures show the reference design for LCM interfaces.

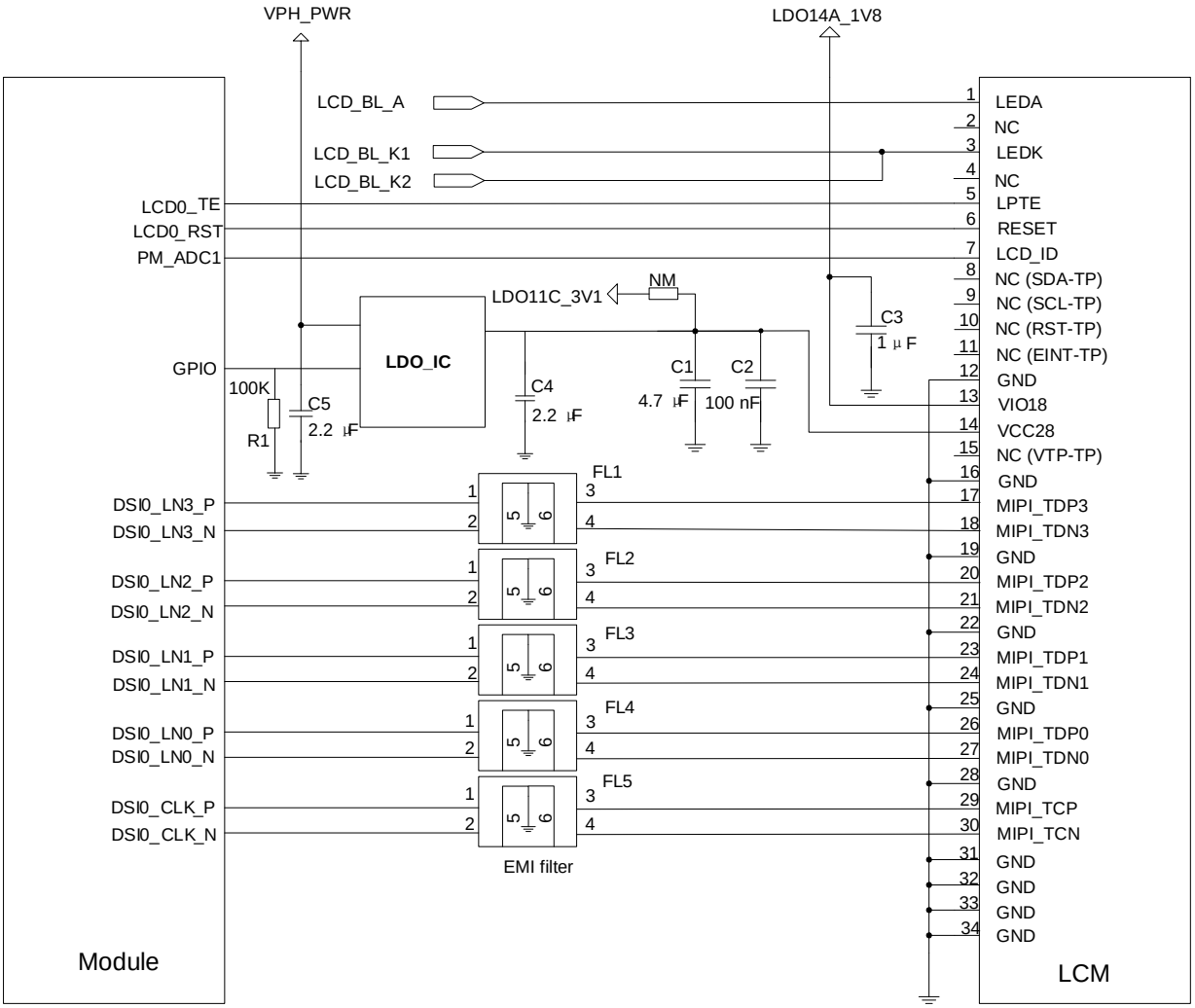

Figure 22: Reference Design for LCM0 Interface

NOTE

The reference design of LCM1 interface is similar to LCM0 interface.

MIPI are high speed signal traces. It is recommended to add common-mode filters in series near the LCM connector to improve protection against electromagnetic radiation interference.

It is recommended to read the LCM ID register through MIPI when compatible design with other displays is required. If several LCMs share the same IC, it is recommended that LCM module factory should burn an OTP register to distinguish different screens. You can also connect the LCD_ID pin of LCM to the ADC pin of the module, but please note that the output voltage of LCD_ID should not exceed the voltage range of the ADC pin.

Backlight driving circuits should be designed for LCMs. The module provides backlight driving output which can be used to drive LCM backlight WLEDs directly. The features are listed below:

- Use the high voltage output (LCD_BL_A) for powering WLED strings, and the output OVP voltage is 32.5 V.
- Support 4 current sinks (LCD_BL_K1, LCD_BL_K2, LCD_BL_K3, LCD_BL_K4), with maximum sink current up to 30 mA for each string.
- Power four strings of WLEDs (about 6s4p WLEDs) with four current sink drivers.

4.13. Touch Panel Interfaces

The module provides 2 I2C interfaces for connection with Touch Panel (TP), and provides the corresponding power supply and interrupt pins. The pin definition of touch panel interfaces is illustrated below.

Table 28: Pin Definition of Touch Panel Interfaces

Pin Name	Pin No.	I/O	Description	Comment
TP0_RST	455	DO	TP0 reset	1.8 V power domain.
TP0_INT	449	DI	TP0 interrupt	
TP0_I2C_SCL	454	OD	TP0 I2C clock	
TP0_I2C_SDA	460	OD	TP0 I2C data	
TP1_RST	421	DO	TP1 reset	
TP1_INT	427	DI	TP1 interrupt	
TP1_I2C_SCL	409	OD	TP1 I2C clock	
TP1_I2C_SDA	415	OD	TP1 I2C data	

A reference design for TP interfaces is shown below.

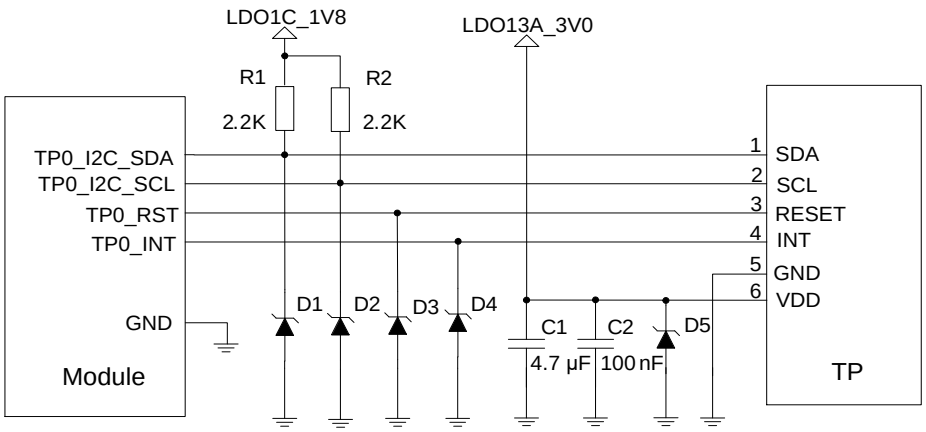

Figure 23: Reference Design for TP0 Interface

NOTE

The reference design of TP1 interface is similar to TP0 interface.

4.14. Camera Interfaces

Based on the standard MIPI CSI video input interface, the module supports 7 cameras, and the maximum pixel of the camera can be up to 64 MP. The video and photo quality are determined by various factors such as the camera sensor, camera lens quality, etc. CCI_I2C/I3C signals are controlled by Linux Kernel code and support connection with video output related devices.

Table 29: Pin Definition of Camera Interfaces

Pin Name	Pin No.	I/O	Description	Comment
CSI0_CLK_P	255	AI	MIPI clock of camera 0 (+)	
CSI0_CLK_N	258	AI	MIPI clock of camera 0 (-)	
CSI0_LN0_P	266	AI	MIPI lane 0 data of camera 0 (+)	
CSI0_LN0_N	265	AI	MIPI lane 0 data of camera 0 (-)	
CSI0_LN1_P	261	AI	MIPI lane 1 data of camera 0 (+)	
CSI0_LN1_N	260	AI	MIPI lane 1 data of camera 0 (-)	

CSI0_LN2_P	257	AI	MIPI lane 2 data of camera 0 (+)
CSI0_LN2_N	256	AI	MIPI lane 2 data of camera 0 (-)
CSI0_LN3_P	254	AI	MIPI lane 3 data of camera 0 (+)
CSI0_LN3_N	253	AI	MIPI lane 3 data of camera 0 (-)
CSI1_CLK_P	298	AI	MIPI clock of camera 1 (+)
CSI1_CLK_N	292	AI	MIPI clock of camera 1 (-)
CSI1_LN0_P	322	AI	MIPI lane 0 data of camera 1 (+)
CSI1_LN0_N	321	AI	MIPI lane 0 data of camera 1 (-)
CSI1_LN1_P	316	AI	MIPI lane 1 data of camera 1 (+)
CSI1_LN1_N	315	AI	MIPI lane 1 data of camera 1 (-)
CSI1_LN2_P	310	AI	MIPI lane 2 data of camera 1 (+)
CSI1_LN2_N	309	AI	MIPI lane 2 data of camera 1 (-)
CSI1_LN3_P	304	AI	MIPI lane 3 data of camera 1 (+)
CSI1_LN3_N	303	AI	MIPI lane 3 data of camera 1 (-)
CSI2_CLK_P	285	AI	MIPI clock of camera 2 (+)
CSI2_CLK_N	291	AI	MIPI clock of camera 2 (-)
CSI2_LN0_P	290	AI	MIPI lane 0 data of camera 2 (+)
CSI2_LN0_N	295	AI	MIPI lane 0 data of camera 2 (-)
CSI2_LN1_P	284	AI	MIPI lane 1 data of camera 2 (+)
CSI2_LN1_N	289	AI	MIPI lane 1 data of camera 2 (-)
CSI2_LN2_P	278	AI	MIPI lane 2 data of camera 2 (+)
CSI2_LN2_N	283	AI	MIPI lane 2 data of camera 2 (-)

CSI2_LN3_P	272	AI	MIPI lane 3 data of camera 2 (+)
CSI2_LN3_N	277	AI	MIPI lane 3 data of camera 2 (-)
CSI3_CLK_P	366	AI	MIPI clock of camera 3 (+)
CSI3_CLK_N	362	AI	MIPI clock of camera 3 (-)
CSI3_LN0_P	343	AI	MIPI lane 0 data of camera 3 (+)
CSI3_LN0_N	338	AI	MIPI lane 0 data of camera 3 (-)
CSI3_LN1_P	349	AI	MIPI lane 1 data of camera 3 (+)
CSI3_LN1_N	344	AI	MIPI lane 1 data of camera 3 (-)
CSI3_LN2_P	355	AI	MIPI lane 2 data of camera 3 (+)
CSI3_LN2_N	350	AI	MIPI lane 2 data of camera 3 (-)
CSI3_LN3_P	361	AI	MIPI lane 3 data of camera 3 (+)
CSI3_LN3_N	356	AI	MIPI lane 3 data of camera 3 (-)
CSI4_CLK_P	302	AI	MIPI clock of camera 4 (+)
CSI4_CLK_N	307	AI	MIPI clock of camera 4 (-)
CSI4_LN0_P	326	AI	MIPI lane 0 data of camera 4 (+)
CSI4_LN0_N	331	AI	MIPI lane 0 data of camera 4 (-)
CSI4_LN1_P	320	AI	MIPI lane 1 data of camera 4 (+)
CSI4_LN1_N	325	AI	MIPI lane 1 data of camera 4 (-)
CSI4_LN2_P	314	AI	MIPI lane 2 data of camera 4 (+)
CSI4_LN2_N	319	AI	MIPI lane 2 data of camera 4 (-)
CSI4_LN3_P	308	AI	MIPI lane 3 data of camera 4 (+)
CSI4_LN3_N	313	AI	MIPI lane 3 data of camera 4 (-)

CSI5_CLK_P	335	AI	MIPI clock of camera 5 (+)
CSI5_CLK_N	329	AI	MIPI clock of camera 5 (-)
CS5_LN0_P	352	AI	MIPI lane 0 data of camera 5 (+)
CSI5_LN0_N	351	AI	MIPI lane 0 data of camera 5 (-)
CSI5_LN1_P	346	AI	MIPI lane 1 data of camera 5 (+)
CSI5_LN1_N	345	AI	MIPI lane 1 data of camera 5 (-)
CSI5_LN2_P	340	AI	MIPI lane 2 data of camera 5 (+)
CSI5_LN2_N	339	AI	MIPI lane 2 data of camera 5 (-)
CSI5_LN3_P	334	AI	MIPI lane 3 data of camera 5 (+)
CSI5_LN3_N	333	AI	MIPI lane 3 data of camera 5 (-)
CAM0_MCLK	118	DO	Master clock of camera 0
CAM1_MCLK	112	DO	Master clock of camera 1
CAM2_MCLK	107	DO	Master clock of camera 2
CAM3_MCLK	99	DO	Master clock of camera 3
CAM4_MCLK	96	DO	Master clock of camera 4
CAM5_MCLK	108	DO	Master clock of camera 5
CAM6_MCLK	100	DO	Master clock of camera 6
CAM0_RST	119	DO	Reset of camera 0
CAM1_RST	114	DO	Reset of camera 1
CAM2_RST	109	DO	Reset of camera 2
CAM3_RST	103	DO	Reset of camera 3
CAM4_RST	115	DO	Reset of camera 4
CAM5_RST	110	DO	Reset of camera 5
CAM6_RST	104	DO	Reset of camera 6
CCI0_I2C_SDA	151	OD	I2C data of CCI0

CCI0_I2C_SCL	157	OD	I2C clock of CCI0	
CCI1_I2C_SDA	150	OD	I2C data of CCI1	
CCI1_I2C_SCL	156	OD	I2C clock of CCI1	
CCI2_I2C_SDA	162	OD	I2C data of CCI2	
CCI2_I2C_SCL	168	OD	I2C clock of CCI2	
CCI3_I2C_SDA	174	OD	I2C data of CCI3	
CCI3_I2C_SCL	180	OD	I2C3clock of CCI3	
CCI_I3C_SDA	462	OD	I3C data of CCI	
CCI_I3C_SCL	456	OD	I3C clock of CCI	
LDO1F_1V1	36	PO	1.1 V output	Power supply for DVDD of camera. Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open.
LDO2F_1V2	48	PO	1.2 V output	Power supply for DVDD of camera. Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open.
LDO3F_1V05	35	PO	1.05 V output	Power supply for DVDD of camera. Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open.
LDO4F_1V2*	47	PO	1.2 V output	Power supply for DVDD of camera. Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open.
LDO5F_2V85	60	PO	2.85 V output	Power supply for AVDD of camera. Add a 4.7 μF bypass capacitor if used. If unused, keep this pin open.
LDO6F_2V8	59	PO	2.8 V output	Power supply for AVDD of camera. Add a 4.7 μF bypass capacitor if used.

				If unused, keep this pin open.
LDO7F_1V8	71	PO	1.8 V output	Power supply for DOVDD of camera. Add a 4.7 μF bypass capacitor if used. If unused, keep this pin open.

The following is a reference circuit design for camera applications.

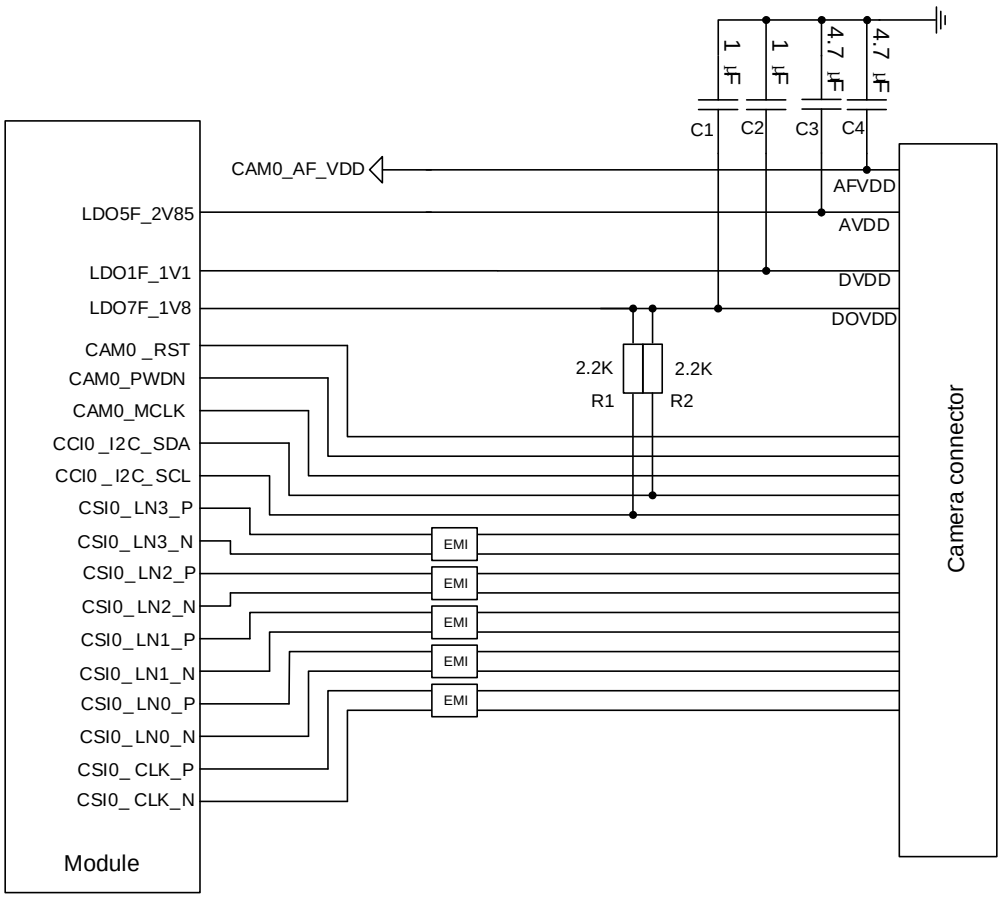

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Figure 24: Reference Design for Camera0 Application

NOTE

The reference design of CSI1, CSI2, CSI3, CSI4 and CSI5 interfaces is similar to CSI0 interface.

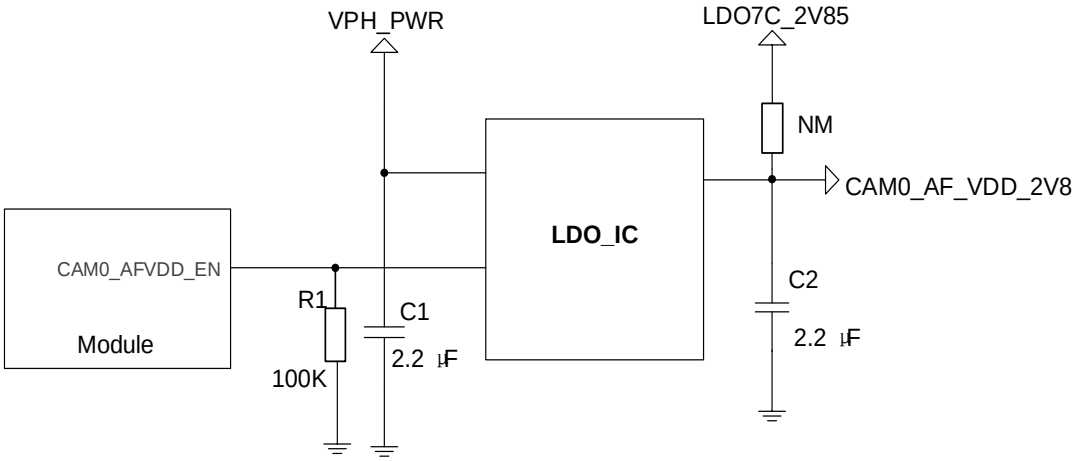


Figure 25: Reference Design of Camera Power Supply

NOTE

CAM0_AFVDD_EN pin can be multiplexed from UART17_CTS.

4.14.1. Design Considerations

- Special attention should be paid to the pin definition of LCM/camera connectors. Assure the module and the connectors are correctly connected.
- MIPI is high speed signal traces, supporting maximum data rate up to 2.5 Gbps. The differential impedance should be controlled to 85 Ω. Additionally, it is recommended to route the trace on the inner layer of PCB, and do not cross it with other traces. For the same group of DSI or CSI signals, all the MIPI traces should keep the same length.
- To avoid crosstalk, spacing the lanes according to the following rules:
  a) Intra-pair P to N: 1 × trace width
  b) lane to lane: 1.5 × trace width
  c) lanes to all other signals: 2.5 × trace width
- It is recommended to select a low capacitance TVS for ESD protection and the recommended parasitic capacitance should be below 0.5 pF.
- Route MIPI traces according to the following rules:
  a) The total trace length should be less than 150 mm with -6.5 dB total insertion loss and -3.5 dB cable insertion loss for 2.5 Gbps;
  b) Control the differential impedance to 85 Ω ±10 %;
  c) Control intra-pair length matching (P/N) within 0.7 mm;
  d) Control inter-lane length matching within 1.4 mm.

Table 30: MIPI Trace Length Inside the Module

Signal	Pin No.	Length (mm)	Length Difference (mm)
DSI0_CLK_P	372	22.56	0.15
DSI0_CLK_N	375	22.41	
DSI0_LN0_P	386	22.80	-0.24
DSI0_LN0_N	387	23.04	
DSI0_LN1_P	383	22.85	0.31
DSI0_LN1_N	385	22.54	
DSI0_LN2_P	380	22.40	-0.17
DSI0_LN2_N	382	22.57	
DSI0_LN3_P	376	22.89	0.04
DSI0_LN3_N	379	22.85	
DSI1_CLK_P	363	25.24	0.08
DSI1_CLK_N	368	25.16	
DSI1_LN0_P	378	25.78	0.3
DSI1_LN0_N	384	25.48	
DSI1_LN1_P	374	25.69	0.16
DSI1_LN1_N	381	25.53	
DSI1_LN2_P	369	24.99	-0.01
DSI1_LN2_N	377	25	
DSI1_LN3_P	364	25.06	0.25
DSI1_LN3_N	373	24.81	
CSI0_CLK_P	255	19.59	0.32
CSI0_CLK_N	258	19.27	
CSI0_LN0_P	266	19	0.27

CSI0_LN0_N	265	18.73	
CSI0_LN1_P	261	18.78	0.08
CSI0_LN1_N	260	18.70	
CSI0_LN2_P	257	19.89	0.34
CSI0_LN2_N	256	19.55	
CSI0_LN3_P	254	19.25	-0.12
CSI0_LN3_N	253	19.37	
CSI1_CLK_P	298	18.14	-0.06
CSI1_CLK_N	292	18.2	
CSI1_LN0_P	322	18.57	0.26
CSI1_LN0_N	321	18.31	
CSI1_LN1_P	316	18.08	-0.09
CSI1_LN1_N	315	18.17	
CSI1_LN2_P	310	17.87	0.24
CSI1_LN2_N	309	17.63	
CSI1_LN3_P	304	18.84	0.08
CSI1_LN3_N	303	18.76	
CSI2_CLK_P	285	14.82	0.05
CSI2_CLK_N	291	14.77	
CSI2_LN0_P	290	14.27	-0.22
CSI2_LN0_N	295	14.49	
CSI2_LN1_P	284	14.63	0.24
CSI2_LN1_N	289	14.39	
CSI2_LN2_P	278	14.3	-0.13
CSI2_LN2_N	283	14.43	

CSI2_LN3_P	272	14.83	0.3
CSI2_LN3_N	277	14.53	
CSI3_CLK_P	366	31.35	-0.28
CSI3_CLK_N	362	31.63	
CSI3_LN0_P	343	30.96	-0.12
CSI3_LN0_N	338	31.08	
CSI3_LN1_P	349	31.16	0.22
CSI3_LN1_N	344	30.94	
CSI3_LN2_P	355	30.94	-0.04
CSI3_LN2_N	350	30.98	
CSI3_LN3_P	361	31.86	0.25
CSI3_LN3_N	356	31.61	
CSI4_CLK_P	302	14.90	0.23
CSI4_CLK_N	307	14.67	
CSI4_LN0_P	326	15.38	0.07
CSI4_LN0_N	331	15.31	
CSI4_LN1_P	320	14.67	0
CSI4_LN1_N	325	14.67	
CSI4_LN2_P	314	15.83	-0.12
CSI4_LN2_N	319	15.95	
CSI4_LN3_P	308	14.62	-0.03
CSI4_LN3_N	313	14.65	
CSI5_CLK_P	335	19.20	-0.25
CSI5_CLK_N	329	19.45	
CS5_LN0_P	352	19.48	0.21

CSI5_LN0_N	351	19.27	
CSI5_LN1_P	346	18.92	0.28
CSI5_LN1_N	345	18.64	
CSI5_LN2_P	340	18.65	-0.02
CSI5_LN2_N	339	18.67	
CSI5_LN3_P	334	19.26	-0.19
CSI5_LN3_N	333	19.45	

Table 31: CSI and DSI Data Rate and Max. Trace Length (D-PHY)

Data Rate	Total Insertion Loss (dB)	Cable Insertion Loss (dB)	Max. Trace Length (mm)
500 Mbps/lane	-2.1	-0.5	< 260
		-1	< 190
750 Mbps/lane	-2.3	-0.7	< 210
		-1.15	< 155
1.0 Gbps/lane	-2.3	-0.75	< 200
		-1.4	< 125
1.5 Gbps/lane	-2.5	-0.9	< 145
		-1.8	< 60
2.1 Gbps/lane	-2.5	-1.3	< 170
		-2.3	< 90
2.5 Gbps/lane	-2.5	-2.1	< 210
		-3.5	<150

4.14.2. Flashlight Interfaces

The module supports 3 flash LED drivers, FLASH_LED1 and FLASH_LED2 are both with maximal output current up to 1.5 A per channel in flash mode and 300 mA in torch mode. FLASH_LED3 with maximal output current up to 0.75 A in flash mode and 300 mA in torch mode.

Table 32: Pin Definition of Flashlight Interfaces

Pin Name	Pin No.	I/O	Description	Comment
FLASH_LED1	249	AO	Flash/torch driver output 1	
FLASH_LED2	242	AO	Flash/torch driver output 2	
FLASH_LED3	243	AO	Flash/torch driver output 3	
FLASH_STROBE	237	DI	Flash LED strobe	If unused, connect it to GND.

A reference circuit design is shown below.

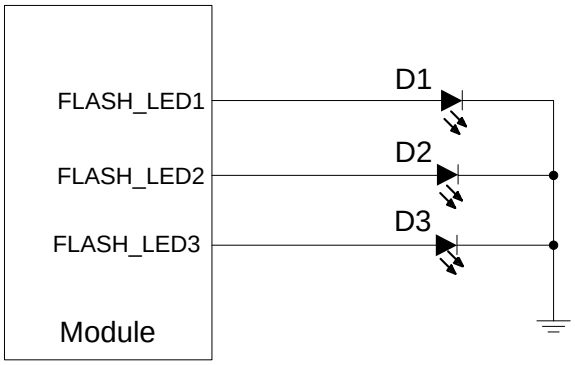


Figure 26: Reference Design for Flashlight Interfaces

4.15. Sensor Interfaces

The module supports communication with sensors via I2C/I3C/SPI interface, and it supports various sensors such as acceleration sensor, gyroscopic sensor, compass, light sensor, temperature sensor, etc. The SENSOR_I2C/I3C interface only supports sensors of the aDSP architecture.

Table 33: Pin Definition of Sensor Interfaces

Pin Name	Pin No.	I/O	Description
SENSOR_I2C_SDA	97	OD	I2C clock for external sensor
SENSOR_I2C_SCL	98	OD	I2C data for external sensor
SENSOR_I3C_SDA	72	OD	I3C data for external sensor
SENSOR_I3C_SCL	83	OD	I3C clock for external sensor
SENSOR_SPI_CLK	89	DO	SPI clock for external sensor
SENSOR_SPI_CS	95	DO	SPI chip select for external sensor
SENSOR_SPI_MOSI	78	DO	SPI master-out slave-in for external sensor
SENSOR_SPI_MISO	84	DI	SPI master-in slave-out for external sensor
MAG_INT	163	DI	MAG interrupt
HALL_INT	169	DI	HALL interrupt
ALPS_INT	175	DI	ALPS interrupt
IMU_INT1	141	DI	IMU interrupt 1
IMU_INT2	145	DI	IMU interrupt 2

4.16. Audio Interfaces

The module provides SoundWire and digital MIC interface. One SoundWire interface which dedicated to transmit data between the module and analog codec WCD938x. The other SoundWire interface which dedicated to transmit data between the module and audio amplifier WSA881x.

Table 34: Pin Definition of Audio Interfaces

Pin Name	Pin No.	I/O	Description
WSA1_EN	45	DO	WSA enable 1
WSA2_EN	51	DO	WSA enable 2
WSA_SWR_CLK	43	DO	WSA SoundWire clock

WSA_SWR_DATA	49	DIO	WSA SoundWire data
WCD_RST	88	DO	WCD reset
WCD_SWR_TX_CLK	92	DO	WCD SoundWire transmit clock
WCD_SWR_TX_DATA0	91	DO	WCD SoundWire transmit data 0
WCD_SWR_TX_DATA1	87	DO	WCD SoundWire transmit data 1
WCD_SWR_RX_CLK	82	DO	WCD SoundWire receive clock
WCD_SWR_RX_DATA0	85	DI	WCD SoundWire receive data 0
WCD_SWR_RX_DATA1	81	DI	WCD SoundWire receive data 1
LPI_DMIC3_CLK	46	DO	LPI digital MIC3 clock
LPI_DMIC3_DATA	52	DI	LPI digital MIC3 data

4.17. I2S Interfaces

The module provides three I2S interfaces which can support TDM function and also can be multiplexed to PCM. For more details about PCM interface, see ***document [2]***. The following table shows the pin definition.

Table 35: Pin Definition of I2S Interfaces

Pin Name	Pin No.	I/O	Description
LPI_MI2S1_SCLK	62	DO	LPI MI2S1 bit clock
LPI_MI2S1_WS	58	DO	LPI MI2S1 word select
LPI_MI2S1_DATA0	67	DIO	LPI MI2S1 Data channel 0
LPI_MI2S1_DATA1	61	DIO	LPI MI2S1 Data channel 1
MI2S0_MCLK	63	DO	MI2S0 master clock
MI2S0_SCLK	64	DO	MI2S0 bit clock
MI2S0_WS	80	DO	MI2S0 word select
MI2S0_DATA0	70	DIO	MI2S0 data channel 0

MI2S0_DATA1	75	DIO	MI2S0 data channel 1
MI2S2_SCLK	73	DO	MI2S2 bit clock
MI2S2_WS	68	DO	MI2S2 word select
MI2S2_DATA0	69	DIO	MI2S2 data channel 0
MI2S2_DATA1	74	DIO	MI2S2 data channel 1

4.18. SPI Interfaces

The module provides 5 SPI interfaces. These interfaces can only support the master mode. SPI interfaces can be used for fingerprint recognition.

Table 36: Pin Definition of SPI Interfaces

Pin Name	Pin No.	I/O	Description
SPI2_CLK	204	DO	SPI2 clock
SPI2_CS	198	DO	SPI2 chip select
SPI2_MISO	205	DI	SPI2 master-in slave-out
SPI2_MOSI	199	DO	SPI2 master-out slave-in
SPI4_CLK	187	DO	SPI4 clock
SPI4_CS	181	DO	SPI4 chip select
SPI4_MISO	192	DI	SPI4 master-in slave-out
SPI4_MOSI	186	DO	SPI4 master-out slave-in
FP_SPI14_CLK	342	DO	FP SPI14 clock
FP_SPI14_CS	353	DO	FP SPI14 chip select
FP_SPI14_MISO	347	DI	FP SPI14 master-in slave-out
FP_SPI14_MOSI	348	DO	FP SPI14 master-out slave-in
NFC_SE_SPI8_CLK	183	DO	NFC SE SPI8 clock
NFC_SE_SPI8_CS	177	DO	NFC SE SPI8 chip select

NFC_SE_SPI8_MISO	182	DI	NFC SE SPI8 master-in slave-out
NFC_SE_SPI8_MOSI	176	DO	NFC SE SPI8 master-out slave-in
SENSOR_SPI_CLK	89	DO	SPI clock for external sensor
SENSOR_SPI_CS	95	DO	SPI chip select for external sensor
SENSOR_SPI_MOSI	78	DO	SPI master-out slave-in for external sensor
SENSOR_SPI_MISO	84	DI	SPI master-in slave-out for external sensor

4.19. USB_BOOT

USB_BOOT is an emergency download interface. Pull it up to VREG_S4A_1V8 when booting, the module can enter the emergency download mode. There is an emergency option when failures such as abnormal start-up or running occur. For the convenient firmware upgrade and debugging in the future, reserve this pin. The reference circuit design is shown below.

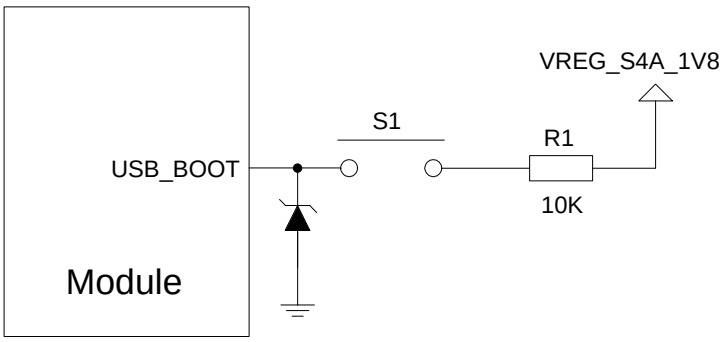


Figure 27: Reference Design for USB_BOOT

5 RF Specifications

5.1. RF Antenna Interface

This module provides 3 antennas, one of which is Wi-Fi/Bluetooth antenna (Wi-Fi and Bluetooth functions share the same antenna), one antenna is single Wi-Fi and one antenna is reserved for Bluetooth. The interface impedance is 50 Ω.

You can connect external antennas such as PCB antenna, sucker antenna and ceramic antenna to the module via these interfaces to achieve Wi-Fi and Bluetooth functions.

5.1.1. Antenna Interface and Frequency Bands

Table 37: Pin Definition of Wi-Fi/Bluetooth Application Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_BT*	133	AIO	Bluetooth antenna interface	Reserved
ANT_WIFI0	143	AIO	Wi-Fi0/Bluetooth antenna interface	
ANT_WIFI1	172	AIO	Wi-Fi1 antenna interface	

5.1.2. Reference Design

A reference circuit design for Wi-Fi/Bluetooth antenna interface is shown as below. To facilitate future debugging, it is recommended to add a π type matching circuit in antenna circuit design. C1 and C2 are not mounted and a 0 Ω resistor (R1) is mounted by default.

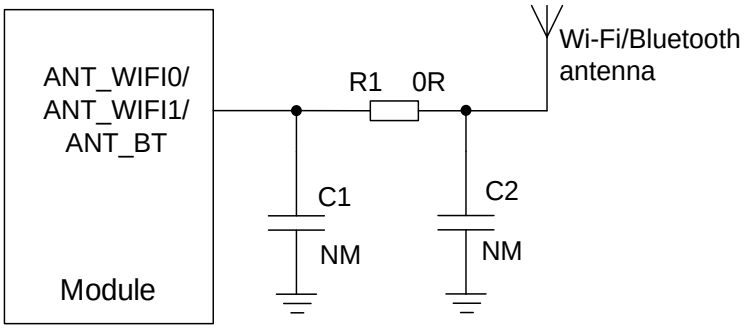


Figure 28: Reference Design for Wi-Fi/Bluetooth Antenna Interface

NOTE

The dedicated Bluetooth antenna circuit should be reserved for future debugging.

5.2. RF Performance

Table 38: Pin Definition of Wi-Fi/Bluetooth Application Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PA_MUTE	190	DI	Wi-Fi xFEM control to disable Wi-Fi PA	If unused, connect it to GND.
WLAN_TXEN	179	DO	Wi-Fi xFEM control to enable Wi-Fi transmit	If unused, connect it to GND with a 10 kΩ resistor.
LAA_RX	196	DI	Wi-Fi xFEM control for LAA/n79 receiver	If unused, connect it to GND
LAA_TXEN	185	DO	Wi-Fi xFEM control to enable LAA/n79 transmit	If unused, connect it to GND.
LAA_AS_EN	129	DI	Allow LAA/n79 to control Wi-Fi xFEM during Wi-Fi sleep mode	If unused, connect it to GND with a 10 kΩ resistor.
COEX_RXD	121	DI	2.4 GHz WWAN & Wi-Fi/Bluetooth coexistence receive	If unused, connect it to GND.
COEX_TXD	125	DO	2.4 GHz WWAN & Wi-Fi/Bluetooth coexistence transmit	If unused, connect it to GND with a 10 kΩ resistor.

Table 39: Wi-Fi/Bluetooth Frequency

Type	Frequency	Unit
Wi-Fi	2402–2482 5170–5835	MHz
BLE 5.1	2402–2480	MHz

5.2.1. Wi-Fi Overview

The module supports 2.4 GHz and 5 GHz double-band WLAN wireless communication based on IEEE 802.11a/b/g/n/ac/ax standard protocols. The maximum data rate is up to 1774.5 Mbps (2 × 2 + 2 × 2 11ax DBS).

The following table lists the Wi-Fi transmitting and receiving performance of the module.

Table 40: Wi-Fi Transmitting Performance

Frequency Bands	Standard	Rate	Output Power
2.4 GHz	802.11b	1 Mbps	18 dBm ±2.5 dB
	802.11b	11 Mbps	18 dBm ±2.5 dB
	802.11g	6 Mbps	18 dBm ±2.5 dB
	802.11g	54 Mbps	17 dBm ±2.5 dB
	802.11n HT20	MCS0	18 dBm ±2.5 dB
	802.11n HT20	MCS7	16 dBm ±2.5 dB
	802.11n HT40	MCS0	18 dBm ±2.5 dB
	802.11n HT40	MCS7	15dBm ±2.5 dB
	802.11ax HE20	MCS0	18 dBm ±2.5 dB
	802.11ax HE20	MCS11	12 dBm ±2.5 dB
	802.11ax HE40	MCS0	18dBm ±2.5 dB
	802.11ax HE40	MCS11	12 dBm ±2.5 dB
5 GHz	802.11a	6 Mbps	18 dBm ±2.5 dB

	802.11a	54 Mbps	15 dBm ±2.5 dB
	802.11n HT20	MCS0	18 dBm ±2.5 dB
	802.11n HT20	MCS7	15 dBm ±2.5 dB
	802.11n HT40	MCS0	18 dBm ±2.5 dB
	802.11n HT40	MCS7	15 dBm ±2.5 dB
	802.11ac VHT20	MCS0	18 dBm ±2.5 dB
	802.11ac VHT20	MCS8	14 dBm ±2.5 dB
	802.11ac VHT40	MCS0	18 dBm ±2.5 dB
	802.11ac VHT40	MCS9	14 dBm ±2.5 dB
	802.11ac VHT80	MCS0	18 dBm ±2.5 dB
	802.11ac VHT80	MCS9	14 dBm ±2.5 dB
	802.11ax HE20	MCS0	18 dBm ±2.5 dB
	802.11ax HE20	MCS11	12 dBm ±2.5 dB
	802.11ax HE40	MCS0	18 dBm ±2.5 dB
	802.11ax HE40	MCS11	12 dBm ±2.5 dB
	802.11ax HE80	MCS0	18 dBm ±2.5 dB
	802.11ax HE80	MCS11	12 dBm ±2.5 dB

Table 41: Wi-Fi Receiving Performance

Frequency Bands	Standard	Rate	Sensitivity
2.4 GHz	802.11b	1 Mbps	-96 dBm
	802.11b	11 Mbps	-90 dBm
	802.11g	6 Mbps	-94 dBm
	802.11g	54 Mbps	-77 dBm
	802.11n HT20	MCS0	-92 dBm

	802.11n HT20	MCS7	-73 dBm
	802.11n HT40	MCS0	-90 dBm
	802.11n HT40	MCS7	-69 dBm
	802.11ax HE20	MCS0	-93 dBm
	802.11ax HE20	MCS11	-64 dBm
	802.11ax HE40	MCS0	-92 dBm
	802.11ax HE40	MCS11	-62 dBm
5 GHz	802.11a	6Mbps	-95 dBm
	802.11a	54Mbps	-78 dBm
	802.11n HT20	MCS0	-93 dBm
	802.11n HT20	MCS7	-74 dBm
	802.11n HT40	MCS0	-90 dBm
	802.11n HT40	MCS7	-71 dBm
	802.11ac VHT20	MCS0	-94 dBm
	802.11ac VHT20	MCS8	-72 dBm
	802.11ac VHT40	MCS0	-92 dBm
	802.11ac VHT40	MCS9	-68 dBm
	802.11ac VHT80	MCS0	-88 dBm
	802.11ac VHT80	MCS9	-64 dBm
	802.11ax HE20	MCS0	-94 dBm
	802.11ax HE20	MCS11	-62 dBm
	802.11ax HE40	MCS0	-92 dBm
	802.11ax HE40	MCS11	-63 dBm
	802.11ax HE80	MCS0	-87 dBm
	802.11ax HE80	MCS11	-58 dBm

NOTE

The module conforms to the IEEE specifications.

5.2.2. Bluetooth Overview

The module supports Bluetooth 5.1 (BR/EDR + BLE) specification, as well as GFSK, 8-DPSK, Π/4-DQPSK modulation modes.

The BR/EDR channel bandwidth is 1 MHz, and can accommodate 79 channels. The BLE channel bandwidth is 2 MHz, and can accommodate 40 channels.

The following table lists the Bluetooth transmitting and receiving performance of the module.

Table 42: Bluetooth Transmitting and Receiving Performance

Transmitting Performance	Conducted RF Output Power
GFSK	12 dBm ±2.5 dB
π/4-DQPSK	12 dBm ±2 dB
8-DQPSK	12 dBm ±2 dB
BLE_1M	11.5 dBm ±2.5 dB
BLE_2M	11.5 dBm ±2.5 dB
Receiving Performance	**Conducted RF Receiving Sensitivity**
GFSK	-92 dBm
π/4-DQPSK	-90 dBm
8-DQPSK	-85 dBm
BLE_1M	-98 dBm
BLE_2M	-96 dBm

5.3. Reference Design of RF Routing

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

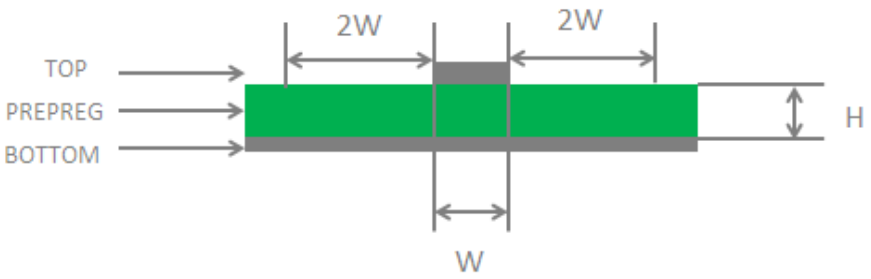


Figure 29: Microstrip Design on a 2-layer PCB

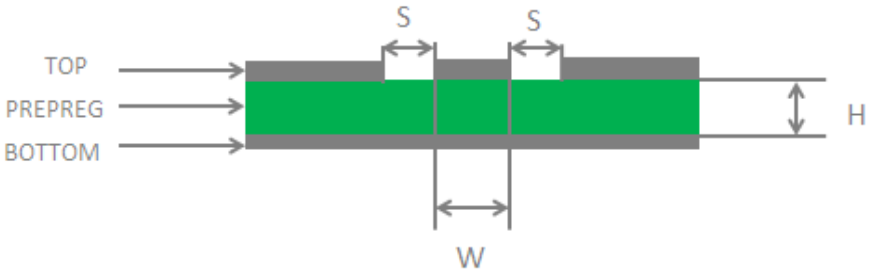


Figure 30: Coplanar Waveguide Design on a 2-layer PCB

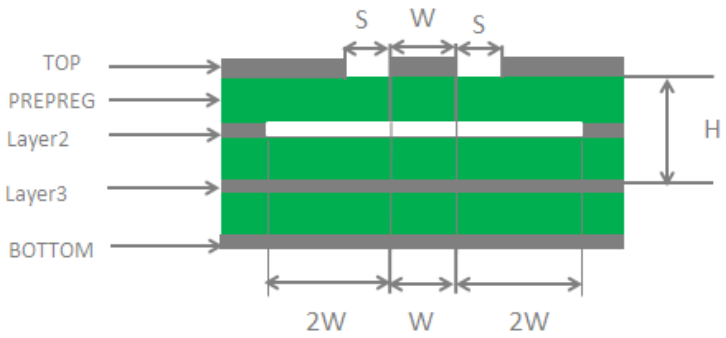


Figure 31: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

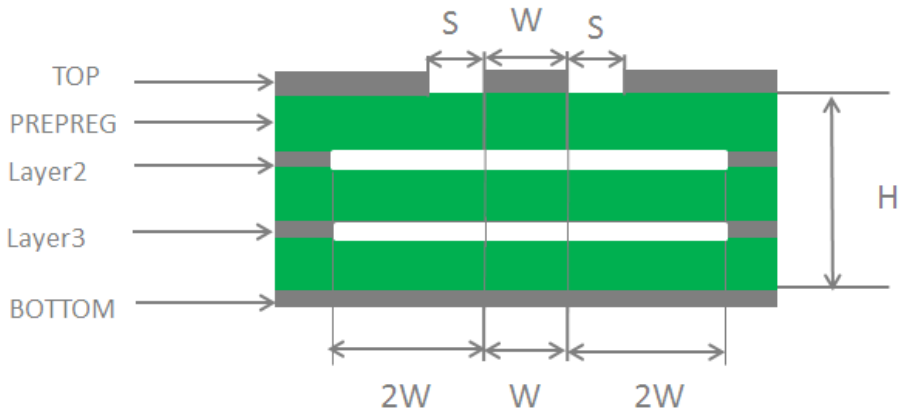


Figure 32: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design :

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).

For more details about RF layout, see ***document [3]***.

5.4. Antenna Design Requirements

Table 43: Antenna Design Requirements

Antenna Type	Requirements
Wi-Fi/Bluetooth	• Frequency Range: 2.402–2.482 GHz 5.170–5.835 GHz • VSWR: ≤ 2 • Gain: 1 dBi • Max input power: 50 W

- Input impedance: 50 Ω
- Polarization type: Vertical
- Cable insertion loss: < 1 dB

5.5. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

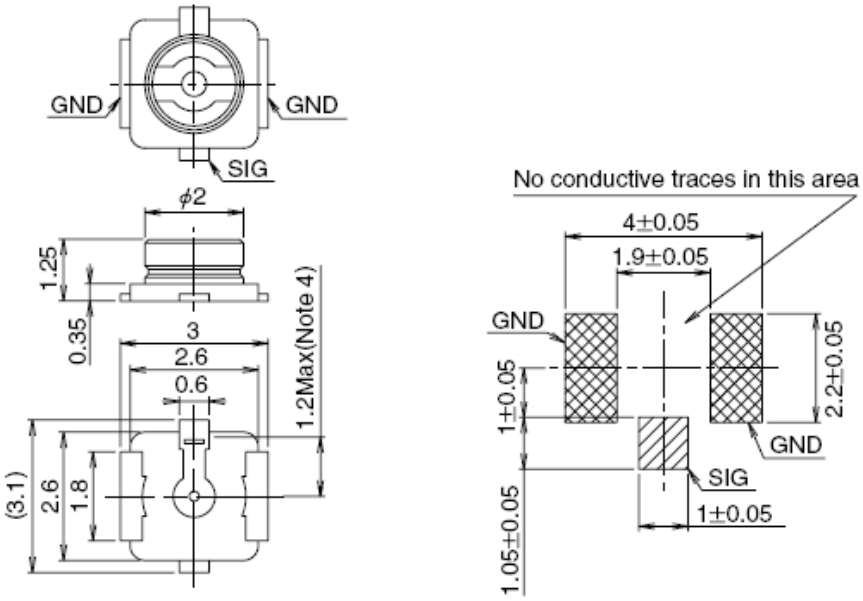


Figure 33: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

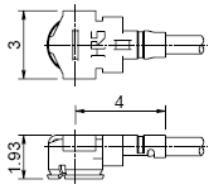
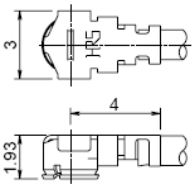
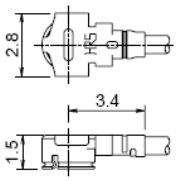
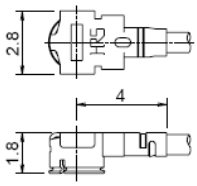
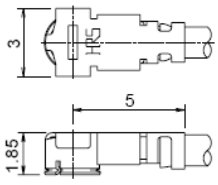
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 34: Specifications of Mated Plugs

The following figure describes the space factor of mated connectors.

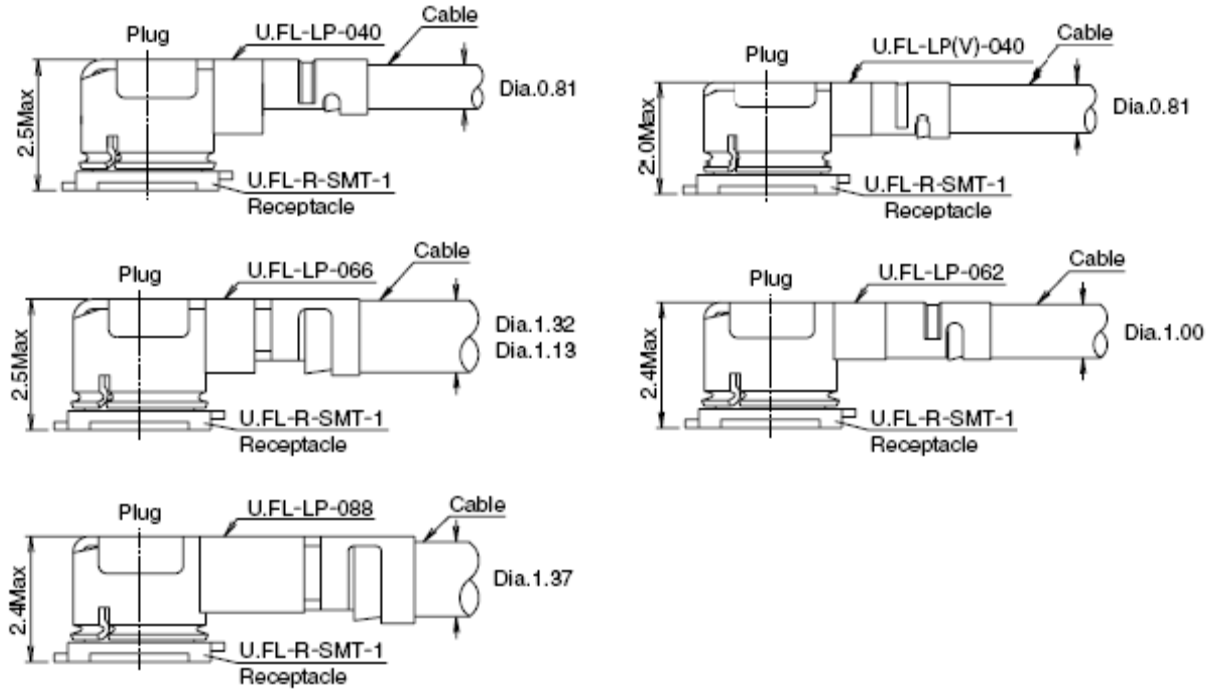


Figure 35: Space Factor of Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings voltage on digital and analog pins of the module are listed in the following table.

Table 44: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.3	6	V
USB_VBUS	-0.3	28	V
Voltage at Digital Pins	-0.3	2.16	V

6.2. Power Supply Ratings

Table 45: Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	Power supply for the module	The actual input voltages must stay between the minimum and maximum values.	3.55	3.8	4.4	V
USB_VBUS	Charging power input. Power supply for OTG device. USB/adaptor insertion detection	-	4.0	5.0	12.6	V

6.3. Power Consumption

Table 46: SG865W-WF Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power off	160	μA
Sleep state	Enter standby after power on	7	mA

Table 47: SG865W-AP Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power off	TBD	μA
Sleep state	Enter standby after power on	TBD	mA

6.4. Digital I/O Characteristic

Table 48: 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	1.17	2.1	V
V_{IL}	Input low voltage	-0.3	0.63	V
V_{OH}	Output high voltage	1.45	1.8	V
V_{OL}	Output low voltage	0	0.45	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 49: Electrostatics Discharge Characteristics (25 °C, 45 % Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±8	±12	kV
Antenna Interfaces	TBD	TBD	kV
Other Interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 50: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [3]	-35	+25	+75	°C
Storage temperature range	-40	-	+90	°C

[3] Within operating temperature range, the module is IEEE compliant.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

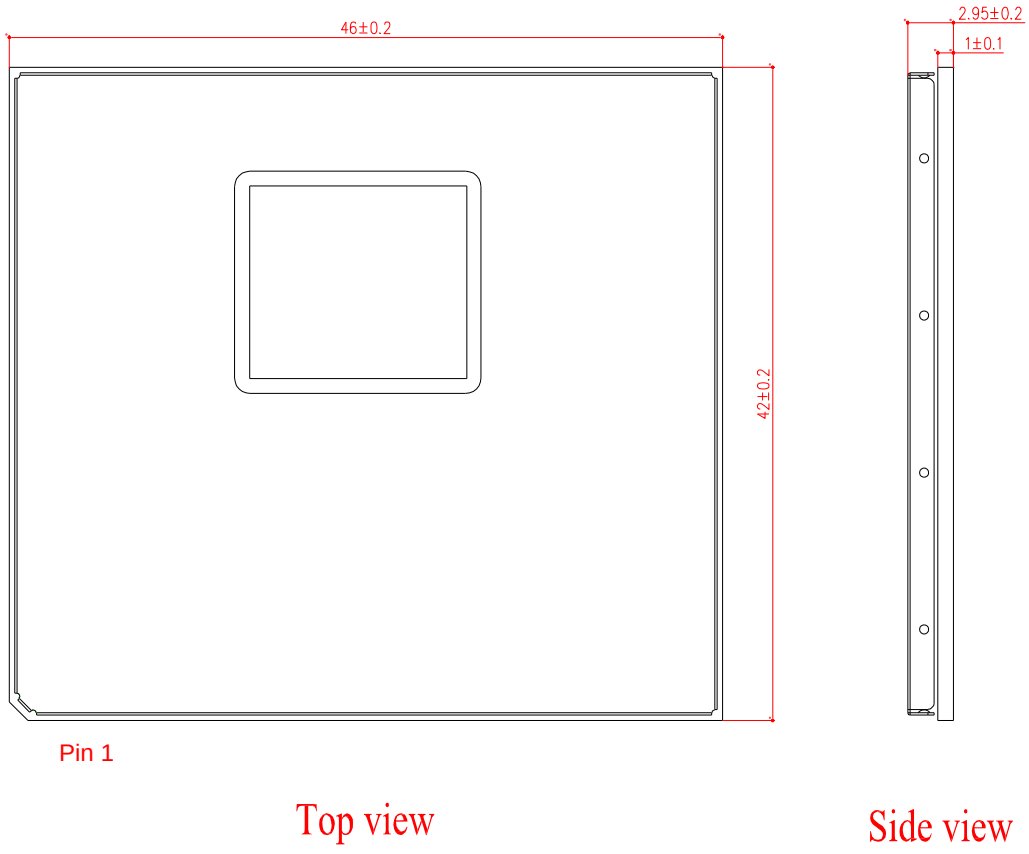


Figure 36: Module Top and Side Dimensions

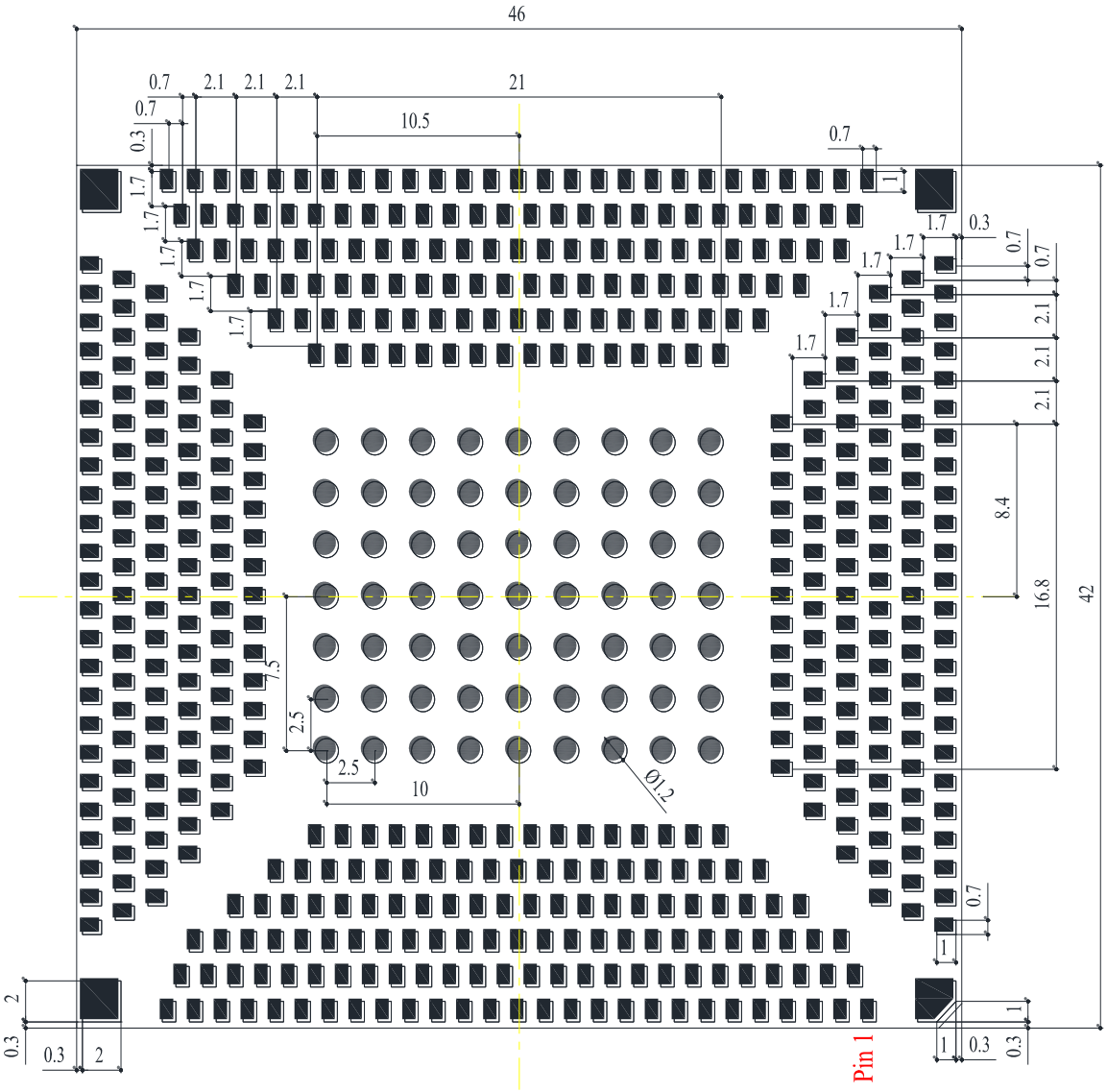


Figure 37: Module Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

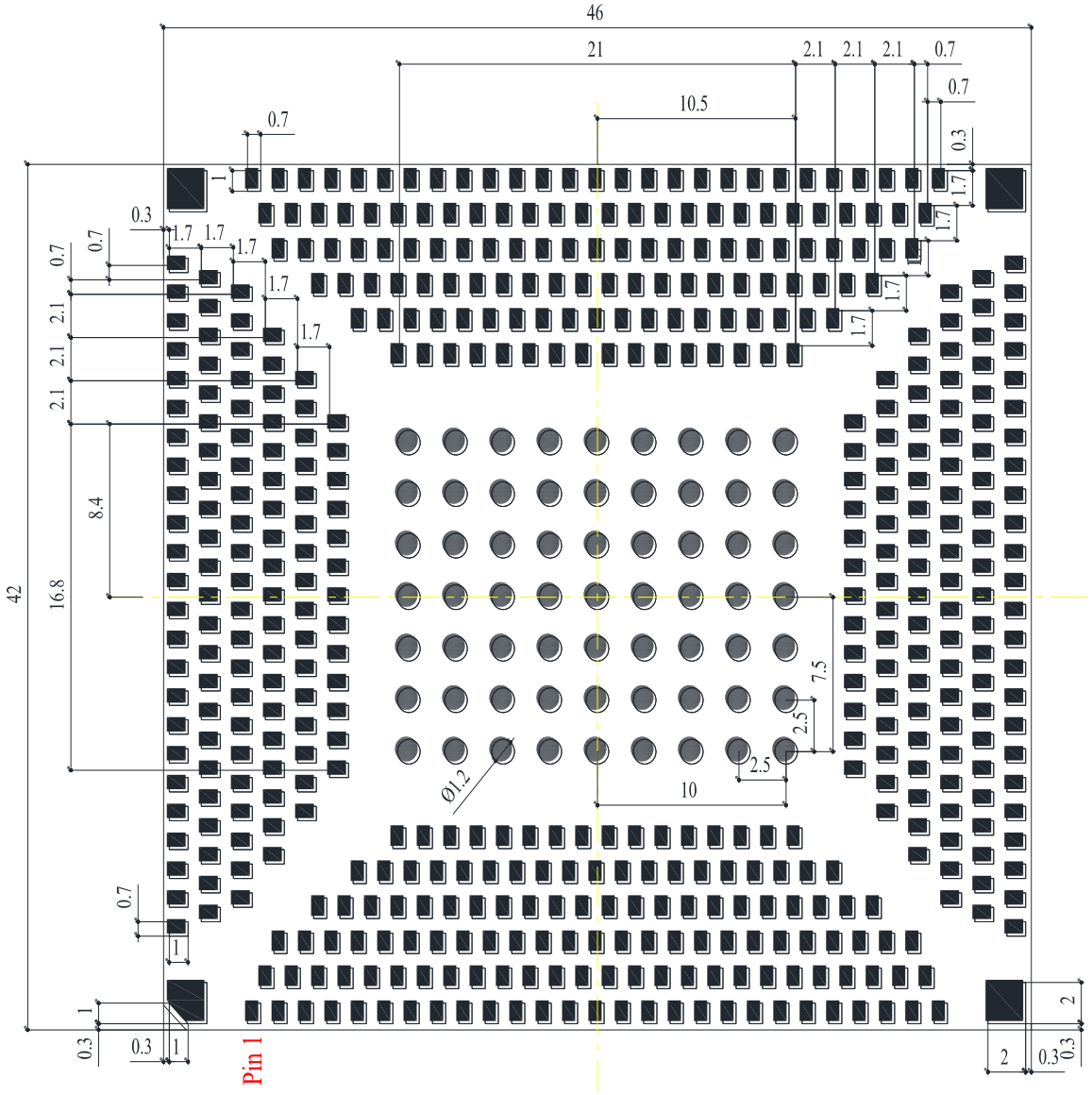


Figure 38: Recommended Footprint (Top View)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

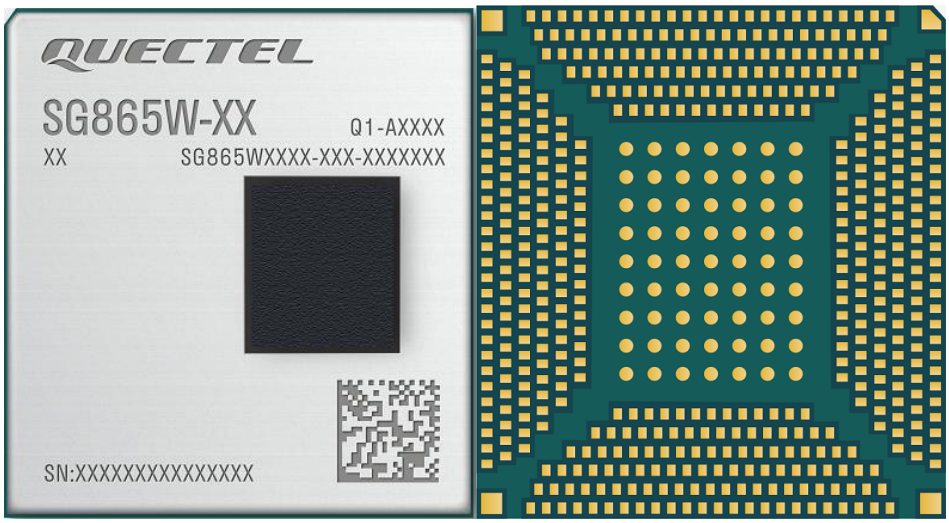


Figure 39: Top and Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [4] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[4] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see ***document [4]***.

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

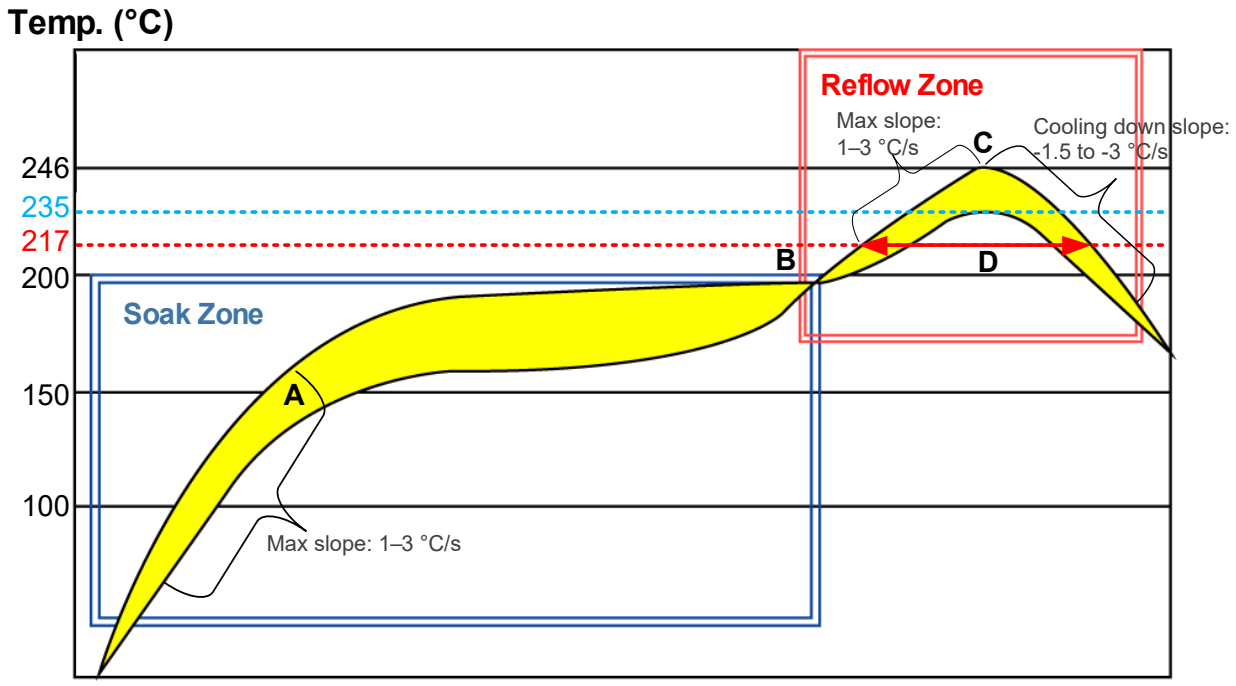


Figure 40: Recommended Reflow Soldering Thermal Profile

Table 51: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	1–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235 °C to 246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
2. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
3. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [4]***.

8.3. Packaging Specifications

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

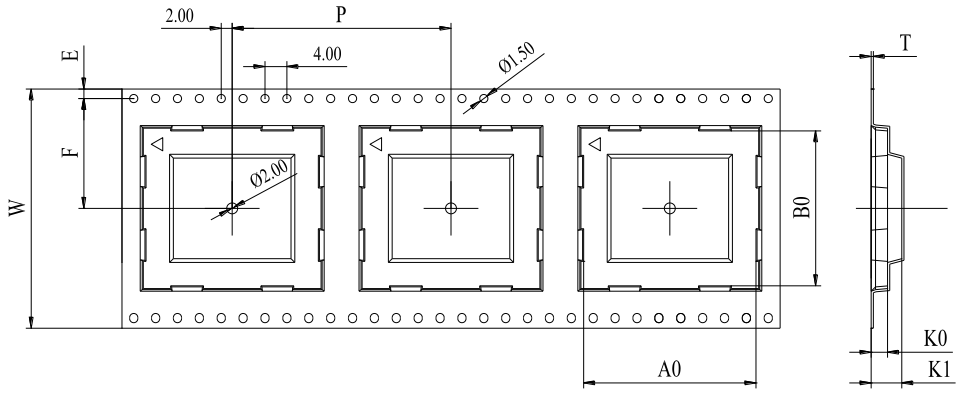


Figure 41: Carrier Tape Dimension Drawing

Table 52: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
72	56	0.4	42.6	46.6	4.25	5.25	34.2	1.75

8.3.2. Plastic Reel

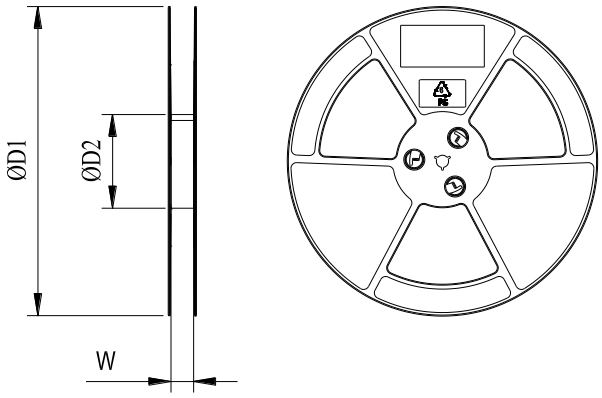
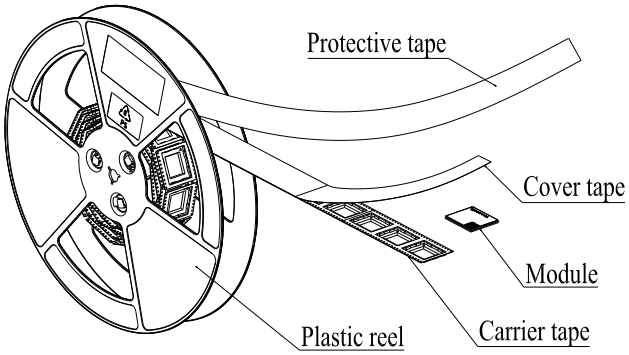


Figure 42: Plastic Reel Dimension Drawing

Table 53: Plastic Reel Dimension Table (Unit: mm)

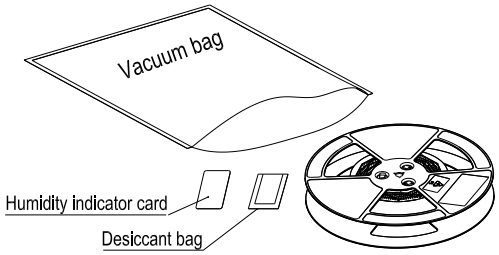
øD1	øD2	W
380	180	72.5

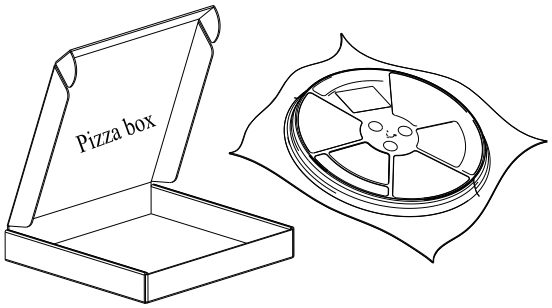
8.3.3. Packaging Process



Place the module into the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. One plastic reel can load 200 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, then vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Put 4 pizza boxes into 1 carton and seal it. One carton can pack 800 modules.

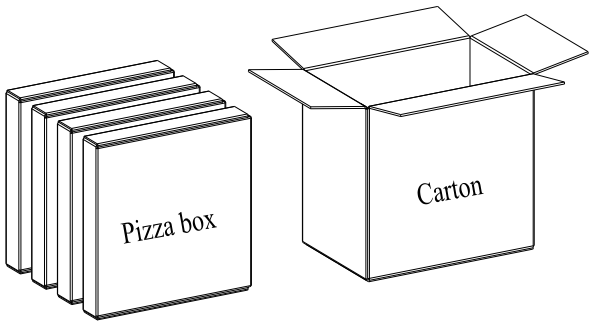


Figure 43: Packaging Process

9 Appendix References

Table 54: Related Documents

Document Name
[1] Quectel_SA800U-WF_EVB_User_Guide
[2] Quectel_SG865W_Series_GPIO_Configuration
[3] Quectel_RF_Layout_Application_Note
[4] Quectel_Module_Secondary_SMT_Application_Note

Table 55: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AI	Artificial Intelligence
AP	Application Processor
BLE	Bluetooth Low Energy
bps	Bits Per Second
BPSK	Binary Phase Shift Keying
DBS	Date Base System
CCI	Camera Control Interface
CPU	Central Processing Unit
CSI	Camera Serial Interface
CTS	Clear to Send
DAI	Digital Audio Interface

DCE	Data Communications Equipment
DDR	Double Data Rate
DL	Downlink
DPU	Data Processing Unit
DSP	Digital Signal Processor
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EDR	Enhanced Data Rate
EFR	Enhanced Full Rate
EMI	Electromagnetic Interference
ERM	Eccentric Rotating Machines
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
FDD	Frequency Division Duplex
FEM	Front-End Module
FP	Fingerprint
FR	Full Rate
GFSK	Gauss Frequency Shift Keying
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying
GPIO	General Purpose Input/Output
GPU	Graphic Processing Unit
IC	Integrated Circuit
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound

IEEE	Institute of Electrical and Electronics Engineers
I/O	Input/Output
ISP	Image Signal Processing
Inom	Nominal Current
LAA	License Assisted Access
LB	Low Band
LCD	Liquid Crystal Display
LCM	Liquid Crystal Monitor
LED	Light Emitting Diode
LDO	Low-dropout Regulator
LGA	Land Grid Array
LRA	Linear Resonant Actuators
LPI	Low Power Island
MAC	Media Access Control
MIMO	Multiple Input Multiple Output
MIPI	Mobile Industry Processor Interface
MT	Mobile Terminated
NFC	Near Field Communication
NTC	Negative Temperature Coefficient
OTA	Over-the-air programming
OTG	On-The-Go
OTP	One Time Programmable
OVP	Over Voltage Protection
PA	Power Amplifier
PAP	Password Authentication Protocol

PC	Personal Computer
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PHY	Physical Layer
PMIC	Power Management Integrated Circuit
POS	Point of Sale
PWM	Pulse Width Modulation
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RI	Ring Indicator
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
Rx	Receive
SE	Security
SMD	Surface Mount Device
SMS	Short Message Service
SPI	Serial Peripheral Interface
STA	Station
SWR	SoundWire
TDM	Time-Division Multiplexing
TDMA	Time Division Multiple Access

Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UFS	Universal Flash Storage
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
$V_{IH}max$	Maximum High-level Input Voltage
$V_{IH}min$	Minimum High-level Input Voltage
$V_{IL}max$	Maximum Low-level Input Voltage
$V_{IL}min$	Minimum Low-level Input Voltage
$V_{I}max$	Absolute Maximum Input Voltage
$V_{I}min$	Absolute Minimum Input Voltage
$V_{OH}max$	Maximum High-level Output Voltage
$V_{OH}min$	Minimum High-level Output Voltage
$V_{OL}max$	Maximum Low-level Output Voltage
$V_{OL}min$	Minimum Low-level Output Voltage
VPU	Video Processing Unit
VSWR	Voltage Standing Wave Ratio
WCN	Windows Connect Now
WLAN	Wireless Local Area Network

Wi-Fi	Wireless Fidelity
WWAN	Wireless Wide Area Network