AF50T Hardware Design

Wi-Fi&BT Module Series

Version: 1.0.1

Date: 2020-12-17

Status: Preliminary

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About the Document

Revision History

Version	Date	Author	Description
-	2019-11-25	Jone CHEN/ Felix FU	Creation of the document
1.0.0	2019-11-25	Jone CHEN/ Felix FU	Preliminary
1.0.1	2020-12-17	Jone CHEN/ Michael DU	Preliminary: 1. Updated the key features (Table 1). 2. Changed the name of pin 48, pin 60, pin 61, pin 3, pin 21 and pin 65 to RESERVED, pin 22 from BT_DBG_RXD to BT_WAKEUP_HOST, pin 23 from BT_DBG_TXD to HOST_WAKEUP_BT. 3. Updated the pin description (Table 3). 4. Updated the recommended operating power supply range (Table 4 and Table 19). 5. Deleted Chapter 3.5.3. 6. Updated the reference circuit for RF antenna interfaces (Figure 12). 7. Added data of current consumption (Chapter 4.4). 8. Updated data of RF performance (Chapter 4.5). 9. Added data of electrostatic discharge (Table 28).

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1 Introduction

This document defines the AF50T module and describes its air interface and hardware interfaces which are connected with customers' applications.

The document helps customers quickly understand module interface specifications, as well as the electrical and mechanical details. Associated with application notes and user guides, customers can use AF50T module to design and set up automotive industry mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

2 Product Concept

2.1. General Description

AF50T is an automotive grade Wi-Fi and Bluetooth (BT) module with low power consumption. It is a single-die WLAN (Wireless Local Area Network) and BT combo solution supporting IEEE 802.11 a/b/g/n/ac/ax 2.4/5 GHz WLAN standards and BT5.1 standard, which enables seamless integration of WLAN and BT Low Energy technologies.

AF50T supports a low-power PCIe Gen 2 interface for WLAN and a UART/PCM interface for BT, and also supports LTE & WLAN/BT coexistence interface. It is designed to be used in conjunction with Quectel 5G V2X module AG55xQ series to provide it with WLAN and BT functions.

2.2. Key Features

The following table describes the key features of AF50T module.

Table 1: Key Features

Features	Details
Power Supply	Core supply voltage: 0.95 V, 1.35 V, 1.9 V I/O supply voltage: 1.8 V RF supply voltage: 3.85 V
Operating Frequency	● 2.4 GHz WLAN: 2.412–2.472 GHz ● 5 GHz WLAN: 5.180–5.825 GHz ● BT: 2.402–2.480 GHz
Transmission Data Rates	● 802.11b: 1 Mbps, 2 Mbps, 5.5 Mbps, 11 Mbps ● 802.11a/g: 6 Mbps, 9 Mbps, 12 Mbps, 18 Mbps, 24 Mbps, 36 Mbps, 48 Mbps, 54 Mbps ● 802.11n: HT20 (MCS0-7), HT40 (MCS0-7) ● 802.11ac: VHT20 (MCS0-8), VHT40 (MCS0-9), VHT80 (MCS0-9) ● 802.11ax: HE20 (MCS0-11), HE40 (MCS0-11), HE80 (MCS0-11)

Transmitting Power	**2.4 GHz** 802.11b/11 Mbps: 20 dBm 802.11g/54 Mbps: 16 dBm 802.11n/HT20 MCS7: 16 dBm 802.11n/HT40 MCS7: 16 dBm 802.11ax/HE20 MCS11: 14 dBm 802.11ax/HE40 MCS11: 14 dBm **5 GHz** 802.11a/54 Mbps: 15 dBm 802.11n/HT20 MCS7: 15 dBm 802.11n/HT40 MCS7: 15 dBm 802.11ac/VHT20 MCS8: 14 dBm 802.11ac/VHT40 MCS9: 13 dBm 802.11ac/VHT80 MCS9: 13 dBm 802.11ax/HE20 MCS11: 12 dBm 802.11ax/HE40 MCS11: 12 dBm 802.11ax/HE80 MCS11: 12 dBm
Protocol Features	● IEEE 802.11 a/b/g/n/ac/ax ● Bluetooth 5.1
Operation Mode	AP, STA
Modulation	CCK, BPSK, QPSK, 16QAM, 64QAM, 256QAM, 1024QAM
WLAN Interface	PCIe
BT Interface	UART and PCM
Antenna Interface	● Wi-Fi/BT antenna interface ● 50 Ω impedance
Physical Characteristics	● Size: (19.5 ±0.2) mm × (21.5 ±0.2) mm × (2.3 ±0.2) mm ● Package: LGA ● Weight: 2.1 g
Temperature Range	● Operating temperature range: -40 °C to +85 °C ● Storage temperature range: -40 °C to +95 °C
RoHS	All hardware components are fully compliant with EU RoHS directive

2.3. Functional Diagram

The following figure shows a block diagram of AF50T module.

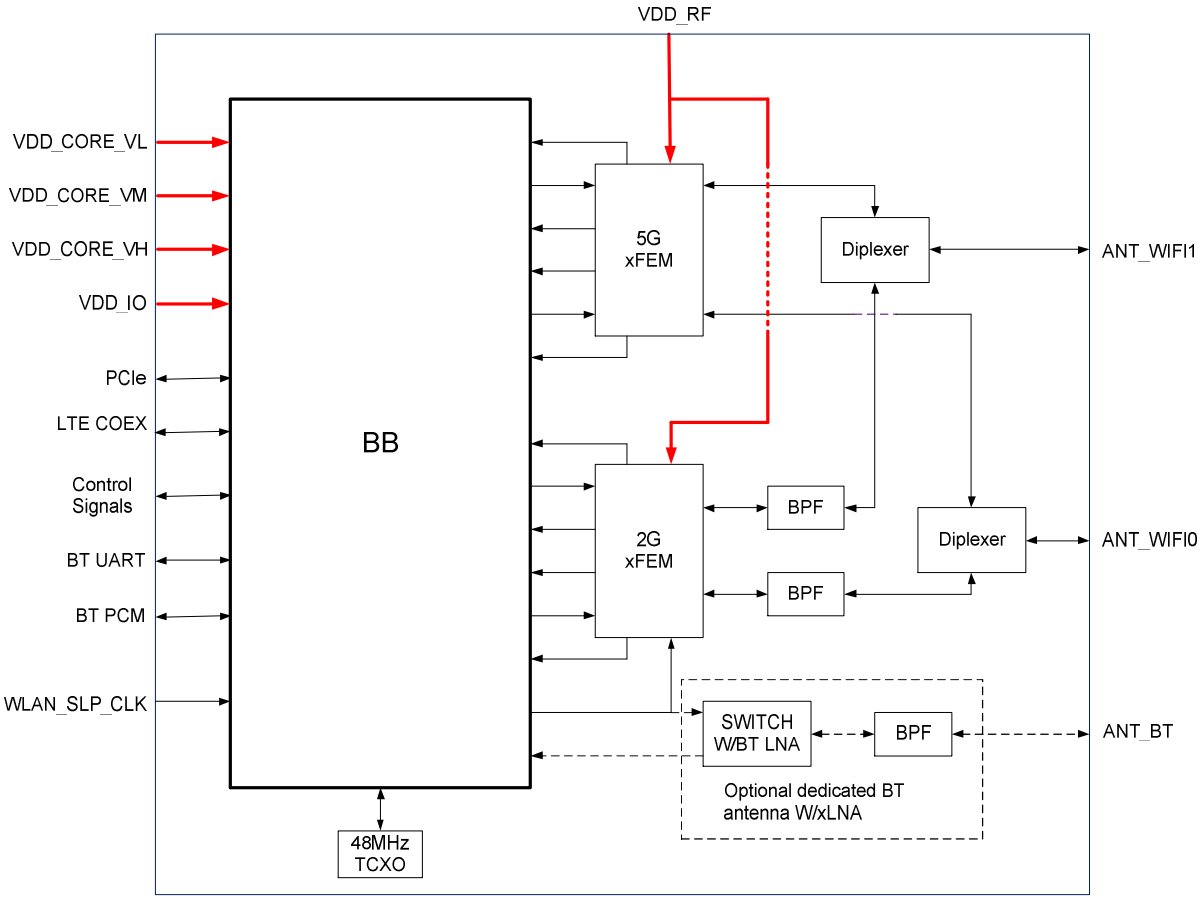


Figure 1: Functional Diagram of AF50T Module

2.4. Evaluation Board

To help customers develop applications with AF50T module conveniently, Quectel supplies the evaluation board (EVB), USB to RS232 converter cable, USB data cable, power adapter, antenna and other peripherals to control or test the module. For more details, see ***document [1]*** and/or ***document [2]***.

3 Application Interfaces

3.1. General Description

AF50T module is equipped with 108 LGA pins that can be connected to the cellular application platform. The subsequent chapters will provide a detailed introduction to the following interfaces and pins of the module:

- Power supply
- WLAN interface
- BT interface
- Control signal pins*
- Coexistence interfaces
- WLAN_SLP_CLK interface
- RF antenna interfaces

3.2. Pin Assignment

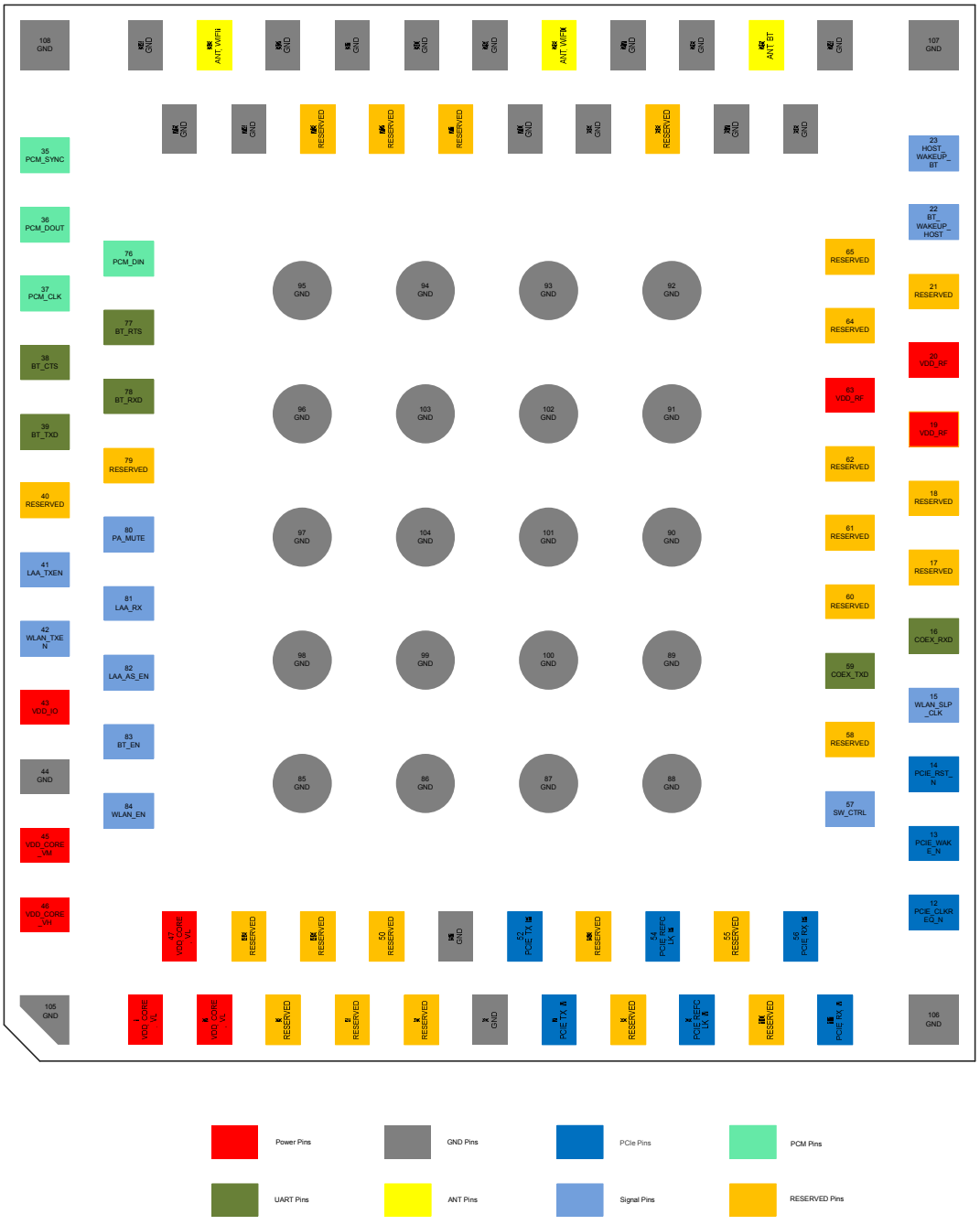


Figure 2: Pin Assignment (Top View)

NOTE

Please keep all RESERVED pins open.

3.3. Pin Description

The following tables show the pin description of AF50T module.

Table 2: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
DI	Digital Input
DO	Digital Output
IO	Bidirectional
PI	Power Input

Table 3: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VDD_CORE_VL	1, 2, 47	PI	Voltage for core, low voltage	Vmin = 0.9 V Vnorm = 0.95 V Vmax = 1.05 V	It must be provided with sufficient current up to 1.7 A.
VDD_CORE_VM	45	PI	Voltage for core, mid voltage	Vmin = 1.28 V Vnorm = 1.35 V Vmax = 1.42 V	It must be provided with sufficient current up to 0.4 A.
VDD_CORE_VH	46	PI	Voltage for core, high voltage	Vmin = 1.85 V Vnorm = 1.9 V Vmax = 2.0 V	It must be provided with sufficient current up to 0.4 A.
VDD_IO	43	PI	Power supply for the module's I/O pins	Vmin = 1.71 V Vnorm = 1.8 V Vmax = 1.89 V	It must be provided with sufficient current up to 50 mA.
VDD_RF	19, 20, 63	PI	Power supply for the module's RF part	Vmin = 3.3 V Vnorm = 3.85 V Vmax = 4.25 V	It must be provided with sufficient current up to 1.3 A.
GND	6, 24, 26, 27, 29, 30, 31, 32, 34, 44, 51, 66, 67, 69, 70, 74, 75, 85 – 108				

WLAN Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_EN	84	DI	WLAN function enable control	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. Active high.
PCIE_ REFCLK_P	54	AI	PCIe reference clock (+)		Require differential impedance of 85 Ω.
PCIE_ REFCLK_M	9	AI	PCIe reference clock (-)		
PCIE_TX_P	52	AO	PCIe transmit (+)		
PCIE_TX_M	7	AO	PCIe transmit (-)		
PCIE_RX_P	56	AI	PCIe receive (+)		
PCIE_RX_M	11	AI	PCIe receive (-)		
PCIE_ CLKREQ_N	12	DO	PCIe clock request	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain
PCIE_RST_N	14	DI	PCIe reset	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain
PCIE_ WAKE_N	13	DO	PCIe wakes up host	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain
BT Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BT_EN	83	DI	BT enable control	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. Active high.
PCM_DIN*	76	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain.
PCM_SYNC*	35	DI	PCM data frame sync	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain.

PCM_CLK*	37	DI	PCM clock	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain.
PCM_DOUT*	36	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
BT_RTS	77	DO	BT UART request to send	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
BT_CTS	38	DI	BT UART clear to send	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain.
BT_TXD	39	DO	BT UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
BT_RXD	78	DI	BT UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain.
Control Signal Pins*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SW_CTRL	57	DO	Control PMIC outputs	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
HOST_ WAKEUP_	23	DI	Host wakes up BT	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. If unused, keep this pin open.
BT_WAKEUP_ HOST	22	DO	BT wakes up the host	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
Coexistence Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
COEX_TXD	59	DO	LTE/WLAN & BT coexistence transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
COEX_RXD	16	DI	LTE/WLAN & BT coexistence receive	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. If unused, keep this pin open.
LAA_AS_EN*	82	DI	Allow LAA to control	V_{IL}min = -0.3 V	1.8 V power domain.

			WLAN FEM during WLAN sleep mode	V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	If unused, keep this pin open.
LAA_TXEN*	41	DI	WLAN XFEM control LAA TX enable	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. If unused, keep this pin open.
LAA_RX*	81	DI	WLAN XFEM control for LAA receiver	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. If unused, keep this pin open.
WLAN_TXEN*	42	DO	WLAN XFEM control for WLAN TX enable	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
PA_MUTE*	80	DI	WLAN XFEM control to disable WLAN PA	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. If unused, keep this pin open.

RF Antenna Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ANT_WIFI0	28	IO	BT and 2.4/5 GHz WLAN antenna interface 0		50 Ω impedance
ANT_WIFI1	33	IO	2.4/5 GHz WLAN antenna interface 1		50 Ω impedance
ANT_BT	25	IO	Reserved dedicated BT antenna interface		50 Ω impedance

WLAN_SLP_CLK Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
WLAN_SLP_CLK	15	DI	External 32.768 kHz sleep clock input	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain.

RESERVED Interfaces

Pin Name	Pin No.	Comment
RESERVED	3, 4, 5, 8, 10, 17, 18, 21, 40, 48, 49, 50, 53, 55, 58, 60, 61,62, 64, 65, 68, 71–73, 79	Keep these pins open.

NOTES

1. Please keep all RESERVED and unused pins open.
2. "*" means under development.

3.4. Power Supply

The following table shows the power supply pins and ground pins of AF50T module.

Table 4: Definition of Power Supply and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VDD_CORE_VL	1, 2, 47	Voltage for core, low voltage	0.9	0.95	1.05	V
VDD_CORE_VM	45	Voltage for core, mid voltage	1.28	1.35	1.42	V
VDD_CORE_VH	46	Voltage for core, high voltage	1.85	1.9	2.0	V
VDD_IO	43	Power supply for the module's I/O pins	1.71	1.8	1.89	V
VDD_RF	19, 20, 63	Power supply for the module's RF part	3.3	3.85	4.25	V
GND	6, 24, 26, 27, 29, 30, 31, 32, 34, 44, 51, 66, 67, 69, 70, 74, 75, 85 – 108					

The VDD_CORE_VL, VDD_CORE_VM, VDD_CORE_VH, and VDD_IO can be powered by AG55xQ series module, as the following figure shows.

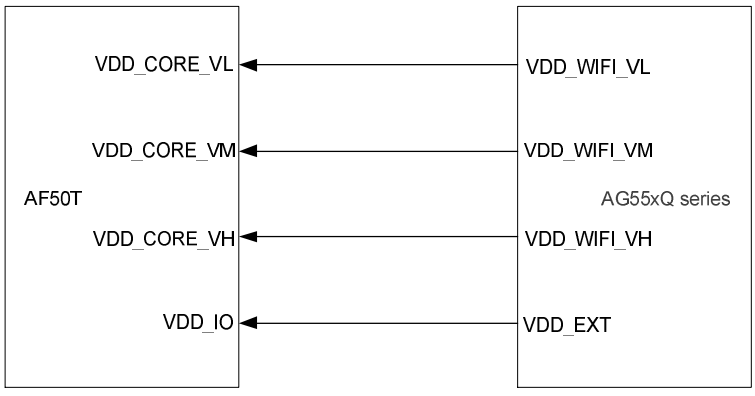


Figure 3: Reference Circuit for VDD_CORE_VL, VDD_CORE_VM, VDD_CORE_VH, and VDD_IO

AF50T module is powered by VDD_RF, and it is recommended to use a power supply chip, which is able to output a current of 1.3 A at least.

The following figure shows a reference design for VDD_RF which is controlled by WLAN_PWR_EN1 of AG55xQ series. WLAN_PWR_EN1 of TPS62130A-Q1 should be connected to the pin 222 (WLAN_PWR_EN1) of AG55xQ series module. For more details, see ***document [3]***.

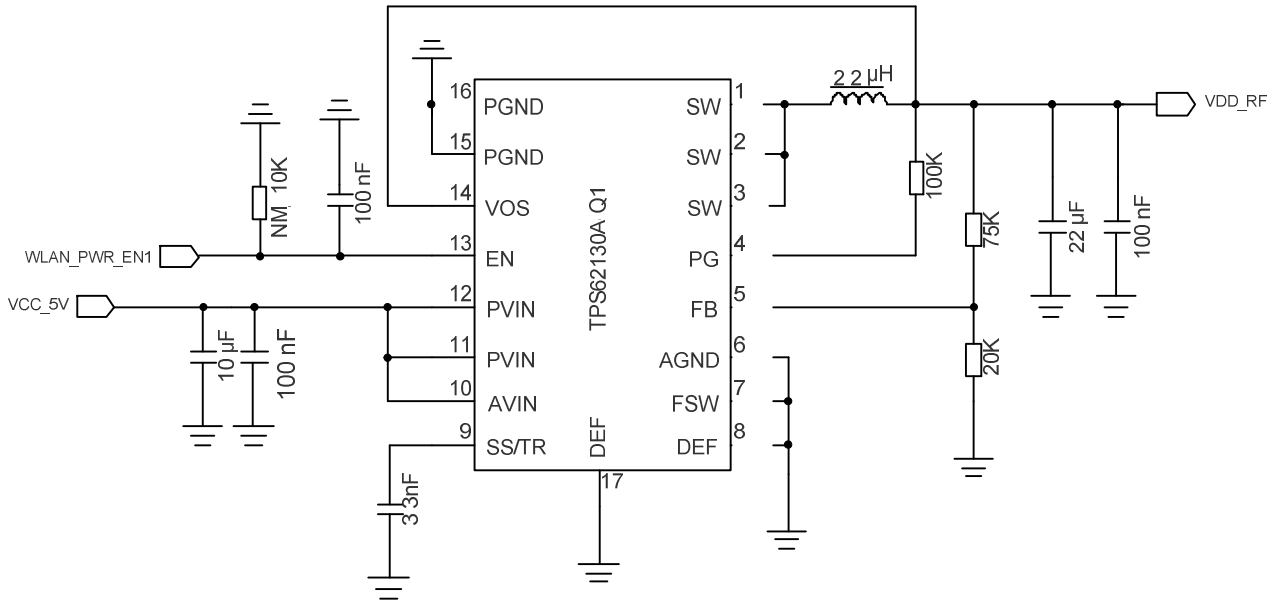


Figure 4: Reference Circuit for VDD_RF

3.5. WLAN Interface

The following figure shows the WLAN interface connection between AF50T and AG55xQ series modules.

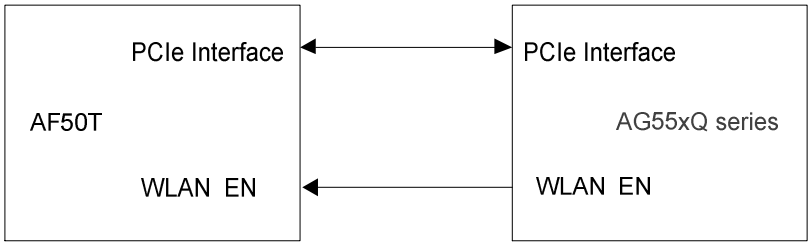


Figure 5: WLAN Interface Connection

3.5.1. WLAN_EN

WLAN_EN is used to control the WLAN function of AF50T module. WLAN function will be enabled when WLAN_EN is at high level.

Table 5: Pin Definition of WLAN_EN

Pin Name	Pin No.	I/O	Description	Comment
WLAN_EN	84	DI	WLAN function enable control	Active high

NOTE

WLAN_EN is a sensitive signal, and it should be ground shielded and be routed as close to AF50T as possible.

3.5.2. PCIe Interface

The following table shows the pin definition of the PCIe interface of AF50T.

Table 6: Pin Definition of PCIe Interface

Pin Name	Pin No.	I/O	Description	Comment
PCIE_REFCLK_P	54	AI	PCIe reference clock (+)	Require differential impedance of 85 Ω.
PCIE_REFCLK_M	9	AI	PCIe reference clock (-)	
PCIE_TX_P	52	AO	PCIe transmit (+)	
PCIE_TX_M	7	AO	PCIe transmit (-)	
PCIE_RX_P	56	AI	PCIe receive (+)	
PCIE_RX_M	11	AI	PCIe receive (-)	
PCIE_CLKREQ_N	12	DO	PCIe clock request	1.8 V power domain.
PCIE_RST_N	14	DI	PCIe reset	
PCIE_WAKE_N	13	DO	PCIe wakes up host	

The following figure shows the PCIe interface connection between AF50T and AG55xQ series modules.

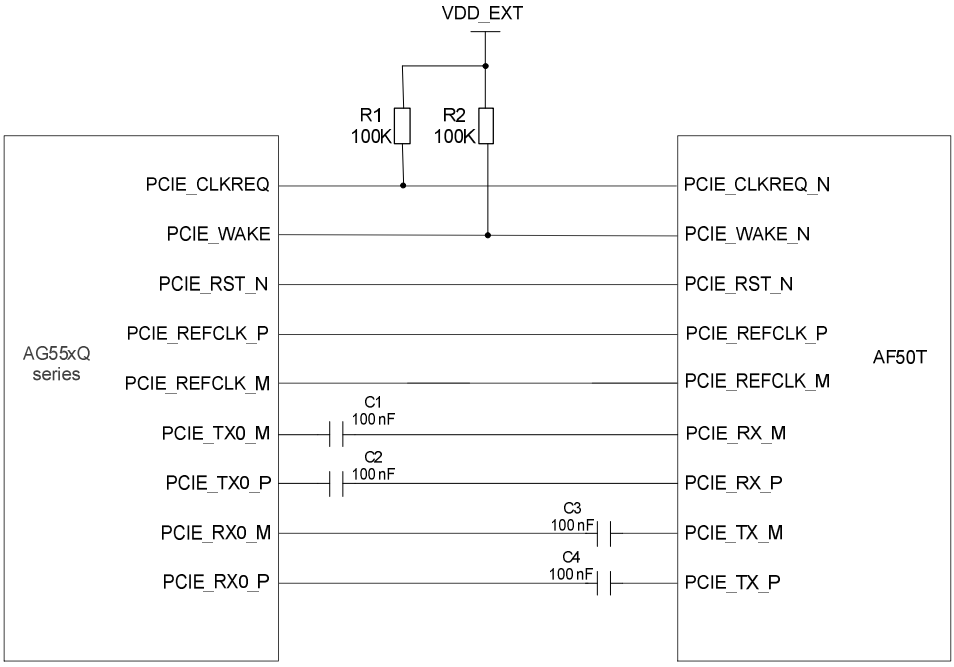


Figure 6: PCIe Interface Connection

To ensure the signal integrity of PCIe interface, C1 and C2 should be placed close to the AG55xQ series module, and C3 and C4 should be placed close to the AF50T. The extra stubs of traces must be as short as possible.

The following principles of PCIe interface design should be complied with, so as to meet PCIe Gen2 specifications.

- It is important to route the PCIe signal traces as differential pairs with total grounding. And the differential impedance is 85 Ω ±10 %.
- For PCIe signal traces, the maximum length of each differential data pair (TX/RX/REFCLK) is recommended to be less than 300 mm, and each differential data pair matching should be less than 0.7 mm (5 ps).
- Spacing to all other signals (inter-interface) is four times of trace width.
- Do not route signal traces under crystals, oscillators, magnetic devices, or RF signal traces. It is important to route the PCIe differential traces in inner-layer of the PCB and surround the traces with ground on that layer and with ground planes above and below.

3.6. BT Interface

The following figure shows the block diagram of BT interface connection between AF50T and AG55xQ series modules.

If BT function of AF50T module is used, the UART and PCM interfaces of AF50T must be connected to that of AG55xQ series module.

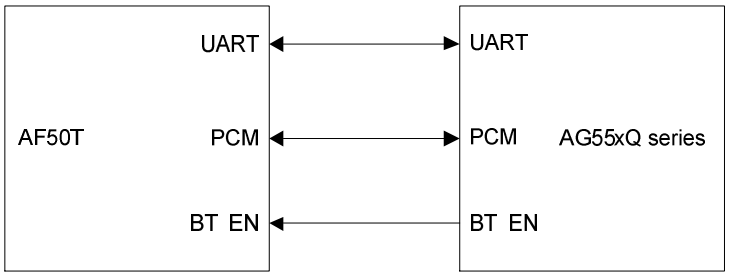


Figure 7: Block Diagram of BT Interface Connection

3.6.1. BT_EN

BT_EN is used to control the BT function of AF50T module. BT function will be enabled when BT_EN is at high level.

Table 7: Pin Definition of BT_EN

Pin Name	Pin No.	I/O	Description	Comment
BT_EN	83	DI	BT enable control	Active high.

3.6.2. PCM Interface*

The following table shows the pin definition of PCM interface.

Table 8: Pin Definition of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	76	DI	PCM data input	1.8 V power domain
PCM_SYNC	35	DI	PCM data frame sync	1.8 V power domain
PCM_CLK	37	DI	PCM clock	1.8 V power domain
PCM_DOUT	36	DO	PCM data output	1.8 V power domain

The following figure shows the PCM interface connection between AF50T and AG55xQ series modules.

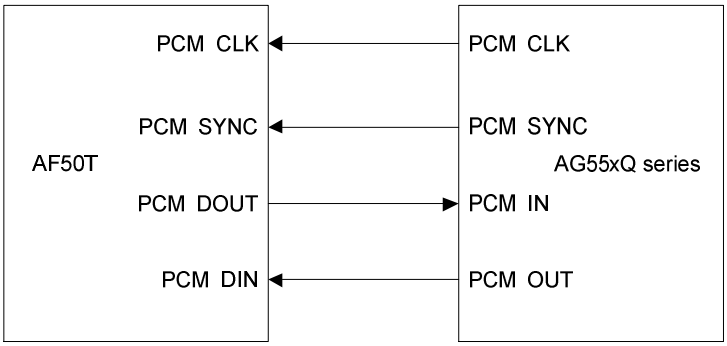


Figure 8: PCM Interface Connection

NOTE

"*" means BT PCM interface of AF50T is still under development.

3.6.3. UART Interface

The following table shows the pin definition of UART interface.

Table 9: Pin Definition of UART Interface

Pin Name	Pin No.	I/O	Description	Comment
BT_RTS	77	DO	BT UART request to send	1.8 V power domain
BT_CTS	38	DI	BT UART clear to send	1.8 V power domain
BT_TXD	39	DO	BT UART transmit	1.8 V power domain
BT_RXD	78	DI	BT UART receive	1.8 V power domain

The following figure shows the reference design for UART interface connection between AF50T and AG55xQ series modules.

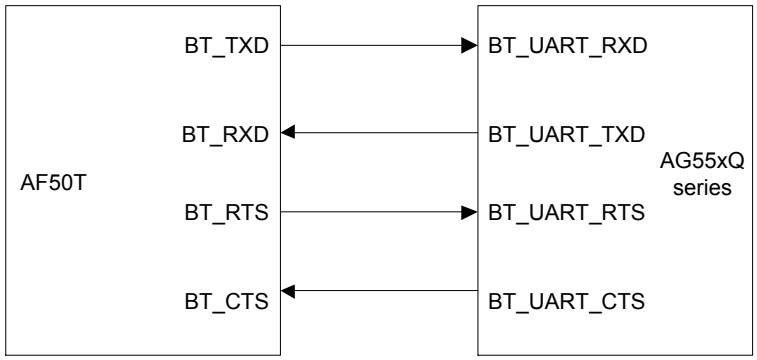


Figure 9: UART Interface Connection

3.7. Control Signal Pins*

3.7.1. SW_CTRL

The following table shows the pin definition of SW_CTRL.

Table 10: Pin Definition of SW_CTRL

Pin Name	Pin No.	I/O	Description	Comment
SW_CTRL	57	DO	Control PMIC outputs	Active high. Under development.

The following figure shows the reference design for SW_CTRL connection between AF50T and AG55xQ series modules.

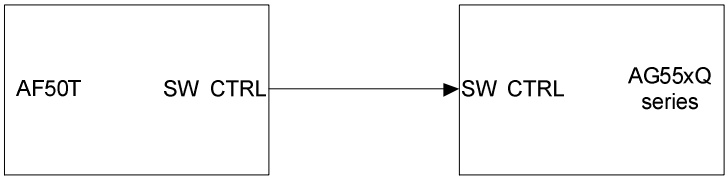


Figure 10: SW_CTRL Connection

3.7.2. HOST_WAKEUP_BT and BT_WAKEUP_HOST

The following table shows the pin definition of HOST_WAKEUP_BT and BT_WAKEUP_HOST.

These two pins are only used for AF50T + third-part host application. For AF50T + AG55xQ series application, they are not needed.

Table 11: Pin Definition of HOST_WAKEUP_BT and BT_WAKEUP_HOST

Pin Name	Pin No.	I/O	Description	Comment
HOST_WAKEUP_BT	23	DI	Host wakes up BT	1.8 V power domain. Under development.
BT_WAKEUP_HOST	22	DO	BT wakes up the host	1.8 V power domain. Under development.

NOTE

"*" means under development.

3.8. Coexistence Interfaces

3.8.1. UART Coexistence Interface

The following table shows the pin definition of UART coexistence interface.

Table 12: Pin Definition of UART Coexistence Interface

Pin Name	Pin No.	I/O	Description	Comment
COEX_TXD	59	DO	LTE/WLAN & BT coexistence transmit	If unused, keep this pin open.
COEX_RXD	16	DI	LTE/WLAN & BT coexistence receive	If unused, keep this pin open.

The module supports LTE & WLAN coexistence and LTE & BT coexistence. The following figure shows the UART coexistence interface connection between AF50T and AG55xQ series modules.

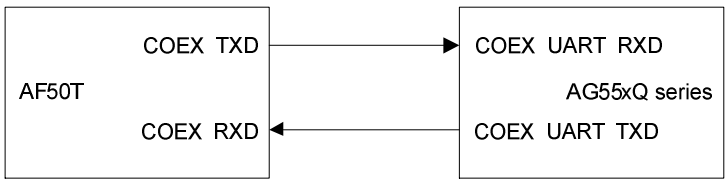


Figure 11: UART Coexistence Interface Connection

3.8.2. Other Coexistence Interfaces*

The following table shows the pin definition of other coexistence interfaces.

Table 13: Pin Definition of Other Coexistence Interface

Pin Name	Pin No.	I/O	Description	Comment
LAA_AS_EN	82	DI	Allow LAA to control WLAN FEM during WLAN sleep mode	If unused, keep this pin open.
LAA_TXEN	41	DI	WLAN XFEM control LAA TX enable	If unused, keep this pin open.
LAA_RX	81	DI	WLAN XFEM control for LAA receiver	If unused, keep this pin open.
WLAN_TXEN	42	DO	WLAN XFEM control for WLAN TX enable	If unused, keep this pin open.
PA_MUTE	80	DI	WLAN XFEM control to disable WLAN PA	If unused, keep this pin open.

NOTE

"*" means under development.

3.9. WLAN_SLP_CLK Interface

An external 32.768 kHz sleep clock connecting to WLAN_SLP_CLK is necessary. AF50T is unable to boot up and work without sleep clock.

Table 14: Pin Definition of WLAN_SLP_CLK Interface

Pin Name	Pin No.	I/O	Description	Comment
WLAN_SLP_CLK	15	DI	External 32.768 kHz sleep clock input	1.8 V power domain.

3.10. RF Antenna Interfaces

The following table shows the pin definition of RF antenna interfaces.

Table 15: Pin Definition of RF Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_WIFI0	28	IO	BT and 2.4/5 GHz WLAN antenna interface 0	50 Ω impedance
ANT_WIFI1	33	IO	2.4/5 GHz WLAN antenna interface 1	50 Ω impedance
ANT_BT	25	IO	Reserved dedicated BT antenna interface	50 Ω impedance

3.10.1. Operating Frequency

Table 16: Operating Frequency of the Module

Feature	Frequency	Unit
2.4 GHz WLAN	2.412 – 2.472	GHz
5 GHz WLAN	5.180 – 5.825	GHz
BT	2.402 – 2.480	GHz

3.10.2. Reference Design of RF Antenna Interfaces

AF50T module provides three RF antenna interfaces for antenna connection. A reference circuit design for an RF antenna interface is shown below.

It is recommended to reserve a π-type and LCs matching circuit for better RF performance, and add a TVS for ESD protection. the π-type matching components (C3, C4, and R1), the LCs (C1, C2, L1 and L2) and TVS (D1) should be placed as close to the antenna as possible. The capacitors and inductors are not mounted by default. the parasitic capacitance of TVS should be less than 0.05 pF

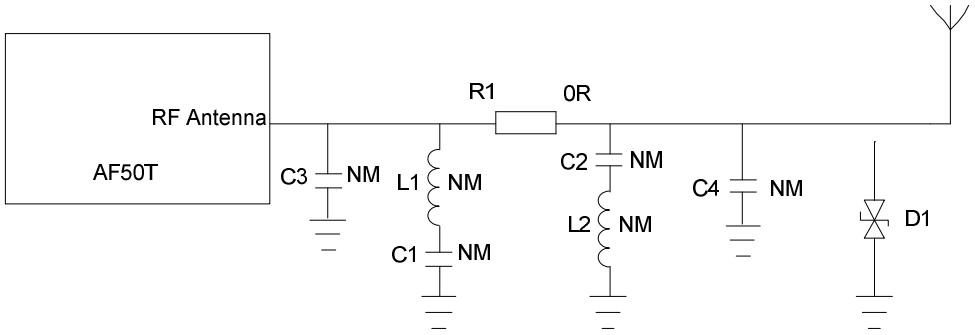


Figure 12: Reference Circuit for RF Antenna Interfaces

3.10.3. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

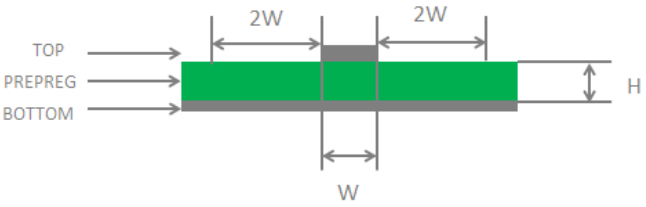


Figure 13: Microstrip Design on a 2-layer PCB

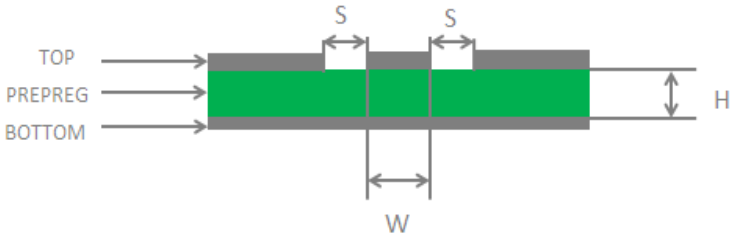


Figure 14: Coplanar Waveguide Design on a 2-layer PCB

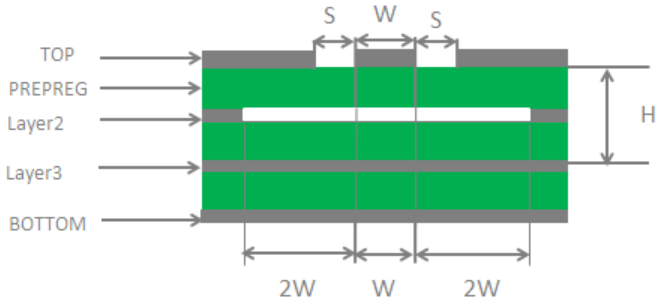


Figure 15: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

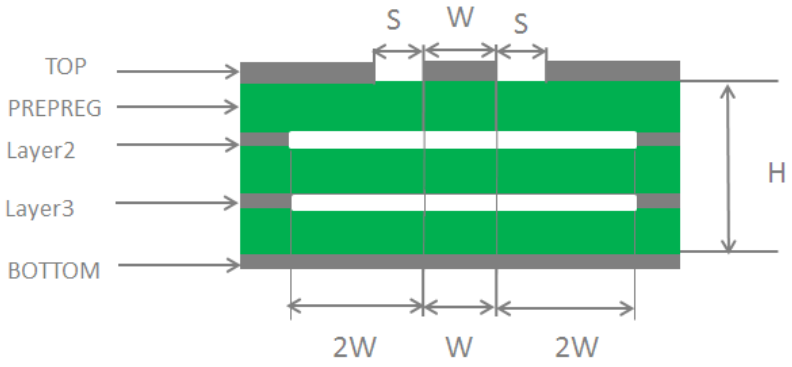


Figure 16: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [4]***.

3.10.4. Antenna Requirements

The following tables show the requirements on antenna cables and antennas.

Table 17: Antenna Cable Requirements

Type	Requirements
2.412 – 2.472 GHz	Cable insertion loss <1 dB
5.180 – 5.825 GHz	Cable insertion loss <1 dB

Table 18: Antenna Requirements

Type	Requirements
Frequency Range	2.412 – 2.472 GHz 5.180 – 5.825 GHz
VSWR	< 2:1 recommended
Gain (dBi)	Typical 3
Max Input Power (W)	50
Input Impedance (Ω)	50
Polarization Type	Vertical

Freq. (MHz)	2400	2410	2420	2430	2440	2450	2460	2470	2480	2490	2500
Efficiency (%)	70.3	69.6	70.2	72.8	75.6	77.5	77.6	76.5	76.0	76.2	75.2
Gain (dBi)	2.78	2.71	2.56	2.62	2.74	2.77	2.89	3.08	2.95	2.91	2.85
Freq. (MHz)	5150	5200	5250	5300	5350	5400	5450	5500	5550	5600	5650
Efficiency (%)	70.9	68.8	62.7	73.7	72.7	75.7	74.9	73.0	78.1	71.4	73.3
Gain (dBi)	1.21	1.14	1.29	1.58	2.18	2.02	2.09	2.05	1.97	1.49	1.71
Freq. (MHz)	5700	5750	5800	5850							
Efficiency (%)	67.9	68.4	69.6	65.4							
Gain (dBi)	1.57	1.85	2.34	1.60							

3.10.5. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

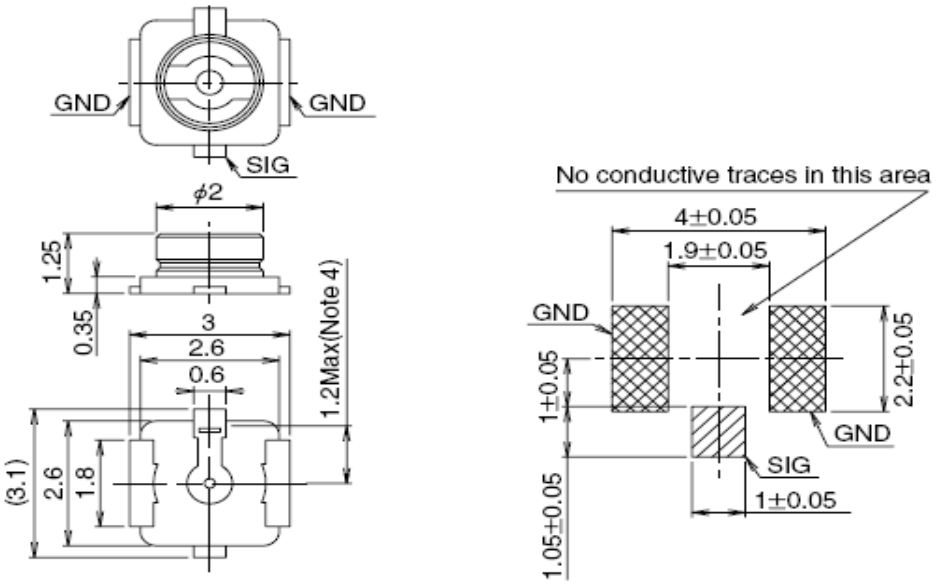


Figure 17: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

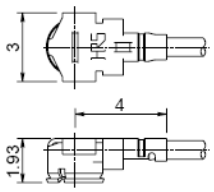
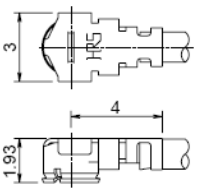
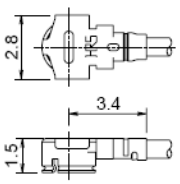
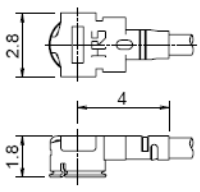
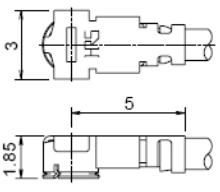
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 18: Mechanicals of UF.L-LP Connectors (Unit: mm)

The following figure describes the space factor of mated connector

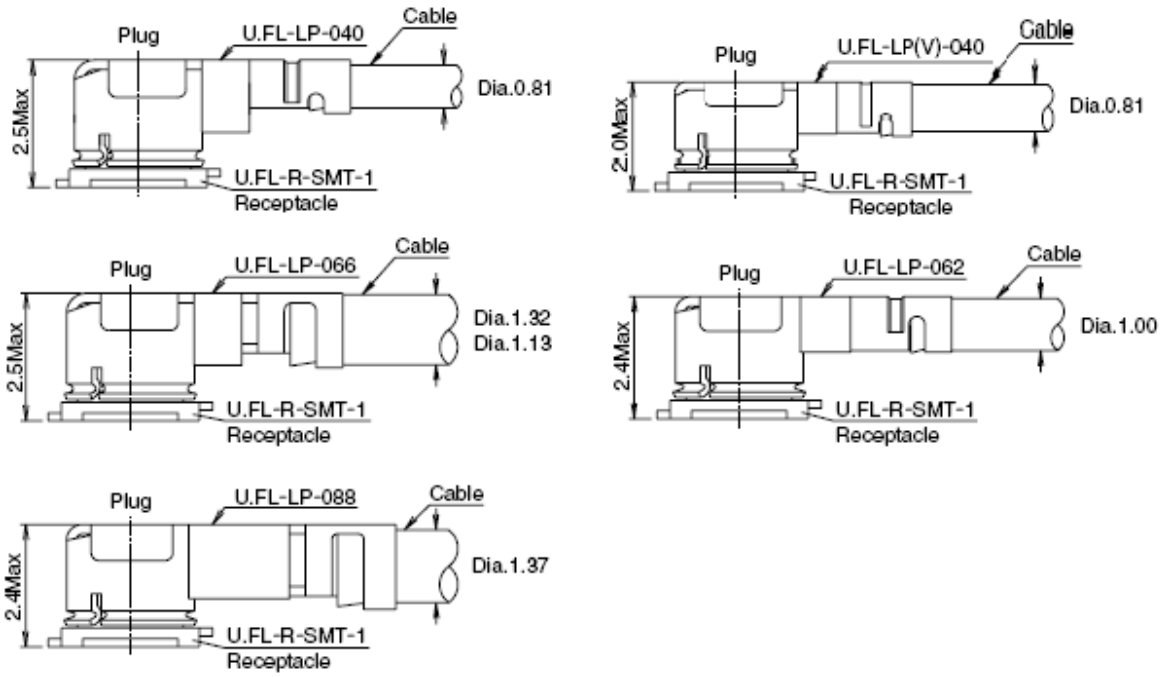


Figure 19: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://www.hirose.com.

4 Reliability, Radio and Electrical Characteristics

4.1. General Description

This chapter mainly introduces electrical and radio frequency characteristics of AF50T module. The details are listed in the subsequent chapters.

4.2. Electrical Characteristics

The following table shows the absolute maximum ratings.

Table 19: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VDD_CORE_VL	-0.3	V_{DDX} + 0.2	V
VDD_CORE_VM	-0.3	V_{DDX} + 0.2	V
VDD_CORE_VH	-0.3	V_{DDX} + 0.2	V
VDD_IO	-0.3	V_{DDX} + 0.2	V
VDD_RF	3.0	4.8	V
Digital I/O Input Voltage	-0.3	VDD_IO + 0.2	V

NOTE

V_{DDX} is the supply voltage associated with the input pin to which the test voltage is applied.

The following table shows the recommended operating conditions of AF50T module.

Table 20: Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
VDD_CORE_VL	0.9	0.95	1.05	V
VDD_CORE_VM	1.28	1.35	1.42	V
VDD_CORE_VH	1.85	1.9	2.0	V
VDD_IO	1.71	1.8	1.89	V
VDD_RF	3.3	3.85	4.25	V

4.3. I/O Interface Characteristics

The following table shows the general DC electrical characteristics over recommended operating conditions (unless otherwise specified).

Table 21: General DC Electrical Characteristics

Symbol	Parameter	Min.	Max.	Unit
V_{IH}	High Level Input Voltage	0.65 × VDD_IO	VDD_IO + 0.3	V
V_{IL}	Low Level Input Voltage	-0.3	0.35 × VDD_IO	V
V_{OH}	High Level Output Voltage	VDD_IO-0.45	VDD_IO	V
V_{OL}	Low Level Output Voltage	0	0.45	V
I_{IL}	Input Leakage Current	TBD	TBD	μA

4.4. Current Consumption

The values of current consumption are shown as below.

Table 22: Current Consumption of the Module (Normal Operation)

Description	Conditions	$I_{VDD\_CORE\_VL}$	$I_{VDD\_CORE\_VM}$	$I_{VDD\_CORE\_VH}$	I_{VDD_IO}	I_{VDD_RF}	Unit
802.11b	TX 1 Mbps @ 20 dBm	217.67	108.08	68.87	3.54	264.02	mA
	TX 11 Mbps @ 20 dBm	233.00	105.72	67.09	3.57	241.41	mA
802.11g	TX 6 Mbps @ 19 dBm	213.63	108.56	69.03	3.57	260.45	mA
	TX 54 Mbps @ 16 dBm	210.15	104.86	66.24	3.57	205.70	mA
802.11n	TX HT20-MCS0 @ 19 dBm	211.14	108.69	69.10	3.57	259.55	mA
	TX HT20-MCS7 @ 16 dBm	212.25	108.73	68.73	3.57	233.53	mA
	TX HT40-MCS0 @ 19 dBm	231.78	108.56	69.23	3.54	271.37	mA
	TX HT40-MCS7 @ 16 dBm	231.08	108.32	68.80	3.57	238.83	mA
802.11a (5 GHz)	TX 6 Mbps @ 17 dBm	229.91	126.78	69.15	3.79	252.32	mA
	TX 54 Mbps @ 15 dBm	224.22	122.03	66.44	3.75	198.96	mA
802.11n (5 GHz)	TX HT20-MCS0 @ 17 dBm	217.62	129.90	69.17	3.79	251.08	mA
	TX HT20-MCS7 @ 15 dBm	219.53	126.77	68.88	3.79	224.83	mA
	TX HT40-MCS0 @ 17 dBm	234.52	126.83	69.18	3.79	254.55	mA
	TX HT40-MCS7 @ 15 dBm	234.52	126.81	68.92	3.79	226.08	mA
802.11ac (5 GHz)	TX VHT20 MCS0 @ 17 dBm	221.39	126.93	69.12	3.79	250.87	mA
	TX VHT20 MCS8 @ 14 dBm	220.38	126.61	68.85	3.79	215.73	mA
	TX VHT40 MCS0 @ 17 dBm	235.04	127.06	68.83	3.78	254.31	mA
	TX VHT40 MCS9 @ 13 dBm	234.20	126.71	68.71	3.77	207.46	mA
	TX VHT80 MCS0 @ 17 dBm	291.13	129.01	69.18	3.79	254.92	mA
	TX VHT80 MCS9 @ 13 dBm	291.01	128.36	68.80	3.79	206.90	mA
802.11ax	TX HE20-MCS0 @ 19 dBm	221.40	131.58	68.68	3.52	259.90	mA

(2.4 GHz)	TX HE20-MCS11 @ 14 dBm	222.32	131.51	68.60	3.57	222.00	mA
	TX HE40-MCS0 @ 19 dBm	237.86	133.69	69.10	3.58	269.26	mA
	TX HE40-MCS11 @ 14 dBm	238.90	133.92	68.70	3.58	224.56	mA
802.11ax (5 GHz)	TX HE20-MCS0 @ 17 dBm	235.56	138.64	77.94	3.78	251.82	mA
	TX HE20-MCS11 @ 12 dBm	234.59	138.54	77.64	3.79	199.67	mA
	TX HE40-MCS0 @ 17 dBm	248.84	140.28	78.11	3.79	252.54	mA
	TX HE40-MCS11 @ 12 dBm	248.43	139.83	77.72	3.79	200.42	mA
	TX HE80-MCS0 @ 17 dBm	299.44	143.77	78.14	3.79	253.93	mA
	TX HE80-MCS11 @ 12 dBm	306.87	143.34	77.80	3.79	198.52	mA

4.5. RF Performances

The following tables summarize the transmitting and receiving performances of AF50T.

4.5.1. Conducted RF Performance of Wi-Fi

Table 23: Conducted RF Output Power at 2.4 GHz (SISO)

Frequency	Min.	Typ.	Max.	Unit
802.11b @ 1 Mbps	18	20	22	dBm
802.11b @ 11 Mbps	18	20	22	dBm
802.11g @ 6 Mbps	17	19	21	dBm
802.11g @ 54 Mbps	14	16	18	dBm
802.11n, HT20 @ MCS0	17	19	21	dBm
802.11n, HT20 @ MCS7	14	16	18	dBm
802.11n, HT40 @ MCS0	17	19	21	dBm
802.11n, HT40 @ MCS7	14	16	18	dBm
802.11ax, HE20 @ MCS0	17	19	21	dBm

802.11ax, HE20 @ MCS11	12	14	16	dBm
802.11ax, HE40 @ MCS0	17	19	21	dBm
802.11ax, HE40 @ MCS11	12	14	16	dBm

Table 24: Conducted RF Output Power at 2.4 GHz (MIMO)

Frequency	Min.	Typ.	Max.	Unit
802.11n, HT20 @ MCS0	20	22	24	dBm
802.11n, HT20 @ MCS7	17	19	21	dBm
802.11n, HT40 @ MCS0	20	22	24	dBm
802.11n, HT40 @ MCS7	17	19	21	dBm
802.11ax, HE20 @ MCS0	20	22	24	dBm
802.11ax, HE20 @ MCS11	15	17	19	dBm
802.11ax, HE40 @ MCS0	20	22	24	dBm
802.11ax, HE40 @ MCS11	15	17	19	dBm

Table 25: Conducted RF Output Power at 5 GHz (SISO)

Frequency	Min.	Typ.	Max.	Unit
802.11a @ 6 Mbps	15	17	19	dBm
802.11a @ 54 Mbps	13	15	17	dBm
802.11n, HT20 @ MCS0	15	17	19	dBm
802.11n, HT20 @ MCS7	13	15	17	dBm
802.11n, HT40 @ MCS0	15	17	19	dBm
802.11n, HT40 @ MCS7	13	15	17	dBm
802.11ac, VHT20 @ MCS0	15	17	19	dBm
802.11ac, VHT20 @ MCS8	12	14	16	dBm

802.11ac, VHT40 @ MCS0	15	17	19	dBm
802.11ac, VHT40 @ MCS9	11	13	15	dBm
802.11ac, VHT80 @ MCS0	15	17	19	dBm
802.11ac, VHT80 @ MCS9	11	13	15	dBm
802.11ax, HE20 @ MCS0	15	17	19	dBm
802.11ax, HE20 @ MCS11	10	12	14	dBm
802.11ax, HE40 @ MCS0	15	17	19	dBm
802.11ax, HE40 @ MCS11	10	12	14	dBm
802.11ax, HE80 @ MCS0	15	17	19	dBm
802.11ax, HE80 @ MCS11	10	12	14	dBm

Table 26: Conducted RF Output Power at 5 GHz (MIMO)

Frequency	Min.	Typ.	Max.	Unit
802.11n, HT20 @ MCS0	18	20	22	dBm
802.11n, HT20 @ MCS7	16	18	20	dBm
802.11n, HT40 @ MCS0	18	20	22	dBm
802.11n, HT40 @ MCS7	16	18	20	dBm
802.11ac, VHT20 @ MCS0	18	20	22	dBm
802.11ac, VHT20 @ MCS8	15	17	19	dBm
802.11ac, VHT40 @ MCS0	18	20	22	dBm
802.11ac, VHT40 @ MCS9	14	16	18	dBm
802.11ac, VHT80 @ MCS0	18	20	22	dBm
802.11ac, VHT80 @ MCS9	14	16	18	dBm
802.11ax, HE20 @ MCS0	18	20	22	dBm
802.11ax, HE20 @ MCS11	13	15	17	dBm

802.11ax, HE40 @ MCS0	18	20	22	dBm
802.11ax, HE40 @ MCS11	13	15	17	dBm
802.11ax, HE80 @ MCS0	18	20	22	dBm
802.11ax, HE80 @ MCS11	13	15	17	dBm

Table 27: Conducted RF Receiving Sensitivity at 2.4 GHz

Frequency	Receiving Sensitivity (Typ.)
802.11b @ 1 Mbps	-96 dBm
802.11b @ 11 Mbps	-87 dBm
802.11g @ 6 Mbps	-92 dBm
802.11g @ 54 Mbps	-74 dBm
802.11n, HT20 @ MCS0	-92 dBm
802.11n, HT20 @ MCS7	-73 dBm
802.11n, HT40 @ MCS0	-89 dBm
802.11n, HT40 @ MCS7	-71 dBm
802.11ax, HE20 @ MCS0	-92 dBm
802.11ax, HE20 @ MCS11	-62 dBm
802.11ax, HE40 @ MCS0	-89 dBm
802.11ax, HE40 @ MCS11	-60 dBm

Table 28: Conducted RF Receiving Sensitivity at 5 GHz

Frequency	Receiving Sensitivity (Typ.)
802.11a @ 6 Mbps	-92 dBm
802.11a @ 54 Mbps	-75 dBm
802.11n, HT20 @ MCS0	-92 dBm

802.11n, HT20 @ MCS7	-74 dBm
802.11n, HT40 @ MCS0	-90 dBm
802.11n, HT40 @ MCS7	-72 dBm
802.11ac, VHT20 @ MCS0	-93 dBm
802.11ac, VHT20 @ MCS8	-71 dBm
802.11ac, VHT40 @ MCS0	-90 dBm
802.11ac, VHT40 @ MCS9	-67 dBm
802.11ac, VHT80 @ MCS0	-87 dBm
802.11ac, VHT80 @ MCS9	-62 dBm
802.11ax, HE20 @ MCS0	-93 dBm
802.11ax, HE20 @ MCS11	-63 dBm
802.11ax, HE40 @ MCS0	-90 dBm
802.11ax, HE40 @ MCS11	-60 dBm
802.11ax, HE80 @ MCS0	-87 dBm
802.11ax, HE80 @ MCS11	-56 dBm

4.5.2. Conducted RF Performance of Bluetooth

Table 29: Conducted RF Performance of Bluetooth

Frequency	Transmitting Power (Typ.)	Transmitting Power (Max.)	Receiving Sensitivity (Typ.)	Unit
BR	8	10	-93	dBm
EDR(π /4-DQPSK)	6	10	-92	dBm
EDR(8-DPSK)	6	10	-86	dBm
BLE(1M)	6	10	-97	dBm

4.6. Electrostatic Discharge

The module is not protected against Electrostatic Discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module electrostatic discharge characteristics.

Table 30: Electrostatic Discharge Characteristics

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VDD, GND	±5	±10	kV
All Antenna Interfaces	±6	±10	kV
Other Interfaces	±0.5	±1	kV

5 Mechanical Dimensions

This chapter describes the mechanical dimensions of AF50T module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.05 mm unless otherwise specified.

5.1. Mechanical Dimensions of the Module

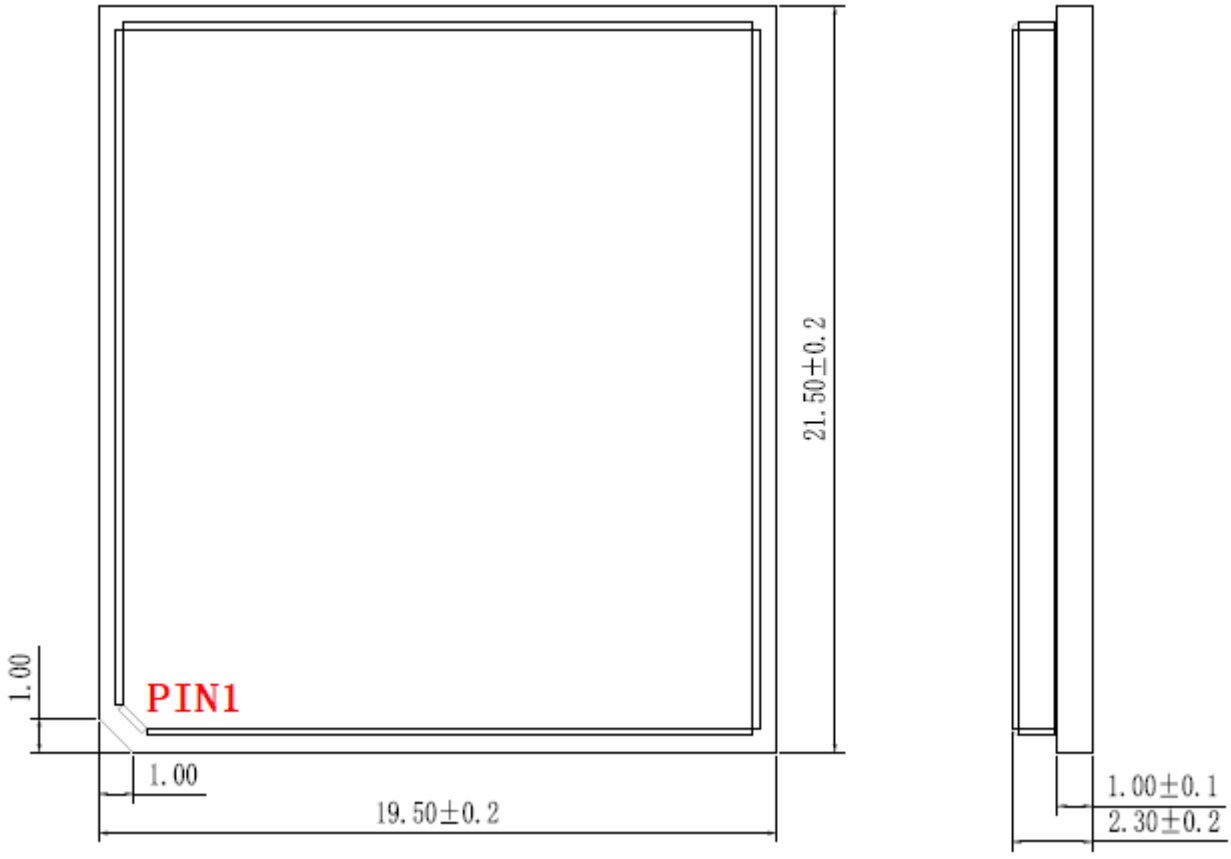


Figure 20: AF50T Top and Side Dimensions

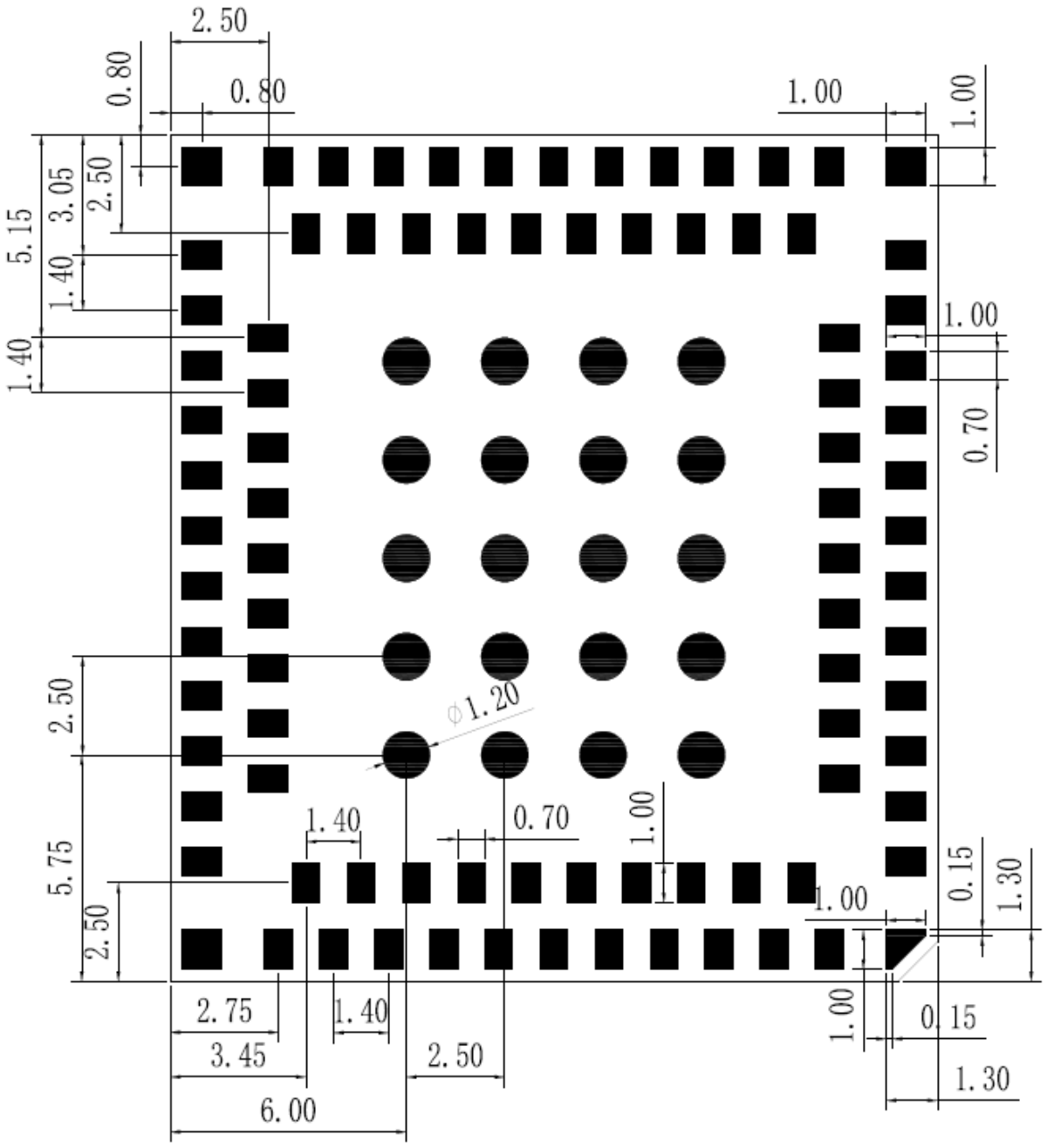


Figure 21: AF50T Bottom Dimension (Bottom View)

NOTE

The package warpage level of the module conforms to *JEITA ED-7306* standard.

5.2. Recommended Footprint

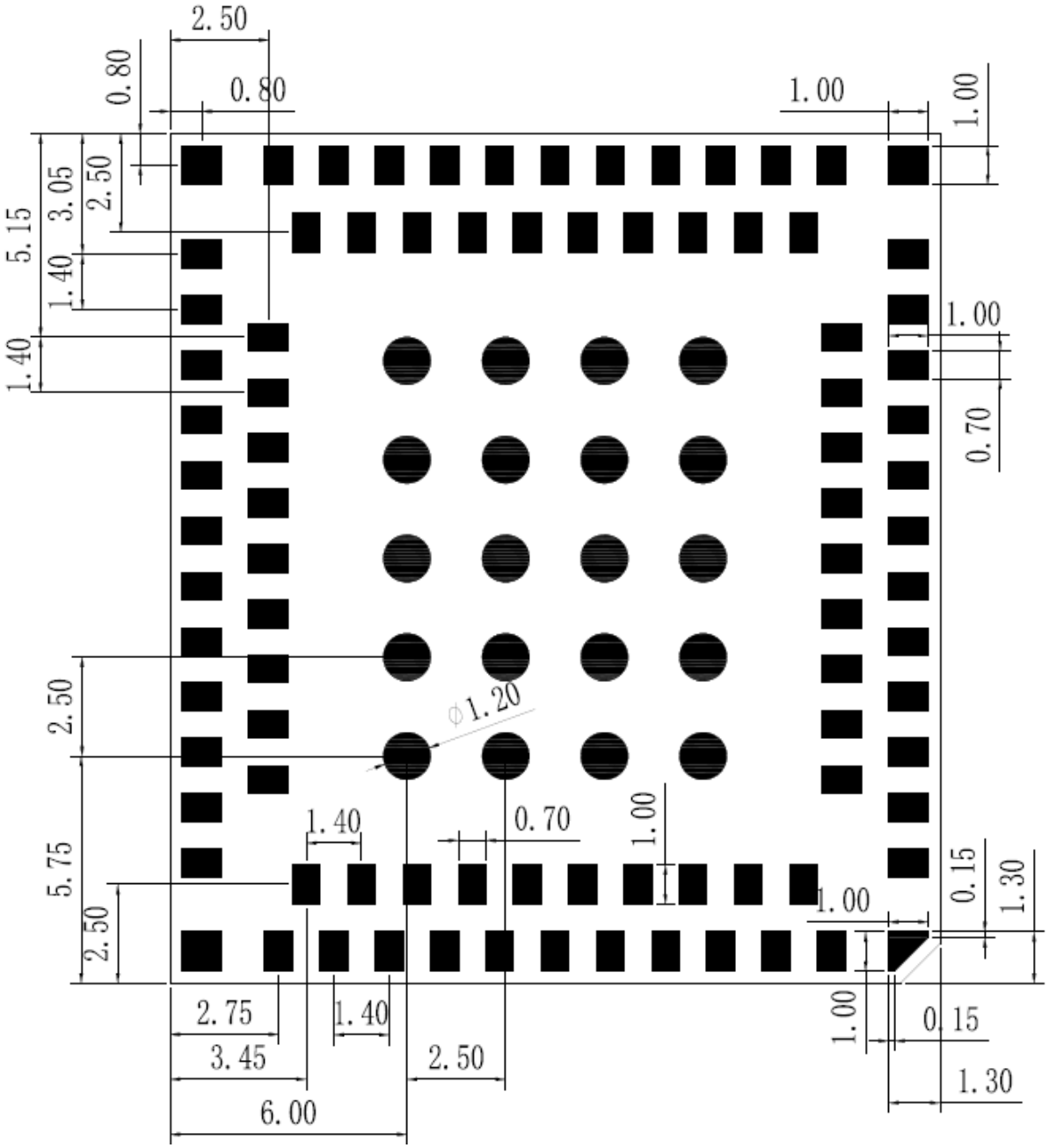


Figure 22: Recommended Footprint (Bottom View)

NOTES

1. For easy maintenance of the module, please keep about 3mm spaces between the module and other components on host PCB.
2. Keep all RESERVED pins open.

5.3. Top and Bottom Views of the Module

Figure 23: Top View of the Module

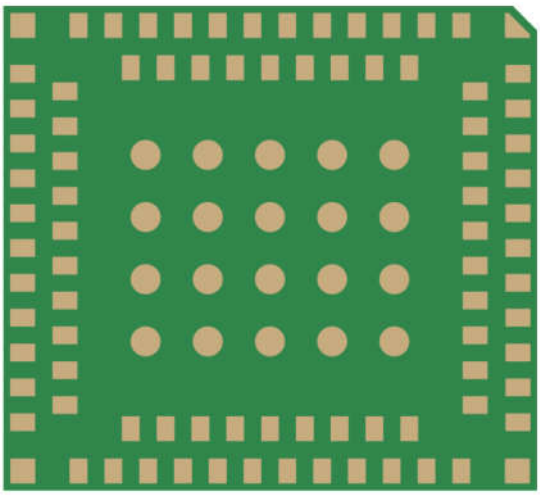


Figure 24: Bottom View of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

6 Storage, Manufacturing and Packaging

6.1. Storage

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35 %–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours [1)] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

NOTES

1. [1)] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*.
2. To avoid blistering, layer separation and other soldering issues, it is forbidden to expose the modules to the air for a long time. If the temperature and moisture do not conform to *IPC/JEDEC J-STD-033* or the relative moisture is over 60 %, it is recommended to start the solder reflow process within 24 hours after the package is removed. And do not remove the packages of tremendous modules if they are not ready for soldering.
3. Take the module out of the packaging and put it on high-temperature resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.

6.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [5]***.

It is suggested that the peak reflow temperature is 238 °C to 246 ºC, and the absolute maximum reflow temperature is 246 ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

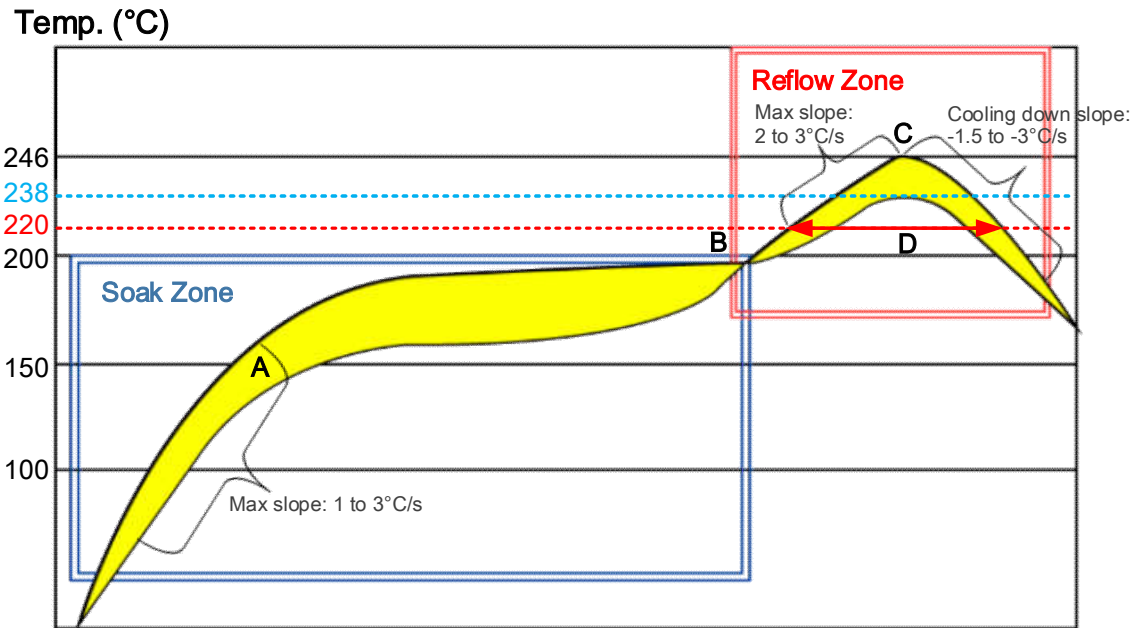


Figure 25: Recommended Reflow Soldering Thermal Profile

Table 31: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	2–3 °C/s
Reflow time (D: over 220 °C)	45–70 s
Max temperature	238 °C to 246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTES

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.

6.3. Packaging

AF50T module is packaged in a vacuum-sealed bag which is ESD protected. The bag should not be opened until the devices are ready to be soldered onto the application.

AF50T is packaged in tape and reel carriers.

Table 32: Reel Packaging

Model Name	MOQ for MP	Minimum Package: TBD	Minimum Package TBD
AF50T	TBD	Size: TBD N.W: TBD G.W: TBD	Size: TBD N.W: TBD G.W: TBD

7 Appendix A References

Table 33: Related Documents

SN	Document Name	Description
[1]	Quectel_LTE_OPEN_EVB_User_Guide	EVB user guide for Quectel LTE-QuecOpen modules
[2]	Quectel_UMTS&LTE_EVB_User_Guide	UMTS&LTE EVB user guide
[3]	Quectel_AG55xQ_Series_QuecOpen_Reference_Design	AG55xQ series reference design
[4]	Quectel_RF_Layout_Application_Note	RF layout application note
[5]	Quectel_Module_Secondary_SMT_User_Guide	Module secondary SMT user guide

Table 34: Terms and Abbreviations

Abbreviation	Description
AP	Access Point
BPSK	Binary Phase Shift Keying
BT	Bluetooth
CCK	Complementary Code Keying
CTS	Clear To Send
ESD	Electrostatic Discharge
GND	Ground
HT	High Throughput
IEEE	Institute of Electrical and Electronics Engineers
I_{IL}	Input Leakage Current
I/O	Input/Output

LTE	Long Term Evolution
Mbps	Megabits per second
MCS	Modulation and Coding Scheme
MOQ	Minimum Order Quantity
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RH	Relative Humidity
RoHS	Restriction of Hazardous Substances
RTS	Request To Send
RX	Receive
SDIO	Secure Digital Input/Output
TBD	To Be Determined
TX	Transmit
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VHT	Very High Throughput
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value

VSWR	Voltage Standing Wave Ratio
Wi-Fi	Wireless-Fidelity
WLAN	Wireless Local Area Network

FCC Certification Requirements.
According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.
And the following conditions must be met:
1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based timeaveraging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.
2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.
3. A label with the following statements must be attached to the host end product: This device contains FCC ID: XMR202102AF50T
4. This module must not transmit simultaneously with any other antenna or transmitter
5. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.
For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093
If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.
For this device, OEM integrators must be provided with labeling instructions of finished products.
Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:
A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).
For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module FCC ID: XMR202102AF50T" or "Contains FCC ID: XMR202102AF50T" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.
The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Supplier's Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Wireless Access Systems including Radio Local Area Networks (WAS/RLANs) frequency range 5150 – 5350 MHz is Restricted to indoor use in EU, this device contains 5150-5250 MHz.