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EC25-T

Hardware Design

LTE Standard Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.

Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.

Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.

Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.

The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.

In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2022-05-19	Joe MA/ Ethan SHAN	Creation of the document
1.0	2022-07-07	Joe MA/ Ethan SHAN	First official release

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1 Introduction

This document defines EC25-T and describes its air interface and hardware interfaces which are connected with your applications.

This document can help you quickly understand module interface specifications, electrical and mechanical details, as well as other related information of EC25-T. To facilitate its application in different fields, relevant reference design is also provided for your reference. Associated with application note and user guide, you can use EC25-T to design and set up mobile applications easily.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDC2_DATA[0:3] refers to all four SDC2_DATA pins: SDC2_DATA0, SDC2_DATA1, SDC2_DATA2, and SDC2_DATA3.

2 Product Overview

2.1. Frequency Bands and Functions

EC25-T is an LTE wireless communication module with Rx-diversity. It provides data connectivity on LTE-FDD networks. It also provides GNSS [1] and voice functionality [2] for your specific applications.

The following table shows the frequency bands GNSS and function of EC25-T.

Table 2: Frequency Bands and GNSS Function

Network Type	Frequency Bands/Function
LTE-FDD	B2/B4/B5/B12/B66/B71
GNSS [1]	GPS/GLONASS/BDS/Galileo/QZSS

With a compact profile of 29.0 mm × 32.0 mm × 2.4 mm, EC25-T meets almost all requirements for M2M applications such as automation, metering, tracking system, security, router, wireless POS, mobile computing device, PDA phone, and tablet PC.

EC25-T is an SMD type module which can be embedded into applications through its 144 pins, including 80 LCC pins and 64 LGA pins.

[1] GNSS function is optional.
[2] EC25-T contains **Data + Voice** version and **Data-only** version.

2.2. Key Features

The following table describes the detailed features of EC25-T.

Table 3: Key Features

Features	Description
Power Supply	● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
Transmitting Power	● Class 3 (23 dBm ±2 dB) for LTE-FDD bands
LTE Features	● Supports up to non-CA Cat 4 FDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Supports MIMO in DL direction ● LTE-FDD: Max. 150 Mbps (DL)/Max. 50 Mbps (UL)
Internet Protocol Features	● Supports TCP/UDP/PPP/FTP/FTPS/HTTP/HTTPS/NTP/PING/QMI/NITZ/SMTP/SSL/MQTT/FILE/CMUX/SMTPS/MMS protocols ● Supports PAP and CHAP protocols for PPP connections
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
USIM Interface	Supports USIM card: 1.8 V, 3.0 V
Audio Features	● Supports one digital audio interface: PCM interface ● LTE: AMR/AMR-WB ● Supports echo cancellation and noise suppression
PCM Interface	● Used for audio function with external codec ● Supports 16-bit linear data format ● Supports long frame synchronization and short frame synchronization ● Supports master and slave modes, but must be the master in long frame synchronization
USB Interface	● Compliant with USB 2.0 specification (slave only); the data transfer rate can reach up to 480 Mbps ● Used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging, firmware upgrade and voice over USB ● Supports USB serial drivers for: Windows 7/8/8.1/10/11, Linux 2.6–5.18, Android 4.x–12.x, etc.
UART Interfaces	**Main UART:** ● Used for AT command communication and data transmission ● Baud rate: reach up to 921600 bps, 115200 bps by default

	● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for Linux console and log output ● 115200 bps baud rate
SD Card Interface	Supports SD 3.0 protocol
Rx-diversity	Supports LTE Rx-diversity
GNSS Features	● Protocol: NMEA 0183 ● Data update rate: 1 Hz by default
AT Commands	● Compliant with *3GPP TS 27.007*, *3GPP TS 27.005* ● Quectel enhanced AT commands
Network Indication	Two pins including NET_MODE and NET_STATUS to indicate network connectivity status
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● Rx-diversity antenna interface (ANT_DIV) ● GNSS antenna interface (ANT_GNSS)
Physical Characteristics	● Size: (29.0 ±0.15) mm × (32.0 ±0.15) mm × (2.4 ±0.2) mm ● Weight: approx. 4.9 g
Temperature Range	● Operating temperature range: -35 to +75 °C [3] ● Extended temperature range: -40 to +85 °C [4] ● Storage temperature range: -40 to +90 °C
Firmware Upgrade	USB 2.0 interface or DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

3 Application Interfaces

3.1. General Description

EC25-T is equipped with 80 LCC pins and 64 LGA pins that can be connected to cellular application platform. The subsequent chapters will provide detailed descriptions of the following interfaces/functions.

[3] Within the operating temperature range, the module meets 3GPP specifications.
[4] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

- Power supply
- USIM interface
- USB interface
- UART interfaces
- PCM and I2C interfaces
- SD card interface
- ADC interfaces
- Indication signals
- USB_BOOT interface

3.2. Pin Assignment

The following figure shows the pin assignment of EC25-T.

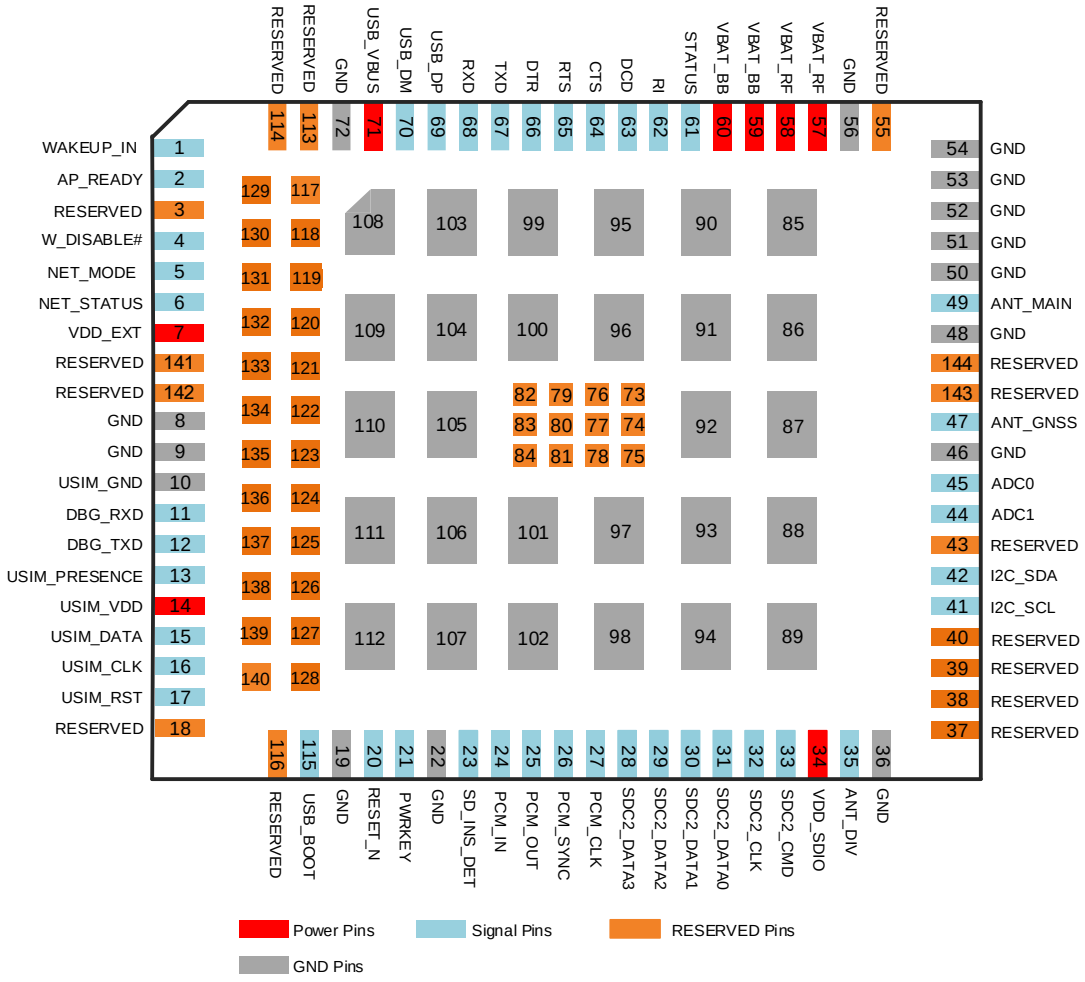


Figure 1: Pin Assignment (Top View)

NOTE

1. WAKEUP_IN, NET_MODE and USB_BOOT pins cannot be pulled up before startup.
2. PWRKEY output voltage is 0.8 V because of the diode drop in the baseband chipset.
3. Digital audio (PCM) interface is only supported on **Data + Voice** version.
4. Keep all RESERVED pins and unused pins unconnected.
5. GND pins 85–112 should be connected to ground in the design. Pins 73–84 (RESERVED) should not be designed in schematic and PCB decal, and these pins should be served as a keepout area.

3.3. Pin Description

The following tables show the pin definition of EC25-T.

Table 4: I/O Parameters Definition

Type	Description
AI	Analog input
AO	Analog output
AIO	Analog Input/Output
DI	Digital input
DO	Digital output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

Table 5: Pin Description

Power Supply

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VBAT_BB	59, 60	PI	Power supply for module's baseband part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 0.8 A.
VBAT_RF	57, 58	PI	Power supply for module's RF part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 1.8 A in a burst transmission.
VDD_EXT	7	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. If unused, keep it open.
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 85–112				
Power-on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	21	DI	Turn on/off the module		The output voltage is 0.8 V because of the diode drop in the baseband chipset.
RESET_N	20	DI	Reset the module	V_{IH}max = 2.1 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	If unused, keep it open.
Status Indication Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	61	OD	Indicate the module's operation status		The driving current should be less than 0.9 mA. An external pull-up resistor is required. If unused, keep it open.
NET_MODE	5	DO	Indicate the module's network registration mode	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. It cannot be pulled up before startup. If unused, keep it open.
NET_STATUS	6	DO	Indicate the module's network activity status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.
USB Interface					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_VBUS	71	PI	USB connection detection	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	Typ. 5.0 V. If unused, keep it open.
USB_DP	69	AIO	USB differential data (+)		USB 2.0 Compliant. Require differential impedance of 90 Ω. If unused, keep them open.
USB_DM	70	AIO	USB differential data (-)		
USIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_GND	10		Specified ground for USIM card		
USIM_ PRESENCE	13	DI	USIM card hot plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
USIM_VDD	14	PO	USIM card power supply	$I_O$max = 50 mA **For 1.8 V USIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V USIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM_DATA	15	DIO	USIM card data	**For 1.8 V USIM:** V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V USIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM_CLK	16	DO	USIM card clock	**For 1.8 V USIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
USIM_RST	17	DO	USIM card reset		

				For 3.0 V USIM: V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RI	62	DO	Main UART ring indicator	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
DCD	63	DO	Main UART data carrier detection		
CTS	64	DO	DTE clear to send signal from DCE		1.8 V power domain. If unused, keep it open. Connect to DTE's RTS.
RTS	65	DI	DTE request to send signal to DCE	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open. Connect to DTE's CTS.
DTR	66	DI	Main UART data terminal ready, sleep mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Pulled up by default. DTR can wake up the module when DTR remains at low level. If unused, keep it open.
TXD	67	DO	Main UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
RXD	68	DI	Main UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	12	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
DBG_RXD	11	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

ADC0	45	AI	General-purpose ADC interface	Voltage range: 0.3 V to VBAT_BB	If unused, keep them open.
ADC1	44	AI	General-purpose ADC interface		
PCM Interface [5]					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_IN	24	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
PCM_OUT	25	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
PCM_SYNC	26	DIO	PCM frame sync	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Serve as output signal in master mode. Serve as input signal in slave mode. If unused, keep them open.
PCM_CLK	27	DIO	PCM clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	41	OD	I2C serial clock. (for external codec)		An external 1.8 V pull-up resistor is required. If unused, keep them open.
I2C_SDA	42	OD	I2C serial data. (for external codec)		
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDC2_DATA3	28	DIO	SD card SDIO data bit 3	**1.8 V signaling:** V_{OL}max = 0.45 V	SDIO signal level can be selected according to the

[5] The pins of PCM interface are used for audio design on EC25-T and Bluetooth function on FC20 series/FC21 module.

SDC2_DATA2	29	DIO	SD card SDIO data bit 2	V_{OH}min = 1.4 V V_{IL}min = -0.3 V V_{IL}max = 0.58 V V_{IH}min = 1.27 V V_{IH}max = 2.0 V **3.0 V signaling:** V_{OL}max = 0.38 V V_{OH}min = 2.01 V V_{IL}min = -0.3 V V_{IL}max = 0.76 V V_{IH}min = 1.72 V V_{IH}max = 3.34 V	signal level supported by SD card; see SD 3.0 protocol for more details. If unused, keep them open.
SDC2_DATA1	30	DIO	SD card SDIO data bit 1		
SDC2_DATA0	31	DIO	SD card SDIO data bit 0		
SDC2_CLK	32	DO	SDIO clock	**1.8 V signaling:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V **3.0 V signaling:** V_{OL}max = 0.38 V V_{OH}min = 2.01 V	
SDC2_CMD	33	DIO	SD card SDIO command	**1.8 V signaling:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V V_{IL}min = -0.3 V V_{IL}max = 0.58 V V_{IH}min = 1.27 V V_{IH}max = 2.0 V **3.0 V signaling:** V_{OL}max = 0.38 V V_{OH}min = 2.01 V V_{IL}min = -0.3 V V_{IL}max = 0.76 V V_{IH}min = 1.72 V V_{IH}max = 3.34 V	
SD_INS_DET	23	DI	SD card insertion detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If SD card function is unused, keep this pin open.
VDD_SDIO	34	PO	SD card SDIO pull-up power	$I_O$max = 50 mA	1.8/2.85 V configurable. Cannot be used for SD card power supply. If unused, keep it open.

RF Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_DIV	35	AI	Diversity antenna interface		50 Ω impedance. If unused, keep it open.
ANT_MAIN	49	AIO	Main antenna interface		50 Ω impedance.
ANT_GNSS	47	AI	GNSS antenna interface		50 Ω impedance. If unused, keep it open.
Other Interface Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WAKEUP_IN	1	DI	Sleep mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Cannot be pulled up before startup. Low level can wake up the module. If unused, keep it open.
W_DISABLE#	4	DI	Airplane mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Pull-up by default. At low level, the module can enter airplane mode. If unused, keep it open.
AP_READY	2	DI	Application processor sleep state detection	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
USB_BOOT Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	115	DI	Force the module to enter emergency download mode	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Cannot be pulled up before startup. It is recommended to reserve test point.
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	3, 18, 37–40, 43, 55, 73–84, 113, 114, 116, 117, 118–139, 140–144				Keep these pins unconnected.

3.4. Operating Modes

The following table briefly outlines the operating modes to be mentioned in the following chapters.

Table 6: Overview of Operating Modes

Modes	Details	
Full functionality Mode	Idle	The module remains registered on the network, and is ready to send and receive data. In this mode, the software is active.
	Voice/ Data	The module is connected to network. Its current consumption varies with the network setting and data transfer rate.
Airplane Mode	**AT+CFUN=4** or W_DISABLE# pin can set the module to airplane mode where the RF function is invalid.	
Minimum Functionality Mode	**AT+CFUN=0** can set the module into a minimum functionality mode without removing the power supply. In this mode, both RF function and USIM card are invalid.	
Sleep Mode	The module remains the ability to receive paging message, SMS, voice call and TCP/UDP data from the network normally. In this mode, the current consumption of the module is reduced to a very low level.	
Power Down Mode	The module's power supply is cut off by its power management unit. In this mode, the software is inactive, the serial interfaces are inaccessible, while the operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

For details of the commands, see ***document [2]***.

3.5. Sleep Mode

EC25-T can reduce its current consumption to a minimum value during the sleep mode. The following

section describes the power saving procedures of EC25-T.

3.5.1. UART Application Scenario

If the host communicates with the module via UART interface, the following preconditions can let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode. For details of the command, see ***document [2]***.
- Drive DTR to high level.

The following figure shows the connection between the module and the host.

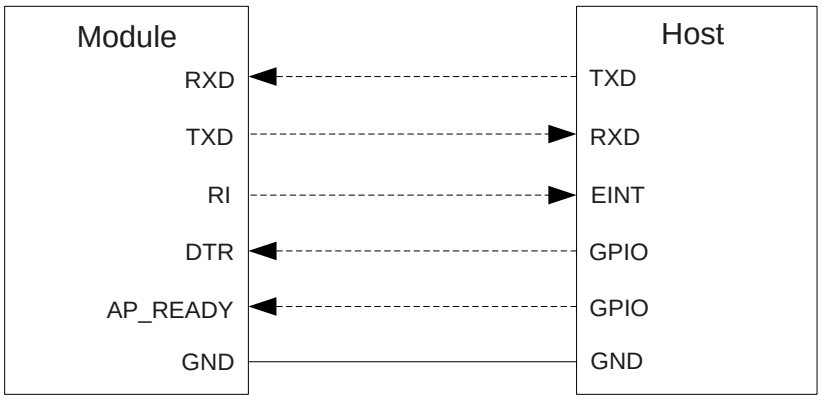


Figure 2: Sleep Mode Application via UART

- Driving the module's DTR to low level will wake up the module.
- When EC25-T has a URC to report, RI signal will wake up the host. See ***Chapter 3.16.3*** for details about RI behaviors.
- AP_READY will detect the sleep state of the host (can be configured to high level or low level detection). See ***document [3]*** for details about **AT+QCFG="apready"**.

3.5.2. USB Application Scenario

3.5.2.1. USB Application with USB Remote Wakeup Function

If the host supports USB suspend/resume and remote wakeup functions, the following three preconditions must be met to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure shows the connection between the module and the host.

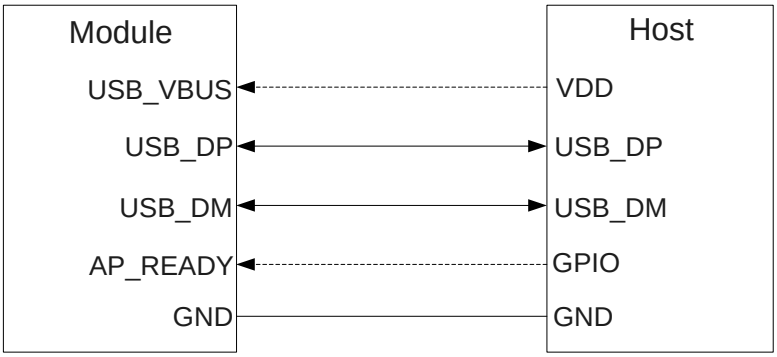


Figure 3: Sleep Mode Application with USB Remote Wakeup

- Sending data to EC25-T via USB will wake up the module.
- When EC25-T has a URC to report, the module will send remote wake-up signals via USB bus to wake up the host.

3.5.2.2. USB Application with USB Suspend/Resume and RI Function

If the host supports USB suspend and resume, but does not support remote wake-up function, the RI signal is needed to wake up the host.
There are three preconditions to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure shows the connection between the module and the host.

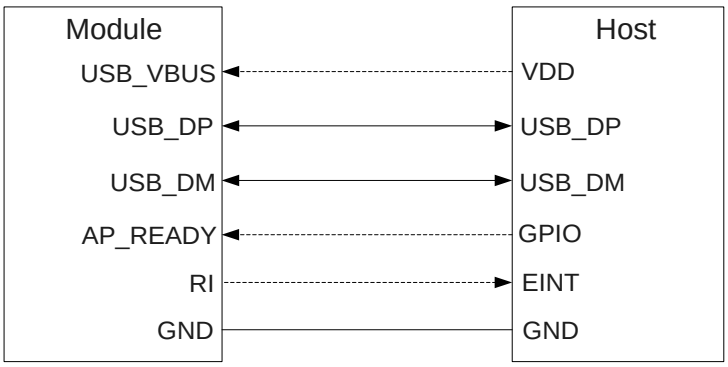


Figure 4: Sleep Mode Application with RI

- Sending data to EC25-T via USB will wake up the module.
- When EC25-T has a URC to report, RI signal will wake up the host.

3.5.2.3. USB Application without USB Suspend Function

If the host does not support USB suspend function, USB_VBUS should be disconnected via an additional control circuit to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

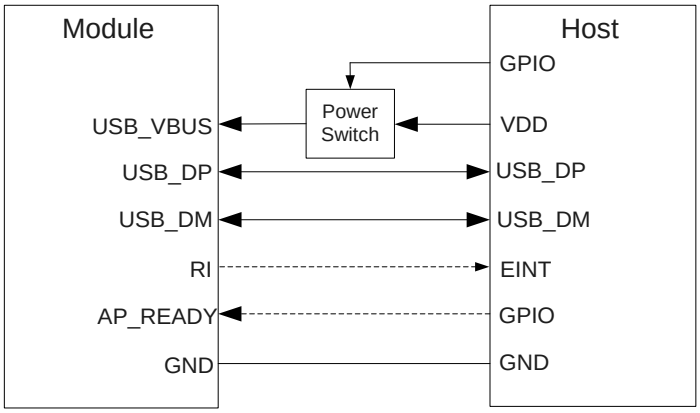


Figure 5: Sleep Mode Application without Suspend Function

Switching on the power switch to supply power to USB_VBUS will wake up the module.

NOTE

Pay attention to the voltage-level matching of the circuit in dotted line between the module and the host. For more details about EC25-T power management application, see ***document [4]***.

3.5.3. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default. Driving it to low level will let the module enter airplane mode.

Software:

AT+CFUN provides the choice of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode. Both USIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

NOTE

1. The W_DISABLE# control function is disabled in firmware by default. It can be enabled by **AT+QCFG="airplanecontrol"**.
2. The execution of **AT+CFUN** will not affect GNSS function.

3.6. Power Supply

3.6.1. Power Supply Pins

EC25-T provides four VBAT pins for connection with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part
- Two VBAT_BB pins for module's baseband part

The following table shows the details of VBAT pins and ground pins.

Table 7: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	57, 58	Power supply for module's RF part	3.3	3.8	4.3	V
VBAT_BB	59, 60	Power supply for module's baseband part	3.3	3.8	4.3	V
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 85–112		-	0	-	V

3.6.2. Decrease Voltage Drop

The power supply range of EC25-T is from 3.3–4.3 V. Please make sure that the input voltage will never drop below 3.3 V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 3G and 4G networks.

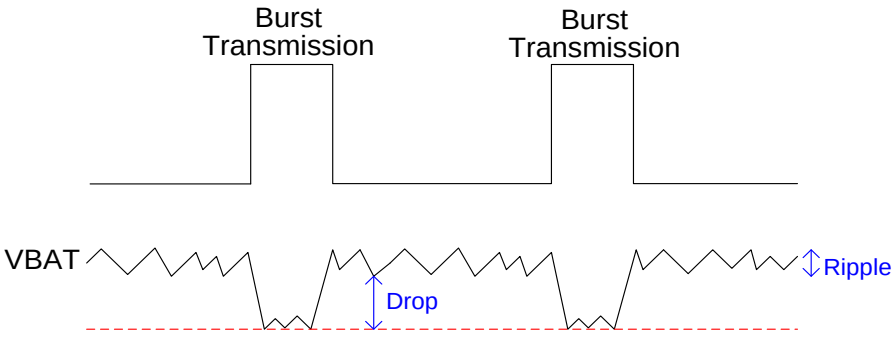


Figure 6: Power Supply Limits During Burst Transmission

To decrease the voltage drop, bypass capacitors of about 100 μF with low ESR (ESR = 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT_BB/VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1 mm; and the width of VBAT_RF trace should be no less than 2 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to avoid the damage caused by electric surge and ESD, it is suggested that a TVS component with suggested low reverse stand-off voltage V_{RWM} 4.5 V, low clamping voltage V_C and high reverse peak pulse current I_{PP} should be used. The following figure shows the star structure of the power supply.

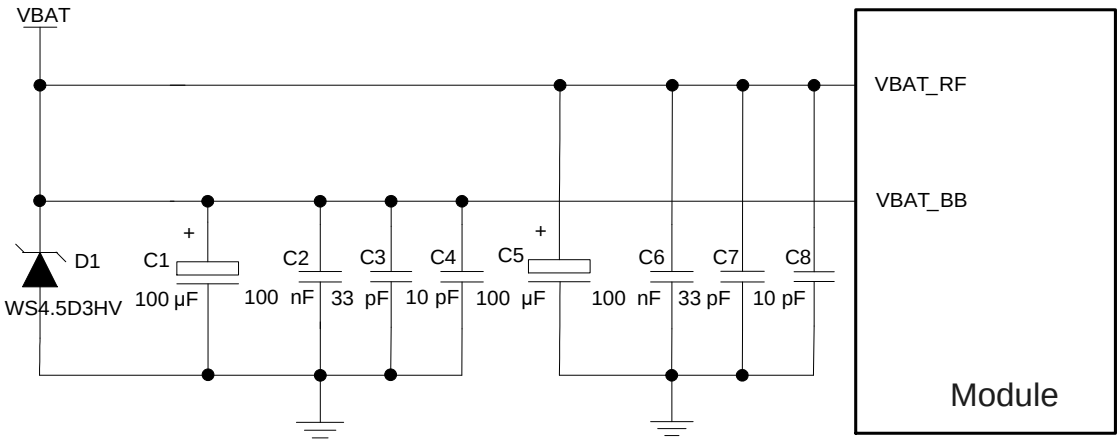


Figure 7: Star Structure of the Power Supply

3.6.3. Reference Design for Power Supply

The performance of the module largely depends on the power source. The power supply should be able to provide sufficient current up to 2.0 A at least. If the voltage drop between the input and output is not too

high, it is suggested that an LDO should be used to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5.0 V input power source. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

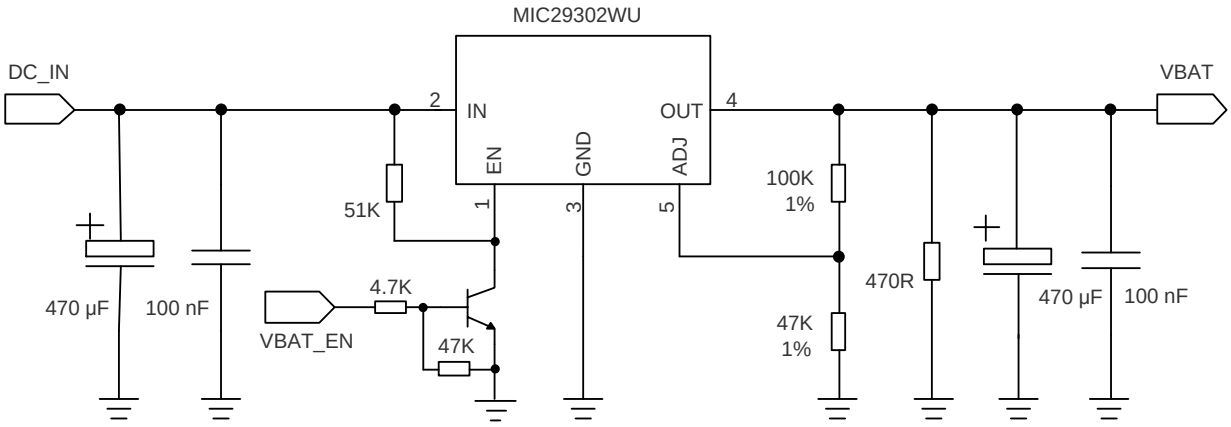


Figure 8: Reference Circuit of Power Supply

NOTE

To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, then the power supply can be cut off.

3.6.4. Power Supply Voltage Monitoring

AT+CBC can be used to monitor the VBAT_BB voltage value. For more details, see ***document [2]***.

3.7. Turn On

3.7.1. Turn On with PWRKEY

The following table shows the pin definition of PWRKEY.

Table 8: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment

PWRKEY	21	DI	Turn on/off the module	The output voltage is 0.8 V because of the diode drop in the chipset.

When the module is in power down mode, it can be turned on by driving PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY. After STATUS pin (require external pull-up resistor) outputs a low level, PWRKEY pin can be released.

A simple reference circuit is illustrated in the following figure.

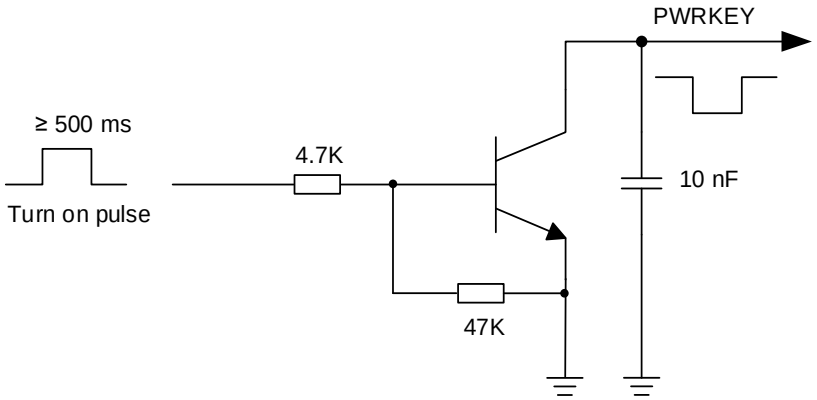


Figure 9: Turn On the Module by Using Driving Circuit

The other way to control the PWRKEY is using a button directly. When pressing the button, electrostatic strike may generate from fingers. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

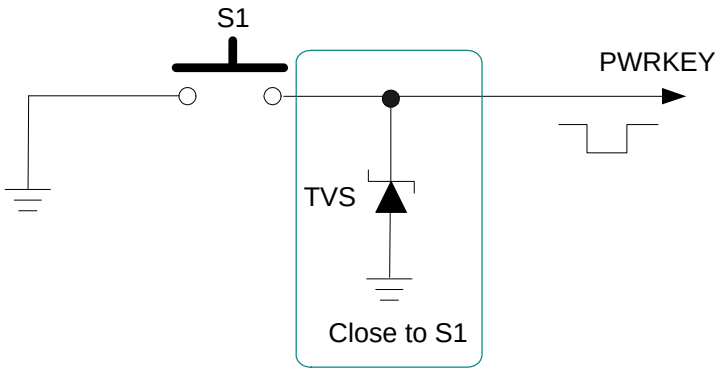


Figure 10: Turn On the Module by Using a Button

The power-up scenario is illustrated in the following figure.

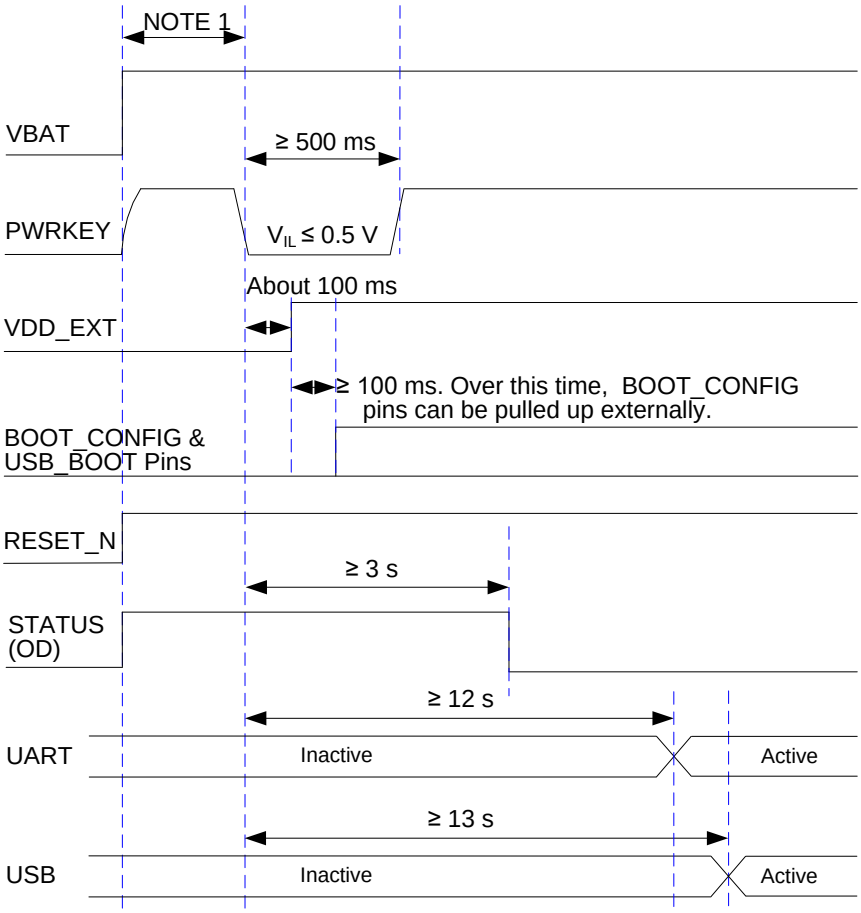


Figure 11: Power-up Timing

NOTE

1. Make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.
2. PWRKEY can be pulled down directly to GND with a recommended 10 kΩ resistor if module needs to be powered on automatically and shutdown is not needed.
3. The output voltage of PWRKEY is 0.8 V because of the diode drop in the baseband chipset.
4. BOOT_CONFIG pins (WAKEUP_IN, NET_MODE and USB_BOOT) cannot be pulled up before statup.

3.8. Turn Off

The following procedures can be used to turn off the module normally:

- Turn off the module using the PWRKEY pin.
- Turn off the module using **AT+QPOWD**. For details of the command, see ***document [2]***.

3.8.1. Turn Off with PWRKEY

Driving the PWRKEY pin to low for at least 650 ms, the module will execute power-off procedure after the PWRKEY is released. The power-down scenario is illustrated in the following figure.

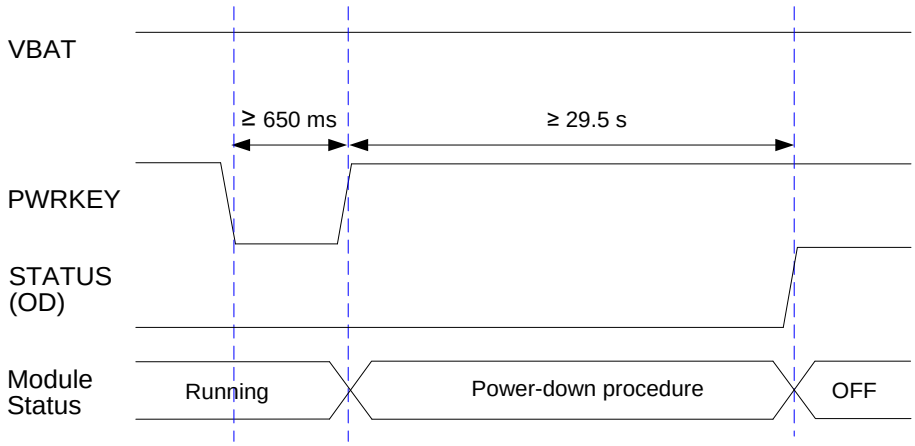


Figure 12: Power-down Timing

3.8.2. Turn Off with AT Command

It is also a safe way to use **AT+QPOWD** to turn off the module, which is similar to turning off the module via PWRKEY pin. See ***document [2]*** for details about **AT+QPOWD**.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, then the power supply can be cut off.
2. When turning off module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on again after a successful turn-off.

3.9. Reset

The RESET_N pin can be used to reset the module. The module can be reset by driving RESET_N low for 150–460 ms.

Table 9: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	20	DI	Reset the module	1.8 V power domain

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

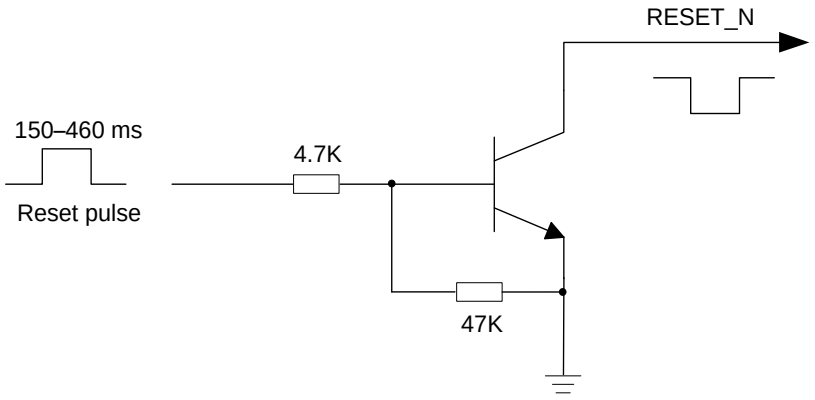


Figure 13: Reference Circuit of RESET_N by Using Driving Circuit

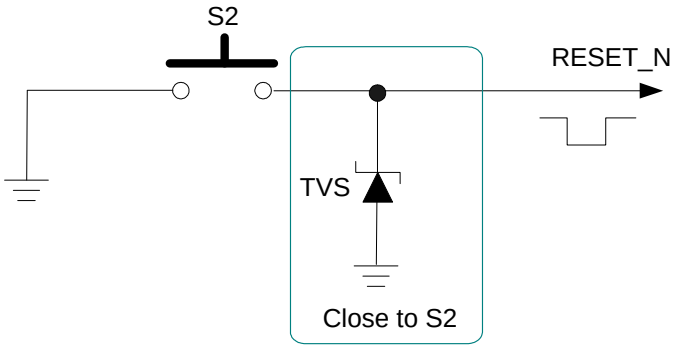


Figure 14: Reference Circuit of RESET_N by Using a Button

The reset timing is illustrated in the following figure.

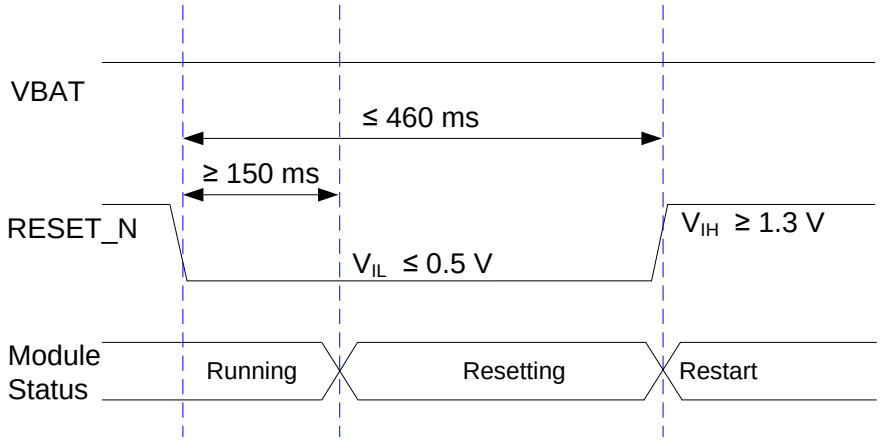


Figure 15: Reset Timing

NOTE

1. Use RESET_N only when failed to turn off the module by **AT+QPOWD** and PWRKEY pin.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

3.10. USIM Interface

The USIM interface circuitry meets ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V USIM cards are supported.

Table 10: Pin Definition of USIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	14	PO	USIM card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM_DATA	15	DIO	USIM card data	
USIM_CLK	16	DO	USIM card clock	
USIM_RST	17	DO	USIM card reset	
USIM_ PRESENCE	13	DI	USIM card hot plug detection	1.8 V power domain. If unused, keep it open.
USIM_GND	10		Specified ground for USIM card	

EC25-T supports USIM card hot-plug via the USIM_PRESENCE pin. The function supports low level and high level detections. By default, it is disabled, and can be configured via **AT+QSIMDET**. See ***document [2]*** for more details about the command.

The following figure shows a reference design for USIM interface with an 8-pin USIM card connector.

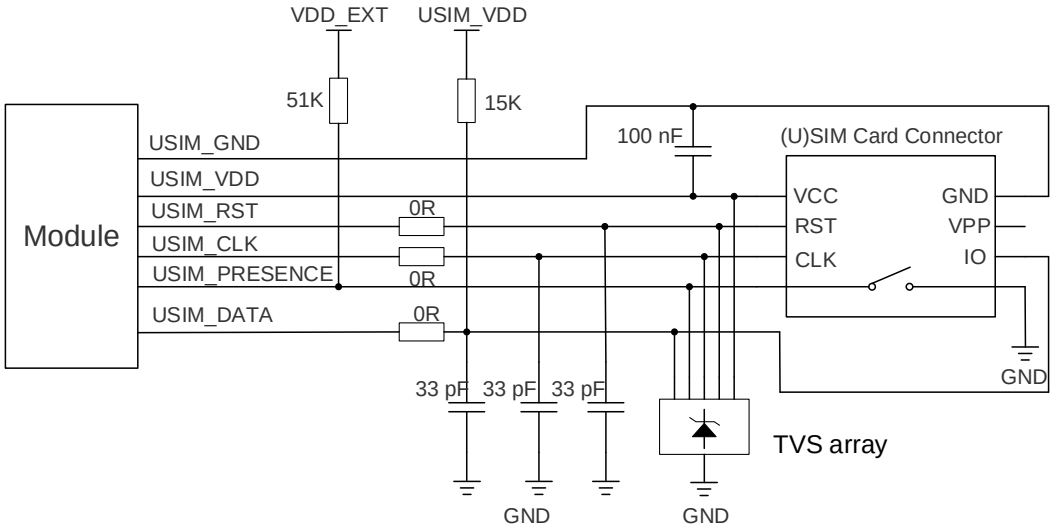


Figure 16: Reference Circuit of USIM Interface with an 8-pin USIM Card Connector

If USIM card detection function is not needed, keep USIM_PRESENCE unconnected. A reference circuit for USIM interface with a 6-pin USIM card connector is illustrated in the following figure.

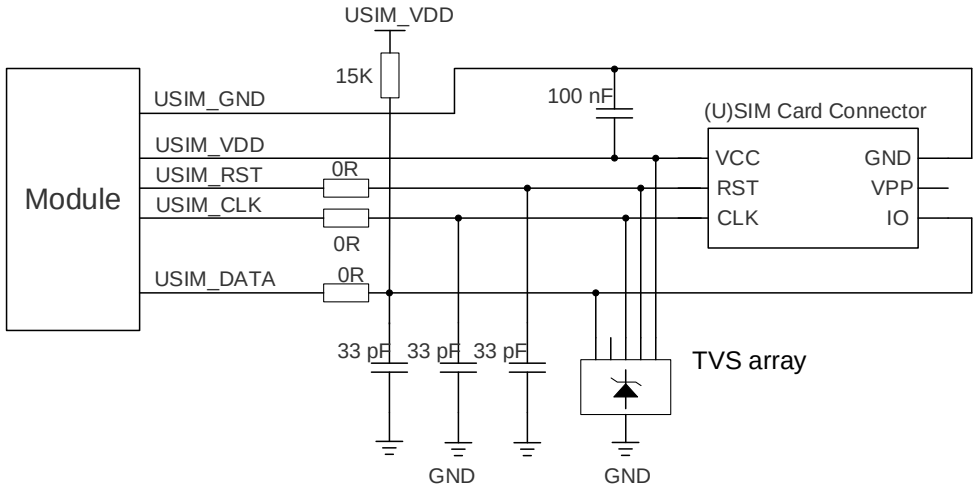


Figure 17: Reference Circuit of USIM Interface with a 6-pin USIM Card Connector

To enhance the reliability and availability of the USIM card in your applications, please follow the criteria below in USIM circuit design:

- Keep placement of USIM card connector to the module as close as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep SIM card signals away from RF and power supply traces.
- Make sure the bypass capacitor between USIM_VDD and USIM_GND less than 1 μF, and place it as close to (USIM card connector as possible. If the ground is complete on customers' PCB, USIM_GND can be connected to PCB ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- For better ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should not be more than 15 pF. The 0 Ω resistors should be added in series between the module and the USIM card to facilitate debugging. The 33 pF capacitors are used for filtering interference of EGSM900. Please note that the USIM peripheral circuit should be close to the USIM card connector.
- The pull-up resistor on USIM_DATA trace can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the USIM card connector.

3.11. USB Interface

EC25-T contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480 Mbps) and full-speed (12 Mbps) modes. The USB interface can only serve as a slave device.

The interface can be used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging, firmware upgrade and voice over USB.
The following table shows the pin definition of USB interface.

Table 11: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	69	AIO	USB differential data (+)	USB 2.0 Compliant. Require differential impedance of 90 Ω. If unused, keep them open.
USB_DM	70	AIO	USB differential data (-)	
USB_VBUS	71	PI	USB connection detection	Typ. 5.0 V
GND	72		Ground	

For more details about the USB 2.0 specifications, visit http://www.usb.org/home.

The USB interface is recommended to be reserved for firmware upgrade in your designs. The following figure shows a reference circuit of USB interface.

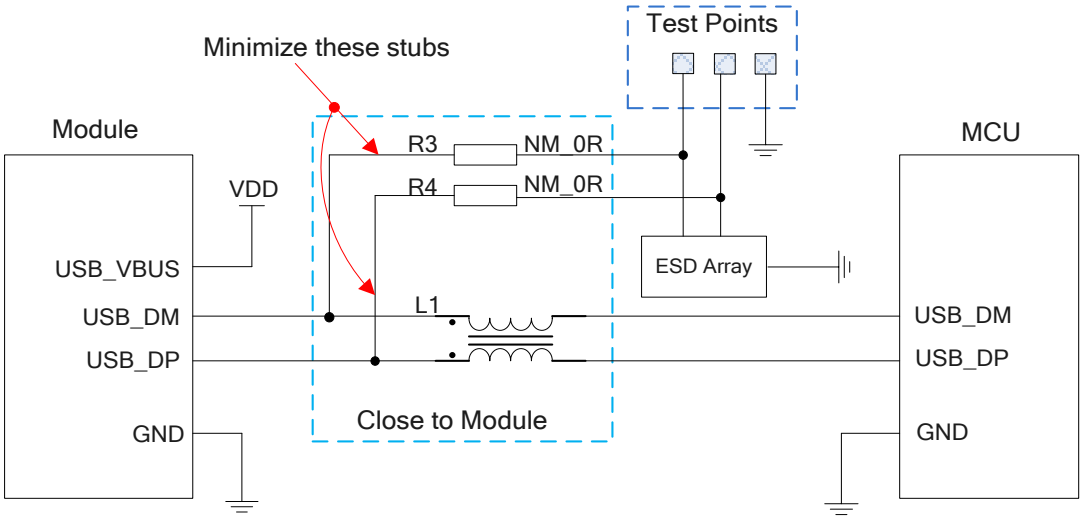


Figure 18: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and MCU to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R3 and R4) should be added in series between the module and the test points to facilitate debugging, and the resistors are not mounted by default. In order to ensure the integrity of USB data trace signal, L1 & R3 & R4 components must be placed close to the module, and these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

To meet USB 2.0 specification, the following principles should be complied with when design the USB interface.

- It is important to route the USB signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Junction capacitance of the ESD protection components might cause influences on USB data traces, so pay attention to the selection of the component. Typically, the stray capacitance should be less than 2 pF.
- Keep the ESD protection components to the USB connector as close as possible.

3.12. UART Interfaces

The module provides two UART interfaces: main UART and debug UART. The following shows their features.

- The main UART interface supports 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800 and

921600 bps baud rates, and the default is 115200 bps. It also supports RTS and CTS hardware flow control, and can be used for data transmission and AT command communication.

- The debug UART interface supports 115200 bps baud rate. It is used for Linux console and log output.

The following tables show the pin definition of the UART interfaces.

Table 12: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
RI	62	DO	Main UART ring indication	1.8 V power domain
DCD	63	DO	Main UART data carrier detected	
CTS	64	DO	DTE clear to send signal from DCE	1.8 V power domain Connect to DTE's RTS.
RTS	65	DI	DTE request to send signal to DCE	1.8 V power domain Connect to DTE's CTS.
DTR	66	DI	Main UART data terminal ready, sleep mode control	1.8 V power domain Pulled up by default. DTR can wake up the module when DTR remains at low level.
TXD	67	DO	Main UART transmit	1.8 V power domain
RXD	68	DI	Main UART receive	

Table 13: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	12	DO	Debug UART transmit	1.8 V power domain If unused, keep them open.
DBG_RXD	11	DI	Debug UART receive	

The module provides 1.8 V UART interface. A voltage-level translator should be used if your application is equipped with a 3.3 V UART interface. A voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

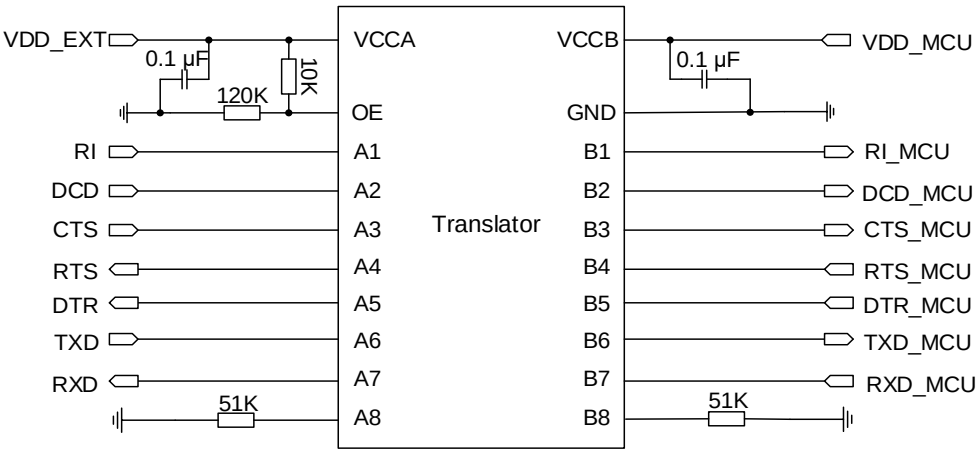


Figure 19: Reference Circuit with Translator Chip

Visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

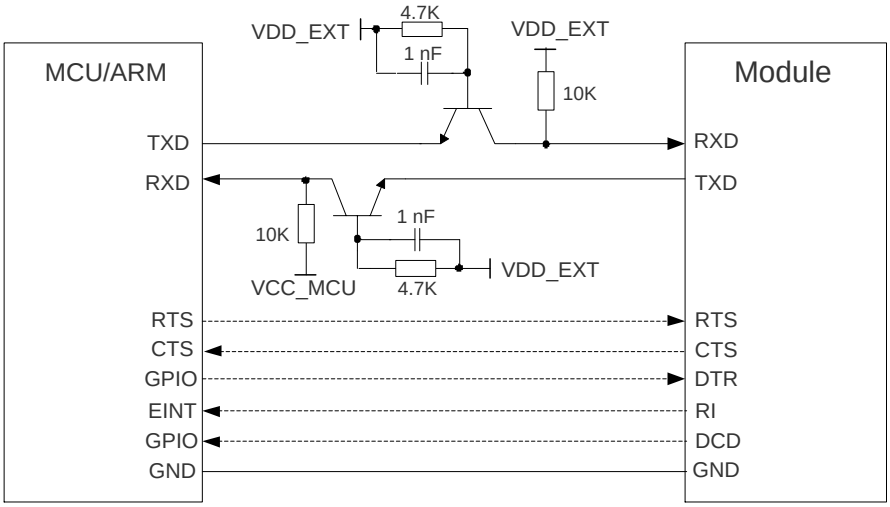


Figure 20: Reference Circuit with Transistor Circuit

NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to the host's CTS, and the module's RTS is connected to the host's RTS.

3.13. PCM and I2C Interfaces

EC25-T provides one I2C interface and one Pulse Code Modulation (PCM) digital interface for audio design, which supports the following modes:

- Short frame synchronization, works as both master and slave)
- Long frame synchronization, works as master only)

In short frame sync mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In long frame sync mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, the PCM interface operates with a 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK and an 8 kHz, 50% duty cycle PCM_SYNC.

EC25-T supports 16-bit linear data format. The following figures show the short frame sync mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the long frame sync mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

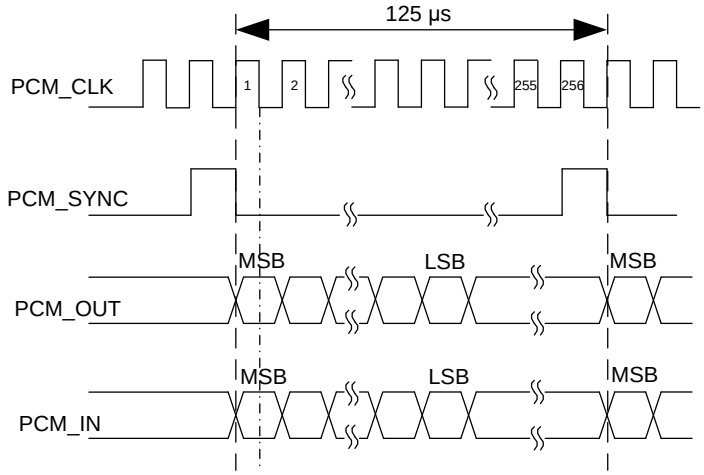


Figure 21: Short Frame Sync Mode Timing

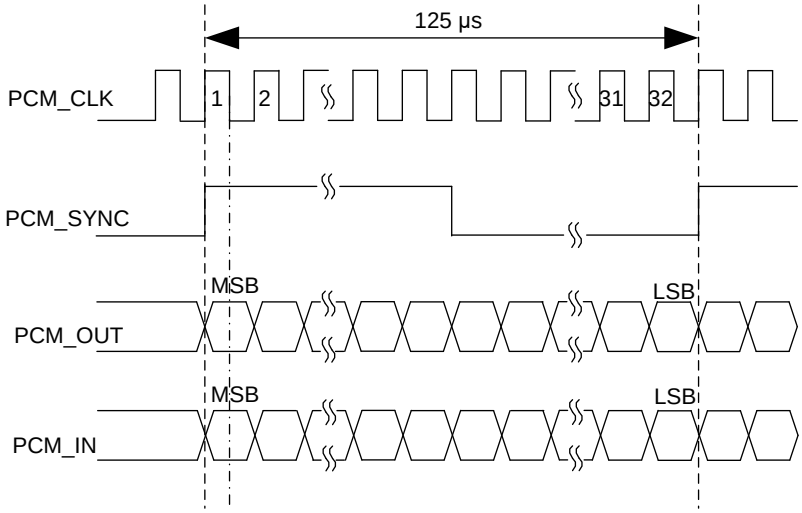


Figure 22: Long Frame Sync Mode Timing

Clock and mode can be configured by AT command, and the default configuration is master mode using short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. See ***document [2]*** for more details about **AT+QDAI**.

The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 14: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_IN	24	DI	PCM data input	1.8 V power domain If unused, keep them open.
PCM_OUT	25	DO	PCM data output	
PCM_SYNC	26	DIO	PCM frame sync	1.8 V power domain Serve as output signal in master mode or input signal in slave mode. If unused, keep them open.
PCM_CLK	27	DIO	PCM clock	
I2C_SCL	41	OD	I2C serial clock (for external codec)	Require external pull-up to 1.8 V. If unused, keep them open.
I2C_SDA	42	OD	I2C serial data (for external codec)	

The following figure shows a reference design of PCM and I2C interfaces with an external codec IC.

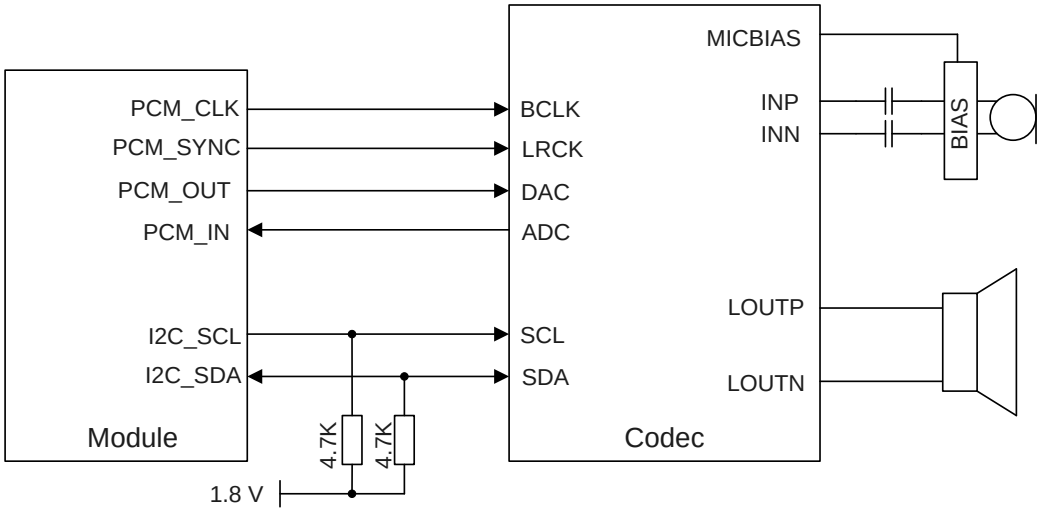


Figure 23: Reference Circuit of PCM and I2C Application with Audio Codec

NOTE

1. It is recommended to reserve an RC (R = 22 Ω, C = 22 pF) circuits on the PCM traces, and close to codec, especially for PCM_CLK.
2. EC25-T only works as a master device pertaining to I2C interface.

3.14. SD Card Interface

EC25-T supports SDIO 3.0 interface for SD card. The following table shows the pin definition of SD card interface.

Table 15: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SDC2_DATA3	28	DIO	SD card SDIO data bit 3	SDIO signal output voltage can be selected according to the signal output voltage supported by SD card; see SD 3.0 protocol for more details. If unused, keep them open.
SDC2_DATA2	29	DIO	SD card SDIO data bit 2	
SDC2_DATA1	30	DIO	SD card SDIO data bit 1	
SDC2_DATA0	31	DIO	SD card SDIO data bit 0	
SDC2_CLK	32	DO	SD card SDIO clock	

SDC2_CMD	33	DIO	SD card SDIO command	
VDD_SDIO	34	PO	SD card SDIO pull-up power	1.8/2.85 V configurable. Cannot be used for SD card power. If unused, keep it open.
SD_INS_DET	23	DI	SD card insertion detection	1.8 V power domain. If SD card function is unused, keep this pin open.

The following figure shows a reference design of SD card.

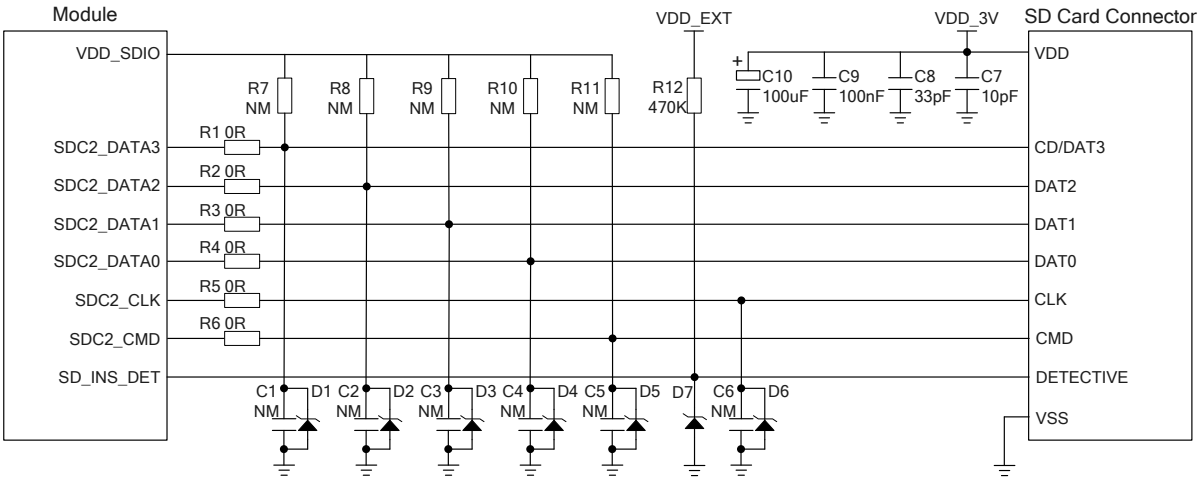


Figure 24: Reference Circuit of SD Card Interface

In SD card interface design, in order to ensure good communication performance with SD card, the following design principles should be complied with:

- SD_INS_DET must be connected when used for SD card.
- The voltage range of SD card power supply VDD_3V is 2.7–3.6 V and a sufficient current up to 0.8 A should be provided. As the maximum output current of VDD_SDIO is 50 mA which can only be used for SDIO pull-up resistors, an externally power supply is needed for SD card.
- To avoid jitter of bus, resistors R7–R11 are needed to pull up the SDIO to VDD_SDIO. Value of these resistors is among 10–100 kΩ and the recommended value is 100 kΩ. VDD_SDIO should be used as the pull-up power.
- In order to adjust signal quality, it is recommended to add 0 Ω resistors R1–R6 in series between the module and the SD card. The bypass capacitors C1–C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- For better ESD protection, it is recommended to add a TVS array on SD card pins near the SD card connector with junction capacitance less than 15 pF.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.

- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50 Ω (±10%).
- Make sure the adjacent trace spacing is two times of the trace width and the load capacitance of SDIO bus should be less than 15 pF.
- It is recommended to keep the trace length difference between SDC2_CLK and SDC2_DATA[0:3]/SDC2_CMD less than 1 mm and the total routing length less than 50 mm. The total trace length inside the module is 27 mm, so the exterior total trace length should be less than 23 mm.

3.15. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces.

AT+QADC=0 can be used to read the voltage value of ADC0 pin.
AT+QADC=1 can be used to read the voltage value of ADC1 pin.

For more details about these AT commands, see ***document [2]***.

To improve the accuracy of ADC, the trace should be surrounded by ground.

Table 16: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Description
ADC0	45	General-purpose ADC interface
ADC1	44	General-purpose ADC interface

The following table describes the characteristic of ADC function.

Table 17: Characteristic of ADC

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0.3	-	VBAT_BB	V
ADC1 Voltage Range	0.3	-	VBAT_BB	V
ADC Resolution	-	15	-	bits

NOTE

1. ADC input voltage must not exceed that of VBAT_BB.
2. It is prohibited to supply any voltage to ADC pins when the power supply for VBAT is removed.
3. It is recommended to use a resistor divider circuit for ADC application.

3.16. Indication Signals

3.16.1. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides pins NET_MODE and NET_STATUS. The following tables describe the pin definition and logic level changes in different network status.

Table 18: Pin Definition of Network Connection Status/Activity Indicator

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	5	DO	Indicate the module's network registration mode	1.8 V power domain Cannot be pulled up before startup. If unused, keep it open.
NET_STATUS	6	DO	Indicate the module's network activity status	1.8 V power domain If unused, keep it open.

Table 19: Working State of Network Connection Status/Activity Indicator

Pin Name	Logic Level Changes	Network Status
NET_MODE	Always High	Registered on LTE network
	Always Low	Others
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Data transfer is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

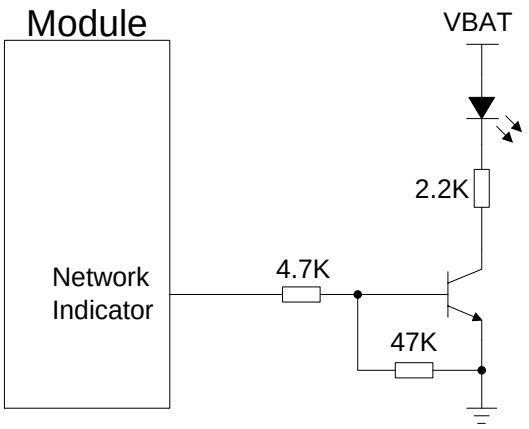


Figure 25: Reference Circuit of the Network Indicator

3.16.2. STATUS

The STATUS pin is an open drain output for indicating the module's operation status. It can be connected to a GPIO of DTE with a pull-up resistor, or as LED indication circuit as below. When the module is turned on normally, the STATUS will present the low state. Otherwise, the STATUS will present high-impedance state.

Table 20: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	61	OD	Indicate the module's operation status	An external pull-up resistor is required. If unused, keep it open.

The following figure shows different circuit designs of STATUS, and you can choose either one according to your application demands.

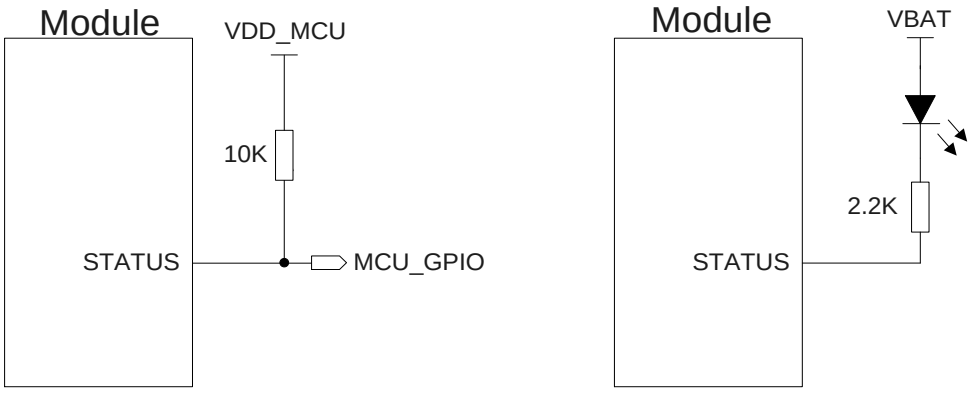


Figure 26: Reference Circuits of STATUS

NOTE

The STATUS pin cannot be used as the indication of the module shutdown status when the power supply for VBAT is removed.

3.16.3. RI

AT+QCFG="risignaltype","physical" can be used to configure RI behavior. No matter on which port a URC is presented, the URC will trigger the behaviors of RI pin.

In addition, RI behavior can be configured flexibly. The default behaviors of the RI are shown as below.

Table 21: Behaviors of RI

State	Response
Idle	RI keeps at high level
URC	RI outputs 120 ms low pulse when a new URC returns

The RI behavior can be changed by **AT+QCFG="urc/ri/ring"**. See ***document [3]*** for details.

NOTE

A URC can be outputted from UART port, USB AT port and USB modem port through configuration via **AT+QURCCFG**. The default port is USB AT port. See ***document [2]*** for details.

3.17. USB_BOOT Interface

EC25-T provides a USB_BOOT pin. You can pull up USB_BOOT to 1.8 V before VDD_EXT is powered up, and the module will enter emergency download mode when it is powered on. In this mode, the module supports firmware upgrade over USB interface.

Table 22: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	115	DI	Force the module to enter emergency download mode	1.8 V power domain. Active high. It is recommended to reserve test points.

The following figure shows a reference circuit of USB_BOOT interface.

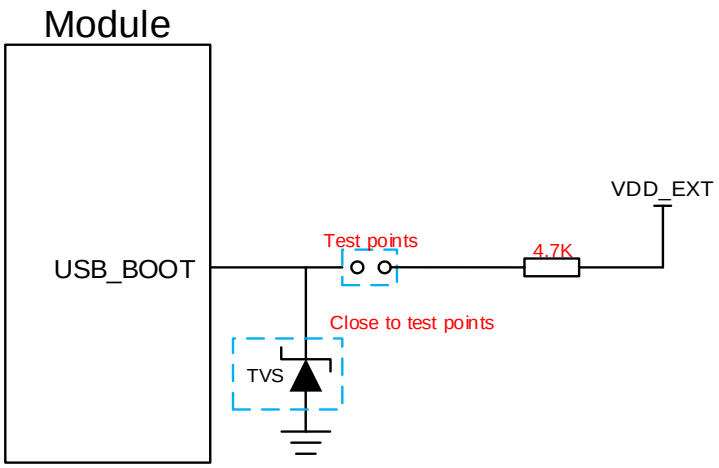


Figure 27: Reference Circuit of USB_BOOT Interface

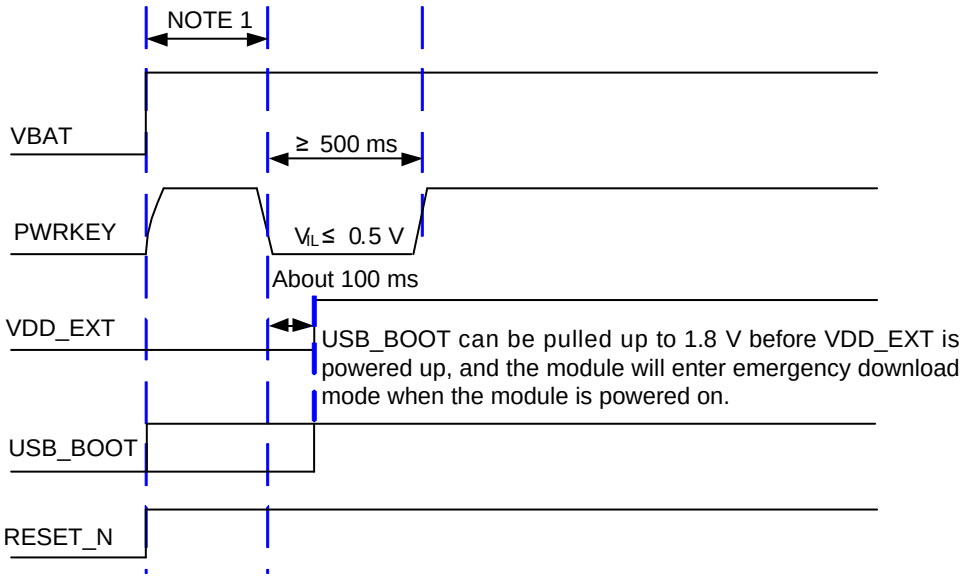


Figure 28: Timing Sequence for Entering Emergency Download Mode

NOTE

1. Make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.
2. The output voltage of PWRKEY is 0.8 V because of the diode drop in the baseband chipset.
3. When using MCU to control module to enter the emergency download mode, please follow the above timing sequence. It is not recommended to pull up USB_BOOT to 1.8 V before powering up VBAT. Connect the test points as shown in ***Figure 27*** can manually force the module to enter download mode.

4 RF Specifications

EC25-T antenna interfaces include a main antenna interface, an Rx-diversity antenna interface which is used to resist the fall of signals caused by high-speed movement and multipath effect, and a GNSS antenna interface. The impedance of antenna ports is 50 Ω.

4.1. Celluar Network

4.1.1. Antenna Interfaces & Frequency Bands

The pin definition of main antenna and Rx-diversity antenna interfaces is shown below.

Table 23: Pin Definition of RF Antennas

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	49	AIO	Main antenna interface	50 Ω impedance
ANT_DIV	35	AI	Diversity antenna interface	50 Ω impedance. If unused, keep it open.

4.1.2. Operating Frequency

Table 24: Module Operating Frequencies

3GPP Bands	Transmit	Receive	Unit
LTE-FDD B2	1850–1910	1930–1990	MHz
LTE-FDD B4	1710–1755	2110–2155	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B12	699–716	729–746	MHz
LTE-FDD B66	1710–1780	2110–2180	MHz

LTE-FDD B71	663–698	617–652	MHz

4.1.3. Tx Power

The following table shows the Tx power of EC25-T.

Table 25: Tx Power

Frequency Bands	Max. Tx Output Power	Min. Tx Output Power
LTE-FDD bands	23 dBm ±2 dB	< -39 dBm

NOTE

In GPRS 4 slots TX mode, the maximum output power is reduced by 3.0 dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

4.1.4. Rx Sensitivity

The following tables show the conducted Rx sensitivity of EC25-T.

4.1.4.1. EC25-T Conducted Rx Sensitivity

Table 26: EC25-T Conducted Rx Sensitivity

Frequency Bands	Primary	Diversity	SIMO [6]	3GPP (SIMO)
LTE-FDD B2 (10 MHz)	-98.0 dBm	-99.0dBm	-100.5 dBm	-94.3 dBm
LTE-FDD B4 (10 MHz)	-98.0 dBm	-98.0 dBm	-100.5 dBm	-96.3 dBm
LTE-FDD B5 (10 MHz)	-99.0 dBm	-99.5 dBm	-101.5 dBm	-94.3 dBm
LTE-FDD B12 (10 MHz)	-98.0 dBm	-98.0 dBm	-100.5 dBm	-93.3 dBm
LTE-FDD B66 (10 MHz)	-98.0 dBm	-98.0 dBm	-100 dBm	-95.8 dBm
LTE-FDD B71 (10 MHz)	-99.0 dBm	-99.5 dBm	-101 dBm	-93.5 dBm

[6] SIMO is a smart antenna technology that uses a single antenna at the transmitter side and two antennas at the receiver side, which can improve Rx performance.

4.1.5. Reference Design

A reference design of ANT_MAIN and ANT_DIV antenna pins is shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

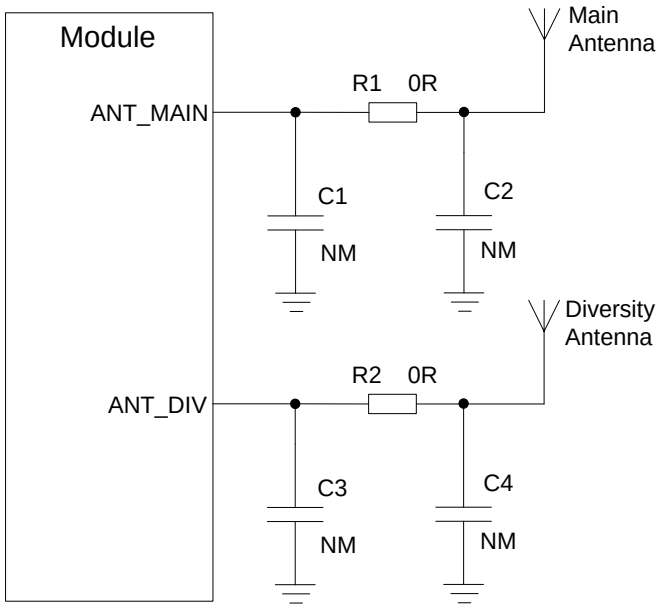


Figure 29: Reference Circuit of RF Antenna Interface

NOTE

1. Keep a proper distance between the main antenna and the Rx-diversity antenna to improve the receiving sensitivity.
2. ANT_DIV function is enabled by default. **AT+QCFG="divctl",0** can be used to disable receive diversity. See ***document [3]*** for details.
3. Place the π-type matching components (R1 & C1 & C2, R2 & C3 & C4) as close to the antenna as possible.

4.2. GNSS

EC25-T includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BDS, Galileo, and QZSS.

EC25-T supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via USB interface by default.

By default, EC25-T GNSS engine is switched off. It has to be switched on via AT command. For more

details about GNSS engine technology and configurations, see ***document [5]***.

4.2.1. Antenna Interfaces & Frequency Bands

The following tables show the pin definition and frequency specification of GNSS antenna interface.

Table 27: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	47	AI	GNSS antenna	50 Ω impedance. If unused, keep it open.

Table 28: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz
BDS	1561.098 ±2.046	MHz
QZSS	1575.42	MHz

4.2.2. GNSS Performance

The following table shows the GNSS performance of the module.

Table 29: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Acquisition	Autonomous	-146	dBm
	Reacquisition	Autonomous	-157	dBm
	Tracking	Autonomous	-157	dBm
TTFF(GNSS)	Cold start @ open sky	Autonomous	35	s

		XTRA enabled	18	s
	Warm start @ open sky	Autonomous	26	s
		XTRA enabled	2.2	s
	Hot start @ open sky	Autonomous	2.5	s
		XTRA enabled	1.8	s
Accuracy (GNSS)	CEP-50	Autonomous @ open sky	2.5	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

4.2.3. Reference Design

A reference design of GNSS antenna is shown as below.

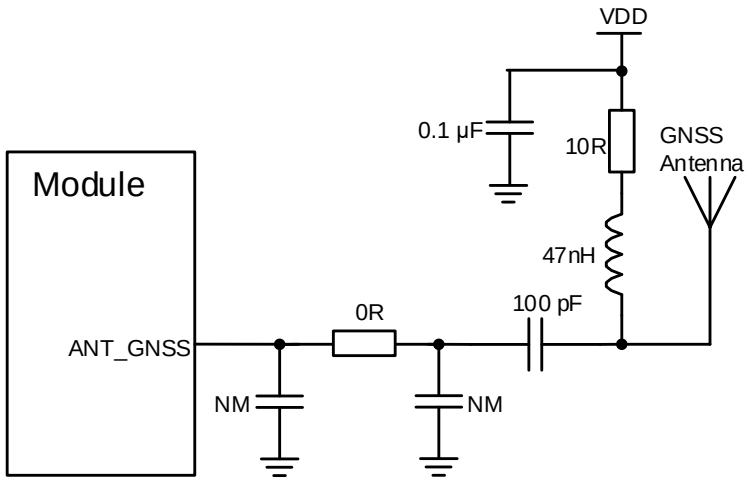


Figure 30: Reference Circuit of GNSS Antenna

NOTE

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then power supply (VDD) circuit is not needed.

4.2.4. Layout Guidelines

The following layout guidelines should be taken into account in your designs.

- Maximize the distance among GNSS antenna, main antenna, and Rx-diversity antenna.
- Digital circuits such as USIM card, USB interface, camera module and display connector should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep 50 Ω characteristic impedance for the ANT_GNSS trace.

4.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

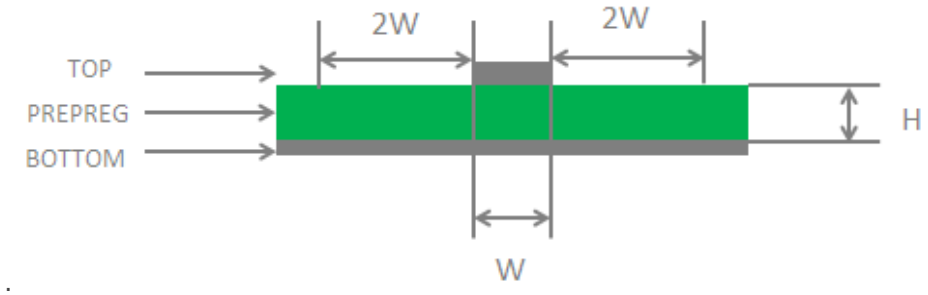


Figure 31: Microstrip Design on a 2-layer PCB

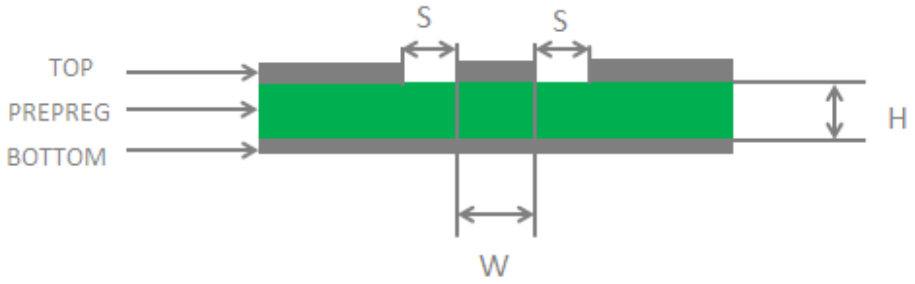


Figure 32: Coplanar Waveguide Design on a 2-layer PCB

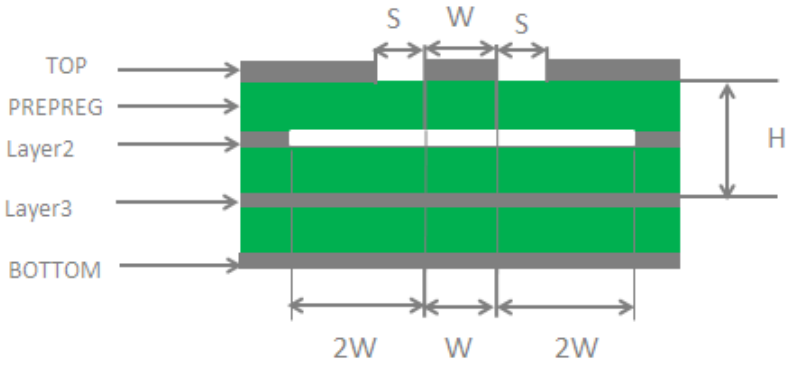


Figure 33: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

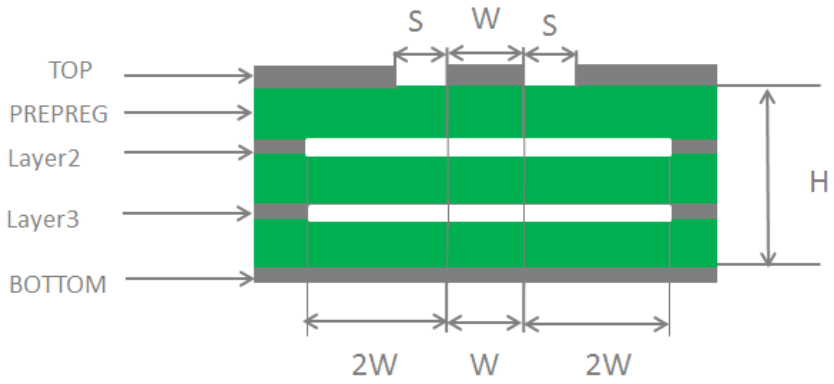


Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the

right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [6]***.

4.4. Antenna Design Requirements

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

Table 30: Antenna Design Requirements

Type	Requirements
GNSS	Frequency range: 1559–1609 MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive antenna gain: > 0 dBi Active antenna noise figure: < 1.5 dB Active antenna gain: > 0 dBi Active antenna embedded LNA gain: < 17 dB
LTE	VSWR: ≤ 2 Efficiency: > 30 % Max input power: 50 W Input impedance: 50 Ω Cable insertion loss: **< 1 dB:** LB (<1 GHz) **< 1.5 dB:** MB (1–2.3 GHz)

4.5. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

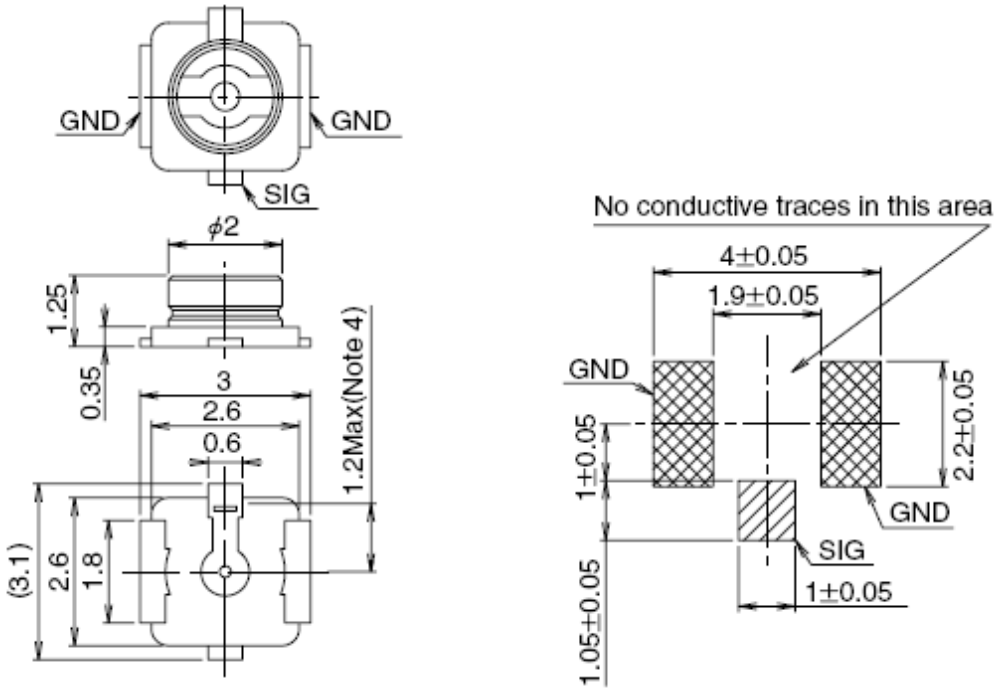


Figure 35: Dimensions of the Receptacle (Unit: mm)

U.FL-LP mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

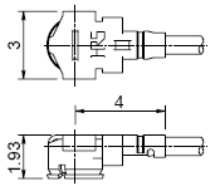
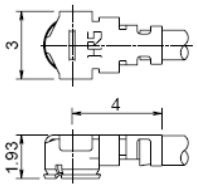
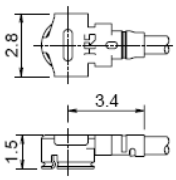
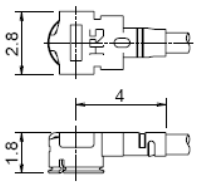
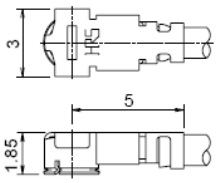
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 36: Specifications of Mated Plugs

The following figure describes the space factor of mated connectors.

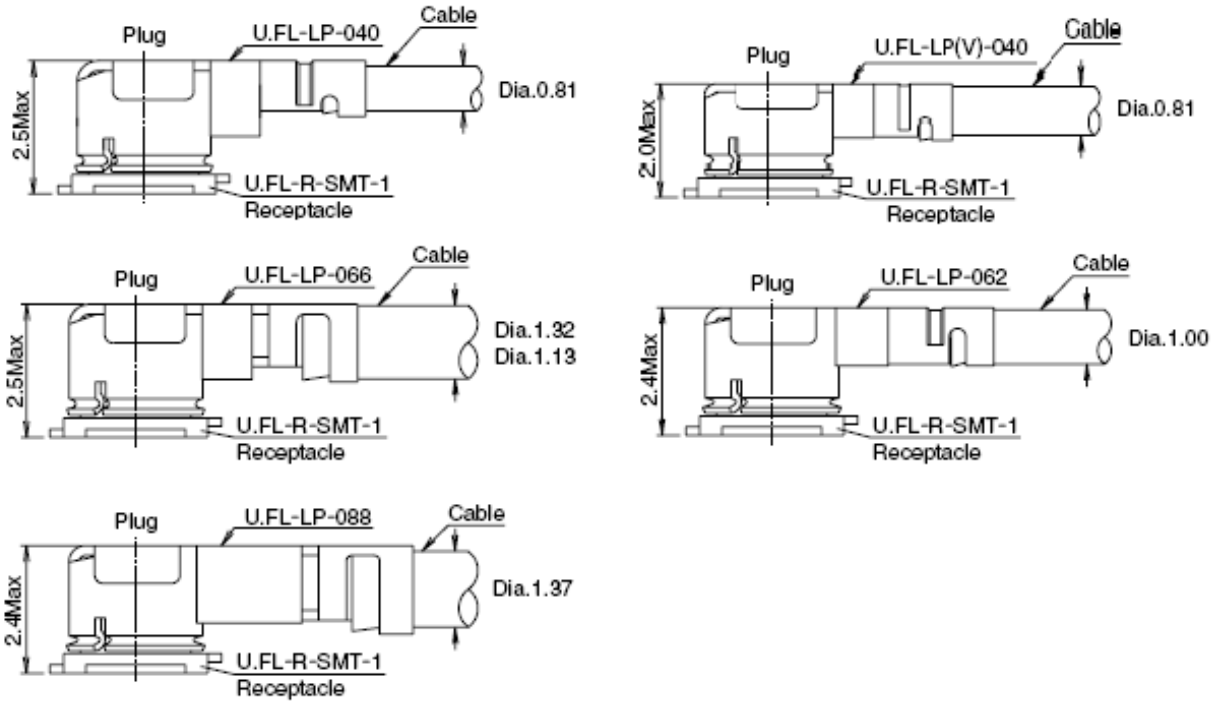


Figure 37: Space Factor of Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

5 Electrical Characteristics and Reliability

5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 31: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	0.8	A
Peak Current of VBAT_RF	-	1.8	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT_BB	V
Voltage at ADC1	0	VBAT_BB	V

5.2. Power Supply Ratings

Table 32: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.3	V
	Voltage drop during burst transmission	Maximum power control level on EGSM900	-	-	400	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level on EGSM900	-	1.8	2.0	A
USB_VBUS	USB connection detection	-	3.0	5.0	5.25	V

5.3. Operating and Storage Temperatures

The operating and storage temperatures are listed in the following table.

Table 33: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [7]	-35	+25	+75	ºC
Extended Temperature Range [8]	-40	-	+85	ºC
Storage Temperature Range	-40	-	+90	ºC

[7] Within the operating temperature range, the module meets 3GPP specifications.
[8] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

5.4. Power Consumption

The values of power consumption are shown below.

Table 34: EC25-T Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	7	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	0.79	mA
	AT+CFUN=0 (USB suspend)	1.00	mA
	AT+CFUN=4 (USB disconnected)	0.88	mA
	AT+CFUN=4 (USB suspend)	1.09	mA
	LTE-FDD PF = 32 (USB disconnected)	3.05	mA
	LTE-FDD PF = 64 (USB disconnected)	2.11	mA
	LTE-FDD PF = 64 (USB suspend)	2.17	mA
	LTE-FDD PF = 128 (USB disconnected)	1.68	mA
	LTE-FDD PF = 256 (USB disconnected)	1.13	mA
Idle state	LTE-FDD PF = 64 (USB disconnected)	18.71	mA
	LTE-FDD PF = 64 (USB active)	27.74	mA
LTE data transfer (GNSS OFF)	LTE-FDD B2 @ 23.1 dBm	650	mA
	LTE-FDD B4 @ 23.5 dBm	750	mA
	LTE-FDD B5 @ 23.2 dBm	600	mA
	LTE-FDD B12 @ 23.2 dBm	670	mA
	LTE-FDD B66 @ 22.3 dBm	730	mA
	LTE-TDD B71 @ 23.05 dBm	650	mA

Table 35: GNSS Power Consumption

Description	Conditions	Typ.	Unit
Searching (**AT+CFUN=0**)	Cold start @ Passive Antenna	54.0	mA
	Lost state @ Passive Antenna	53.9	mA
Tracking (**AT+CFUN=0**)	Instrument Environment	30.5	mA
	Open Sky @ Passive Antenna	33.2	mA
	Open Sky @ Active Antenna	40.8	mA

5.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

The following table shows the module's electrostatics discharge characteristics.

Table 36: Electrostatics Discharge Characteristics (Temperature: 25 ºC, Humidity: 45 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

5.6. Thermal Dissipation

In order to achieve better performance of the module, it is recommended to comply with the following principles for thermal consideration:

- On customers' PCB design, please keep placement of the module away from heating sources, especially high power components such as ARM processor, audio power amplifier, power supply, etc.

- Do not place components on the opposite side of the PCB area where the module is mounted, in order to facilitate adding of heatsink when necessary.
- Do not apply solder mask on the opposite side of the PCB area where the module is mounted, so as to ensure better heat dissipation performance.
- The reference ground of the area where the module is mounted should be complete, and add ground vias as many as possible for better heat dissipation.
- Make sure the ground pads of the module and PCB are fully connected.
- According to customers' application demands, the heatsink can be mounted on the top of the module, or the opposite side of the PCB area where the module is mounted, or both of them.
- The heatsink should be designed with as many fins as possible to increase heat dissipation area. Meanwhile, a thermal pad with high thermal conductivity should be used between the heatsink and module/PCB.

The following shows two kinds of heatsink designs for reference and customers can choose one or both of them according to their application structure.

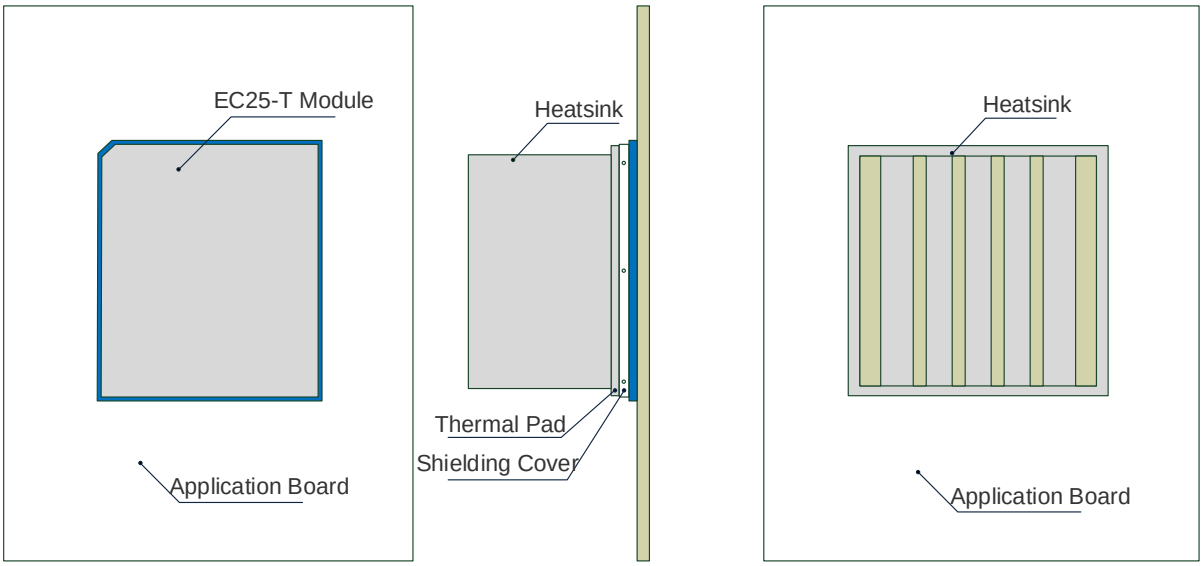


Figure 38: Referenced Heatsink Design (Heatsink at the Top of the Module)

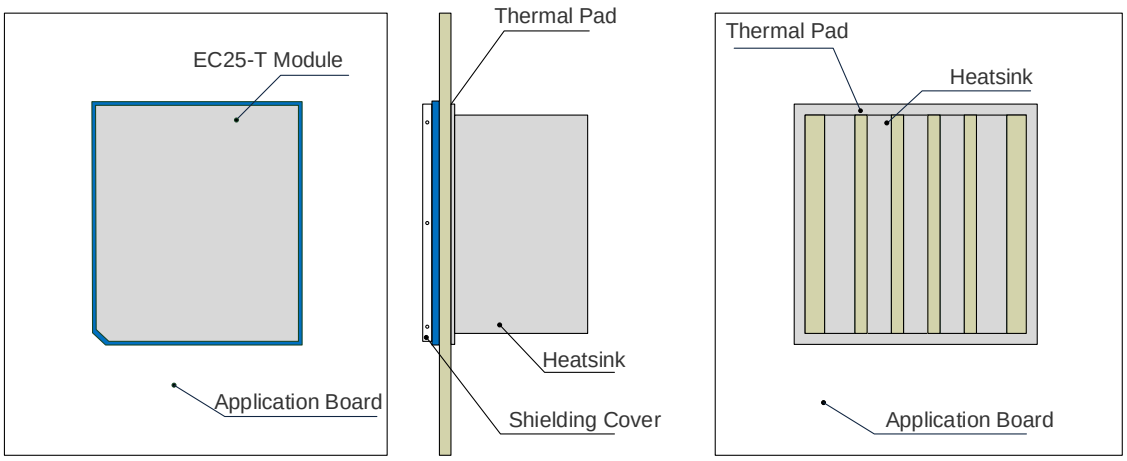


Figure 39: Referenced Heatsink Design (Heatsink at the Backside of Customers' PCB)

NOTE

1. The module offers the best performance when the internal BB chip stays below 105 °C. When the maximum temperature of the BB chip reaches or exceeds 105 °C, the module works normal but provides reduced performance (such as RF output power, data rate, etc.). When the maximum BB chip temperature reaches or exceeds 115 °C, the module will disconnect from the network, and it will recover to network connected state after the maximum temperature falls below 115 °C. Therefore, the thermal design should be maximally optimized to make sure the maximum BB chip temperature always maintains below 105 °C. You can execute **AT+QTEMP** and get the maximum BB chip temperature from the first returned value. For details of the command, see ***document [7]***.
2. For more detailed guidelines on thermal design, see ***document [8]***.

6 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

6.1. Mechanical Dimensions

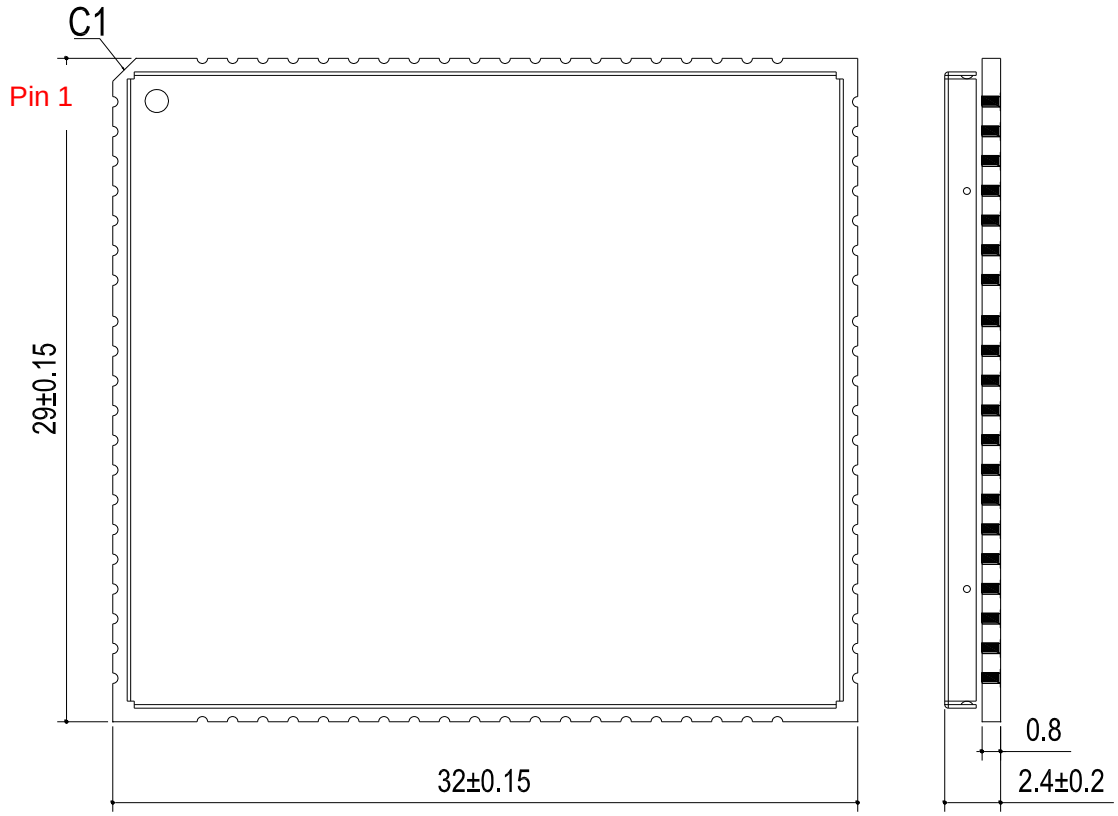


Figure 40: Module Top and Side Dimensions

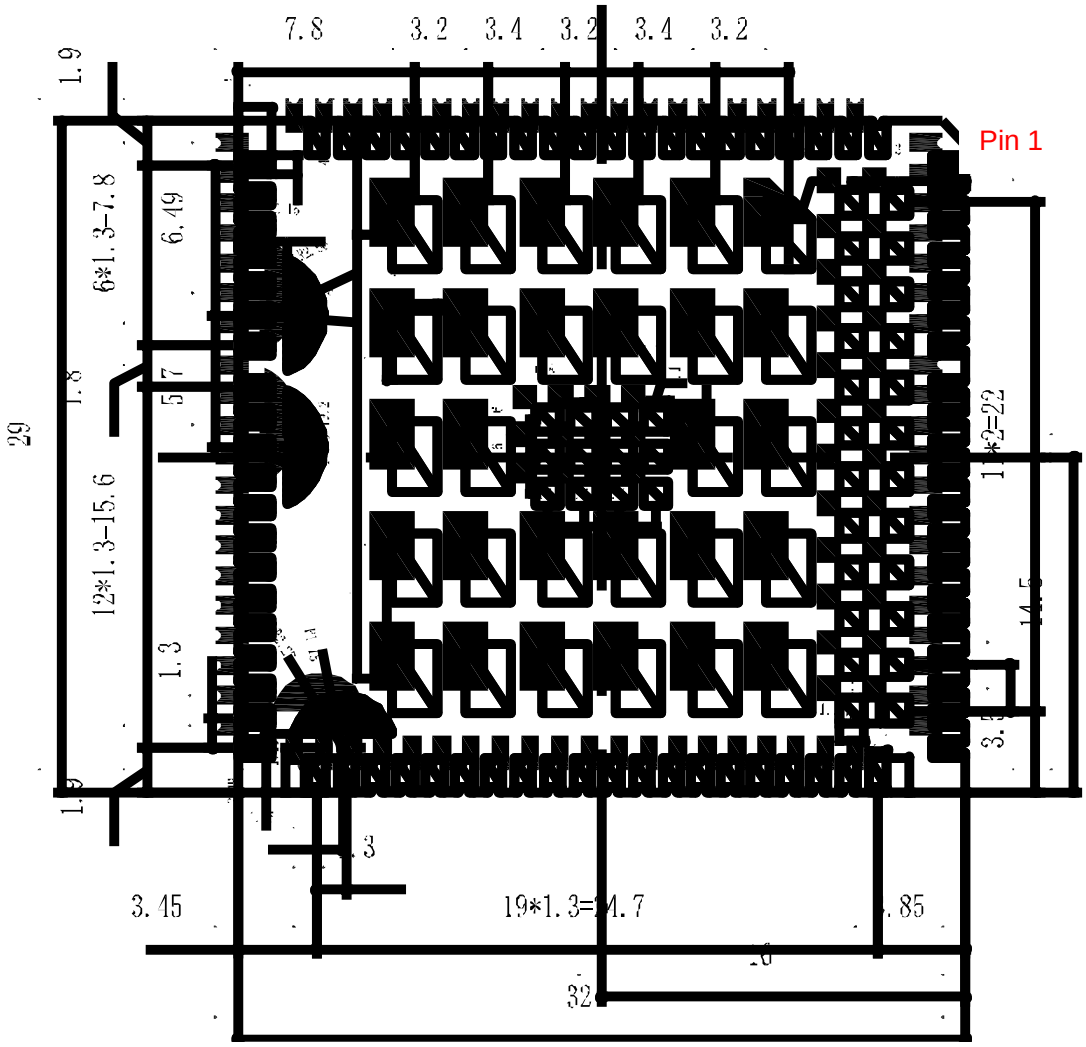


Figure 41: Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to *JEITA ED-7306* standard.

6.2. Recommended Footprint

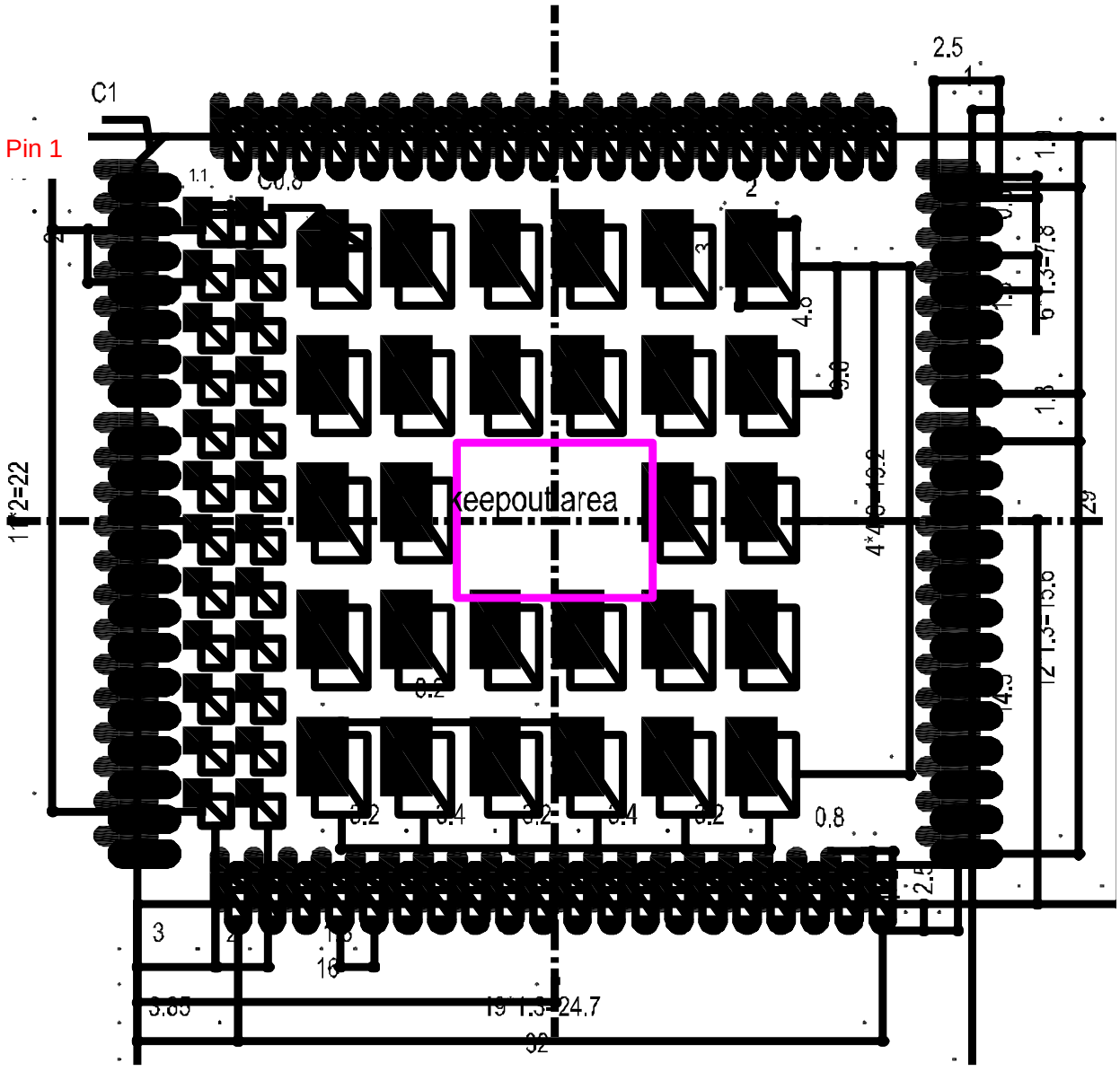


Figure 42: Recommended Footprint (Top View)

NOTE

1. The keepout area (pin 73–84) should not be designed.
2. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

6.3. Top and Bottom Views

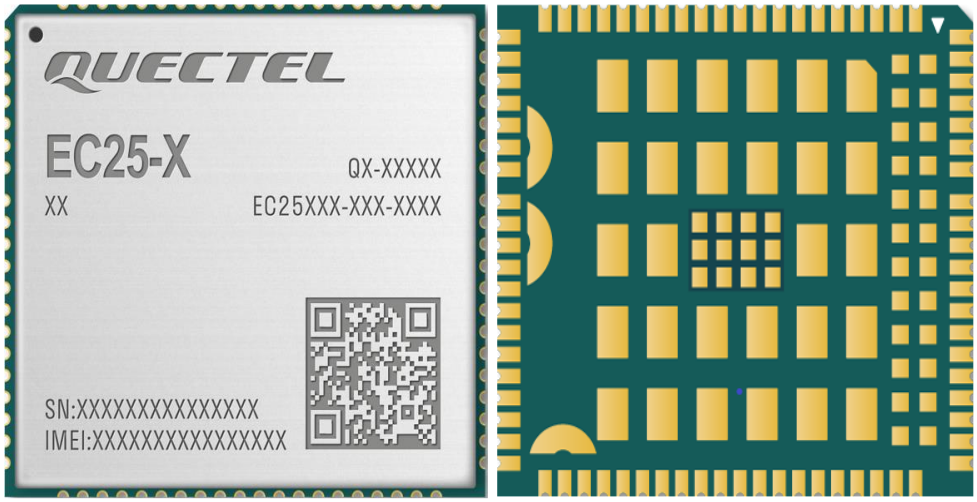


Figure 43: Top and Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

7 Storage, Manufacturing and Packaging

7.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [9] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[9] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. All modules must be soldered to PCB within 24 hours after the baking, otherwise put them in the drying oven. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.18–0.20 mm. For more details, see ***document [9]***.

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

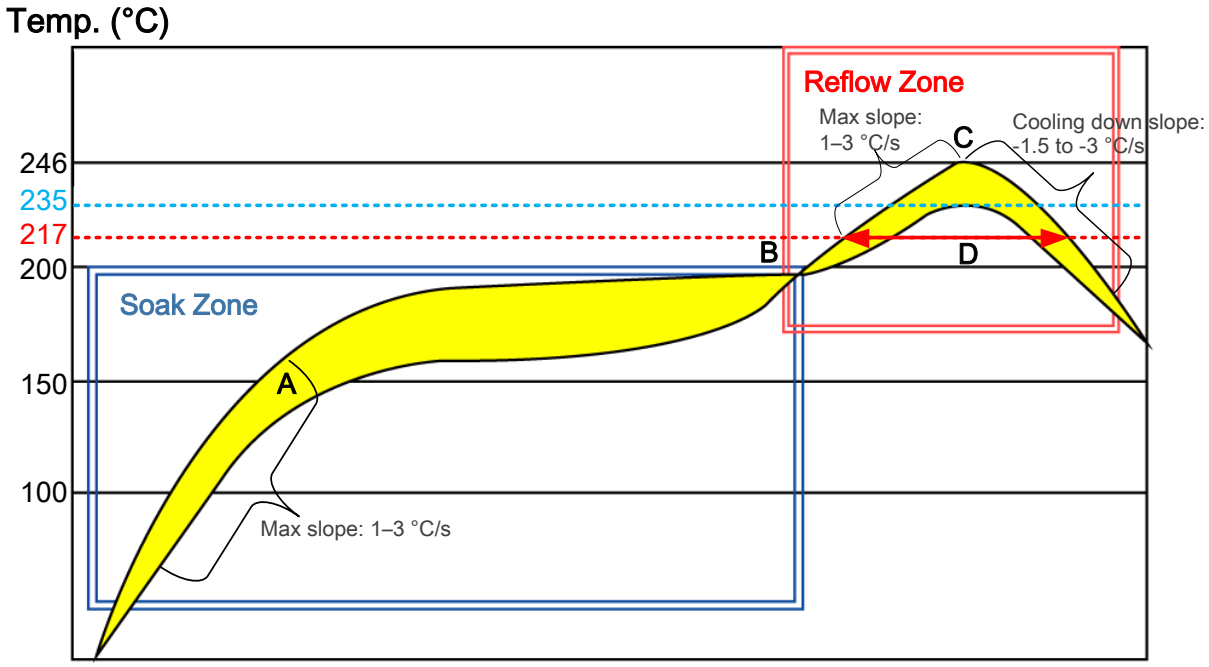


Figure 44: Reflow Soldering Thermal Profile

Table 37: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	1–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235 °C to 246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max re-flow cycle	1

NOTE

1. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
2. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
3. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic soldering) that is not mentioned in ***document [9]***.

7.3. Packaging Specification

The module adopts carrier tape packaging and details are as follow:

7.3.1. Carrier Tape

Dimension details are as follow:

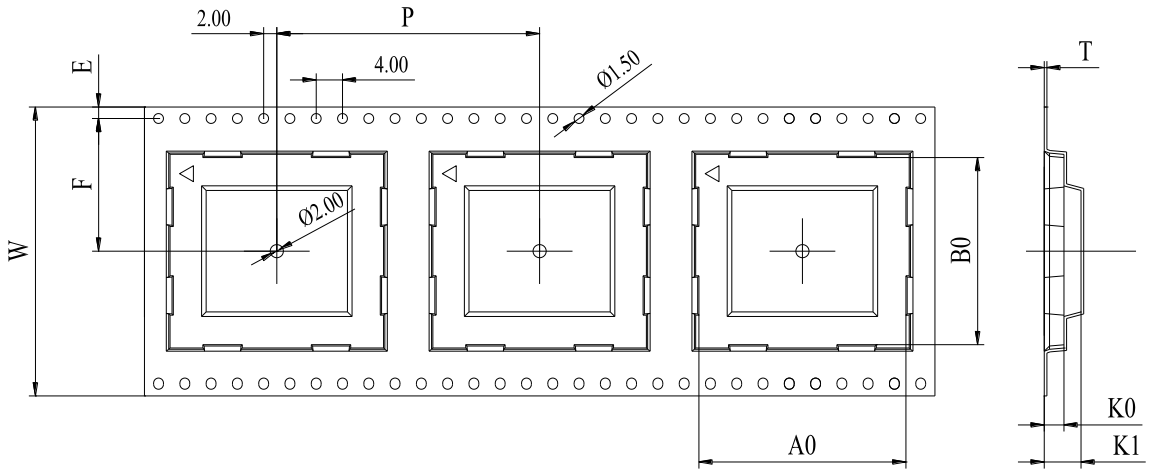


Figure 45: Carrier Tape Dimension Drawing

Table 38: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	44	0.35	32.5	29.5	3.0	3.8	20.2	1.75

7.3.2. Plastic Reel

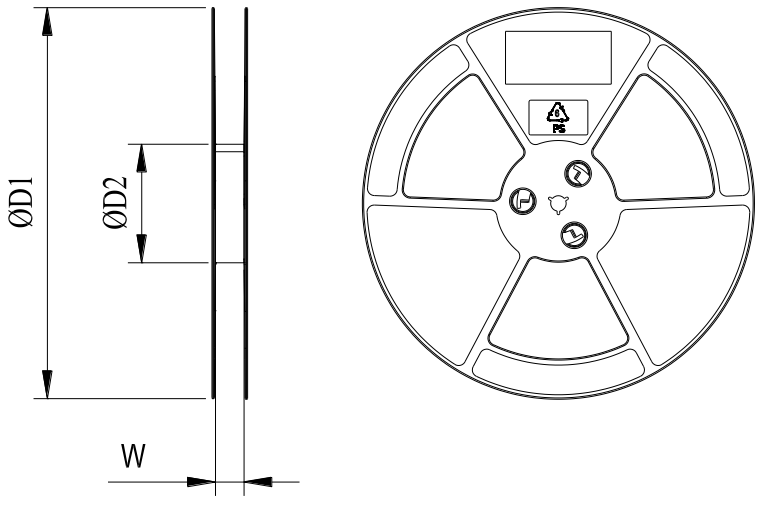
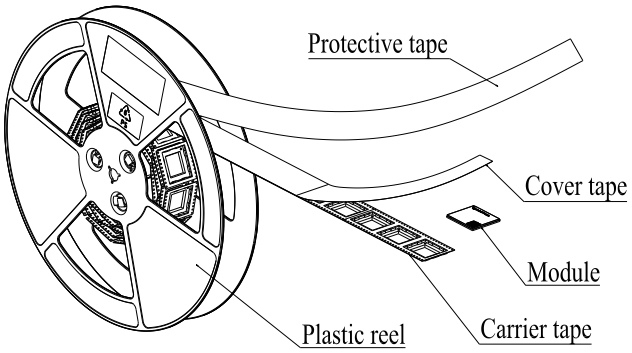


Figure 46: Plastic Reel Dimension Drawing

Table 39: Plastic Reel Dimension Table (Unit: mm)

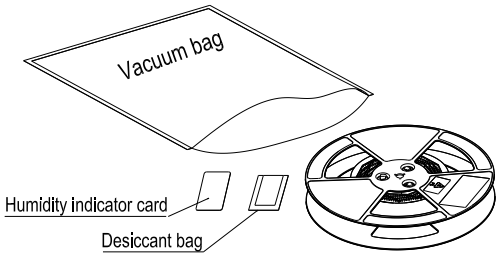
øD1	øD2	W
330	100	44.5

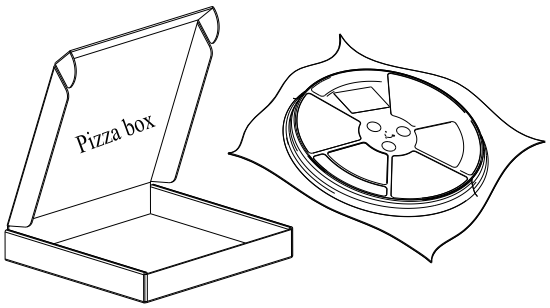
7.3.3. Packaging Process



Place the module into the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. One plastic reel can load 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, then vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Put 4 pizza boxes into 1 carton and seal it. One carton can pack 1000 modules.

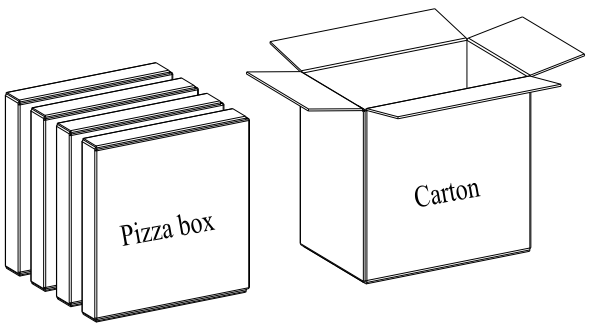


Figure 47: Packaging Process

8 Appendix References

Table 40: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_EC2x&EG9x&EG2x-G&EM05_Series_AT_Commands_Manual
[3] Quectel_EC2x&EG9x&EG2x-G&EM05_Series_QCFG_AT_Commands_Manual
[4] Quectel_EC2x&EGxx_Power_Management_Application_Note
[5] Quectel_EC2x&EG9x&EG2x-G&EM05_Series_GNSS_Application_Note
[6] Quectel_RF_Layout_Application_Note
[7] Quectel_EC2x&EG9x&EG2x-G&EM05_Series_Thermal_Mitigation_User_Guide
[8] Quectel_Module_Thermal_Design_Guide
[9] Quectel_Module_Secondary_SMT_Application_Guide

Table 41: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-rate
APT	Average Power Tracking
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol

CMUX	Connection Multiplexing
CS	Coding Scheme
CTS	Clear to Send
DCE	Data Communications Equipment
DC-HSPA+	Dual-carrier High Speed Packet Access
DCS	Digital Communication System
DFOTA	Delta Firmware Upgrade Over-The-Air
DL	Downlink
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EDGE	Enhanced Data Rates for GSM Evolution
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
FDD	Frequency Division Duplex
FR	Full Rate
FTPS	FTP over SSL
GLONASS	Russian Global Navigation Satellite System
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communications

HR	Half Rate
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
I/O	Input/Output
LCC	Leadless Chip Carrier (package)
LDO	Low-dropout Regulator
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LTE	Long Term Evolution
M2M	Machine to Machine
MCS	Modulation and Coding Scheme
MDIO	Management Data Input/Output
MIMO	Multiple Input Multiple Output
MLCC	Multi-layer Ceramic Chip
MMS	Multimedia Messaging Service
MO	Mobile Originated
MQTT	Message Queuing Telemetry Transport
MSB	Most Significant Bit
MT	Mobile Terminated
NITZ	Network Identity and Time Zone / Network Informed Time Zone
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
NTP	Network Time Protocol

PA	Power Amplifier
PAM	Power Amplifier Module
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PCS	Personal Communication System
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PING	Packet Internet Groper
PMIC	Power Management IC
POS	Point of Sale
PPP	Point-to-Point Protocol
PTP	Precision Time Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
RoHS	Restriction of Hazardous Substances
Rx	Receive
SAW	Surface Acoustic Wave
SDR	Software-Defined Radio
SGMII	Serial Gigabit Media Independent Interface
SIM	Subscriber Identification Module
SIMO	Single Input Multiple Output

SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
TDMA	Time Division Multiple Access
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
TX	Transmitting Direction
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage

VLAN	Virtual Local Area Network
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

FCC Statement

Warning: Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.
However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

The device must not be co-located or operating in conjunction with any other antenna or transmitter. This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions : (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Radiation Exposure Statement
This equipment should be installed and operated with minimum distance 20cm between the radiator and your body.

Does not comply with the use restrictions of the product:
Portable devices used close with human's body (within 20cm), Like Cell phone, Notebook etc.

Integration instructions for host product manufacturers according to KDB 996369 D04 OEM Manual

2.2 List of applicable FCC rules
FCC Part 15 & 22& 24& 27.
2.3 Specific operational use conditions
The module can be used for mobile applications with a maximum 3.95 dBi antenna. The host manufacturer installing this module into their product must ensure that the final compos it product complies with the FCC requirements by a technical assessment or evaluation to the FCC rules, including the transmitter operation. The host manufacturer has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module The end user manual shall include all required regulatory information/warning as show in this manual.

2.4 Limited module procedures

Not applicable The module is a Single module and complies with the requirement of FCC Part 15.212.

2.5 Trace antenna designs

Not applicable The module has its own antenna, and doesn’t need a hosts printed board micro strip trace antenna etc.

2.6 RF exposure considerations

The module must be installed in the host equipment such that at least 20cm is maintained between the antenna and users" body; and if RF exposure statement or module layout is changed, then the host product manufacturer required to take responsibility of the module through a change in FCC ID or new application The FCC ID of the module cannot be used on the final product In these circumstances, the host manufacturer will be responsible for reevaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

2.7 Antennas

Antenna Specification are as follows:
Type: Dipole Antenna
Gain: 3.95 dBi Max
This device is intended only for host manufacturers under the following conditions: The transmitter module may not be co-located with any other transmitter or antenna; The module shall be only used with the internal antenna(s) that has been originally tested and certified with this module. The antenna must be either permanently attached or employ a “unique" antenna coupler.
As long as the conditions above are met, further transmitter test will not be required However, the host manufacturer is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc).

2.8 Label and compliance information

Host product manufacturers need to provide a physical or e-label stating "Contains FCC ID: XMR202012EC25T" with their finished product.

2.9 Information on test modes and additional testing requirements

Host manufacturer must perform test of radiated & conducted emission and spurious emission, e.t.c according to the actual test modes for a stand-alone modular transmitter in a host, as well as for multiple simultaneously transmitting modules or other transmitters in a host product. Only when all the test results of test modes comply with FCC requirements, then the end product can be sold legally.

2.10 Additional testing, Part 15 Subpart B disclaimer

If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

Federal Communication Commission Statement (FCC, U S)

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant

to Part 15 of the FCC Rules These limits are designed to provide reasonable protection against harmful interference in a residential installation This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications However, there is no guarantee that
interference will not occur in a particular installation If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

This device complies with Part 15 of the FCC Rules Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Caution:

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

IMPORTANT NOTES

Co-location warning:

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

OEM integration instructions:

This device is intended only for OEM integrators under the following conditions:

The transmitter module may not be co-located with any other transmitter or antenna The module shall be only used with the external antenna(s) that has been originally tested and certified with this module.

As long as the conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

Validity of using the module certification:

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization for this module in combination with the host equipment is no longer considered valid and the FCC ID of the module cannot be used on the final product In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End product labeling:

The final end product must be labeled in a visible area with the following: "Contains Transmitter Module FCC ID: XMR202012EC25T"

Information that must be placed in the end user manual:

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.