EG12 Hardware Design

LTE-A Module Series

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1 Introduction

This document defines the EG12 module and describes its air interface and hardware interfaces which are connected with customers' applications.

This document can help customers quickly understand module interface specifications, electrical and mechanical details, as well as other related information of EG12 module. Associated with application note and user guide, customers can use EG12 module to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of the operation, such as usage, service or repair of any cellular terminal or mobile incorporating EG12 module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid (U)SIM card). When emergent help is needed in such conditions, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

EG12 is a series LTE-FDD/LTE-TDD/WCDMA wireless communication module with receive diversity. It provides data connectivity on LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, and WCDMA networks.

EG12 supports embedded operating systems such as Windows, Linux and Android. It also provides GNSS [1)] and voice functionality [2)] to meet customers' specific application demands.

EG12 contains three variants: EG12-GT, EG12-EA, and EG12-NA*. Customers can choose a dedicated variant based on the region or operator.

The following table shows the frequency bands and GNSS types of EG12 series module.

Table 1: Frequency Bands of EG12 Series Module

Mode	EG12-GT	EG12-EA	EG12-NA*
LTE-FDD (with Rx-diversity)	Not supported	B1/B3/B5/B7/ B8/B20/B28	B2/B4/B5/B7/B12/B13/ B14/B17/B25/B26/B29/ B30/B66/B71
LTE-TDD (with Rx-diversity)	B42/B43/B48	B38/B40/B41	B41
2×CA (DL)	B42+B42; B48+B48	B1+B1/B3/B5/B7/B8/ B20/B28/B38/B40/B41; B3+B3/B5/B7/B8/B20/ B28/B38/B40/B41; B7+B5/B7/B8/B20/B28; B20+B38/B40; B38+B38; B40+B40; B41+B41	B2+B2/B4/B5/B7/B12/B13/B14/ B17/B29/B30/B66/B71; B25+B5/B12/B25/B26/B41; B4+B4/B5/B7/B12/B13/B17/B29/ B30/B71; B66+B5/B7/B12/B13/B14/B29/ B30/B66/B71; B7+B5/B7/B12; B30+B5/B12/B14/B29; B26+B41
2×CA (UL)	B42+B42	B3+B3; B7+B7;	B7+B7; B41+B41

		B38+B38; B40+B40; B41+B41	
3×CA (DL)	B42+B42+B42; B48+B48+B48	B1+B3+B3/B5/B7/B8/B20/B28/B38/B41; B1+B40+B40; B1+B41+B41; B1+B7+B20; B3+B3+B7/B20/B28; B3+B7+B7/B8/B20/B28; B3+B40+B40; B3+B41+B41; B7+B7+B20/B28; B40+B40+B40; B41+B41+B41	B2+B4+B5/B13/B71; B2+B5+B66; B2+B12+B30; B2+B13+B66; B2+B7+B12/B66; B4+B30+B5/B12/B29; B4+B7+B12; B30+B66+B5/B12/B29; B2+B2+B5/B12/B13/B29/B66; B5+B5+B2/B30/B66; B7+B7+B2/B4/B5; B66+B66+B2/B5/B13/B66; B41+B41+B25/B26/B41;
WCDMA (with Rx-diversity)	Not supported	B1/B3/B5/B8	B2/B4/B5
GNSS	GPS GLONASS BeiDou Galileo QZSS	GPS GLONASS BeiDou Galileo QZSS	GPS GLONASS BeiDou Galileo QZSS

NOTES

1. [1)] GNSS function is optional.
2. [2)] EG12 series module contains **Telematics** version and **Data-only** version. **Telematics** version supports voice and data functions, while **Data-only** version only supports data function.
3. "*" means under development.

With a compact profile of 37.0mm × 39.5mm × 2.8mm, EG12 meets almost all requirements for M2M applications such as automotive, security, 4G router, CPE, wireless POS Terminal, mobile computing device, PDA phone, and tablet PC.

EG12 is an SMD type module and can be embedded in applications through its 299 LGA pins.

2.2. Key Features

The following table describes the detailed features of EG12.

Table 2: Key Features of EG12

Feature	Details
Power Supply	Supply voltage: 3.3V~4.3V Typical supply voltage: 3.8V
Transmitting Power	Class 3 (23dBm±2dB) for LTE-TDD bands Class 3 (23dBm±2dB) for LTE-FDD bands Class 3 (24dBm+1/-3dB) for WCDMA bands
LTE Features	Support FDD/TDD LTE Category 12 with CA and MIMO Support uplink QPSK and 16-QAM and 64-QAM modulation Support downlink QPSK, 16-QAM and 64-QAM and 256-QAM modulation Support 1.4MHz to 60MHz (3×CA) RF bandwidth Support 4×4 MIMO in DL direction FDD: Max 600Mbps (DL)/150Mbps (UL) TDD: Max 430Mbps (DL)/90Mbps (UL)
UMTS Features	Support 3GPP R9 DC-HSDPA, DC-HSUPA, HSPA+, HSDPA, HSUPA and WCDMA Support QPSK, 16-QAM and 64-QAM modulation DC-HSDPA: Max 42Mbps DC-HSUPA: Max 11.2Mbps WCDMA: Max 384Kbps (DL)/384Kbps (UL)
Internet Protocol Features	Support PPP/QMI/TCP*/UDP*/FTP*/HTTP*/NTP*/PING*/HTTPS*/SMTP*/MMS*/FTPS*/SMTPS*/SSL* protocols Support the PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) usually used for PPP connections
SMS	Text and PDU mode Point to point MO and MT SMS cell broadcast SMS storage: ME by default
(U)SIM Interfaces	Support (U)SIM card: 1.8V/3.0V Dual SIM Single Standby
Audio Features	Provide one digital audio interface: PCM interface LTE: AMR/AMR-WB Support echo cancellation and noise suppression
PCM Interface	Used for audio function with external codec Support 16-bit linear data format

	Support long frame synchronization and short frame synchronization Support master and slave modes, but must be the master in long frame synchronization
USB Interface	Comply with USB 3.0 and 2.0 specifications, with maximum transmission rates up to 5Gbps on USB 3.0 and 480Mbps on USB 2.0 Used for AT command communication, data transmission, firmware upgrade, software debugging, GNSS NMEA sentence output, and voice over USB* Support USB serial drivers for: Windows 7/8/8.1/10; Linux 2.6/3.x/4.1~4.15; Android 4.x/5.x/6.x/7.x/8.x/9.x
UART Interfaces	**Main UART interface:** Used for AT command communication and data transmission Baud rate reaches up to 921600bps, 115200bps by default Support RTS and CTS hardware flow control **Debug UART interface:** Used for Linux console and log output 115200bps baud rate **BT UART interface:** Used for Bluetooth communication and can be multiplexed into SPI interface 115200bps baud rate
PCIe Interface*	Comply with PCI Express Specification Revision 2.1 and support 5Gbps per lane Used for data transmission
Rx-diversity	Support LTE/WCDMA Rx-diversity and LTE HO-diversity
GNSS Features	Gen9HT-Lite of Qualcomm Protocol: NMEA 0183
AT Commands	Comply with 3GPP TS 27.007 and 27.005, and Quectel enhanced AT commands
Network Indication	Two pins (NET_MODE and NET_STATUS) to indicate network connectivity status
Antenna Interfaces	Main antenna interface (ANT_MAIN) Rx-diversity antenna interface (ANT_DIV) Two MIMO antenna interfaces (ANT_MIMO1, ANT_MIMO2) GNSS antenna interface (ANT_GNSS)
Physical Characteristics	Size: (37.0±0.15)mm × (39.5±0.15)mm × (2.8±0.2)mm Weight: approx. 9.0g
Temperature Range	Operation temperature range: -35°C~ +75°C [1)] Extended temperature range: -40°C~ +85°C [2)] Storage temperature range: -40°C ~ +90°C
Firmware Upgrade	USB 2.0 interface and DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. "*" means under development.
2. [1] Within operating temperature range, the module is 3GPP compliant.
3. [2] Within extended temperature range, proper mounting, heating sinks and active cooling may be required to make certain functions of the module such as voice, SMS, data transmission, emergency call to be realized. Only one or more parameters like Pout might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operating temperature levels, the module will meet 3GPP specifications again.

2.3. Functional Diagram

The following figure shows a block diagram of EG12 and illustrates the major functional parts.

- Power management
- Baseband
- LPDDR2 SDRAM+NAND Flash
- Radio frequency
- Peripheral interfaces

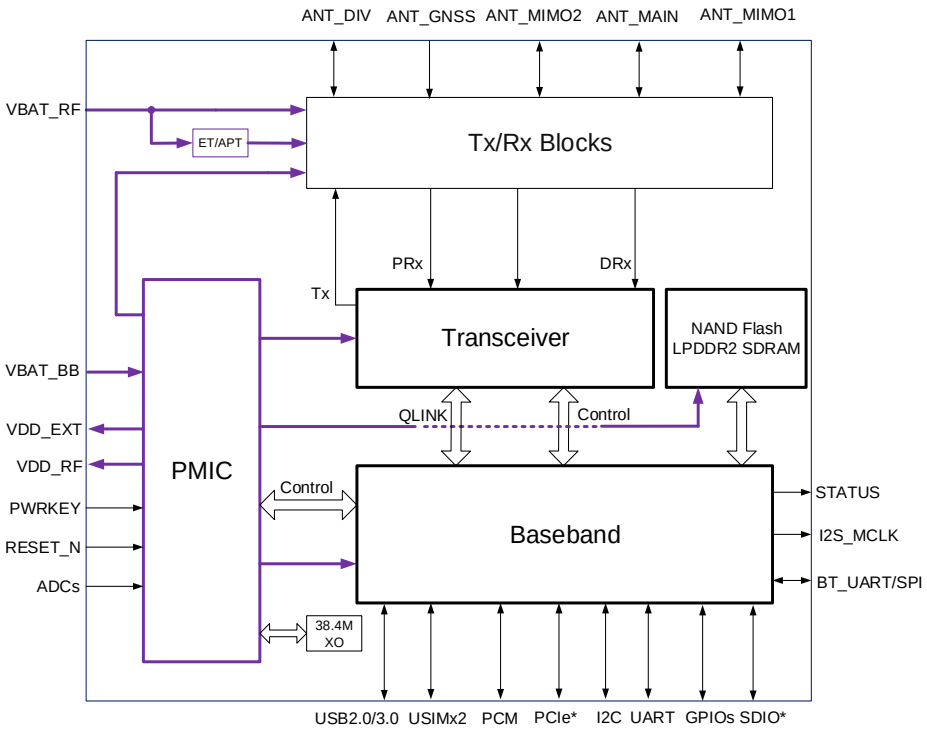


Figure 1: Functional Diagram

2.4. Evaluation Board

In order to help customers develop applications with EG12, Quectel supplies an evaluation board (EVB), USB to RS-232 converter cable, earphone, antenna, and other peripherals to control or test the module. For more details, please refer to ***document [1]***.

3 Application Interfaces

3.1. General Description

EG12 is designed with 299 LGA pins that can be connected to cellular application platform. This chapter mainly describes the following application interfaces and indication signals of EG12:

- Power supply
- (U)SIM interfaces
- USB interface
- UART interfaces
- SPI interface [1)]
- PCM and I2C interfaces
- ADC interfaces
- Network status indication
- Module operation status indication
- PCIe interface*
- SDIO interface*
- RFFE interface*
- USB_BOOT interface
- GPIOs

NOTES

1. "*" means under development.
2. [1)] SPI interface is multiplexed from BT UART interface.

3.2. Pin Assignment

The following figure shows the pin assignment of EG12.

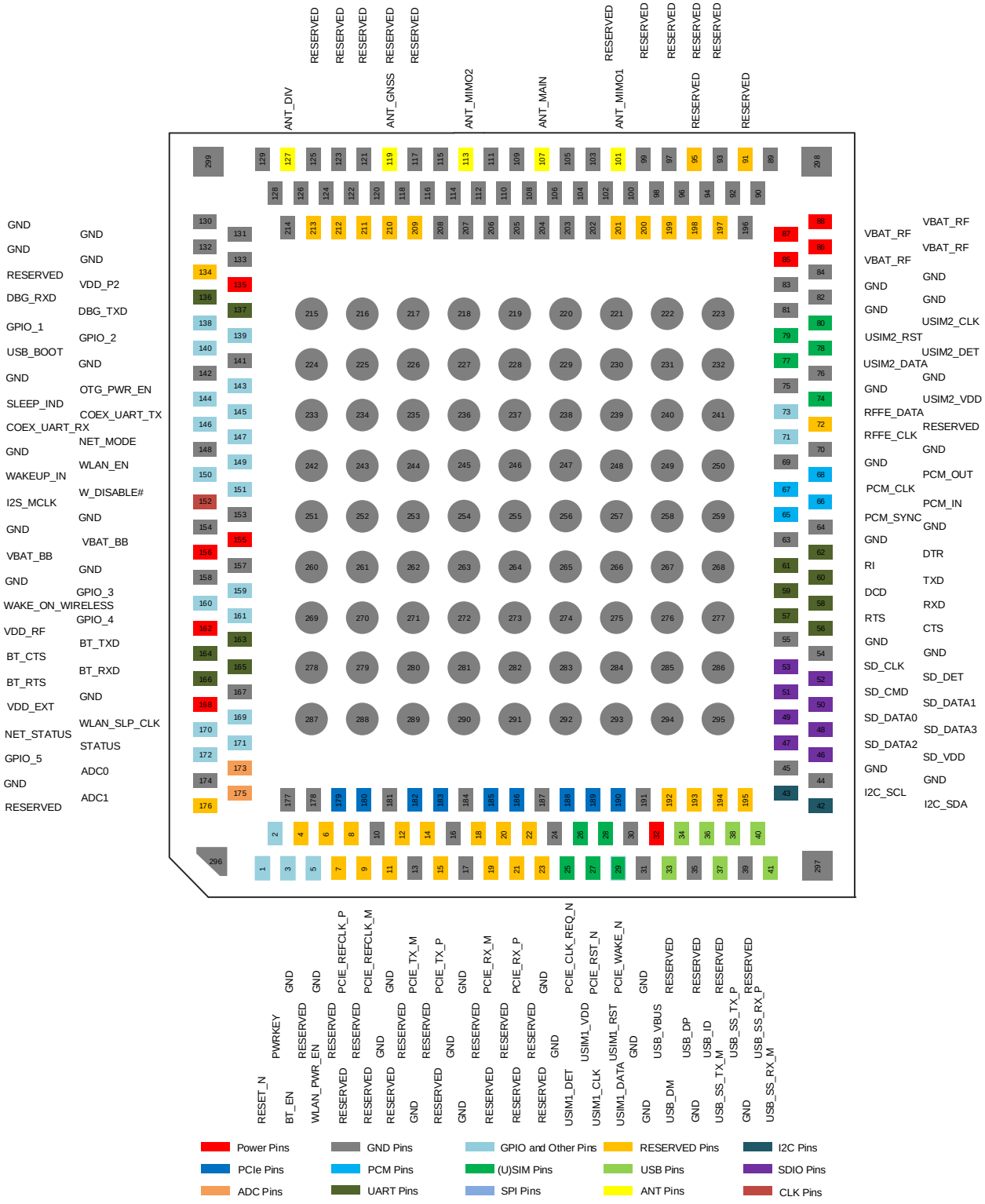


Figure 2: Pin Assignment (Top View)

NOTES

1. Keep all RESERVED pins and unused pins unconnected.
2. GND pins 215~299 should be connected to ground in the design.

3.3. Pin Description

The following tables show the pin definition and description of EG12.

Table 3: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
DI	Digital Input
DO	Digital Output
IO	Bidirectional
OD	Open Drain
PI	Power Input
PO	Power Output

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	155, 156	PI	Power supply for the module's baseband part.	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	It must be able to provide sufficient current up to 1.0A.
VBAT_RF	85, 86, 87, 88	PI	Power supply for the module's RF part.	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	It must be able to provide with sufficient current up to 1.5A in a transmitting burst.

VDD_P2	135	PI	SD card power supply		If an SD card is used, connect VDD_P2 to SD_VDD. If an eMMC* is used or SDIO interface is unused, connect VDD_P2 to VDD_EXT.
VDD_EXT	168	PO	Provide 1.8V for external circuit.	Vnorm=1.8V $I_O$max=50mA	
VDD_RF	162	PO	Provide 2.85V for external RF circuit.	Vnorm=2.85V $I_O$max=120mA	
GND	10, 13, 16, 17, 24, 30, 31, 35, 39, 44, 45, 54, 55, 63, 64, 69, 70, 75, 76, 81~84, 89, 90, 92~94, 96~100, 102~106, 108~112, 114~118, 120~126, 128~133, 141, 142, 148, 153, 154, 157, 158, 167, 174, 177, 178, 181, 184, 187, 191, 196, 202~208, 214~299	Ground			

Turn on/off

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RESET_N	1	DI	Reset the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	1.8V power domain. Pulled up internally. Active low.
PWRKEY	2	DI	Turn on/off the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	1.8V power domain. Pulled up internally. Active low.

Status Indication

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
NET_MODE	147	DO	Indicate the module's network registration mode	V_{OH}min=1.35V V_{OL}max=0.45V	1.8V power domain. If unused, keep it open.
NET_ STATUS	170	DO	Indicate the module's network activity status	V_{OH}min=1.35V V_{OL}max=0.45V	1.8V power domain. If unused, keep it open.
STATUS	171	DO	Indicate the module's operation status	V_{OH}min=1.35V V_{OL}max=0.45V	1.8V power domain. If unused, keep it open.
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_DET	25	DI	(U)SIM1 card insertion detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
USIM1_VDD	26	PO	Power supply for (U)SIM1 card	For 1.8V (U)SIM: Vmax=1.9V Vmin=1.7V For 3.0V (U)SIM: Vmax=3.05V Vmin=2.75V $I_O$max=50mA	Either 1.8V or 3.0V is supported by the module automatically.
USIM1_CLK	27	DO	Clock signal of (U)SIM1 card	For 1.8V (U)SIM: V_{OL}max=0.4V V_{OH}min=1.45V For 3.0V (U)SIM: V_{OL}max=0.4V V_{OH}min=2.3V	
USIM1_RST	28	DO	Reset signal of (U)SIM1 card	For 1.8V (U)SIM: V_{OL}max=0.4V V_{OH}min=1.45V For 3.0V (U)SIM: V_{OL}max=0.4V V_{OH}min=2.3V	
USIM1_ DATA	29	IO	Data signal of (U)SIM1 card	For 1.8V (U)SIM: V_{IL}max=0.36V V_{IH}min=1.26V	

				V_{OL}max=0.4V V_{OH}min=1.45V For 3.0V (U)SIM: V_{IL}max=0.57V V_{IH}min=2.0V V_{OL}max=0.4V V_{OH}min=2.3V	
USIM2_VDD	74	PO	Power supply for (U)SIM2 card	For 1.8V (U)SIM: Vmax=1.9V Vmin=1.7V For 3.0V (U)SIM: Vmax=3.05V Vmin=2.75V IOmax=50mA	Either 1.8V or 3.0V is supported by the module automatically. If (U)SIM2 interface is unused, keep it open.
USIM2_DATA	77	IO	Data signal of (U)SIM2 card	For 1.8V (U)SIM: V_{IL}max=0.36V V_{IH}min=1.26V V_{OL}max=0.4V V_{OH}min=1.45V For 3.0V (U)SIM: V_{IL}max=0.57V V_{IH}min=2V V_{OL}max=0.4V V_{OH}min=2.3V	If (U)SIM2 interface is unused, keep it open.
USIM2_DET	78	DI	(U)SIM2 card insertion detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If (U)SIM2 interface is unused, keep it open.
USIM2_RST	79	DO	Reset signal of (U)SIM2 card	For 1.8V (U)SIM: V_{OL}max=0.4V V_{OH}min=1.45V For 3.0V (U)SIM: V_{OL}max=0.4V V_{OH}min=2.3V	If (U)SIM2 interface is unused, keep it open.
USIM2_CLK	80	DO	Clock signal of (U)SIM2 card	For 1.8V (U)SIM: V_{OL}max=0.4V V_{OH}min=1.45V For 3.0V (U)SIM: V_{OL}max=0.4V	If (U)SIM2 interface is unused, keep it open.

				V_{OH}min=2.3V	
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	32	PI	USB connection detection	Vmax=5.25V Vmin=3.3V Vnorm=5.0V	
USB_DM	33	IO	USB 2.0 differential data bus - minus		Comply with USB 2.0 standard specifications. Require differential impedance of 90Ω.
USB_DP	34	IO	USB 2.0 differential data bus - plus		
USB_SS_TX_M	37	AO	USB 3.0 super speed transmission - minus		Comply with USB 3.0 standard specifications. Require differential impedance of 90Ω.
USB_SS_TX_P	38	AO	USB 3.0 super speed transmission - plus		
USB_SS_RX_P	40	AI	USB 3.0 super speed receiving - plus		
USB_SS_RX_M	41	AI	USB 3.0 super speed receiving - minus		
USB_ID	36	DI	OTG identification	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
OTG_PWR_EN	143	DO	OTG power control	V_{OL}max=0.45V V_{OH}min=1.35V	
SDIO Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_VDD	46	PO	**SD card application**: SDIO pull up power source **eMMC application**: Keep it open when used for eMMC	For 1.8V SD card: Vmax=1.9V Vmin=1.75V For 3.0V SD card: Vmax=3.05V Vmin=2.75V $I_O$max=50mA	Either 1.8V or 3.0V is supported by the module automatically. Power of SD card must be provided by an external power supply.

SD_DATA0	49	IO	SDIO data signal (bit 0)	For 1.8V SD card: V_{OL}max=0.45V V_{OH}min=1.4V V_{IL}min=-0.3V V_{IL}max=0.58V V_{IH}min=1.3V V_{IH}max=2.0V For 3.0V SD card: V_{OL}max=0.35V V_{OH}min=2.15V V_{IL}min=-0.3V V_{IL}max=0.7V V_{IH}min=1.8V V_{IH}max=3.15V	If unused, keep it open.
SD_DATA1	50	IO	SDIO data signal (bit 1)		If unused, keep it open.
SD_DATA2	47	IO	SDIO data signal (bit 2)		If unused, keep it open.
SD_DATA3	48	IO	SDIO data signal (bit 3)		If unused, keep it open.
SD_CMD	51	DO	SDIO command signal		If unused, keep it open.
SD_ DET	52	DI	SD card insertion detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain, If unused, keep it open.
SD_CLK	53	DO	SDIO clock signal		If unused, keep it open.
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CTS	56	DO	Clear to send	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
RTS	57	DI	Request to send	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
RXD	58	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.

DCD	59	DO	Data carrier detection	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
TXD	60	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
RI	61	DO	Ring indication	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
DTR	62	DI	Data terminal ready, sleep mode control	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Pulled up by default. Pulling down to low level will wake up the module. If unused, keep it open.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	136	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
DBG_TXD	137	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
BT UART Interface (Can be multiplexed into SPI interface)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BT_EN	3	DO	BT function enable control	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
BT_TXD	163	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open. BT UART interface pin by default. Can be multiplexed into SPI_MOSI.
BT_CTS	164	DO	Clear to send	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.

					BT UART interface pin by default. Can be multiplexed into SPI_CLK.
BT_RXD	165	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open. BT UART interface pin by default. Can be multiplexed into SPI_MISO.
BT_RTS	166	DI	Request to send	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open. BT UART interface pin by default. Can be multiplexed into SPI_CS.
PCM & I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SDA	42	OD	I2C serial interface used for external codec		1.8V power domain. An external pull-up resistor is required. If unused, keep it open.
I2C_SCL	43	OD			
PCM_SYNC	65	IO	PCM data frame synchronization signal	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_IN	66	DI	PCM data input	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
PCM_CLK	67	IO	PCM clock	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it

					open.
PCM_OUT	68	DO	PCM data output	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
I2S_MCLK	152	DO	Clock output		Provide a digital clock output for an external audio codec. If unused, keep it open.
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	107	IO	Support all band main antenna interface		50Ω impedance
ANT_DIV	127	AI	Support all band RXD antenna interface		50Ω impedance If unused, keep them open.
ANT_ MIMO1	101	AI	Support all band 4x4 MIMO antenna interface		
ANT_MIMO2	113	AI	Support all band 4x4 MIMO antenna interface		
ANT_GNSS	119	AI	GNSS antenna interface		
WLAN Control Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_PWR_EN	5	DO	WLAN power supply enable control	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
COEX_UART_TX	145	DO	LTE/WLAN coexistence signal	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
COEX_UART_RX	146	DI	LTE/WLAN coexistence signal	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
WLAN_EN	149	DO	WLAN function enable control	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. Active high.

					If unused, keep it open.
WAKE_ON_WIRELESS	160	DI	Wake up the host (EG12) by an external Wi-Fi module	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Active low. If unused, keep it open.
WLAN_SLP_CLK	169	DO	WLAN sleep clock	V_{OL}max=0.45V V_{OH}min=1.35V	If unused, keep it open.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	173	AI	General purpose analog to digital converter interface	Voltage range: 0V to 1.875V	If unused, keep it open.
ADC1	175	AI	General purpose analog to digital converter interface	Voltage range: 0V to 1.875V	If unused, keep it open.
PCIe Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE_REFCLK_P	179	AI/AO	Input/Output PCIe reference clock - plus		Comply with PCIe 2.1 standard specifications. Require differential impedance of 95Ω.
PCIE_REFCLK_M	180	AI/AO	Input/Output PCIe reference clock - minus		
PCIE_TX_M	182	AO	PCIe transmission - minus		
PCIE_TX_P	183	AO	PCIe transmission - plus		
PCIE_RX_M	185	AI	PCIe receiving - minus		
PCIE_RX_P	186	AI	PCIe receiving - plus		
PCIE_CLK_REQ_N	188	IO	PCIe clock request	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	In master mode, it is an input signal. In slave mode, it is an output signal. If unused, keep it open.
PCIE_RST_N	189	IO	PCIe reset	V_{OL}max=0.45V V_{OH}min=1.35V	In master mode, it is an output signal.

				V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	In slave mode, it is an input signal. If unused, keep it open.
PCIE_WAKE_N	190	IO	PCIe wake up	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V V_{IH}max=2.0V	In master mode, it is an input signal. In slave mode, it is an output signal. If unused, keep it open.
GPIO Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO_1	138	IO	General purpose input/output port	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	If unused, keep them open.
GPIO_2	139	IO			
GPIO_3	159	IO			
GPIO_4	161	IO			
GPIO_5	172	IO			
RFFE Interface*					
Pin Name	**Pin Name**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RFFE_CLK	71	DO	RFFE serial interface used for external tuner control	V_{OL}max=0.45V V_{OH}min=1.35V	If unused, keep it open.
RFFE_DATA	73	IO		V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	If unused, keep it open.
Other Pins					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_BOOT	140	DI	Force the module to enter into emergency download mode	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Active high If unused, keep it open.
SLEEP_IND	144	DO	Sleep indication	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
WAKEUP_IN	150	DI	Sleep mode control	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Pulled up by default. Low level wakes up the module. If unused, keep it open.
W_DISABLE#	151	DI	Airplane mode control	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Pulled up by default. In low voltage level, the module can enter into airplane mode. If unused, keep it open.
RESERVED Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	4, 6~9, 11, 12, 14, 15, 18~23, 72, 91, 95, 134, 176, 192~195, 197~201, 209~213		Reserved		Keep these pins unconnected.

3.4. Operating Modes

The table below summarizes different operating modes of EG12.

Table 5: Overview of Operating Modes

Mode	Details	
Normal Operation mode	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** command can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN=4** command or driving W_DISABLE# pin to low level can set the module to airplane mode. In this case, RF function will be invalid.	
Sleep Mode	In this mode, the current consumption of the module will be reduced to the minimal level. During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.	
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is not active. The serial interfaces are not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

3.5. Power Saving

3.5.1. Sleep Mode

DRX of EG12 is able to reduce the current consumption to a minimum value during the sleep mode, and DRX cycle index values are broadcasted by the wireless network. The figure below shows the relationship between the DRX run time and the current consumption in sleep mode. The longer the DRX cycle is, the lower the current consumption will be.

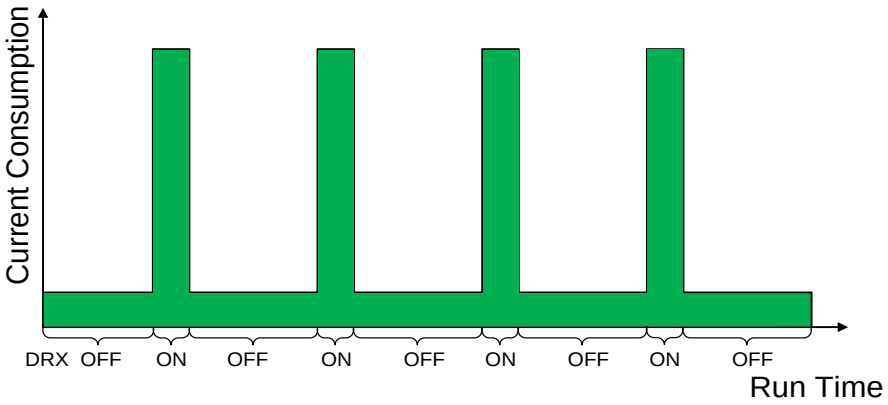


Figure 3: DRX Run Time and Current Consumption in Sleep Mode

The following section describes power saving procedure of EG12.

3.5.1.1. UART Application

If the host communicates with the module via UART interfaces, the following preconditions can let the module enter into sleep mode.

- Keep DTR at high level (pulled up by default).
- Execute **AT+QSCLK=1** command to enable sleep mode.

The following figure shows the connection between the module and the host.

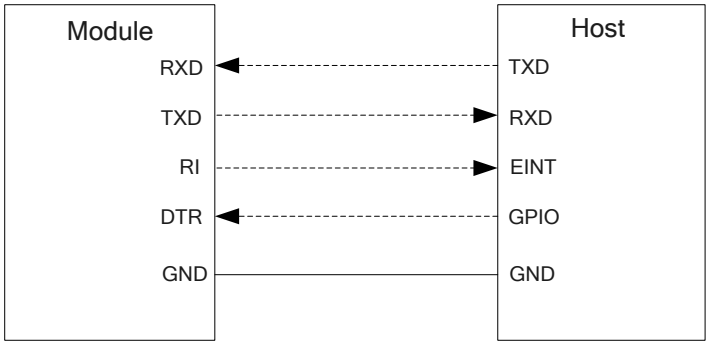


Figure 4: Sleep Mode Application via UART Interfaces

- Driving the host DTR to low level will wake up the module.
- When EG12 has a URC to report, RI signal will wake up the host. Please refer to ***Chapter 3.17*** for details about RI behavior.

3.5.1.2. USB Application with USB Remote Wakeup Function

If the host supports USB suspend/resume and remote wakeup function, the following three preconditions must be met to let the module enter into the sleep mode.

- Keep DTR at high level (pulled up by default).
- Execute **AT+QSCLK=1** command to enable the sleep mode.
- The host's USB bus, which is connected with the module's USB interface, has entered into suspend state.

The following figure shows the connection between the module and the host.

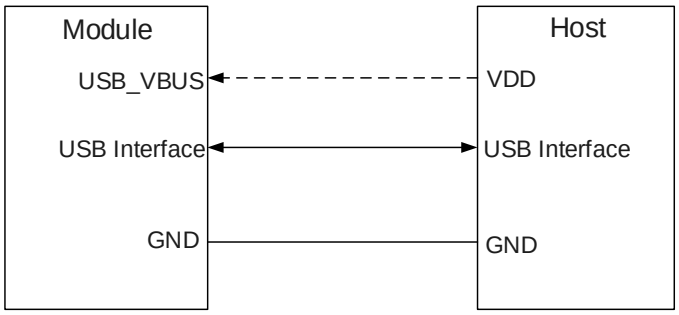


Figure 5: Sleep Mode Application with USB Remote Wakeup

- Sending data to EG12 through USB will wake up the module.
- When EG12 has a URC to report, the module will send remote wake-up signals via USB bus to wake up the host.

3.5.1.3. USB Application with USB Suspend/Resume and RI Function

If the host supports USB suspend/resume, but does not support remote wake-up function, the RI signal is needed to wake up the host.

There are three preconditions to let the module enter into the sleep mode.

- Keep DTR at high level (pulled up by default).
- Execute **AT+QSCLK=1** command to enable the sleep mode.
- The host's USB bus, which is connected with the module's USB interface, has entered into suspend state.

The following figure shows the connection between the module and the host.

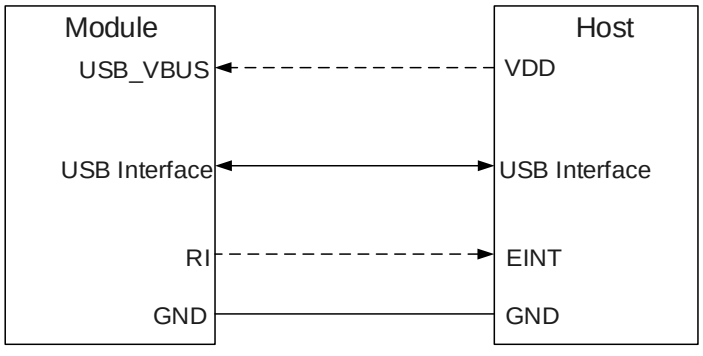


Figure 6: Sleep Mode Application with RI

- Sending data to EG12 through USB will wake up the module.

- When EG12 has a URC to report, RI signal will wake up the host.

3.5.1.4. USB Application without USB Suspend Function

If the host does not support USB suspend function, USB_VBUS should be disconnected with an external control circuit to let the module enter into sleep mode.

- Keep DTR at high level (pulled up by default).
- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

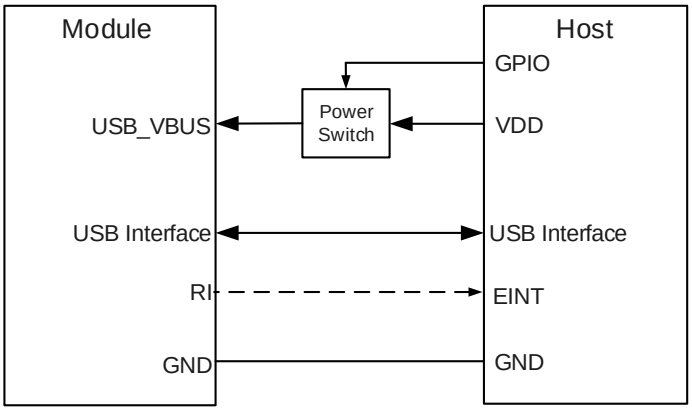


Figure 7: Sleep Mode Application without Suspend Function

Switching on the power switch to supply power to USB_VBUS will wake up the module.

NOTE

Please pay attention to the level match of the connection shown in dotted line between the module and the host.

3.5.2. Airplane Mode

EG12 provides a W_DISABLE# signal to disable or enable airplane mode through hardware operation. The W_DISABLE# pin is pulled up by default. Driving it to low level will let the module enter into airplane mode.

In airplane mode, the RF function will be disabled. The RF function can also be enabled or disabled through software AT commands. The following table shows the RF function status of the module.

Table 6: RF Function Status

W_DISABLE#	AT Commands	RF Function	Module Operation
High Level	**AT+CFUN=1**	RF Enabled	Normal mode
	AT+CFUN=0 **AT+CFUN=4**	RF Disabled	**AT+CFUN=0**: Minimum functionality mode **AT+CFUN=4**: Airplane mode
Low Level	**AT+CFUN=0** **AT+CFUN=1** **AT+CFUN=4**	RF Disabled	Airplane mode

NOTES

1. The W_DISABLE# control function is disabled in firmware by default. It can be enabled by **AT+QCFG="airplanecontrol"** command, and this command is under development.
2. The execution of **AT+CFUN** command will not affect GNSS function.

3.6. Power Supply

3.6.1. Power Supply Pins

EG12 provides six VBAT pins dedicated to connection with an external power supply. There are two separate voltage domains for VBAT.

- Four VBAT_RF pins for module's RF part
- Two VBAT_BB pins for module's baseband part

The following table shows details of VBAT pins and ground pins.

Table 7: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	85, 86 87, 88	Power supply for the module's RF part	3.3	3.8	4.3	V
VBAT_BB	155, 156	Power supply for the module's baseband part	3.3	3.8	4.3	V
GND	10, 13, 16, 17, 24, 30, 31, 35, 39, 44, 45, 54, 55, 63, 64, 69, 70, 75, 76, 81~84, 89, 90,	Ground	-	0	-	V

	92~94, 96~100, 102~106, 108~112, 114~118, 120~126, 128~133, 141, 142, 148, 153, 154, 157, 158, 167, 174, 177, 178, 181, 184, 187, 191, 196, 202~208, 214~299

3.6.2. Decrease Voltage Drop

The power supply range of the module is from 3.3V to 4.3V. Please make sure the input voltage will never drop below 3.3V. The following figure shows the voltage drop during Tx power in 3G and 4G networks.

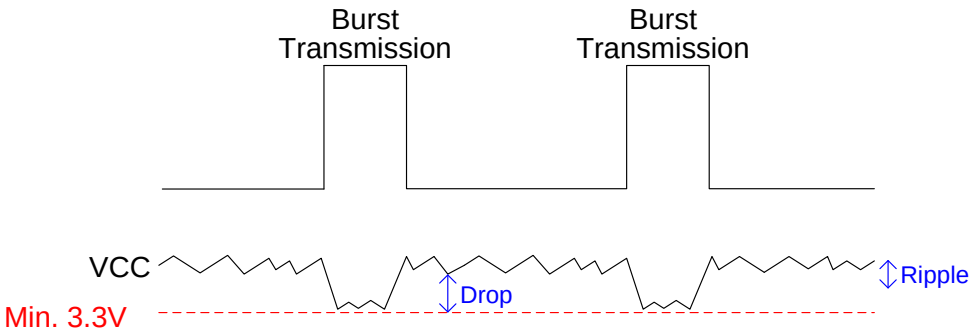


Figure 8: Power Supply Limits during Tx Power

To decrease voltage drop, a bypass capacitor of about 100μF with low ESR should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100nF, 33pF, 10pF) for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1mm; and the width of VBAT_RF trace should be no less than 2mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, in order to get a stable power source, it is suggested to use a zener diode of which reverse zener voltage is 5.1V and dissipation power is more than 0.5W. The following figure shows the star structure of the power supply.

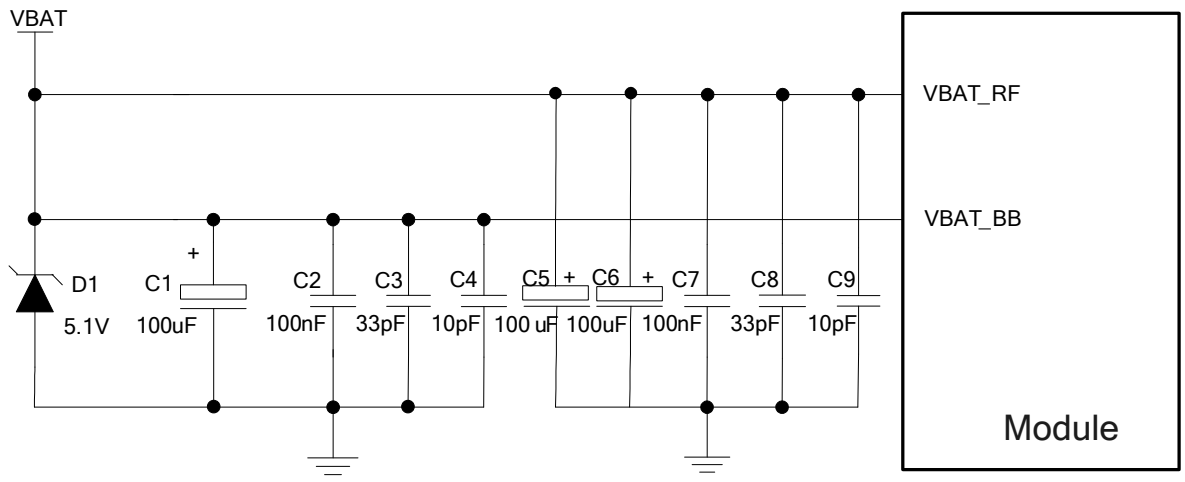


Figure 9: Star Structure of the Power Supply

3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply of EG12 should be able to provide sufficient current up to 2A at least. If the voltage drop between the input and output is not too high, an LDO is suggested to be used to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5V input power source. In this design, output of the power supply is about 3.8V and the maximum load current is 3A.

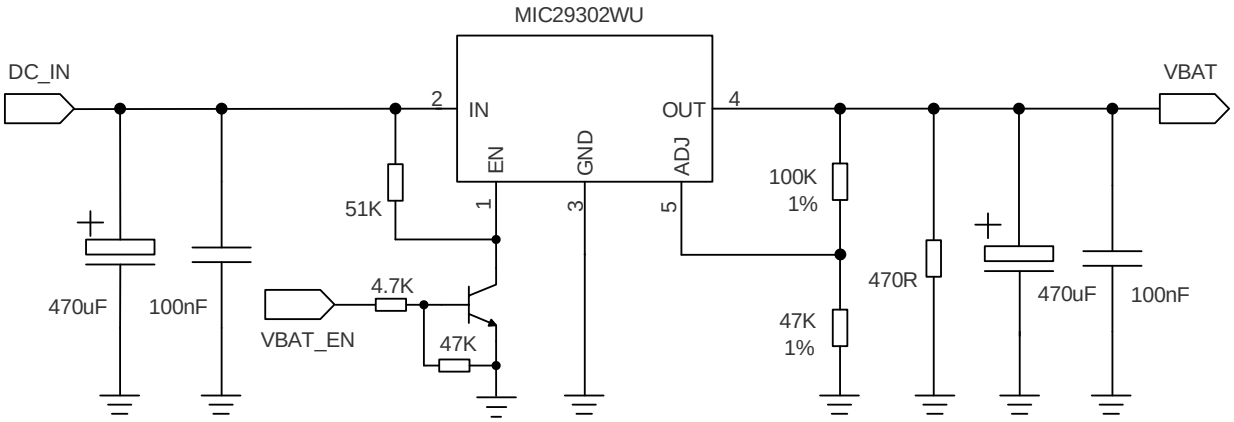


Figure 10: Reference Circuit of Power Supply

NOTE

In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, the power supply can be cut off.

3.6.4. Monitor the Power Supply

AT+CBC command can be used to monitor the VBAT_BB voltage value. For more details, please refer to ***document [2]***.

3.7. Turn on and off Scenarios

3.7.1. Turn on the Module Using PWRKEY

The following table shows the pin definition of PWRKEY.

Table 8: PWRKEY Pin Description

Pin Name	Pin No.	Description	DC Characteristics	Comment
PWRKEY	2	Turn on/off the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	1.8V power domain. Pulled-up internally. Active low.

When EG12 is in power down mode, it can be turned on and enter into normal mode by driving the PWRKEY pin to a low level for at least 500ms. It is recommended to use an open drain/collector driver to control the PWRKEY. After STATUS outputs a high level, PWRKEY can be released. A simple reference circuit is illustrated in the following figure.

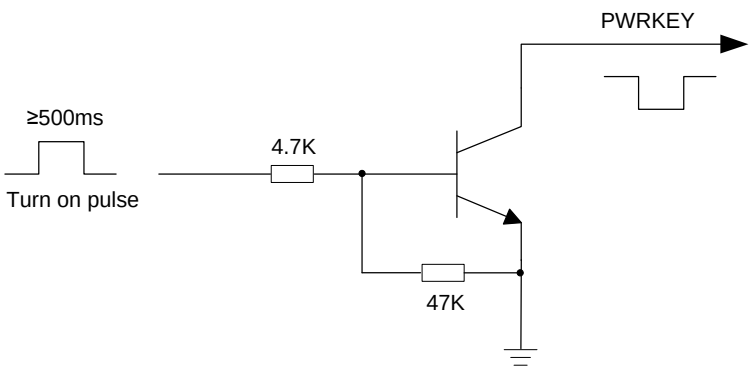


Figure 11: Turn on the Module with a Driving Circuit

Another way to control the PWRKEY is using a button directly. When pressing the key, electrostatic strike may generate from fingers. Therefore, it is necessary to place a TVS component nearby the button for ESD protection. A reference circuit is shown in the following figure:

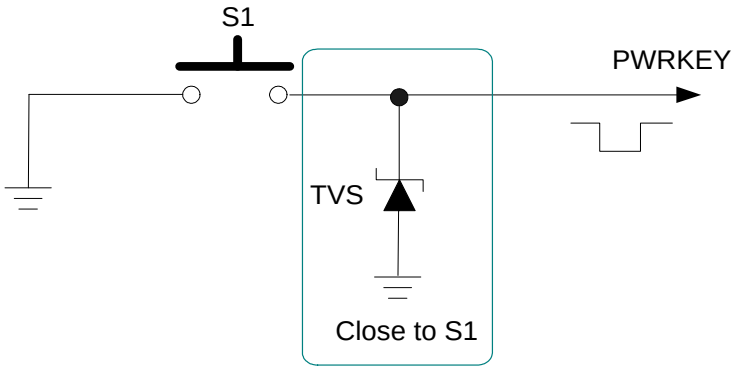


Figure 12: Turn on the Module Using a Button

The turn-on scenario is illustrated in the following figure.

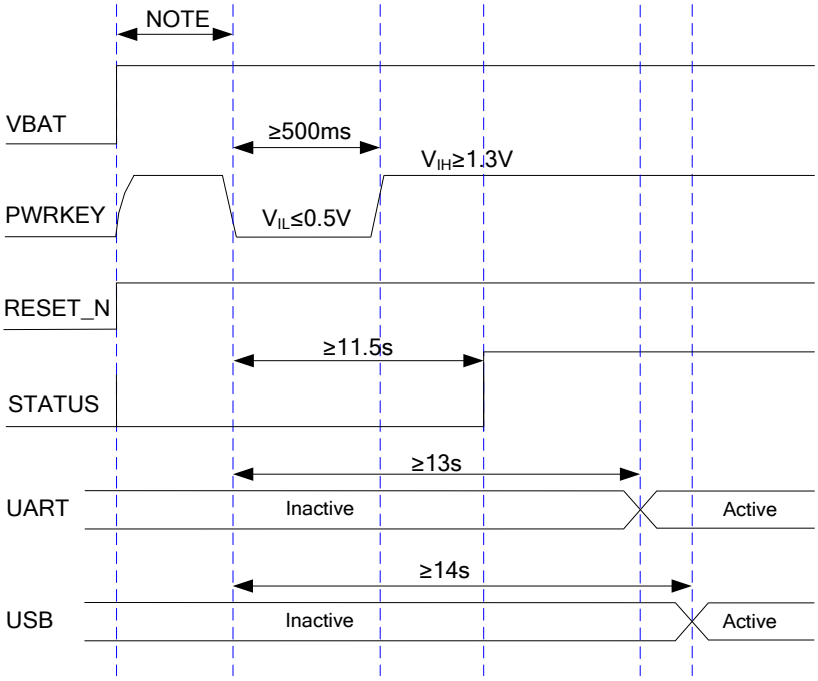


Figure 13: Timing of Turning on Module

NOTE

Please ensure that VBAT is stable for no less than 30ms before pulling down the PWRKEY.

3.7.2. Turn off the Module

The following two methods can be used to turn off the module: using PWRKEY or AT+QPOWD command.

3.7.2.1. Turn off the Module Using PWRKEY

Driving PWRKEY to a low level voltage for at least 800ms, the module will execute power-down procedure after the PWRKEY is released. The turn-off scenario is illustrated in the following figure.

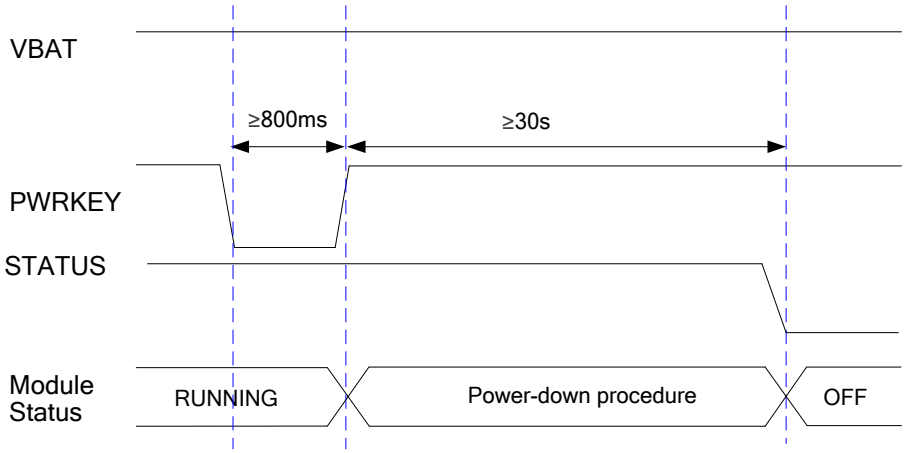


Figure 14: Timing of Turning off the Module

3.7.2.2. Turn off the Module Using AT Command

It is also a safe way to use **AT+QPOWD** command to turn off the module. Please refer to ***document [2]*** for more details about the command.

NOTES

1. In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, the power supply can be cut off.
2. When turning off module with AT command, please keep PWRKEY at high level after the execution of power-off command. Otherwise the module will be turned on again after successful turn-off.

3.8. Reset the Module

The module can be reset by driving RESET_N to a low level voltage for 250ms~600ms and then releasing it.

Table 9: RESET_N Pin Description

Pin Name	Pin No.	Description	DC Characteristics	Comment
RESET_N	1	Reset the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	

An open drain/collector driver or button can be used to control the RESET_N. A reference circuit is shown as below.

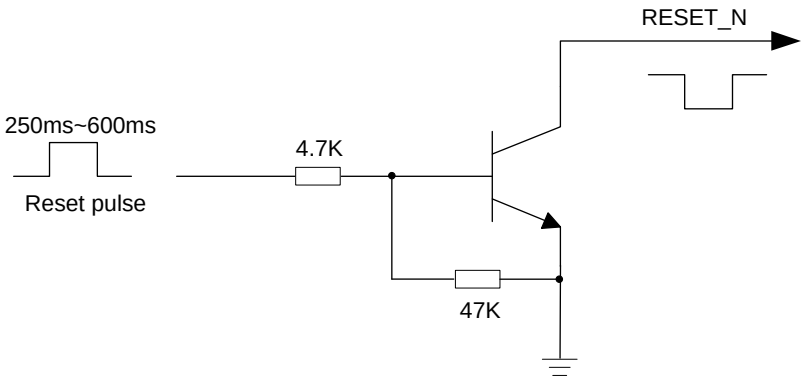


Figure 15: Reference Circuit of RESET_N with a Driving Circuit

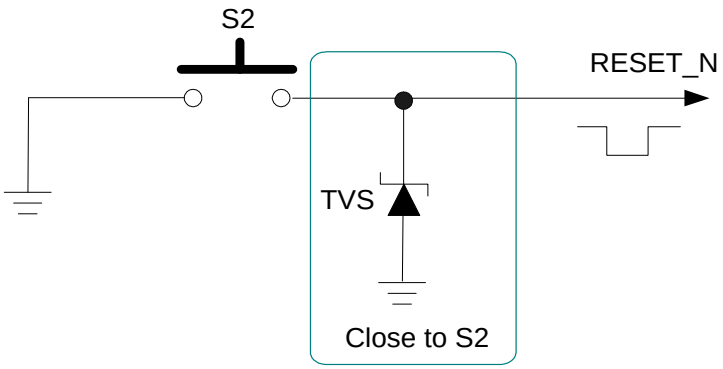


Figure 16: Reference Circuit of RESET_N with a Button

The reset scenario is illustrated in the following figure.

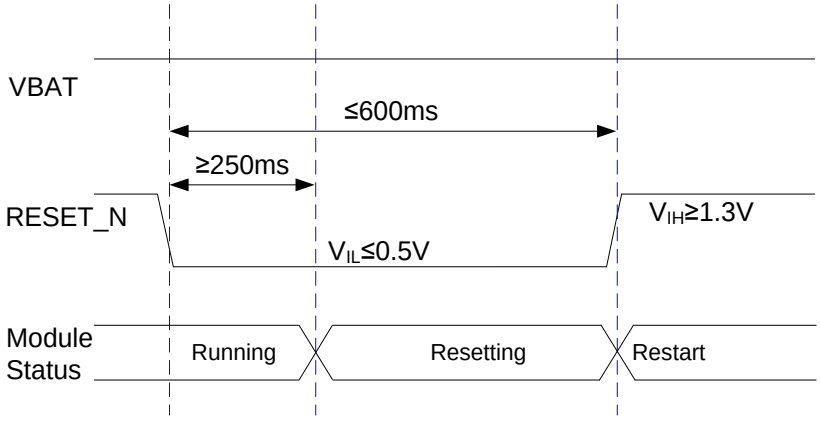


Figure 17: Timing of Resetting the Module

NOTES

1. RESET_N can only be used when turning off the module failed either by **AT+QPOWD** command or PWRKEY.
2. Please ensure that there is no large capacitance on PWRKEY and RESET_N.

3.9. (U)SIM Interfaces

EG12 provides two (U)SIM interfaces. The circuitry of (U)SIM interfaces meets ETSI and IMT-2000 requirements. Either 1.8V or 3.0V (U)SIM cards are supported. Dual SIM Single Standby function is supported and (U)SIM card switching is enabled by **AT+QUIMSLOT** command. For more details, please refer to ***document [2]***.

Table 10: Pin Definition of the (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_DET	25	DI	(U)SIM1 card insertion detection	
USIM1_VDD	26	PO	Power supply for (U)SIM1 card	Either 1.8V or 3.0V is supported by the module automatically.
USIM1_CLK	27	DO	Clock signal of (U)SIM1 card	
USIM1_RST	28	DO	Reset signal of (U)SIM1 card	

USIM1_DATA	29	IO	Data signal of (U)SIM1 card	
USIM2_VDD	74	PO	Power supply for (U)SIM2 card	Either 1.8V or 3.0V is supported by the module automatically. If (U)SIM2 interface is unused, keep it open.
USIM2_ DATA	77	IO	Data signal of (U)SIM2 card	If (U)SIM2 interface is unused, keep it open.
USIM2_DET	78	DI	(U)SIM2 card insertion detection	If (U)SIM2 interface is unused, keep it open.
USIM2_RST	79	DO	Reset signal of (U)SIM2 card	If (U)SIM2 interface is unused, keep it open.
USIM2_CLK	80	DO	Clock signal of (U)SIM2 card	If (U)SIM2 interface is unused, keep it open.

EG12 supports (U)SIM card hot-plug via USIM_DET pins. The function supports low level and high level detections, and is disabled by default. Please refer to ***document [2]*** for more details about **AT+QSIMDET** command.

The following figure shows a reference design for a (U)SIM interface with an 8-pin (U)SIM card connector.

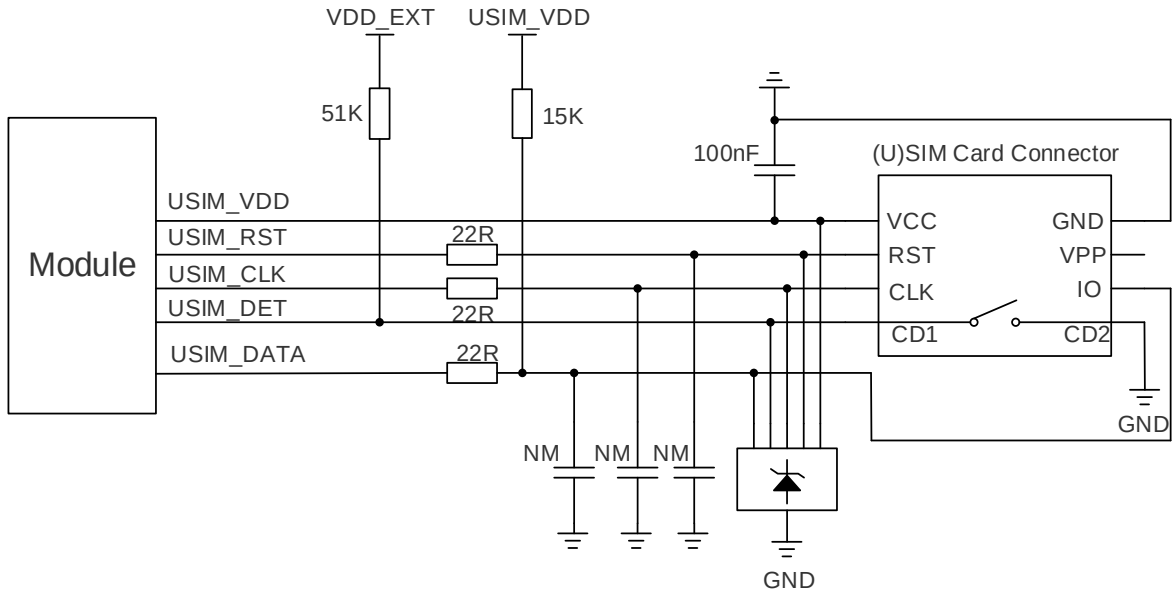


Figure 18: Reference Circuit of a (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_DET pins unconnected. A reference circuit for a (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

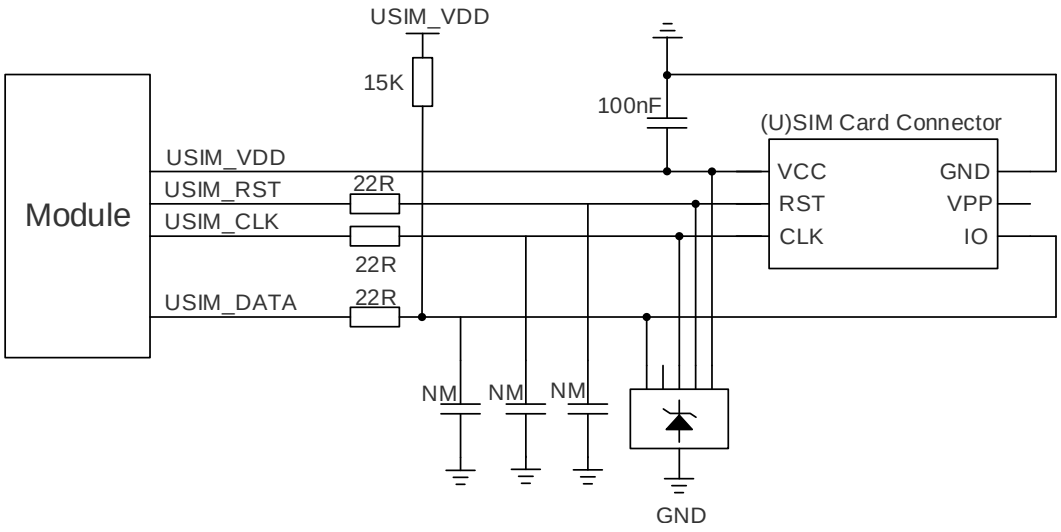


Figure 19: Reference Circuit of a (U)SIM Interface with a 6-Pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in the (U)SIM circuit design:

- Keep placement of the (U)SIM card connector to the module as close as possible. Keep the trace length as less than 200mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Ensure that the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array of which parasitic capacitance should be no more than 50pF. The 22Ω resistors should be added in series between the module and the (U)SIM card connector to facilitate debugging. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

3.10. USB Interface

EG12 provides one integrated Universal Serial Bus (USB) interface which complies with the USB 3.0 and 2.0 specifications. This USB interface supports super speed (5Gbps) on USB 3.0 and high speed (480 Mbps) and full speed (12 Mbps) modes on USB 2.0. It is used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade, and voice over USB*.

The following table shows the pin definition of USB interface.

Table 11: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	32	PI	Used for detecting the USB connection	Typical 5.0V
USB_DP	34	IO	USB 2.0 differential data bus - plus	Require differential impedance of 90Ω
USB_DM	33	IO	USB 2.0 differential data bus - minus	
USB_SS_ TX_M	37	AO	USB 3.0 super-speed transmission - minus	Require differential impedance of 90Ω
USB_SS_ TX_P	38	AO	USB 3.0 super-speed transmission - plus	
USB_SS_ RX_P	40	AI	USB 3.0 super-speed receiving - plus	Require differential impedance of 90Ω
USB_SS_ RX_M	41	AI	USB 3.0 super-speed receiving - minus	
USB_ID	36	DI	OTG identification	1.8V power domain. If unused, keep it open
OTG_PWR_EN	143	DO	OTG power control	

For more details about the USB 2.0 & USB 3.0 specifications, please visit http://www.usb.org/home.

The USB interface is recommended to be reserved for firmware upgrade in customers' designs. The following figure shows a reference circuit of USB 2.0 & USB 3.0 interface.

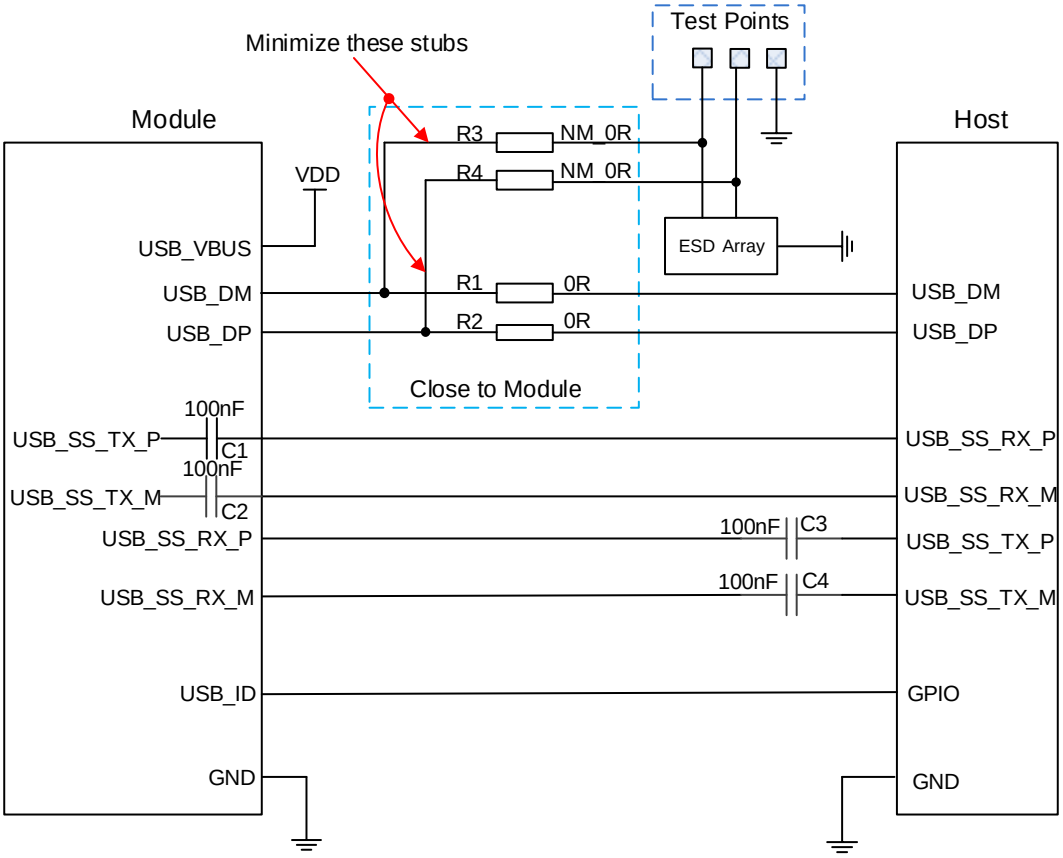


Figure 20: Reference Circuit of USB Application

In order to ensure the signal integrity of USB data lines, C1, and C2 have been already installed in the module; C3 and C4 must be placed close to the host; and R1~R4 should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles of USB interface should be complied with, so as to meet USB 2.0 & USB 3.0 specifications.

- It is important to route the USB 2.0 & 3.0 signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90Ω.
- For USB 2.0 signal traces, the trace length should be less than 120mm, and the differential data pair matching should be less than 2mm (15ps).
- For USB 3.0 signal traces, the maximum length of each differential data pair (TX/RX) is recommended to be less than 100mm, and each differential data pair matching should be less than 0.7mm (5ps).
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- If a USB connector is used, please keep the ESD protection components as close to the USB connector as possible. Pay attention to the influence of junction capacitance of ESD protection components on USB data lines. Typically, the capacitance value should be less than 2.0pF for USB

2.0, and less than 0.4pF for USB 3.0.

- If possible, reserve a 0Ω resistor on USB_DP and USB_DM lines respectively.

NOTE

"*" means under development.

3.11. UART Interfaces

The module provides three UART interfaces: main UART interface, debug UART interface, and BT UART interface. Features of these interfaces are shown as below:

- Main UART interface supports 4800bps, 9600bps, 19200bps, 38400bps, 57600bps, 115200bps (default), 230400bps, 460800bps, and 921600bps baud rates. This interface is used for data transmission and AT command communication.
- Debug UART interface supports 115200bps baud rate. It is used for Linux console and log output.
- BT UART interface supports 115200bps baud rate. It is used for BT communication and can be multiplexed into SPI interface*.

NOTE

"*" means under development.

3.11.1. Main UART Interface

The following table shows the main UART interface pin definition.

Table 12: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
CTS	56	DO	Clear to send	1.8V power domain
RTS	57	DI	Request to send	1.8V power domain
RXD	58	DI	Receive data	1.8V power domain
DCD	59	DO	Data carrier detection	1.8V power domain
TXD	60	DO	Transmit data	1.8V power domain

RI	61	DO	Ring indication	1.8V power domain
DTR	62	DI	Data terminal ready, sleep mode control	1.8V power domain

3.11.2. Debug UART Interface

The following table shows the Debug UART interface pin definition.

Table 13: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	136	DI	Receive data	1.8V power domain
DBG_TXD	137	DO	Transmit data	1.8V power domain

3.11.3. BT UART Interface

The following table shows the BT UART interface pin definition.

Table 14: Pin Definition of the BT UART Interface

Pin Name	Pin No.	I/O	Description	Comment
BT_EN	3	DO	BT function enable control	1.8V power domain If unused, keep it open.
BT_TXD	163	DO	Transmit data	
BT_CTS	164	DO	Clear to send	
BT_RXD	165	DI	Receive data	
BT_RTS	166	DI	Request to send	

3.11.4. UART Application

EG12 provides 1.8V UART interfaces. A level translator should be used if the application is equipped with a 3.3V UART interface. A level translator TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

The logic levels are described in the following table.

Table 15: Logic Levels of Digital I/O

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

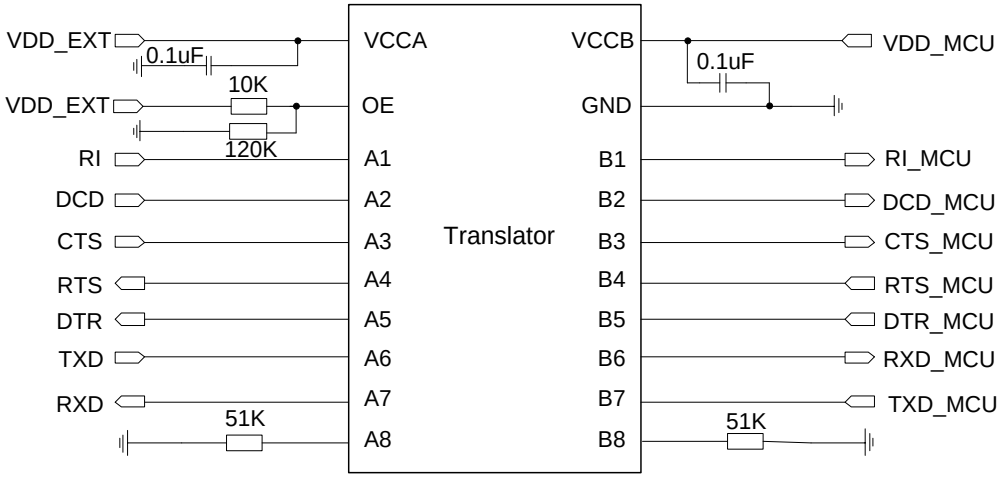


Figure 21: Level Translation Reference Circuit with an IC

Please visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as below. The circuit design of dotted line section can refer to the design of solid line section, and please pay attention to the direction of connection.

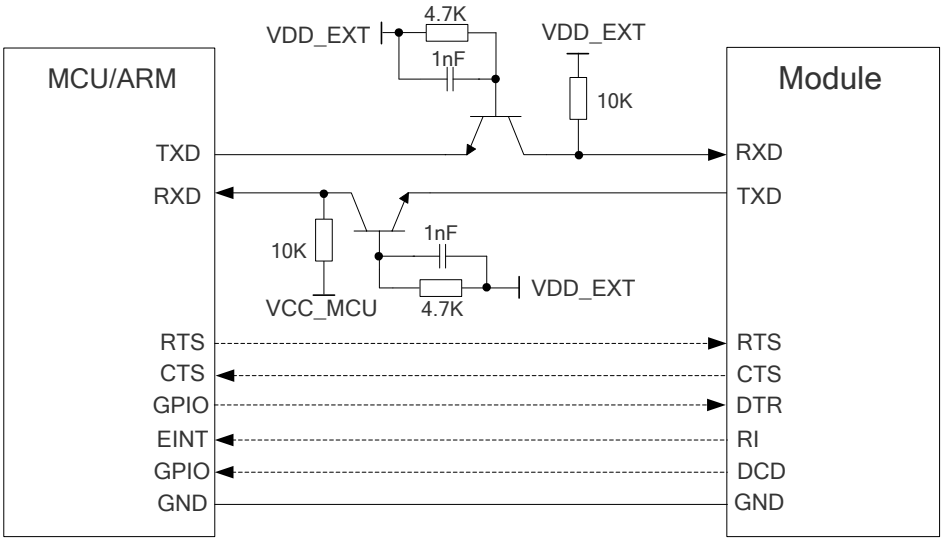


Figure 22: Level Translation Reference Circuit with MOSFETs

NOTE

Transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.

3.12. SPI Interface

EG12 provides one SPI interface multiplexed from BT UART interface. The interface only supports master mode with a maximum clock frequency up to 50MHz. The following table shows the pin definition of SPI interface.

Table 16: Pin Definition of SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
BT_TXD	163	DO	Can be multiplexed into SPI_MOSI.	1.8V power domain
BT_CTS	164	DO	Can be multiplexed into SPI_CLK.	
BT_RXD	165	DI	Can be multiplexed into SPI_MISO.	
BT_RTS	166	DI	Can be multiplexed into SPI_CS.	

The following figure shows the timing relationship of SPI interface.

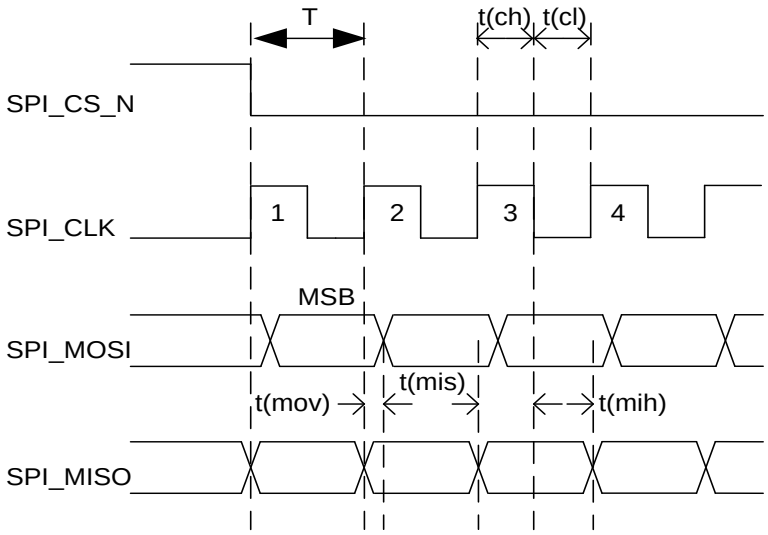


Figure 23: Timing of SPI Interface

The related parameters of SPI timing are shown in the following table.

Table 17: Parameters of SPI Interface Timing

Parameter	Description	Min.	Typ.	Max.	Unit
T	SPI clock period	20.0	-	-	ns
t(ch)	SPI clock high level time	9.0	-	-	ns
t(cl)	SPI clock low level time	9.0	-	-	ns
t(mov)	SPI master data output valid time	-5.0	-	5.0	ns
t(mis)	SPI master data input setup time	5.0	-	-	ns
t(mih)	SPI master data input hold time	1.0	-	-	ns

3.13. PCM and I2C Interfaces

EG12 supports audio communication via Pulse Code Modulation (PCM) digital interface and I2C interfaces. The PCM interface supports the following modes:

- Primary mode (short frame synchronization, works as both master and slave)
- Auxiliary mode (long frame synchronization, works as master only)

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, PCM interface supports 256kHz, 512kHz, 1024kHz or 2048kHz PCM_CLK at 8kHz PCM_SYNC, and also supports 4096kHz PCM_CLK at 16kHz PCM_SYNC.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, PCM interface operates with a 256kHz PCM_CLK and an 8kHz, 50% duty cycle PCM_SYNC only.

EG12 supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8kHz PCM_SYNC and 2048kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8kHz PCM_SYNC and 256kHz PCM_CLK.

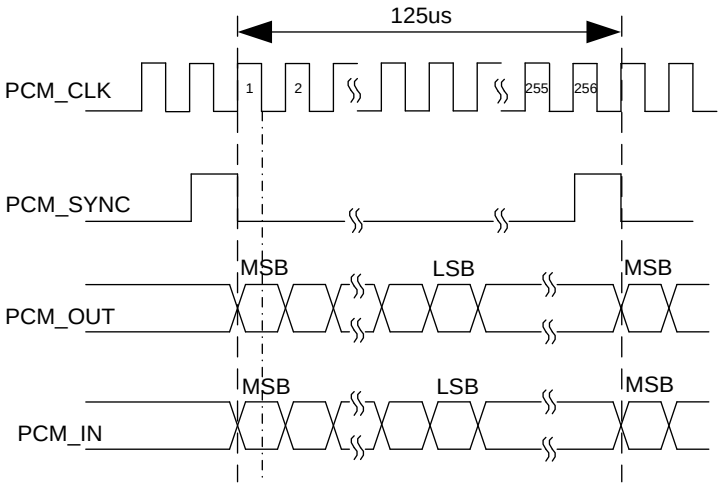


Figure 24: Primary Mode Timing

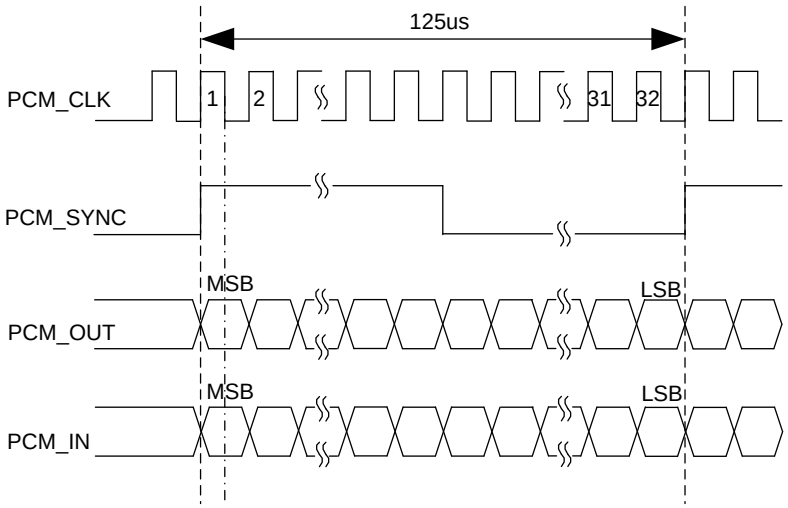


Figure 25: Auxiliary Mode Timing

The following table shows the pin definition of PCM interface and I2C interface, both of which can be applied on audio codec design.

Table 18: Pin Definition of PCM interface and I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_IN	66	DI	PCM data input	1.8V power domain. If unused, keep it open.
PCM_OUT	68	DO	PCM data output	1.8V power domain. If unused, keep it open.
PCM_SYNC	65	IO	PCM data frame synchronization signal	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_CLK	67	IO	PCM data clock	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
I2C_SDA	42	OD	I2C serial data	An external pull-up resistor is required. If unused, keep it open.
I2C_SCL	43	OD	I2C serial clock	An external pull-up resistor is required. If unused, keep it open.
I2S_MCLK	152	DO	Clock output	Provide a digital clock output for an external audio codec. If unused, keep it open.

Clock and mode can be configured by AT command, and the default configuration is master mode using short frame synchronization format with 2048kHz PCM_CLK and 8kHz PCM_SYNC. Please refer to ***document [2]*** for details about **AT+QDAI** command.

The following figure shows a reference design of PCM interface with an external codec IC.

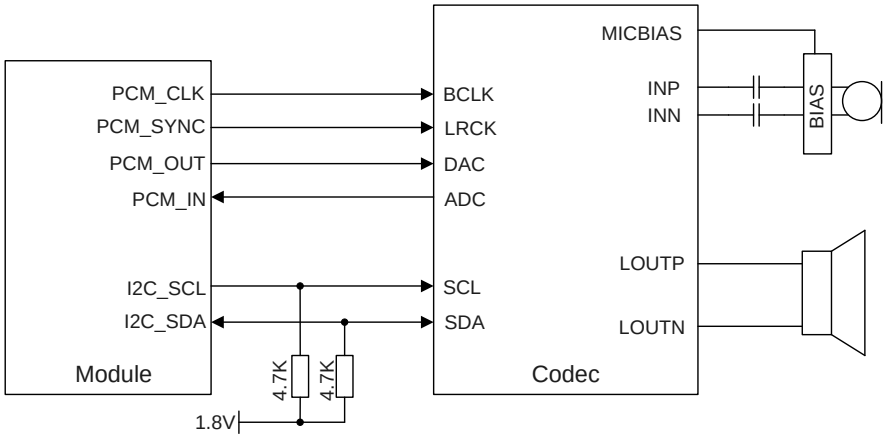


Figure 26: Reference Circuit of PCM Application with Audio Codec

NOTES

1. It is recommended to reserve an RC (R=22Ω, C=22pF) circuit on the PCM lines, especially for PCM_CLK.
2. EG12 works as a master device pertaining to I2C interface.

3.14. ADC Interfaces

The module provides two Analog-to-Digital Converters (ADC) interfaces. **AT+QADC=0** command can be executed to read the voltage value on ADC0. **AT+QADC=1** command can be executed to read the voltage value on ADC1 pin. For more details about these **AT+QADC** commands, please refer to ***document [2]***.

In order to improve the accuracy of ADC, the trace of ADC should be surrounded by ground.

Table 19: Pin Definition of the ADC Interfaces

Pin Name	Pin No.	Description
ADC0	173	General purpose analog to digital converter interface. If unused, keep it open.
ADC1	175	General purpose analog to digital converter interface If unused, keep it open.

The following table describes characteristics of ADC interfaces.

Table 20: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0		1.875	V
ADC1 Voltage Range	0		1.875	V
ADC Resolution		15		bits

NOTES

1. The input voltage of ADC should not exceed 1.875V.
2. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application.

3.15. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The following tables describe pin definition and logic level changes in different network status.

Table 21: Pin Definition of Network Connection Status/Activity Indicator

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	147	DO	Indicate the module's network registration mode.	1.8V power domain If unused, keep it open.
NET_STATUS	170	DO	Indicate the module's network activity status.	1.8V power domain If unused, keep it open.

Table 22: Working State of the Network Connection Status/Activity Indicator

Pin Name	Status	Description
NET_MODE	Always High	Registered on network
	Always Low	Others
NET_STATUS	Flicker slowly (200ms High/1800ms Low)	Network searching
	Flicker slowly (1800ms High/200ms Low)	Idle

	Flicker quickly (125ms High/125ms Low)	Data transfer ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

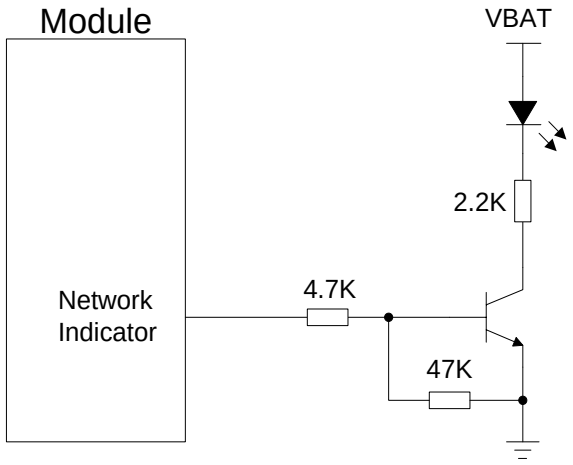


Figure 27: Reference Circuit of the Network Indicator

3.16. STATUS

The STATUS pin is set as the module status indicator. It outputs high level voltage when the module is turned on.

The following table describes pin definition of STATUS.

Table 23: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	171	DO	Indicate the module's operation status	1.8V power domain If unused, keep it open.

A reference circuit is shown as below.

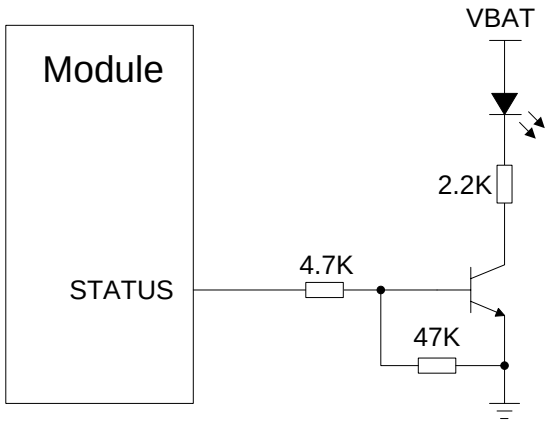


Figure 28: Reference Circuits of STATUS

3.17. Behavior of the RI

AT+QCFG="risignaltype","physical" command can be executed to configure RI behavior.

No matter on which port a URC is presented, the URC will trigger the behavior of RI pin.

NOTE

The URC can be output from UART port, USB AT port and USB modem port by executing **AT+QURCCFG** command. The default port is USB AT port.

In addition, RI behavior can be configured flexibly. The default behavior of the RI is shown as below.

Table 24: Behavior of the RI

State	Response
Idle	RI keeps at high level
URC	RI outputs 120ms low pulse when a new URC returns

The RI behavior can be changed by executing **AT+QCFG="urc/ri/ring"** command. Please refer to ***document [2]*** for more details.

3.18. PCIe Interface*

EG12 provides one integrated PCIe (Peripheral Component Interconnect Express) interface which complies with the PCI Express Specification, Revision 2.1 and supports 5Gbps per lane. The PCIe interface of EG12 is only used for data transmission.

- PCI Express Specification Revision 2.1 compliance
- Data rate at 5Gbps per lane
- Can be used to connect to an external Ethernet IC (MAC and PHY) or WLAN IC

The following table shows the pin definition of PCIe interface.

Table 25: Pin Definition of the PCIe Interface

Pin Name	Pin No.	I/O	Description	Comment
PCIE_REF CLK_P	179	AI/ AO	Input/Output PCIe reference clock - plus	If unused, keep it open.
PCIE_REF CLK_M	180	AI/ AO	Input/Output PCIe reference clock - minus	If unused, keep it open.
PCIE_TX_M	182	AO	PCIe transmit - minus	If unused, keep it open.
PCIE_TX_P	183	AO	PCIe transmit - plus	If unused, keep it open.
PCIE_RX_M	185	AI	PCIe receive - minus	If unused, keep it open.
PCIE_RX_P	186	AI	PCIe receive - plus	If unused, keep it open.
PCIE_CLK_ REQ_N	188	IO	PCIe clock request	In master mode, it is an input signal. In slave mode, it is an output signal. If unused, keep it open.
PCIE_RST_N	189	IO	PCIe reset	In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCIE_WAKE _N	190	IO	PCIe wake	In master mode, it is an input signal. In slave mode, it is an output signal. If unused, keep it open.

EG12 supports either Root Complex (RC) or Endpoint (EP) Mode through software configuration.

3.18.1. Root Complex Mode

In this mode, the module is configured to act as a PCIe RC device. The following figure shows a reference circuit of PCIe RC mode.

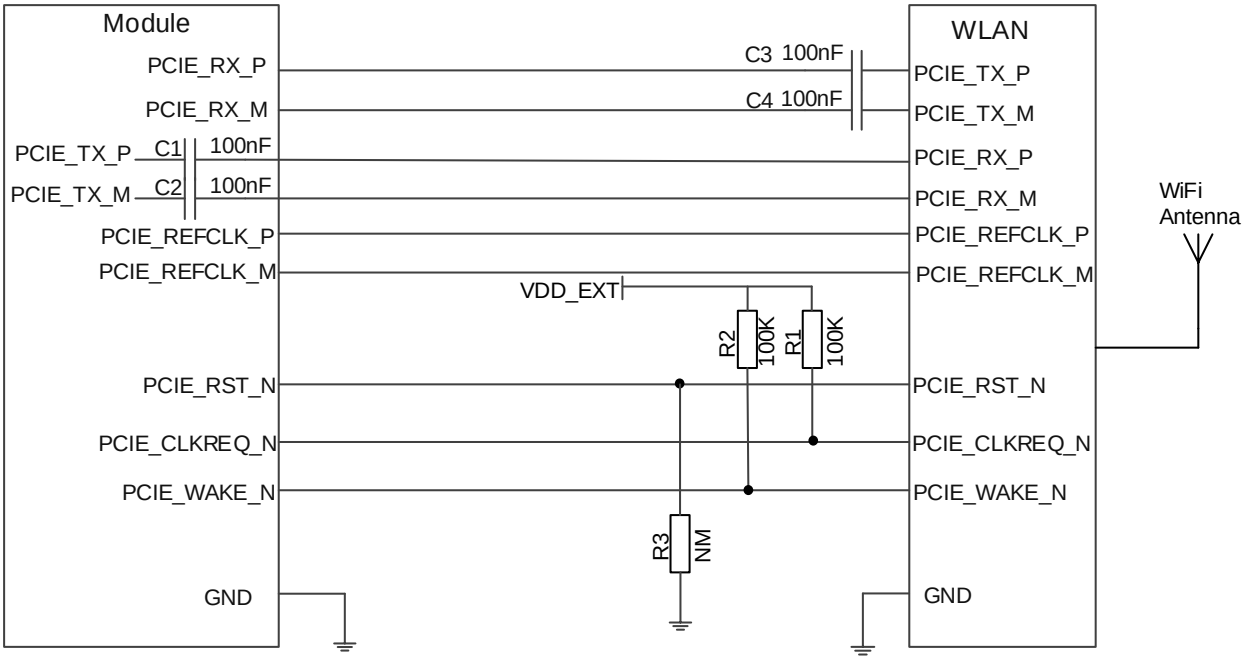


Figure 29: PCIe Interface Reference Circuit (RC Mode)

3.18.2. Endpoint Mode

In this mode, the module is configured to act as a PCIe EP device. The following figure shows a reference circuit of PCIe EP mode.

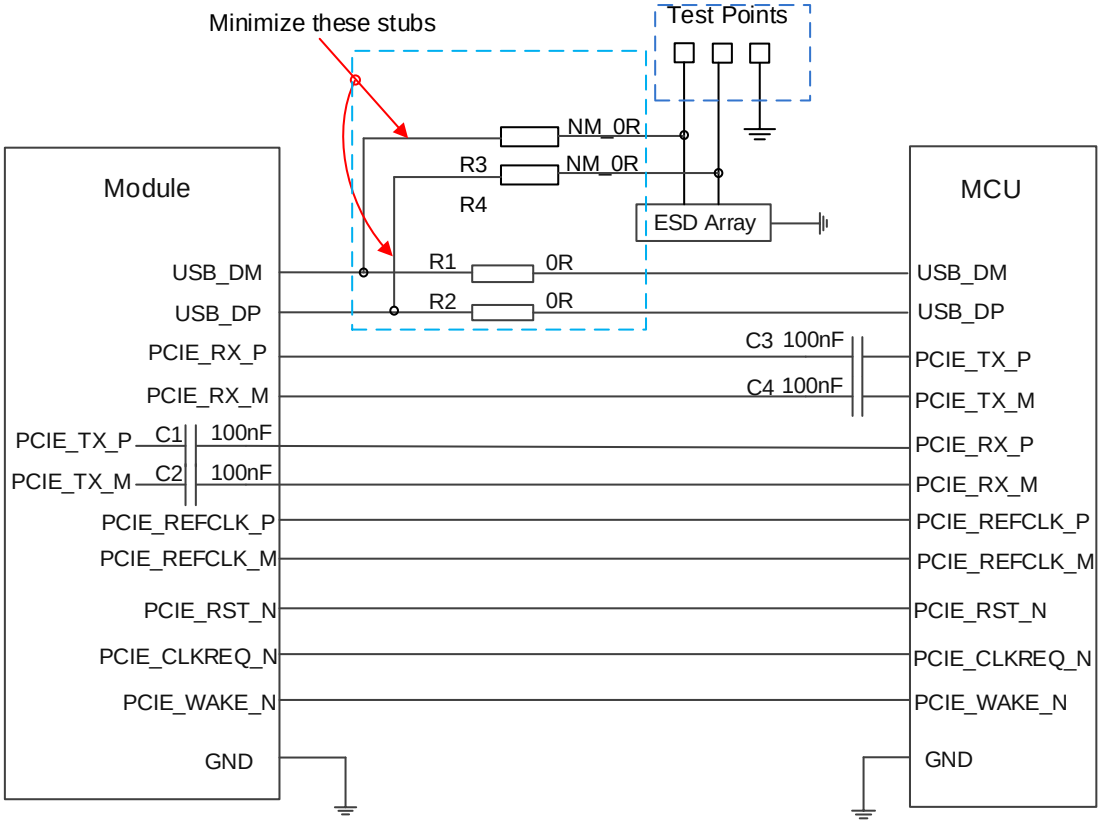


Figure 30: PCIe Interface Reference Circuit (EP Mode)

In order to ensure the signal integrity of PCIe interface, C1 and C2 have been placed inside the module. C3 and C4 should be placed close to the MCU, and R1, R2, R3 and R4 should be placed close to the module and also close to each other. The extra stubs of trace must be as short as possible.

The following principles of PCIe interface design should be complied with, so as to meet PCIe V2.1 specifications.

- It is important to route the USB 2.0 & PCIe signal traces as differential pairs with total grounding.
- For USB 2.0 signal traces, the trace lengths should be less than 120mm, the differential data pair matching should be less than 2mm (15ps).
- For PCIe signal traces, the maximum length of each differential data pair (TX/RX) is recommended to be less than 250mm, and each differential data pair matching should be less than 0.7mm (5ps).
- Do not route signal traces under crystals, oscillators, magnetic devices or RF signal traces. It is important to route the PCIe differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- If possible, reserve a 0Ω resistor on USB_DP and USB_DM lines, respectively.

NOTES

1. USB is required because PCIe does not support features such as firmware upgrade, GNSS NMEA output and software debugging. Firmware upgrade must be over USB2.0, while GNSS NMEA output

and software debugging can be over USB2.0/3.0 (USB2.0 is recommended).
2. "*" means under development.

3.19. SDIO Interface*

EG12 provides one SDIO interface which supports SD 3.0 protocol and eMMC*. The following table shows the pin definition.

Table 26: Pin Definition of SDIO Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_VDD	46	PO	**SD card application**: SDIO pull up power source **eMMC application**: Keep it open when used for eMMC	1.8V/3.0V configurable output. Cannot be used for SD card power supply.
SD_DATA3	48	IO	SDIO data signal (bit 3)	If unused, keep it open.
SD_DATA2	47	IO	SDIO data signal (bit 2)	If unused, keep it open.
SD_DATA1	50	IO	SDIO data signal (bit 1)	If unused, keep it open.
SD_DATA0	49	IO	SDIO data signal (bit 0)	If unused, keep it open.
SD_CMD	51	IO	SDIO command signal	If unused, keep it open.
SD_DET	52	DI	SD card insertion detection	1.8V power domain. If unused, keep it open.
SD_CLK	53	DO	SDIO clock signal	If unused, keep it open.

The following figure shows an SDIO interface reference design.

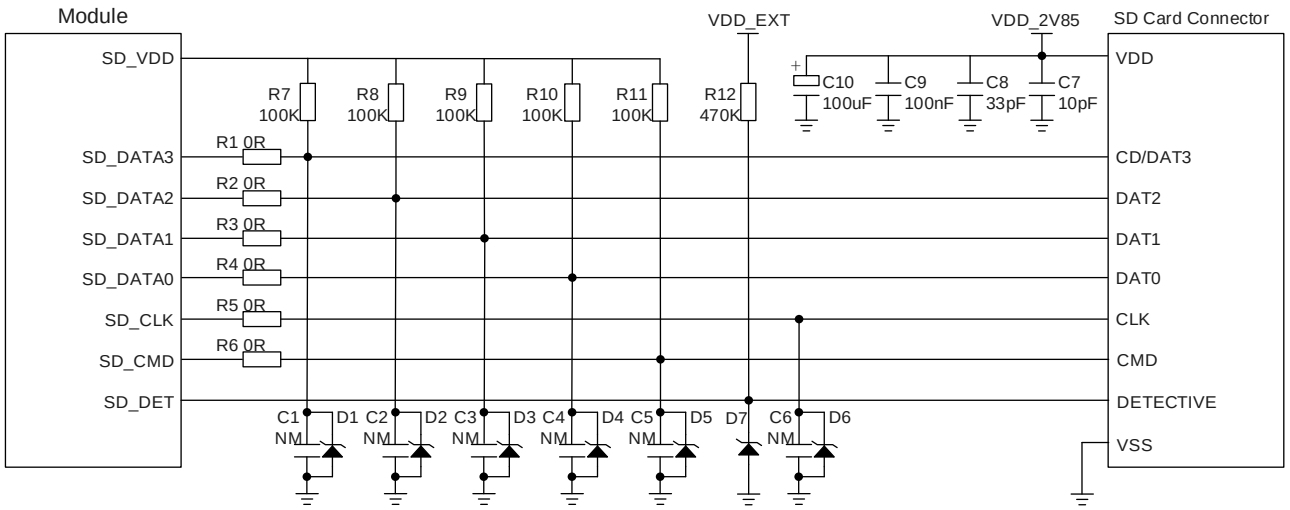


Figure 31: Reference Circuit of SD Card Application

Please follow the principles below in the SD card circuit design:

- The voltage range of SD power supply is 2.7V~3.6V and a sufficient current up to 0.8A should be provided. As the maximum output current of SD_VDD is 50mA which can only be used for SDIO pull-up resistors, an external power supply is needed for SD card.
- To avoid jitter of bus, resistors R7~R11 are needed to pull up the SDIO to SD_VDD. Value of these resistors is among 10kΩ~100kΩ and the recommended value is 100kΩ.
- In order to improve signal quality, it is recommended to add 0Ω resistors R1~R6 in series between the module and the SD card. The bypass capacitors C1~C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- In order to offer good ESD protection, it is recommended to add a TVS diode on SD card pins.
- The load capacitance of SDIO bus needs to be less than 40pF.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50Ω (±10%).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, and analog signals, as well as noisy signals such as clock signals, and DCDC signals.
- It is recommended to keep the trace length difference between CLK and DATA/CMD less than 1mm and the total routing length less than 50mm. The total trace length inside the module is 36mm, so the exterior total trace length should be less than 14mm.
- Make sure the adjacent trace spacing is two times of the trace width and the load capacitance of SDIO bus should be less than 40pF.

3.20. RFFE Interface*

RFFE signals are used for external tuner control and should be routed to an appropriate antenna control circuitry.

Table 27: Pin Definition of RFFE Interface

Pin Name	Pin No.	I/O	Description	Comment
RFFE_CLK	71	DO	RFFE serial interface used for external tuner control.	If unused, keep it open.
RFFE_DATA	73	IO		If unused, keep it open.
VDD_RF	162	PO	Provide 2.85V for external RF circuit.	If unused, keep it open.

NOTE

"*" means under development.

3.21. USB_BOOT Interface

EG12 provides a USB_BOOT pin. Developers can pull up USB_BOOT to VDD_EXT before powering on the module, thus the module will enter into emergency download mode when powered on. In this mode, the module supports firmware upgrade over USB interface.

Table 28: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	140	DI	Force the module to enter into emergency download mode	1.8V power domain. Active high. If unused, keep it open.

The following figure shows a reference circuit of USB_BOOT interface.

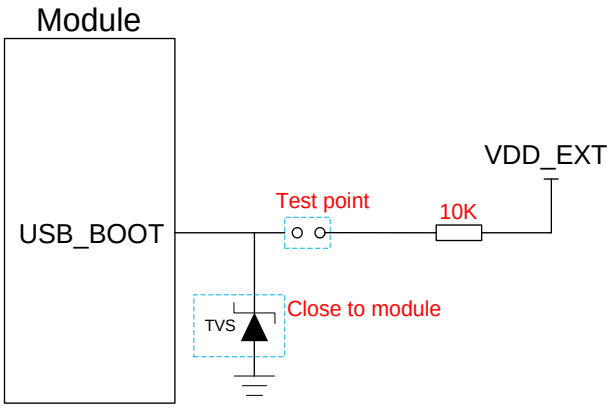


Figure 32: Reference Circuit of USB_BOOT Interface

3.22. GPIOs

The module provides 5 GPIOs for customers' design.

Table 29: Pin Definition of GPIOs

Pin Name	Pin No.	I/O	Description	Comment
GPIO_1	138	IO	General purpose input/output port	If unused, keep it open.
GPIO_2	139	IO		If unused, keep it open.
GPIO_3	159	IO		If unused, keep it open.
GPIO_4	161	IO		If unused, keep it open.
GPIO_5	172	IO		If unused, keep it open.

4 GNSS Receiver

4.1. General Description

EG12 includes a fully integrated global navigation satellite system solution that supports Gen9HT-Lite of Qualcomm (GPS, GLONASS, BeiDou, Galileo and QZSS).

EG12 supports standard NMEA-0183 protocol, and outputs NMEA sentences at 1Hz data update rate via USB interface by default.

By default, EG12 GNSS engine is switched off. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, please refer to ***document [3]***.

4.2. GNSS Performance

The following table shows GNSS performance of EG12.

Table 30: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-147	dBm
	Reacquisition	Autonomous	-159	dBm
	Tracking	Autonomous	-159	dBm
TTFF (GNSS)	Cold start @open sky	Autonomous	35	s
		XTRA enabled	18	s
	Warm start @open sky	Autonomous	30	s
		XTRA enabled	2.5	s

	Hot start @open sky	Autonomous	3	s
		XTRA enabled	2	s
Accuracy (GNSS)	CEP-50	Autonomous @open sky	1.5	m

4.3. Layout Guidelines

The following layout guidelines should be taken into account in customers' design.

- Maximize the distance among GNSS antenna, main antenna and Rx-diversity antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module, display connector and SD card should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep the characteristic impedance for ANT_GNSS trace as 50Ω.

Please refer to ***Chapter 5*** for GNSS reference design and antenna installation information.

5 Antenna Interfaces

EG12 provides a main antenna interface, an Rx-diversity antenna interface, two MIMO antenna interfaces, and a GNSS antenna interface. The impedance of antenna ports is 50Ω.

5.1. Main/Rx-diversity/MIMO Antenna Interfaces

5.1.1. Pin Definition

The pin definition of main antenna interface, Rx-diversity and MIMO antenna interfaces are shown as below.

Table 31: Pin Definition of the Main/Rx-diversity/MIMO Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	107	IO	Main antenna interface	50Ω impedance
ANT_DIV	127	AI	RXD antenna interface	50Ω impedance
ANT_MIMO1	101	AI	4x4 MIMO antenna interface	50Ω impedance
ANT_MIMO2	113	AI	4x4 MIMO antenna interface	50Ω impedance

5.1.2. Operating Frequency

Table 32: EG12-GT Operating Frequencies

3GPP Band	Transmit	Receive	Unit
LTE B42	3400~3600	3400~3600	MHz
LTE B43	3600~3800	3600~3800	MHz
LTE B48	3550~3700	3550~3700	MHz

Table 33: EG12-EA Operating Frequencies

3GPP Band	Transmit	Receive	Unit
WCDMA B1	1920~1980	2110~2170	MHz
WCDMA B3	1710~1785	1805~1880	MHz
WCDMA B5	824~849	869~894	MHz
WCDMA B8	880~915	925~960	MHz
LTE B1	1920~1979.9	2110~2169.9	MHz
LTE B3	1710~1784.9	1805~1879.9	MHz
LTE B5	824~848.9	869~893.9	MHz
LTE B7	2500~2569.9	2620~2689.9	MHz
LTE B8	880~914.9	925~959.9	MHz
LTE B20	832~861.9	791~820.9	MHz
LTE B28	703~747.9	758~802.9	MHz
LTE B38	2570~2619.9	2570~2619.9	MHz
LTE B40	2300~2399.9	2300~2399.9	MHz
LTE B41	2496~2689.9	2496~2689.9	MHz

Table 34: EG12-NA* Operating Frequencies

3GPP Band	Transmit	Receive	Unit
WCDMA B2	1850~1910	1930~1990	MHz
WCDMA B4	1710~1755	2110~2155	MHz
WCDMA B5	824~849	869~894	MHz
LTE B2	1850~1910	1930~1990	MHz
LTE B4	1710~1755	2110~2155	MHz
LTE B5	824~849	869~894	MHz
LTE B7	2500~2570	2620~2690	MHz

LTE B12	699~716	729~746	MHz
LTE B13	777~787	746~756	MHz
LTE B14	788~798	758~768	MHz
LTE B17	704~716	734~746	MHz
LTE B25	1850~1915	1930~1995	MHz
LTE B26	814~849	859~894	MHz
LTE B29	-	717~728	MHz
LTE B30	2305~2315	2350~2360	MHz
LTE B66	1710~1780	2110~2200	MHz
LTE B71	617~652	663~698	MHz

5.1.3. Reference Design of RF Antenna Interfaces

A reference design of ANT_MAIN, ANT_DIV, ANT_MIMO1 and ANT_MIMO2 interfaces is shown as below. It should reserve a π-type matching circuit for better RF performance. The π-type matching components (R1/C1/C2, R2/C3/C4, R3/C5/C6, R4/C7/C8) should be placed as close to the antennas as possible and are mounted according to the actual debugging. C1~C8 are not mounted and a 0Ω resistor is mounted on R1~R4 respectively by default.

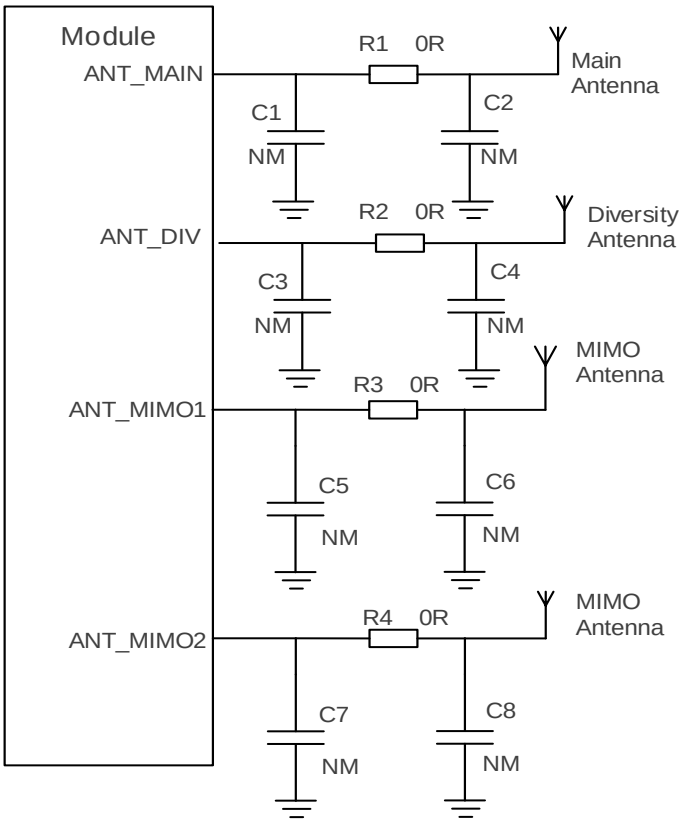


Figure 33: Reference Circuit of RF Antenna Interfaces

NOTE

Keep a proper distance between the main antenna and the Rx-diversity antenna to improve the receiving sensitivity.

5.2. GNSS Antenna Interface

5.2.1. Pin Definition

The following tables show pin definition and frequency specification of GNSS antenna interface.

Table 35: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	119	AI	GNSS antenna interface	50Ω impedance

5.2.2. GNSS Frequency

Table 36: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42±1.023	MHz
GLONASS	1597.5~1605.8	MHz
Galileo	1575.42±2.046	MHz
BeiDou	1561.098±2.046	MHz
QZSS	1575.42	MHz

5.2.3. Reference Design of GNSS Antenna Interface

A reference design of GNSS antenna is shown as below.

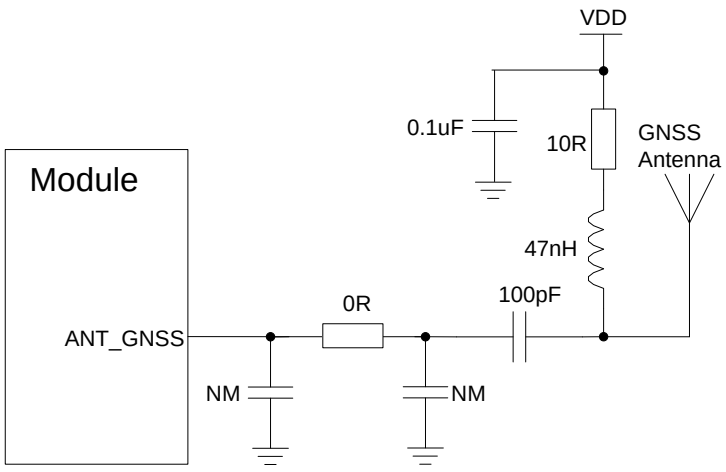


Figure 34: Reference Circuit of GNSS Antenna Interface

NOTES

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

5.3. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, height from the reference ground to the signal layer (H), and the clearance between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

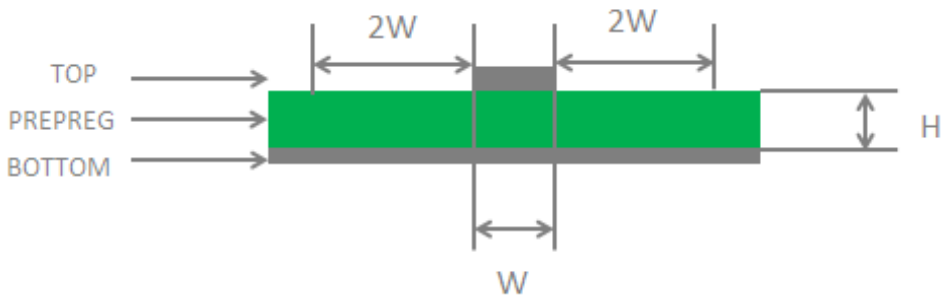


Figure 35: Microstrip Design on a 2-layer PCB

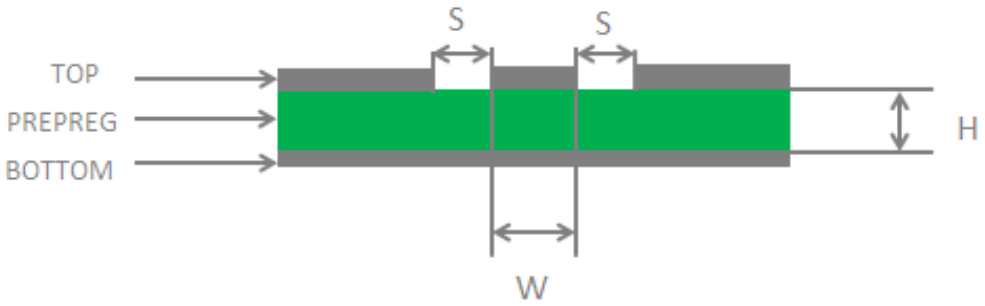


Figure 36: Coplanar Waveguide Design on a 2-layer PCB

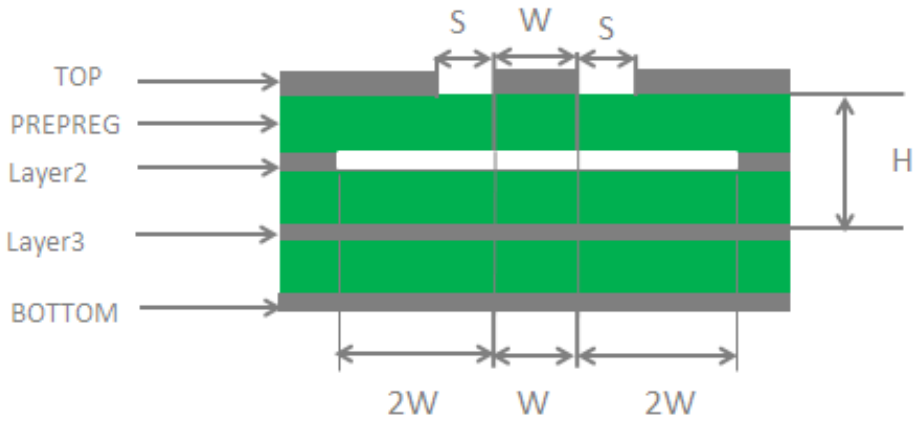


Figure 37: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

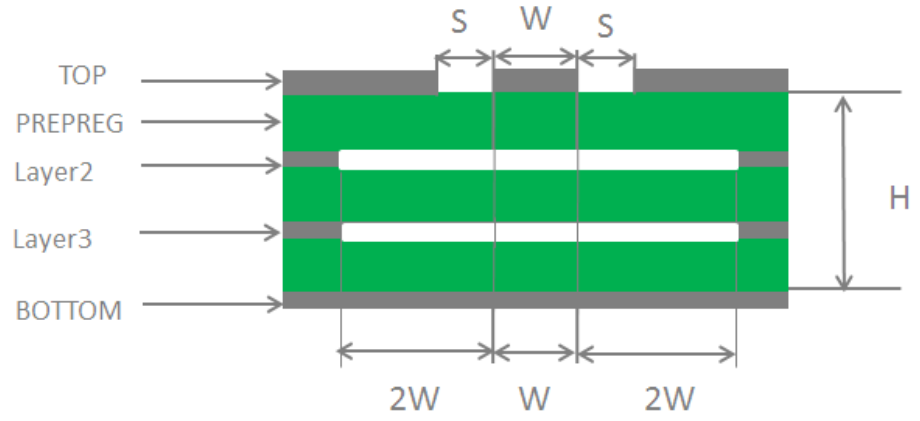


Figure 38: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times as wide as RF signal traces (2*W).

For more details about RF layout, please refer to ***document [6]***.

5.4. Antenna Installation

5.4.1. Antenna Requirements

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

Table 37: Antenna Requirements

Type	Requirements
GNSS [1)]	Frequency range: 1559MHz~1609 MHz Polarization: RHCP or linear VSWR: <2 (Typ.) Passive antenna gain: >0dBi Active antenna noise figure: <1.5dB Active antenna gain: >0dBi Active antenna embedded LNA gain: <17dB
WCDMA/LTE	VSWR: ≤ 2 Efficiency: >30% Max Input Power: 50W Input Impedance: 50Ω Cable Insertion Loss: <1dB (WCDMA B5/B8/, LTE B5/B8/B12/B13/B14/B17/B20/B26/B28/B29/B71) Cable Insertion Loss: <1.5dB (WCDMA B1/B2/B3/B4/, LTE B1/B2/B3/B4/B25/B66) Cable Insertion Loss <2dB (LTE B7/B38/B40/B41/B30/B42/B43/B48)

NOTE

[1)] It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.4.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by *Hirose*.

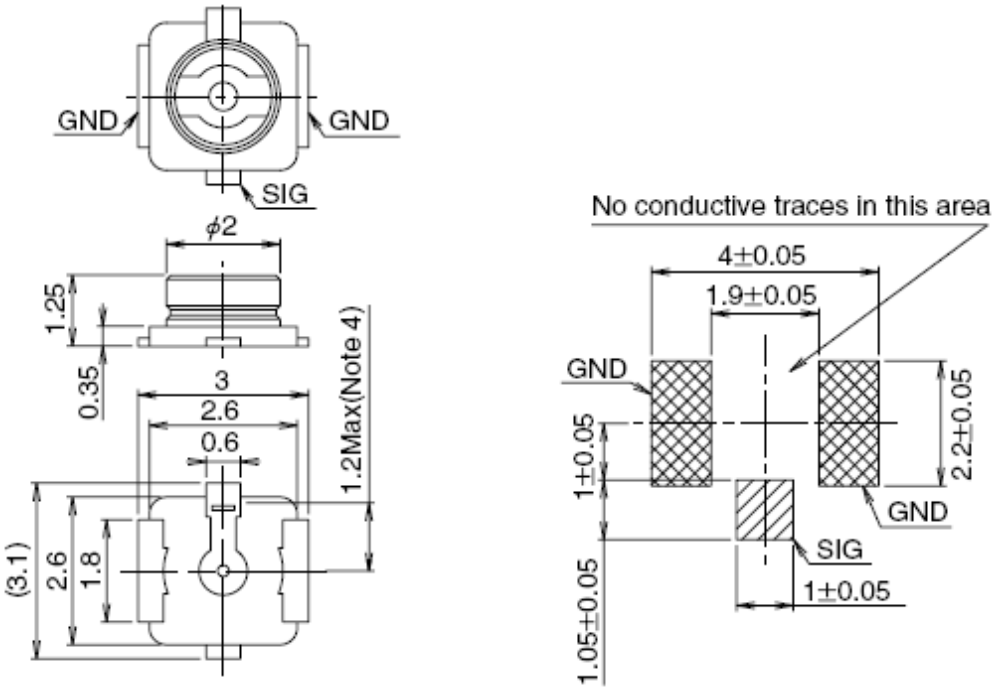


Figure 39: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connector listed in the following figure can be used to match the U.FL-R-SMT.

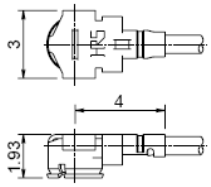
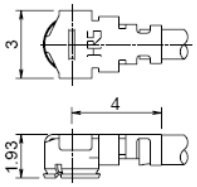
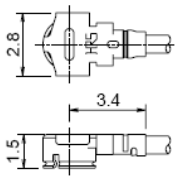
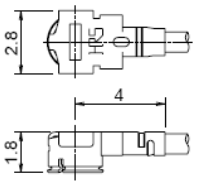
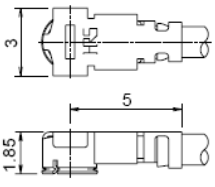
	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
Part No.					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 40: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mating plugs.

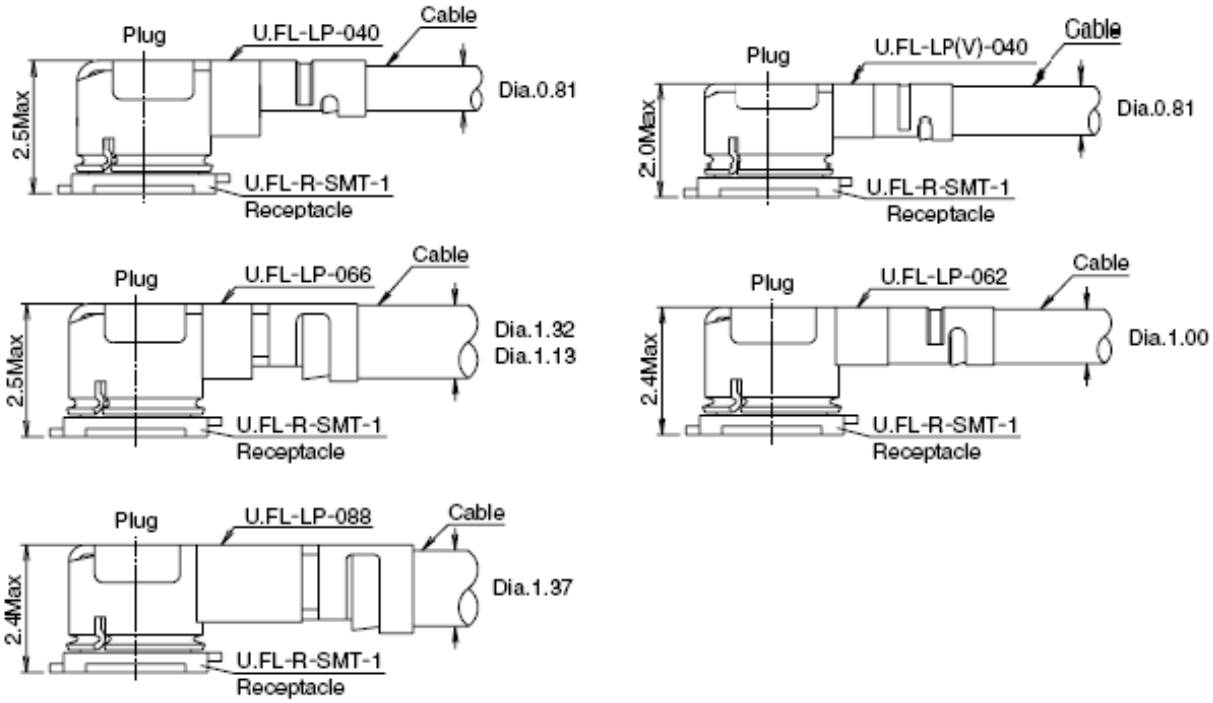


Figure 41: Space Factor of Mating Plugs (Unit: mm)

For more details, please visit http://www.hirose.com.

6 Electrical, Reliability and Radio Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 38: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	1.0	A
Peak Current of VBAT_RF	0	1.5	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	1.875	V
Voltage at ADC1	0	1.875	V

6.2. Power Supply Ratings

Table 39: The Module's Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the	3.3	3.8	4.3	V

		minimum and maximum values.				
USB_VBUS	USB connection detection		3.3	5.0	5.25	V

6.3. Operation and Storage Temperatures

The operation and storage temperatures are listed in the following table.

Table 40: Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range [1)]	-35	+25	+75	ºC
Extended Operation Range [2)]	-40		+85	ºC
Storage temperature range	-40		+90	ºC

NOTES

1. [1)] Within operating temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, proper mounting, heating sinks and active cooling may be required to make certain functions of the module such as voice, SMS, data transmission, emergency call to be realized. Only one or more parameters like Pout might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operating temperature levels, the module will meet 3GPP specifications again.

6.4. Current Consumption

6.4.1. EG12-GT Current Consumption

Table 41: EG12-GT Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	20	uA
I_{VBAT}	Sleep state	**AT+CFUN=0** (USB disconnected)	0.98	mA

		LTE-TDD PF=32 (USB disconnected)	2.54	mA
		LTE-TDD PF=64 (USB disconnected)	1.79	mA
		LTE-TDD PF=128 (USB disconnected)	1.41	mA
		LTE-TDD PF=256 (USB disconnected)	1.13	mA
		LTE-TDD PF=64 (USB Suspend)	2.10	mA
I_{VBAT}	Idle state	LTE-TDD PF=64 (USB disconnected)	9.41	mA
		LTE-TDD PF=64 (USB active)	24.65	mA
I_{VBAT}	LTE data transfer (GNSS OFF)	LTE-TDD B42 CH42590 @22.5dBm	350	mA
		LTE-TDD B43 CH44590 @22.5dBm	320	mA
		LTE-TDD B48 CH55990 @22.5dBm	320	mA
I_{VBAT}	2×CA data transfer	LTE-TDD B42+B42 @22.5dBm	320	mA
		LTE-TDD B48+B48 @22.5dBm	320	mA
I_{VBAT}	3×CA data transfer	LTE-TDD B42+B42+B42 @23.5dBm	400	mA
		LTE-TDD B48+B48+B48 @22.5dBm	420	mA

6.4.2. EG12-EA Current Consumption

Table 42: EG12-EA Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	20	uA
I_{VBAT}	Sleep state	**AT+CFUN=0** (USB disconnected)	0.98	mA
		WCDMA PF=64 (USB disconnected)	2.51	mA
		WCDMA PF=128 (USB disconnected)	1.94	mA
		WCDMA PF=256 (USB disconnected)	1.62	mA
		WCDMA PF=512 (USB disconnected)	1.49	mA
		LTE-FDD PF=32 (USB disconnected)	4.32	mA
		LTE-FDD PF=64 (USB disconnected)	2.74	mA

		LTE-FDD PF=128 (USB disconnected)	2.11	mA
		LTE-FDD PF=256 (USB disconnected)	1.72	mA
		LTE-TDD PF=32 (USB disconnected)	4.39	mA
		LTE-TDD PF=64 (USB disconnected)	2.87	mA
		LTE-TDD PF=128 (USB disconnected)	2.21	mA
		LTE-TDD PF=256 (USB disconnected)	1.78	mA
		WCDMA PF=64 (USB Suspend)	2.74	mA
		LTE-FDD PF=64 (USB Suspend)	2.83	mA
		LTE-TDD PF=64 (USB Suspend)	2.96	mA
I_{VBAT}	Idle state	WCDMA PF=64 (USB disconnected)	9.23	mA
		WCDMA PF=64 (USB active)	24.41	mA
		LTE-FDD PF=64 (USB disconnected)	8.91	mA
		LTE-FDD PF=64 (USB active)	24.82	mA
		LTE-TDD PF=64 (USB disconnected)	9.13	mA
		LTE-TDD PF=64 (USB active)	24.97	mA
I_{VBAT}	WCDMA data transfer (GNSS OFF)	WCDMA B1 HSDPA CH10700 @22.93dBm	481	mA
		WCDMA B1 HSUPA CH10700 @23.04dBm	477	mA
		WCDMA B3 HSDPA CH1338 @22.9dBm	524	mA
		WCDMA B3 HSUPA CH1338 @22.87dBm	540	mA
		WCDMA B5 HSDPA CH4407 @23.19dBm	575	mA
		WCDMA B5 HSUPA CH4407 @23.16dBm	573	mA
		WCDMA B8 HSDPA CH3012 @23.25dBm	576	mA
		WCDMA B8 HSUPA CH3012 @22.99dBm	577	mA
I_{VBAT}	LTE data transfer (GNSS OFF)	LTE-FDD B1 CH300 @22.85dBm	571	mA
		LTE-FDD B3 CH1575 @22.67dBm	554	mA
		LTE-FDD B5 CH2525 @22.91dBm	561	mA
		LTE-FDD B7 CH3100 @22.82dBm	821	mA

		LTE-FDD B8 CH3625 @22.75dBm	583	mA
		LTE-FDD B20 CH6300 @22.6dBm	577	mA
		LTE-FDD B28 CH9435 @22.92dBm	576	mA
		LTE-TDD B38 CH38000 @22.58dBm	356	mA
		LTE-TDD B40 CH39150 @23.09dBm	353	mA
		LTE-TDD B41 CH40620 @22.79dBm	380	mA
I_{VBAT}	2xCA data transfer	LTE-FDD+FDD B1+B1 @23.3dBm	627	mA
		LTE-FDD+FDD B1+ B3 @23.4dBm	565	mA
		LTE-FDD+FDD B1+ B5 @23.05dBm	556	mA
		LTE-FDD+FDD B1+ B7 @23.01dBm	570	mA
		LTE-FDD+FDD B1+ B8 @23.13dBm	558	mA
		LTE-FDD+FDD B1+ B20 @23.07dBm	556	mA
		LTE-FDD+FDD B1+ B28 @22.9dBm	568	mA
		LTE-FDD+TDD B1+ B38 @22.95dBm	562	mA
		LTE-FDD+TDD B1+ B40 @22.95dBm	562	mA
		LTE-FDD+TDD B1+ B41 @23.08dBm	560	mA
		LTE-FDD+FDD B3+ B3 @22.54dBm	593	mA
		LTE-FDD+FDD B3+ B5 @23.05dBm	580	mA
		LTE-FDD+FDD B3+ B7 @22.92dBm	597	mA
		LTE-FDD+FDD B3+ B8 @22.96dBm	582	mA
		LTE-FDD+FDD B3+ B20 @22.95dBm	595	mA
		LTE-FDD+FDD B3+ B28 @22.95dBm	594	mA
		LTE-FDD+TDD B3+ B38 @22.91dBm	594	mA
		LTE-FDD+TDD B3+ B40 @22.97dBm	593	mA
		LTE-FDD+TDD B3+ B41 @22.81dBm	593	mA
		LTE-FDD+FDD B7+ B5 @23.2dBm	796	mA
		LTE-FDD+FDD B7+ B7 @23.2dBm	925	mA

		LTE-FDD+FDD	B7+ B8 @23.1dBm	796	mA
		LTE-FDD+FDD	B7+ B20 @23.08dBm	805	mA
		LTE-FDD+FDD	B7+ B28 @23.2 dBm	807	mA
		LTE-FDD+TDD	B20+ B38 @23.45dBm	643	mA
		LTE-FDD+TDD	B20+ B40 @23.4dBm	640	mA
		LTE-TDD+TDD	B38+ B38 @23.4dBm	398	mA
		LTE-TDD+TDD	B40+ B40 @23.3dBm	376	mA
		LTE-TDD+TDD	B41+ B41 @23.4dBm	398	mA
I_{VBAT}	3xCA data transfer	LTE-FDD+FDD	B1+ B3+B3 @22.92dBm	629	mA
		LTE-FDD+FDD	B1+ B3+B5 @22.92dBm	647	mA
		LTE-FDD+FDD	B1+ B3+B7 @22.84dBm	653	mA
		LTE-FDD+FDD	B1+ B3+B8 @22.85dBm	647	mA
		LTE-FDD+FDD	B1+ B3+B20 @22.94dBm	653	mA
		LTE-FDD+FDD	B1+ B3+B28 @22.85dBm	655	mA
		LTE-FDD+TDD	B1+ B3+B38 @22.96dBm	644	mA
		LTE-FDD+TDD	B1+ B3+B41 @22.86dBm	645	mA
		LTE-FDD+TDD	B1+ B40+B40 @23.03dBm	482	mA
		LTE-FDD+TDD	B1+ B41+B41 @22.78dBm	612	mA
		LTE-FDD+FDD	B1+ B7+B20 @22.83dBm	655	mA
		LTE-FDD+FDD	B3+ B3+B7 @22.99dBm	736	mA
		LTE-FDD+FDD	B3+ B3+B20 @23.2dBm	774	mA
		LTE-FDD+FDD	B3+ B3+B28 @22.92dBm	552	mA
		LTE-FDD+FDD	B3+ B7+B7 @22.92dBm	398	mA
		LTE-FDD+FDD	B3+ B7+B8 @22.92dBm	398	mA
		LTE-FDD+FDD	B3+ B7+B20 @23.02dBm	789	mA
		LTE-FDD+FDD	B3+ B7+B28 @22.58dBm	771	mA
		LTE-FDD+TDD	B3+ B40+B40 @22.63dBm	693	mA

		LTE-FDD+TDD B3+ B41+B41 @22.7dBm	729	mA
		LTE-FDD+FDD B7+ B7+B20 @22.77dBm	772	mA
		LTE-FDD+FDD B7+ B7+B28 @22.65dBm	775	mA
		LTE-TDD+TDD B40+ B40+B40 @23.01dBm	424	mA
		LTE-TDD+TDD B41+ B41+B41 @22.97dBm	525	mA
I_{VBAT}	WCDMA voice call	WCDMA B1 CH10700 @22.94dBm	475	mA
		WCDMA B3 CH1338 @22.99dBm	524	mA
		WCDMA B5 CH4407 @23.19dBm	562	mA
		WCDMA B8 CH3012 @23.25dBm	577	mA

6.5. RF Output Power

The following table shows the RF output power of EG12.

Table 43: RF Output Power

Frequency	Max.	Min.
WCDMA bands	24dBm+1/-3dB	<-50dBm
LTE FDD bands	23dBm±2dB	<-40dBm
LTE TDD bands	23dBm±2dB	<-40dBm

6.6. RF Receiving Sensitivity

The following tables show conducted RF receiving sensitivity of EG12 series module.

6.6.1. EG12-GT Receiving Sensitivity

Table 44: EG12-GT Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO[1)]	3GPP (SIMO)
LTE-TDD B42	-98.4dBm	-99.2dBm	-102dBm	-95dBm
LTE-TDD B43	-98.5dBm	TBD	-101dBm	-95dBm
LTE-TDD B48	-98.2dBm	-99.1dBm	-104dBm	-95dBm

6.6.2. EG12-EA Receiving Sensitivity

Table 45: EG12-EA Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO [1)]	3GPP (SIMO)
WCDMA B1	-111dBm	-111dBm	\	-106.7dBm
WCDMA B3	-111dBm	-111dBm	\	-103.7dBm
WCDMA B5	-112dBm	-112dBm	\	-104.7dBm
WCDMA B8	-111dBm	-112dBm	\	-103.7dBm
LTE-FDD B1 (10M)	-98.2dBm	-98.7dBm	-101.2dBm	-96.3dBm
LTE-FDD B3 (10M)	-98.7dBm	-98.7dBm	-101.7dBm	-93.3dBm
LTE-FDD B5 (10M)	-99.2dBm	-99.4dBm	-102.7dBm	-94.3dBm
LTE-FDD B7 (10M)	-97.7dBm	-97.7dBm	-100.2dBm	-94.3dBm
LTE-FDD B8 (10M)	-98.2dBm	-98.5dBm	-101.7dBm	-93.3dBm
LTE-FDD B20 (10M)	-98.7dBm	-98.8dBm	-102.2dBm	-93.3dBm
LTE-FDD B28 (10M)	-99.7dBm	-99.7dBm	-102.7dBm	-94.8dBm
LTE-TDD B38 (10M)	-98.2dBm	-98.5dBm	-100.7dBm	-96.3dBm
LTE-TDD B40 (10M)	-98.2dBm	-98.9dBm	-100.7dBm	-96.3dBm
LTE-TDD B41 (10M)	-97.2 dBm	-97.4dBm	-99.7dBm	-94.3dBm

NOTE

[1] SIMO is a smart antenna technology that uses a single antenna at the transmitter side and multiple antennas at the receiver side, which can improve Rx performance.

6.7. Electrostatic Discharge

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is important to refer ESD handling precautions applying ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module's electrostatic discharge characteristics (at temperature of 25°C and relative humidity of 45%).

Table 46: Electrostatic Discharge Characteristics

Tested Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.8. Thermal Consideration

In order to achieve better performance of the module, it is recommended to comply with the following principles for thermal consideration:

- On customers' PCB design, please keep placement of the module away from heating sources, especially high power components such as ARM processor, audio power amplifier, power supply, etc.
- Do not place components on the opposite side of the PCB area where the module is mounted and do not fill that area with copper in order to facilitate adding of heatsink when necessary.
- The reference ground of the area where the module is mounted should be complete, and add ground vias as many as possible for better heat dissipation.
- Make sure the ground pads of the module and PCB are fully connected.
- According to customers' application demands, the heatsink can be mounted on the top of the module,

or the opposite side of the PCB area where the module is mounted, or both of them.

- The heatsink should be designed with as many fins as possible to increase heat dissipation area. Meanwhile, a thermal pad with high thermal conductivity should be used between the heatsink and module/PCB.

The following shows two kinds of heatsink designs for reference and customers can choose one or both of them according to their application structure.

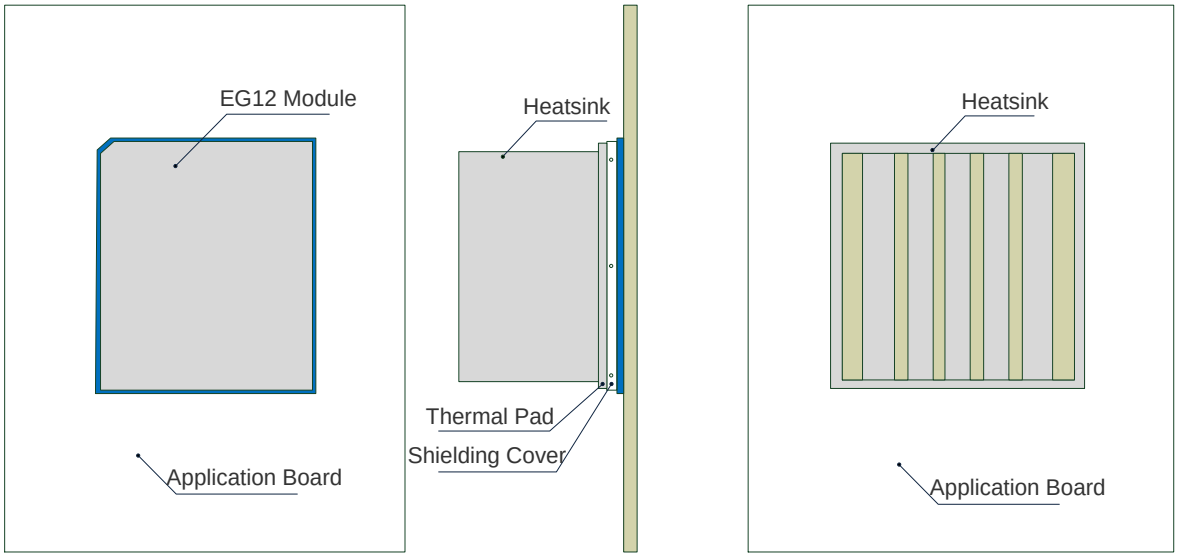


Figure 42: Referenced Heatsink Design (Heatsink at the Top of the Module)

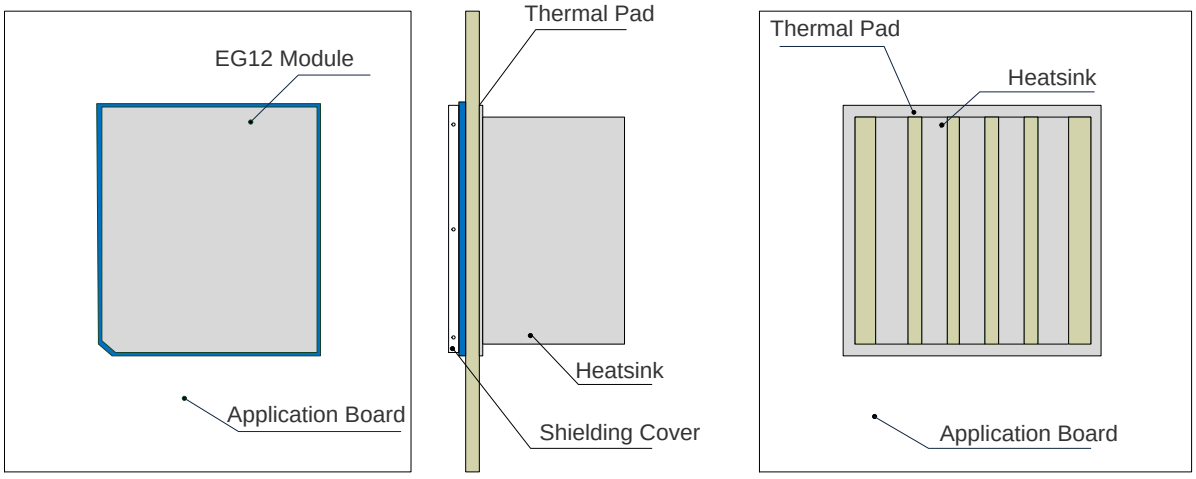


Figure 43: Referenced Heatsink Design (Heatsink at the Backside of Customers' PCB)

NOTES

1. Make sure that customers' PCB design provides sufficient cooling solutions for the module: proper mounting, heatsinks, and active cooling may be required depending on the integrated application.
2. In order to protect the components from damage, the thermal design should be maximally optimized to guarantee that the module's internal temperature always maintains below 105°C. Customers can execute **AT+QTEMP** command to get the module's internal temperature.
3. For more detailed guidelines on thermal design, please refer to ***document [7]***.

7 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm, and the tolerances for dimensions without tolerance values are ±0.05mm.

7.1. Mechanical Dimensions of the Module

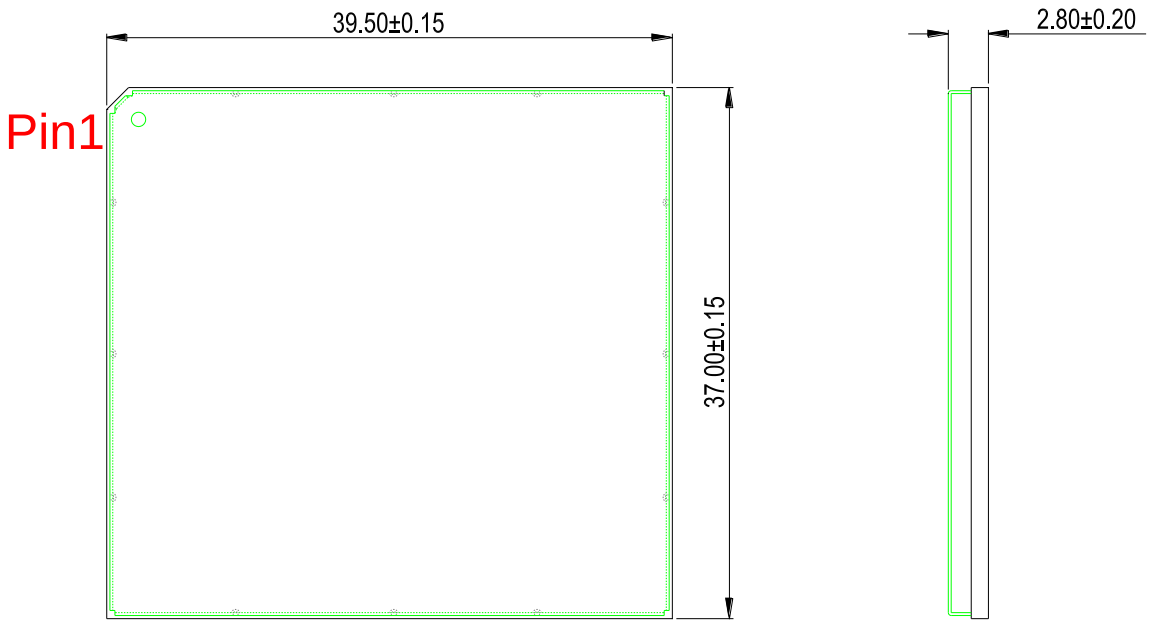


Figure 44: Module Top and Side Dimensions

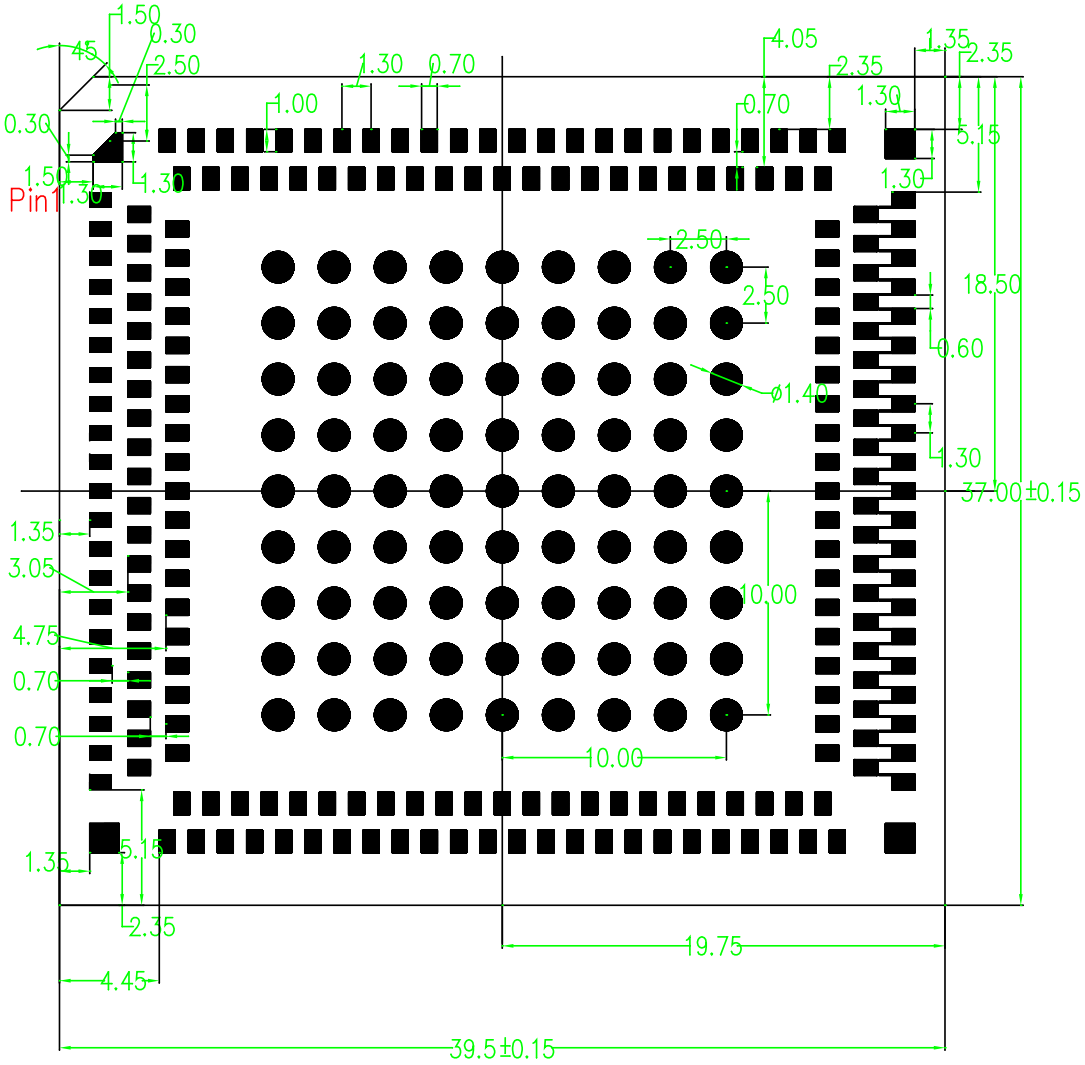


Figure 45: Module Bottom Dimensions (Top View)

7.2. Recommended Footprint

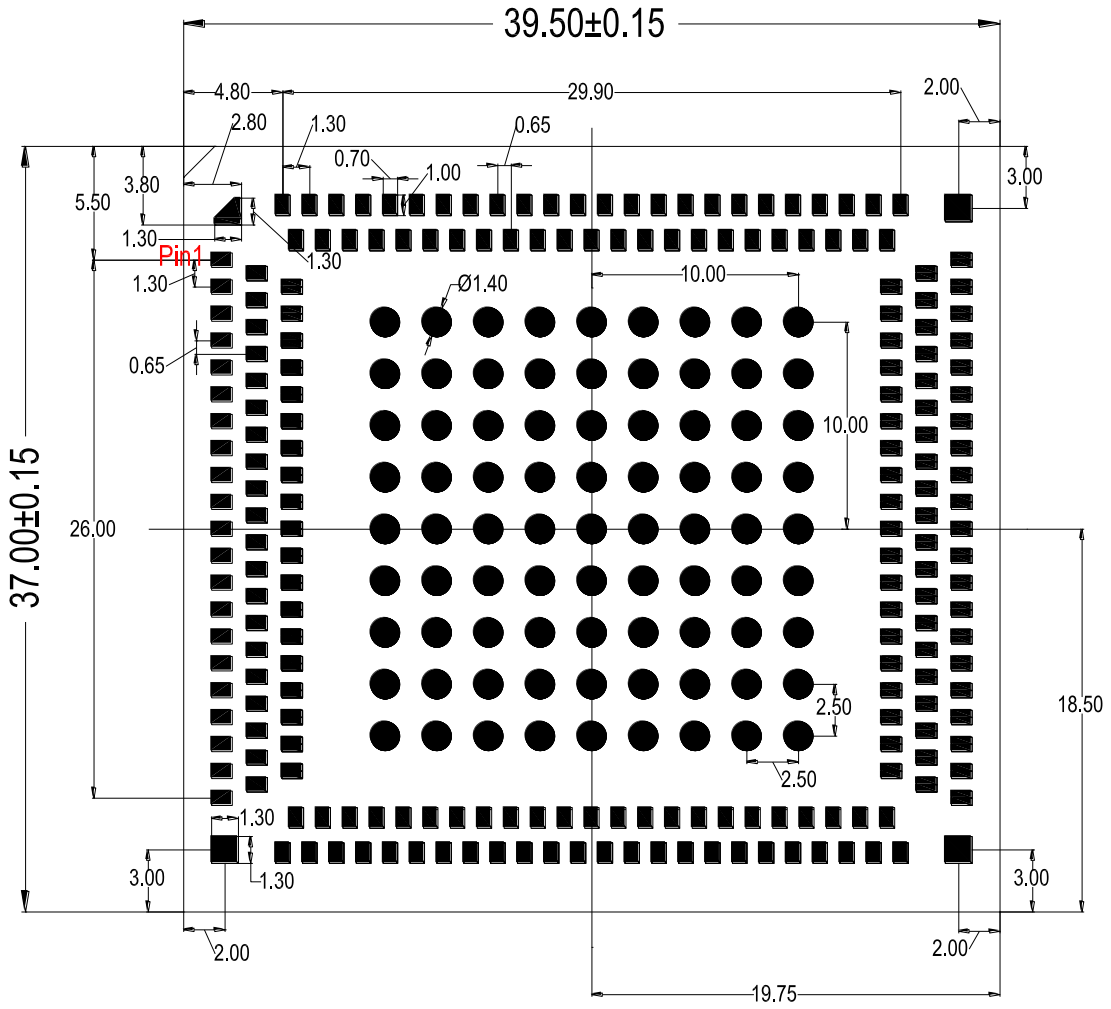


Figure 46: Recommended Footprint (Top View)

NOTE

For easy maintenance of the module, please keep about 3mm between the module and other components in the host PCB.

7.3. Design Effect Drawings of the Module

Figure 47: Top View of the Module

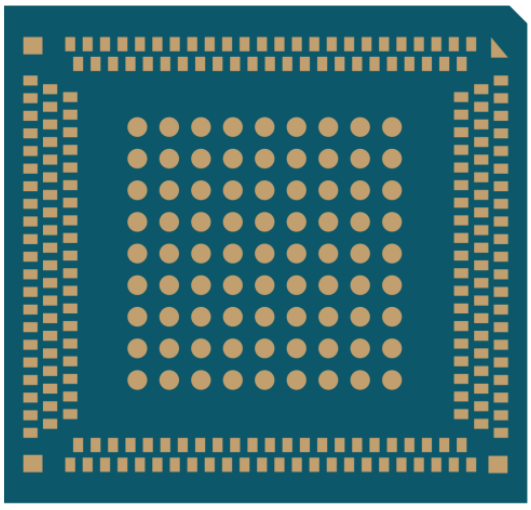


Figure 48: Bottom View of the Module

NOTE

These are renderings of EG12. For authentic appearance, please refer to the module that you receive from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage

EG12 is stored in a vacuum-sealed bag. It is rated at MSL 3, and its storage restrictions are listed below.

1. Shelf life in vacuum-sealed bag: 12 months at <40ºC/90%RH.
2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:
   - Mounted within 168 hours at the factory environment of ≤30ºC/60%RH.
   - Stored at <10% RH.
3. Devices require baking before mounting, if any circumstance below occurs:
   - When the ambient temperature is 23ºC±5ºC and the humidity indicator card shows the humidity is >10% before opening the vacuum-sealed bag.
   - Device mounting cannot be finished within 168 hours at factory conditions of ≤30ºC/60%RH.
4. If baking is required, devices may be baked for 8 hours at 120ºC±5ºC.

NOTE

As the plastic container cannot be subjected to high temperature, it should be removed from devices before high temperature (120ºC) baking. If shorter baking time is desired, please refer to *IPC/JEDECJ-STD-033* for baking procedure.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module should be 0.13-0.15mm. For more details, please refer to ***document [4]***.

It is suggested that the peak reflow temperature is 238ºC ~ 245ºC (for SnAg3.0Cu0.5 alloy). The absolute max reflow temperature is 245ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. Recommended reflow soldering thermal profile is shown below:

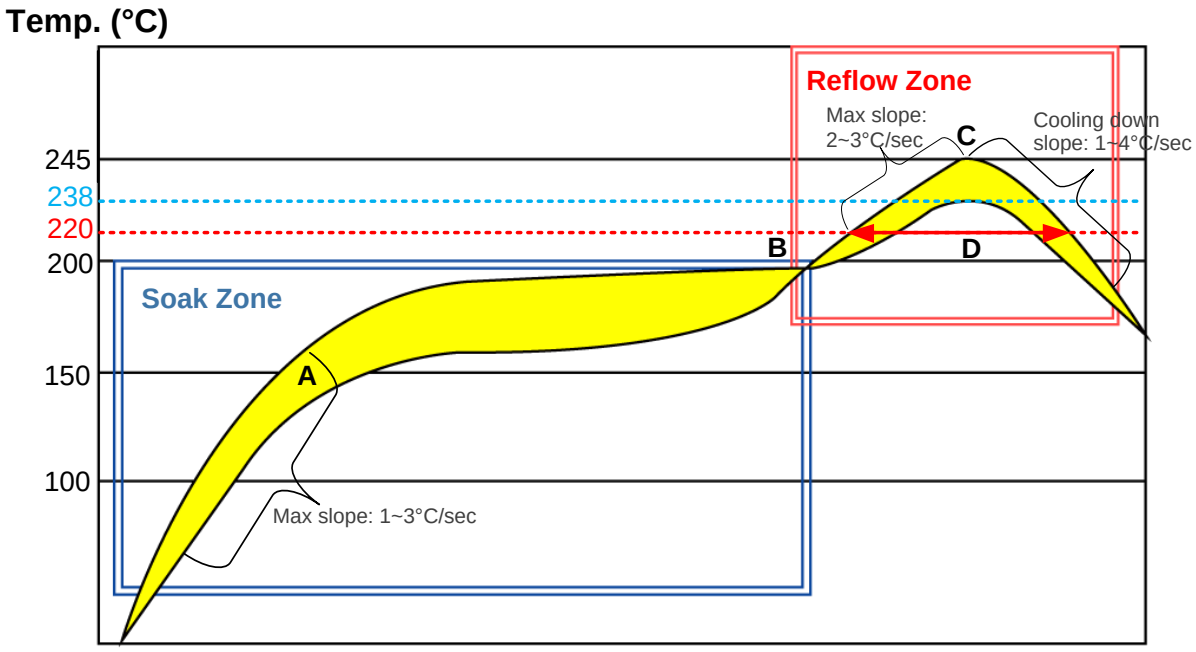


Figure 49: Reflow Soldering Thermal Profile

Table 47: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1 to 3°C/sec
Soak time (between A and B: 150°C and 200°C)	60 to 120 sec

Reflow Zone	
Max slope	2 to 3°C/sec
Reflow time (D: over 220°C)	40 to 60 sec
Max temperature	238°C ~ 245°C
Cooling down slope	1 to 4°C/sec
Reflow Cycle	
Max reflow cycle	1

8.3. Packaging

EG12 is packaged in tape and reel carriers. Each reel is 10.56m long and contains 200 modules. The figures below show the packaging details, measured in mm.

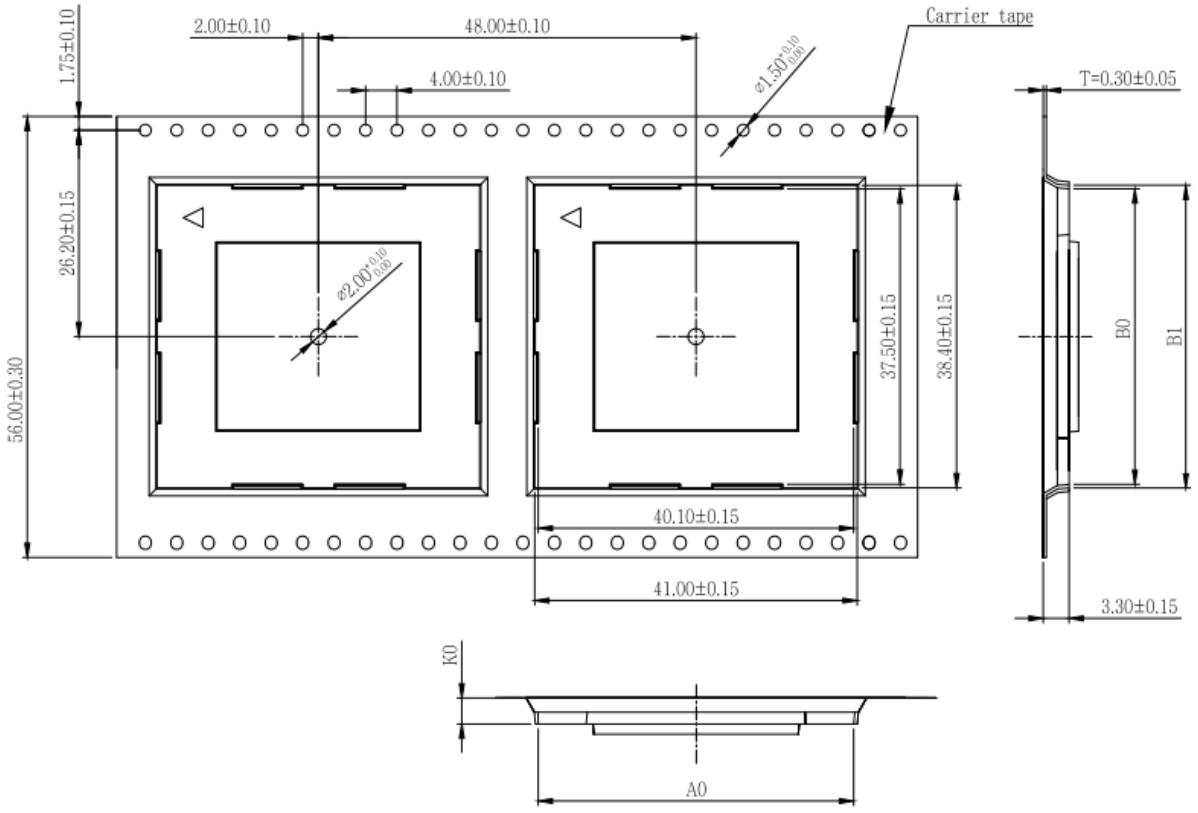


Figure 50: Tape Specifications

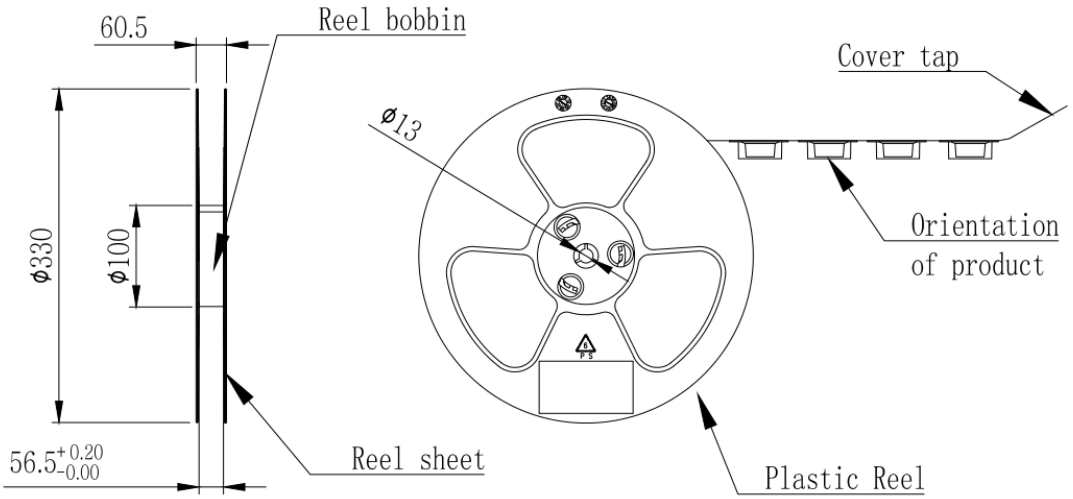


Figure 51: Reel Specifications

9 Appendix A References

Table 48: Related Documents

SN	Document Name	Remark
[1]	Quectel_UMTS&LTE_EVB_R2.0_User_Guide	UMTS&LTE EVB R2.0 User Guide
[2]	Quectel_EM12&EG12&EG18_AT_Commands_Manual	AT Commands Manual for EM12, EG12 and EG18
[3]	Quectel_EM12&EG12&EG18_GNSS_AT_Commands_Manual	GNSS AT Commands Manual for EM12, EG12 and EG18
[4]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide
[5]	Quectel_EM12&EG12&EG18_Reference_Design	Reference Design for EM12, EG12 and EG18
[6]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[7]	Quectel_LTE_Module_Thermal_Design_Guide	Thermal Design Guide for LTE Modules

Table 49: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CPE	Customer Premises Equipment
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear To Send
DC-HSPA+	Dual-carrier High Speed Packet Access

DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DRX	Discontinuous Reception
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FR	Full Rate
GLONASS	GLObalnaya NAvigatsionnaya Sputnikovaya Sistema, the Russian Global Navigation Satellite System
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
HO-RXD	Higher-order Receiver Diversity
HR	Half Rate
I/O	Input/Output
Inorm	Normal Current
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MS	Mobile Station
MT	Mobile Terminated
PAP	Password Authentication Protocol

PCB	Printed Circuit Board
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SGMII	Serial Gigabit Media Independent Interface
SIMO	Single Input Multiple Output
SMS	Short Message Service
TDD	Time Division Duplexing
Tx	Transmitting Direction
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	Universal Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
$V_I$max	Absolute Maximum Input Voltage Value

$V_I$min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution:

- Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.
- This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

This device is intended only for OEM integrators under the following conditions:

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and the maximum antenna gain allowed for use with this device is 1.85dBi for LTE Band 48 and 6.00dBi for LTE band 42 (CA).
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed

IMPORTANT NOTE: In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "**Contains FCC ID: XMR201909EG12GT** ". The grantee's FCC ID can be used only when all FCC compliance requirements are met.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.