Model:SC66-A

SC66 Hardware Design

Smart LTE Module Series

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About the Document

History

Revision	Date	Author	Description
1.0	2019-08-13	Jian WU/ Chris ZHANG	Initial

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OEM/Integrators Installation Manual

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part

15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: XMR2019SC66A ”
“Contains IC: 10224A-2019SC66A “
The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Industry Canada Statement

This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

The device could automatically discontinue transmission in case of absence of information to transmit, or operational failure. Note that this is not intended to prohibit transmission of control or signaling information or the use of repetitive codes where required by the technology.

The device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems;
The maximum antenna gain permitted for devices in the bands 5250–5350 MHz and 5470–5725 MHz shall comply with the e.i.r.p. limit; and
The maximum antenna gain permitted for devices in the band 5725–5825 MHz shall comply with the e.i.r.p. limits specified for point-to-point and non point-to-point operation as appropriate.

L'appareil peut interrompre automatiquement la transmission en cas d'absence d'informations à transmettre ou de panne opérationnelle. Notez que ceci n'est pas destiné à interdire la transmission d'informations de contrôle ou de signalisation ou l'utilisation de codes répétitifs lorsque cela est requis par la technologie.

Le dispositif utilisé dans la bande 5150-5250 MHz est réservé à une utilisation en intérieur afin de réduire le risque de brouillage préjudiciable aux systèmes mobiles par satellite dans le même canal;
Le gain d'antenne maximal autorisé pour les dispositifs dans les bandes 5250-5350 MHz et 5470-5725 MHz doit être conforme à la norme e.r.p. limite; et
Le gain d'antenne maximal autorisé pour les appareils de la bande 5725-5825 MHz doit être conforme à la norme e.i.r.p. les limites spécifiées pour un fonctionnement point à point et non point à point, selon le cas.

CAN ICES-3(B)/ NMB-3(B)

Radiation Exposure Statement

This equipment complies with FCC/IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

1 Introduction

This document defines the SC66 module and describes its air interfaces and hardware interfaces which are connected with customers' applications.

This document can help customers quickly understand module interface specifications, electrical and mechanical details as well as other related information of SC66 module. Associated with application note and user guide, customers can use SC66 module to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating SC66 module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

🚚	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
✈	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft.
⊕	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
SOS	Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid (U)SIM card). When emergent help is needed in such conditions, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength.
♥	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
🔥	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

SC66 is a series of Smart LTE module based on Qualcomm platform and Android operating system, and provides industrial grade performance. Its general features are listed below:

- Support worldwide LTE-FDD, LTE-TDD, DC-HSDPA, DC-HSUPA, HSPA+, HSDPA, HSUPA, WCDMA, TD-SCDMA, EVDO/CDMA, EDGE, GSM and GPRS coverage
- Support short-range wireless communication via Wi-Fi 802.11a/b/g/n/ac and BT5.0 standards
- Integrate GPS/GLONASS/BeiDou satellite positioning systems
- Support multiple audio and video codecs
- Built-in high performance Adreno^{TM} GPU 512 graphics processing unit
- Provide multiple audio and video input/output interfaces as well as abundant GPIO interfaces

SC66 are available in six variants: SC66-CE*, SC66-A*, SC66-J*, SC66-E*, SC66-W* and SC66-MW*. The following table shows the supported frequency bands of SC66.

Table 1: SC66-CE* Frequency Bands

Type	Frequency Bands
LTE-FDD	B1/B3/B5/B8
LTE-TDD	B34/B38/B39/B40/B41
WCDMA	B1/B8
TD-SCDMA	B34/B39
EVDO/CDMA	BC0
GSM	900/1800MHz
Wi-Fi 802.11a/b/g/n/ac	2402MHz~2482MHz; 5180MHz~5825MHz

BT5.0	2402MHz~2480MHz
GNSS	GPS: 1575.42MHz±1.023MHz GLONASS: 1597.5MHz~1605.8MHz BeiDou: 1561.098MHz±2.046MHz

Table 2: SC66-A* Frequency Bands

Type	Frequency Bands
LTE-FDD	B2/B4/B5/B7/B12/B13/B14/B17/B25/B26/B66/B71
LTE-TDD	B41
WCDMA	B2/B4/B5
Wi-Fi 802.11a/b/g/n/ac	2402MHz~2482MHz; 5180MHz~5825MHz
BT 5.0	2402MHz~2480MHz
GNSS	GPS: 1575.42MHz±1.023MHz GLONASS: 1597.5MHz~1605.8MHz BeiDou: 1561.098MHz±2.046MHz

Table 3: SC66-J* Frequency Bands

Type	Frequency Bands
LTE-FDD	B1/B3/B5/B8/B11/B18/B19/B21/B26/B28(A+B)
LTE-TDD	B41
WCDMA	B1/B6/B8/B19
Wi-Fi 802.11a/b/g/n/ac	2402MHz~2482MHz; 5180MHz~5825MHz
BT 5.0	2402MHz~2480MHz
GNSS	GPS: 1575.42MHz±1.023MHz GLONASS: 1597.5MHz~1605.8MHz BeiDou: 1561.098MHz±2.046MHz

Table 4: SC66-E* Frequency Bands

Type	Frequency Bands
LTE-FDD	B1/B2/B3/B4/B5/B7/B8/B20/B28(A+B)
LTE-TDD	B38/B39/B40/B41
WCDMA	B1/B2/B4/B5/B8
GSM	850/900/1800/1900MHz
Wi-Fi 802.11a/b/g/n/ac	2402MHz~2482MHz; 5180MHz~5825MHz
BT 5.0	2402MHz~2480MHz
GNSS	GPS: 1575.42MHz±1.023MHz GLONASS: 1597.5MHz~1605.8MHz BeiDou: 1561.098MHz±2.046MHz

Table 5: SC66-W* Frequency Bands

Type	Frequency Bands
LTE-FDD	/
LTE-TDD	/
WCDMA	/
TD-SCDMA	/
CDMA	/
GSM	/
Wi-Fi 802.11a/b/g/n/ac	2402MHz~2482MHz; 5180MHz~5825MHz
BT 5.0	2402MHz~2480MHz
GNSS	/

Table 6: SC66-MW*(2 × 2 MIMO WIFI) Frequency Bands

Type	Frequency Bands
LTE-FDD	/
LTE-TDD	/
WCDMA	/
TD-SCDMA	/
CDMA	/
GSM	/
Wi-Fi 802.11a/b/g/n/ac	2402MHz~2482MHz; 5180MHz~5825MHz
BT 5.0	2402MHz~2480MHz
GNSS	/

NOTES

1. "*" means under development.
2. SC66-A, SC66-J, SC66-E and SC66-MW support Wi-Fi MIMO function.

SC66 is an SMD type module which can be embedded into applications through its 324 pins (including 152 LCC pads and 172 LGA pads). With a compact profile of 43.0mm × 44.0mm × 2.85mm, SC66 can meet almost all requirements for M2M applications such as smart metering, smart home, security, routers, wireless POS, mobile computing devices, PDA phone, tablet PC and etc. Besides, SC66 supports AI applications such as face recognition and vehicle recognition.

2.2. Key Features

The following table describes the detailed features of SC66 module.

Table 7: SC66 Key Features

Features	Details
Application Processor	Customized 64-bit ARM v8-compliant applications processor ● Kryo Gold: quad high-performance cores targeting 2.2 GHz ● Kryo Silver: quad low-power cores targeting 1.843 GHz ● two quad-core processors with 1MB L2 cache
Modem system	LTE Cat 6 (FDD and TDD), 2 × 20 CA(40MHz)
GPU	Adreno 512 up to 650 MHz
Memory	32GB eMMC＋ 3GB LPDDR4x(default) 64GB eMMC＋ 4GB LPDDR4x (optional)
Operating System	Android 9
Power Supply	VBAT Supply Voltage: 3.55V~4.4V Typical 4.0V
Transmitting Power	Class 4 (33dBm±2dB) for GSM850/EGSM900 Class 1 (30dBm±2dB) for DCS1800/PCS1900 Class E2 (27dBm±3dB) for GSM850/EGSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800/PCS1900 8-PSK Class 3 (24dBm＋1/-3dB) for WCDMA bands Class 3 (24dBm＋3/-1dB) for EVDO/CDMA BC0 Class 2 (24dBm＋1/-3dB) for TD-SCDMA bands Class 3 (23dBm±2dB) for LTE-FDD bands Class 3 (23dBm±2dB) for LTE-TDD bands
LTE Features	Support 3GPP R12 Cat 6 and Cat 4 Support 1.4 MHz to 20MHz RF bandwidth Support Multiuser MIMO in DL direction ● Cat 6 FDD: Max 300Mbps (DL)/Max 50Mbps (UL) ● Cat 6 TDD: Max 265Mbps (DL)/Max 30Mbps (UL) ● Cat 4 FDD: Max 150Mbps (DL)/Max 50Mbps (UL) ● Cat 4 TDD: Max 130Mbps (DL)/Max 30Mbps (UL)
UMTS Features	Support 3GPP R9 DC-HSDPA/DC-HSUPA/HSPA+/HSDPA/HSUPA/WCDMA Support QPSK, 16-QAM and 64-QAM modulation ● DC-HSDPA: Max 42Mbps (DL) ● DC-HSUPA: Max 11.2Mbps (UL)

	● WCDMA: Max 384Kbps (DL)/Max 384Kbps (UL)
TD-SCDMA Features	Support CCSA Release 3 TD-SCDMA ● Max 4.2Mbps (DL)/Max 2.2Mbps (UL)
CDMA2000 Features	Support 3GPP2 CDMA2000 1X Advanced, CDMA2000 1x EV-DO Rev.A ● EVDO: Max 3.1Mbps (DL)/Max 1.8 Mbps (UL) ● 1X Advanced: Max 307.2Kbps (DL)/Max 307.2Kbps (UL)
GSM Features	**R99** CSD: 9.6kbps, 14.4kbps **GPRS** Support GPRS multi-slot class 33 (33 by default) Coding scheme: CS-1, CS-2, CS-3 and CS-4 Max 107Kbps (DL), 85.6Kbps (UL) **EDGE** Support EDGE multi-slot class 33 (33 by default) Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) Downlink coding schemes: CS 1-4 and MCS 1-9 Uplink coding schemes: CS 1-4 and MCS 1-9 Max 296Kbps (DL), 236.8Kbps (UL)
WLAN Features	2.4GHz/5GHz, support 802.11a/b/g/n/ac, maximally up to 433Mbps Support AP and STA mode
Bluetooth Features	BT5.0
GNSS Features	GPS/GLONASS/BeiDou
SMS	Text and PDU mode Point-to-point MO and MT SMS cell broadcast
LCM Interfaces	2560 × 1600 @60fps primary display＋4k @30fps over DP; Dual MIPI DSI
Camera Interfaces	Support three groups of 4-lane MIPI_CSI, up to 2.1Gbps per lane Support 3 cameras (4-lane＋4-lane＋4-lane) or 4 cameras (4-lane＋4-lane＋2-lane＋1-lane) up to 24MP with dual ISP
Video Codec	Video encoding and decoding: up to 4K @30fps Concurrency: encoding up to 1080P @30fps; decoding up to 1080P @60fps
Audio Interfaces	**Audio Input** Three analog microphone inputs, integrating internal bias voltage **Audio Output** Class AB stereo headphone output Class AB earpiece differential output Class D speaker differential amplifier output

Audio Codec	EVRC, EVRC-B, EVRC-WB; G.711, G.729A/AB; GSM-FR, GSM-EFR, GSM-HR; AMR-NB, AMR-WB, AMR-eAMR, AMR-BeAMR
USB Interfaces	Compliant with USB 3.1 and 2.0 specifications, with transmission rates up to 5Gbps on USB 3.1 and 480Mbps on USB 2.0 Support USB OTG Used for AT command communication, data transmission, software debugging and firmware upgrade
UART Interfaces	4 UART Interfaces: UART6, UART1, DEBUG UART and LPI_UART_2 ● UART6: 4-wire UART interface with RTS/CTS hardware flow control, max rate up to 4Mbps ● UART1: 2-wire UART interface ● DEBUG UART: 2-wire UART interface used for debugging ● LPI_UART_2: 2-wire low power UART interface
SD Card Interface	Support SD 3.0 Support SD card hot-plug
(U)SIM Interfaces	2 (U)SIM interfaces Support USIM/SIM card: 1.8V/2.95V Support Dual SIM Dual Standby (supported by default)
I2C Interfaces	Support up to 5 I2C interfaces, used for peripherals such as TP, camera, sensor, etc.
I2S Interfaces	2 I2S interfaces
ADC Interfaces	2 general-purpose ADC interfaces
SPI Interface	1 SPI interface, only support master mode
Real Time Clock	Supported
Antenna Interfaces	Main antenna, Rx-diversity antenna, GNSS antenna, Wi-Fi/BT antenna, FM* antenna and WIFI_MIMO antenna interfaces
Physical Characteristics	Size: (43.0±0.15)mm × (44.0±0.15)mm × (2.85±0.2)mm Package: LCC＋LGA Weight: approx. 12.0g
Temperature Range	Operating temperature range: -35°C ~ +65°C $^{1)}$ Extended temperature range: -40°C ~ +75°C $^{2)}$ Storage temperature range: -40°C ~ +90°C
Firmware Upgrade	A/B OTA firmware upgrade via USB
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. $^{1)}$ Within operation temperature range, the module is 3GPP compliant.
2. $^{2)}$ Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.
3. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of SC66 and illustrates the major functional parts.

- Power management
- Radio frequency
- Baseband
- LPDDR4X+eMMC flash
- Peripheral interfaces
  -- USB interfaces
  -- (U)SIM interfaces
  -- UART interfaces
  -- SD card interface
  -- GPIO interfaces
  -- I2C interfaces
  -- ADC interfaces
  -- LCM (MIPI) interfaces
  -- TP (touch panel) interfaces
  -- Camera (MIPI) interfaces
  -- Audio interfaces
  -- I2S interfaces
  -- SPI interface

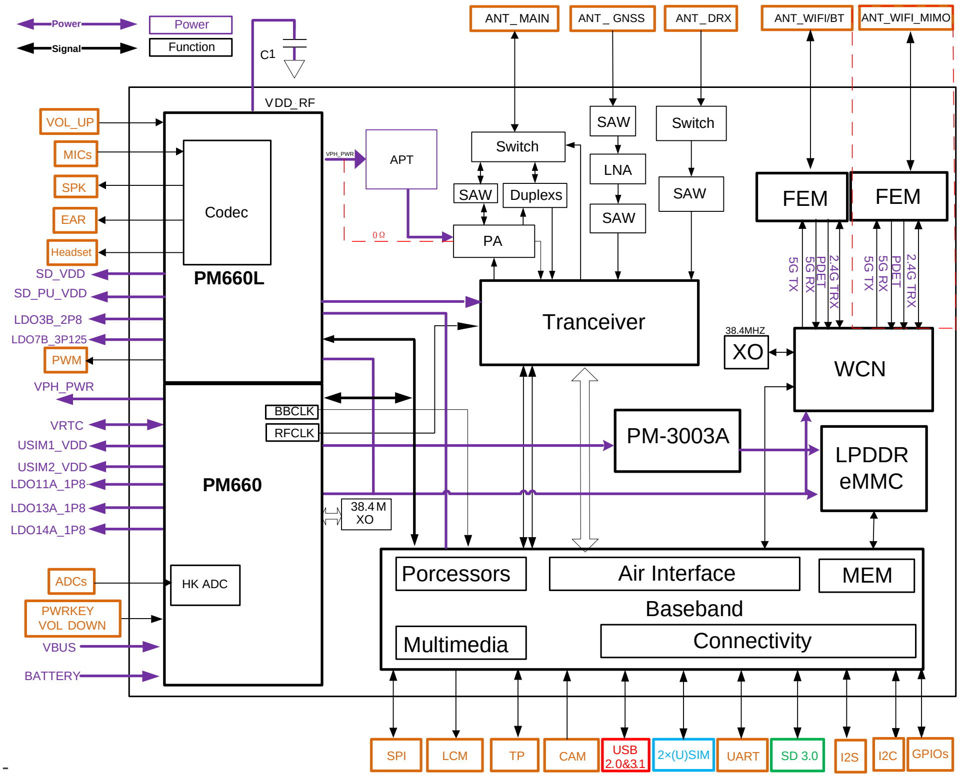

Figure 1: Functional Diagram

NOTE

The red dotted frame is Wi-Fi MIMO path, which is not supported by SC66-CE and SC66-W.

2.4. Evaluation Board

In order to help customers design and test applications with Quectel SC66 modules, Quectel supplies an evaluation kit, which includes an evaluation board, a USB to RS232 converter cable, a USB Type-C data cable, a power adapter, an earphone and antennas. For details, please refer the ***document [1]*** .

3 Application Interfaces

3.1. General Description

SC66 is equipped with 324 pins that can be embedded into cellular application platform. The following chapters provide the detailed description of pins/interfaces listed below.

- Power supply
- Turn on and off function
- VRTC interface
- Power Output
- Charging interface
- USB interfaces
- UART interfaces
- (U)SIM interfaces
- SD card interface
- GPIO interfaces
- I2C interfaces
- I2S interfaces
- SPI interface
- ADC interfaces
- LCM interfaces
- TP (touch panel) interfaces
- Camera interfaces
- Sensor interfaces
- Audio interfaces
- Emergency download interface

3.2. Pin Assignment

The following figure shows the pin assignment of SC66 module.

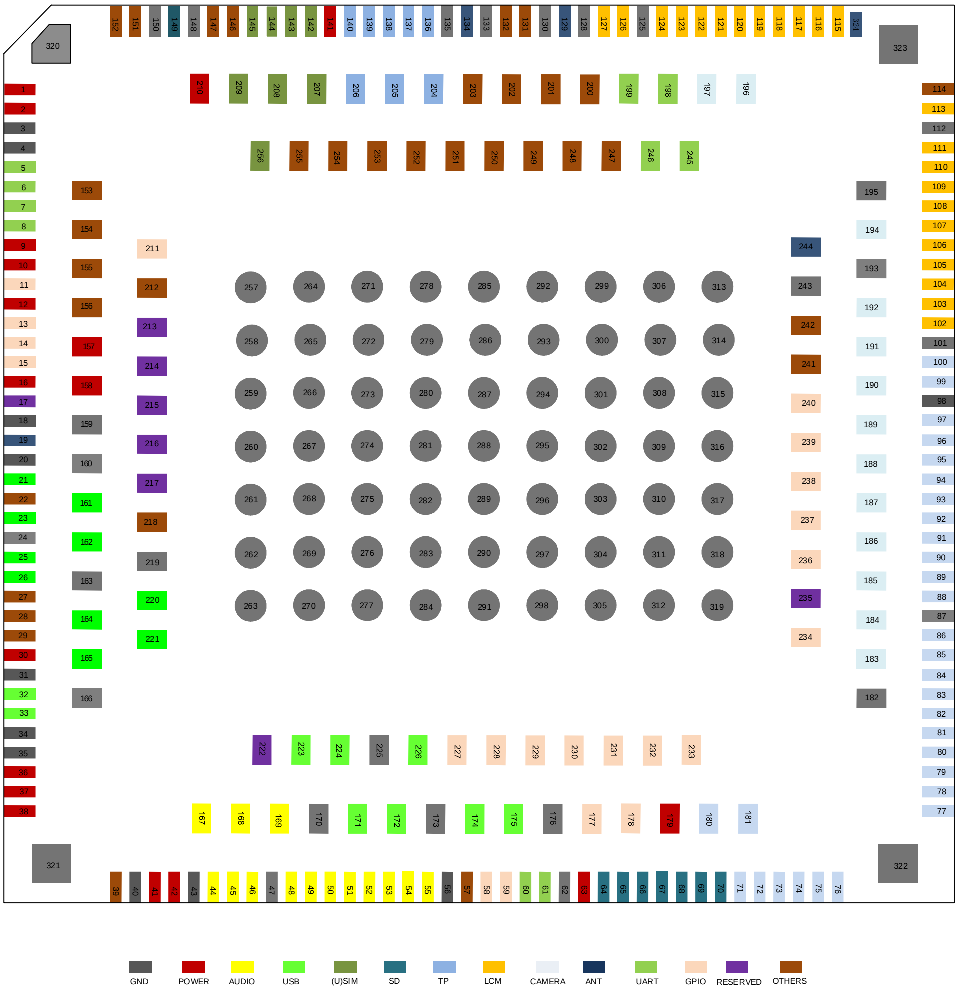

Figure 2: Pin Assignment (Top View)

3.3. Pin Description

Table 8: I/O Parameters Definition

Type	Description
AI	Analog input
AO	Analog output
DI	Digital input
DO	Digital output
IO	Bidirectional
OD	Open drain
PI	Power input
PO	Power output

The following tables show the SC66's pin definition and electrical characteristics.

Table 9: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	36, 37, 38	PI/ PO	Power supply for the module	Vmax=4.4V Vmin=3.55V Vnorm=4.0V	It must be provided with sufficient current up to 3.0A. It is suggested to use a TVS to increase voltage surge withstand capability.
VDD_RF	1, 2	PO	Connect to external bypass capacitors to eliminate voltage fluctuation of RF part.	Vmax=4.4V Vmin=3.55V Vnorm=4.0V	Do not load externally.

VRTC	16	PI/ PO	Power supply for internal RTC circuit	$V_O$max=3.2V; When VBAT is not connected: V_I=2.1V~3.25V	
LDO13A_1P8	9	PO	1.8V output power supply	Vnorm=1.8V $I_O$max=20mA	Power supply for external GPIO's pull up circuits and level shift circuit.
LDO7B_ 3P125	157	PO	3.125V output power supply	Vnorm=3.125V $I_O$max=150mA	Power supply only for DP switch.
LDO11A_1P8	10	PO	1.8V output power supply	Vnorm=1.8V $I_O$max=150mA	Power supply for I/O VDD of cameras, LCDs and TP etc.
LDO14A_1P8	158	PO	1.8V output power supply	Vnorm=1.8V $I_O$max=150mA	Power supply for I/O VDD of sensors.
LDO3B_2P8	12	PO	2.8V output power supply	Vnorm=2.8V $I_O$max=600mA	Power supply for sensor and LCM.
VPH_PWR	30	PO	VBAT output power supply	Vnorm=VBAT $I_O$max=1000mA	Power supply for other ICs.
GND	3, 4, 18, 20, 24, 31, 34, 35, 40, 43, 47, 56, 62, 87, 98, 101, 112, 125, 128, 130, 133, 135, 148, 150, 159, 160, 163, 166, 170, 173, 176, 182,		Ground		

	193, 195, 219, 225, 243, 257~ 323				
Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC_BIAS	167	AO	Microphone bias voltage	V_O=1.6V~2.9V	
MIC1_P	44	AI	Microphone input for channel 1 (+)		
MIC1_M	45	AI	Microphone input for channel 1 (-)		
MIC_GND	168		Microphone reference ground		If unused, connect this pin to the ground.
MIC2_P	46	AI	Microphone input for headset (+)		Headset microphone input.
MIC3_P	169	AI	Microphone input for secondary microphone (+)		Secondary microphone input.
EAR_P	53	AO	Earpiece output (+)		
EAR_M	52	AO	Earpiece output (-)		
SPK_P	55	AO	Speaker output (+)		
SPK_M	54	AO	Speaker output (-)		
HPH_R	51	AO	Headphone right channel output		
HPH_REF	50	AI	Headphone reference ground		It should be connected to main GND.
HPH_L	49	AO	Headphone left channel output		
HS_DET	48	AI	Headset insertion detection		High level by default.
USB Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

USB_VBUS	41, 42	PI/PO	Charging power input; Power supply output for OTG device; USB/charger insertion detection	Vmax=10V Vmin=3.6V Vnorm=5.0V	
USB2_HS_DM	25	IO	USB 2.0 differential data bus (-)		90Ω differential impedance; USB 2.0 standard compliant; Only support host mode.
USB2_HS_DP	26	IO	USB 2.0 differential data bus (+)		
USB1_HS_DM	33	IO	USB 2.0 differential data bus (-)		90Ω differential impedance; USB 2.0 standard compliant; Support OTG Support software download.
USB1_HS_DP	32	IO	USB 2.0 differential data bus (+)		
USB_SS2_TX_P	165	IO	USB 3.1 channel 2 differential transmit (+)		90Ω differential impedance. USB 3.1 standard compliant.
USB_SS2_TX_M	164	IO	USB 3.1 channel 2 differential transmit (-)		
USB_SS2_RX_P	162	IO	USB 3.1 channel 2 differential receive (+)		
USB_SS2_RX_M	161	IO	USB 3.1 channel 2 differential receive (-)		
USB_SS1_RX_P	171	IO	USB 3.1 channel 1 differential receive (+)		90Ω differential impedance; USB 3.1 standard compliant.
USB_SS1_RX_M	172	IO	USB 3.1 channel 1 differential receive (-)		
USB_SS1_TX_P	174	IO	USB 3.1 channel 1 differential transmit (+)		90Ω differential impedance.
USB_SS1_TX_M	175	IO	USB 3.1 channel 1 differential transmit (-)		

USB_CC1	224	AI	USB Type-C detection channel 1		When Micro USB is used, it can be used as USB_ID pin.
USB_CC2	223	AI	USB Type-C detection channel 2		
UUSB_TYPEC	23	DI	uUSB & USB Type-C configuration selection pin		When USB Type-C is used, it should be connected to VPH_PWR through a 10KΩ resistor; When uUSB 1) is used, it should be connected to GND through a 10KΩ resistor. Cannot be multiplexed into a general-purpose GPIO.
SS_DIR_IN	21	DI	CC status detection pin		When USB Type-C is used, it should be connected to SS_DIR_OUT; When uUSB is used, it should be connected to GND. Cannot be multiplexed into a general-purpose GPIO.
SS_DIR_OUT	226	DO	CC status output pin		
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_DET	145	DI	(U)SIM1 card hot-plug detection	V_{IL}max=0.63V V_{IH}min=1.17V	Active Low. Require external pull-up to 1.8V. If unused, keep it open.
USIM1_RST	144	DO	(U)SIM1 card reset signal	VOLmax=0.4V VOHmin= 0.8 × USIM1_VDD	Cannot be multiplexed into general-purpose GPIOs.
USIM1_CLK	143	DO	(U)SIM1 card clock signal		
USIM1_DATA	142	IO	(U)SIM1 card data signal	V_{IL}max= 0.2 × USIM1_VDD	

				V_{IH}min= 0.7 × USIM1_VDD V_{OL}max=0.4V V_{OH}min= 0.8 × USIM1_VDD	
USIM1_VDD	141	PO	(U)SIM1 card power supply		Either 1.8V or 2.95V (U)SIM card is supported.
USIM2_DET	256	DI	(U)SIM2 card hot-plug detection	V_{IL}max=0.63V V_{IH}min=1.17V	Active Low. Need external pull-up to 1.8V. If unused, keep it open.
USIM2_RST	207	DO	(U)SIM2 card reset signal	V_{OL}max=0.4V V_{OH}min= 0.8 × USIM2_VDD	Cannot be multiplexed into general-purpose GPIOs.
USIM2_CLK	208	DO	(U)SIM2 card clock signal	V_{OL}max=0.4V V_{OH}min= 0.8 × USIM2_VDD	
USIM2_DATA	209	IO	(U)SIM2 card data signal	V_{IL}max= 0.2 × USIM2_VDD V_{IH}min= 0.7 × USIM2_VDD V_{OL}max=0.4V V_{OH}min= 0.8 × USIM2_VDD	
USIM2_VDD	210	PO	(U)SIM2 card power supply		Either 1.8V or 2.95V (U)SIM card is supported.
UART Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DEBUG_TXD	5	DO	DEBUG UART transmit data.	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, leave these pins open.
DEBUG_RXD	6	DI	DEBUG UART receive data.	V_{IL}max=0.63V V_{IH}min=1.17V	
UART1_TXD	7	DO	UART1 transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	
UART1_RXD	8	DI	UART1 receive data	V_{IL}max=0.63V V_{IH}min=1.17V	
UART6_RXD	198	DI	UART6 receive data		

UART6_TXD	199	DO	UART6 transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	
UART6_RTS	245	DO	UART6 request to send		
UART6_CTS	246	DI	UART6 clear to send	V_{IL}max=0.63V V_{IH}min=1.17V	
LPI_UART_2_TXD	60	DO	LPI_UART_2 transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	Cannot be multiplexed into general-purpose GPIOs.
LPI_UART_2_RXD	61	DI	LPI_UART_2 receive data	V_{IL}max=0.63V V_{IH}min=1.17V	
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_CLK	70	DO	High speed digital clock signal of SD card	**1.8V SD card:** V_{OL}max=0.45V V_{OH}min=1.4V **2.95V SD card:** V_{OL}max=0.36V V_{OH}min=2.13V	
SD_CMD	69	IO	Command signal of SD card	**1.8V SD card:** V_{IL}max=0.58V V_{IH}min=1.27V V_{OL}max=0.45V V_{OH}min=1.4V **2.95V SD card:** V_{IL}max=0.73V V_{IH}min=1.85V V_{OL}max=0.36V V_{OH}min=2.13V	
SD_DATA0	68	IO	High speed bidirectional digital signal lines of SD card		
SD_DATA1	67	IO			
SD_DATA2	66	IO			
SD_DATA3	65	IO			
SD_DET	64	DI	SD card insertion detection	V_{IL}max=0.63V V_{IH}min=1.17V	Active low.
SD_VDD	63	PO	Power supply for SD card	Vnorm=2.95V $I_O$max=600mA	
SD_PU_VDD	179	PO	1.8V/2.95V output	Vnorm=1.8V/2.95V $I_O$max=50mA	Power supply for SD card's pull-up circuit only.
TP (Touch Panel) Interfaces					
Pin Name	**Pin N**	**I/O**	**Description**	**DC Characteristics**	**Comment**

TP0_RST	138	DO	Reset signal of touch panel (TP0)	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain.
TP0_INT	139	DI	Interrupt signal of touch panel (TP0)	V_{IL}max=0.63V V_{IH}min=1.17V	
TP0_I2C_SCL	140	OD	I2C clock signal of touch panel (TP0)		
TP0_I2C_SDA	206	OD	I2C data signal of touch panel (TP0)		
TP1_RST	136	DO	Reset signal of touch panel (TP1)	V_{OL}max=0.45V V_{OH}min=1.35V	
TP1_INT	137	DI	Interrupt signal of touch panel (TP1)	V_{IL}max=0.63V V_{IH}min=1.17V	
TP1_I2C_SCL	205	OD	I2C clock signal of touch panel (TP1)		
TP1_I2C_SDA	204	OD	I2C data signal of touch panel (TP1)		

LCM Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PWM	152	DO	PWM signal output	The voltage is equal to VBAT voltage.	Cannot be multiplexed into a general-purpose GPIO.
LCD0_RST	127	DO	LCD0 reset signal	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain; It should not be pulled up.
LCD0_TE	126	DI	LCD0 tearing effect signal	V_{IL}max=0.63V V_{IH}min=1.17V	1.8V power domain.
DSI0_CLK_N	116	AO	LCD0 MIPI clock signal (-)		85Ω differential impedance.
DSI0_CLK_P	115	AO	LCD0 MIPI clock signal (+)		
DSI0_LN0_N	118	AO	LCD0 MIPI lane 0 data signal (-)		85Ω differential impedance.
DSI0_LN0_P	117	AO	LCD0 MIPI lane 0 data signal (+)		
DSI0_LN1_N	120	AO	LCD0 MIPI lane 1 data signal (-)		85Ω differential impedance.

DSI0_LN1_P	119	AO	LCD0 MIPI lane 1 data signal (+)		
DSI0_LN2_N	122	AO	LCD0 MIPI lane 2 data signal (-)		85Ω differential impedance.
DSI0_LN2_P	121	AO	LCD0 MIPI lane 2 data signal (+)		
DSI0_LN3_N	124	AO	LCD0 MIPI lane 3 data signal (-)		85Ω differential impedance.
DSI0_LN3_P	123	AO	LCD0 MIPI lane 3 data signal (+)		
LCD1_RST	113	DO	LCD1 reset signal	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain.
DSI1_CLK_N	103		LCD1 MIPI clock signal (-)		85Ω differential impedance.
DSI1_CLK_P	102		LCD1 MIPI clock signal (+)		
DSI1_LN0_N	105		LCD1 MIPI lane 0 data signal (-)		85Ω differential impedance.
DSI1_LN0_P	104		LCD1 MIPI lane 0 data signal (+)		
DSI1_LN1_N	107		LCD1 MIPI lane 1 data signal (-)		85Ω differential impedance.
DSI1_LN1_P	106		LCD1 MIPI lane 1 data signal (+)		
DSI1_LN2_N	109		LCD1 MIPI lane 2 data signal (-)		85Ω differential impedance.
DSI1_LN2_P	108		LCD1 MIPI lane 2 data signal (+)		
DSI1_LN3_N	111		LCD1 MIPI lane 3 data		85Ω differential

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
			signal (-)		impedance.
DSI1_LN3_P	110		LCD1 MIPI lane 3 data signal (+)		
Camera Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CSI1_CLK_N	89	AI	MIPI clock signal of rear camera (-)		85Ω differential impedance.
CSI1_CLK_P	88	AI	MIPI clock signal of rear camera (+)		
CSI1_LN0_N	91	AI	MIPI lane 0 data signal of rear camera (-)		85Ω differential impedance.
CSI1_LN0_P	90	AI	MIPI lane 0 data signal of rear camera (+)		
CSI1_LN1_N	93	AI	MIPI lane 1 data signal of rear camera (-)		85Ω differential impedance.
CSI1_LN1_P	92	AI	MIPI lane 1 data signal of rear camera (+)		
CSI1_LN2_N	95	AI	MIPI lane 2 data signal of rear camera (-)		85Ω differential impedance.
CSI1_LN2_P	94	AI	MIPI lane 2 data signal of rear camera (+)		
CSI1_LN3_N	97	AI	MIPI lane 3 data signal of rear camera (-)		85Ω differential impedance.
CSI1_LN3_P	96	AI	MIPI lane 3 data signal of rear camera (+)		
CSI2_CLK_N	184	AI	MIPI clock signal of depth camera (-)		85Ω differential impedance.

CSI2_CLK_P	183	AI	MIPI clock signal of depth camera (+)	
CSI2_LN0_N	186	AI	MIPI lane 0 data signal of depth camera (-)	85Ω differential impedance.
CSI2_LN0_P	185	AI	MIPI lane 0 data signal of depth camera (+)	
CSI2_LN1_N	188	AI	MIPI lane 1 data signal of depth camera (-)	85Ω differential impedance.
CSI2_LN1_P	187	AI	MIPI lane 1 data signal of depth camera (+)	
CSI2_LN2_N	190	AI	MIPI lane 2 data signal of depth camera (-)	85Ω differential impedance. Can be multiplexed into differential data of the fourth camera (-).
CSI2_LN2_P	189	AI	MIPI lane 2 data signal of depth camera (+)	85Ω differential impedance. Can be multiplexed into differential data of the fourth camera (+).
CSI2_LN3_N	192	AI	MIPI lane 3 data signal of depth camera (-)	85Ω differential impedance. Can be multiplexed into differential clock of the fourth camera (-).
CSI2_LN3_P	191	AI	MIPI lane 3 data signal of depth camera (+)	85Ω differential impedance. Can be multiplexed into differential clock of the fourth camera (+).
CSI0_CLK_N	78	AI	MIPI clock signal of front camera (-)	85Ω differential impedance.
CSI0_CLK_P	77	AI	MIPI clock signal of front camera (+)	
CSI0_LN0_N	80	AI	MIPI lane 0 data signal	85Ω differential

			of front camera (-)		impedance.
CSI0_LN0_P	79	AI	MIPI lane 0 data signal of front camera (+)		
CSI0_LN1_N	82	AI	MIPI lane 1 data signal of front camera (-)		85Ω differential impedance.
CSI0_LN1_P	81	AI	MIPI lane 1 data signal of front camera (+)		
CSI0_LN2_N	84	AI	MIPI lane 2 data signal of front camera (-)		85Ω differential impedance.
CSI0_LN2_P	83	AI	MIPI lane 2 data signal of front camera (+)		
CSI0_LN3_N	86	AI	MIPI lane 3 data signal of front camera (-)		85Ω differential impedance.
CSI0_LN3_P	85	AI	MIPI lane 3 data signal of front camera (+)		
MCAM_MCLK	99	DO	Master clock signal of rear camera	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain.
SCAM_MCLK	100	DO	Master clock signal of front camera		1.8V power domain.
MCAM_RST	74	DO	Reset signal of rear camera		1.8V power domain.
MCAM_PWDN	73	DO	Power down signal of rear camera		1.8V power domain.
SCAM_RST	72	DO	Reset signal of front camera		1.8V power domain.
SCAM_PWDN	71	DO	Power down signal of front camera		1.8V power domain.
CAM_I2C_SCL0	75	OD	I2C clock signal of camera		1.8V power domain.
CAM_I2C_SDA0	76	OD	I2C data signal of camera		1.8V power domain.
DCAM_MCLK	194	DO	Master clock signal of depth camera	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain.
DCAM_RST	180	DO	Reset signal of depth		1.8V power domain.

			camera		
DCAM_PWDN	181	DO	Power down signal of depth camera		1.8V power domain.
CAM_I2C_SDA1	197	OD	I2C data signal of depth camera		1.8V power domain.
CAM_I2C_SCL1	196	OD	I2C data signal of depth camera		1.8V power domain.
Keypad Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	39	DI	Turn on/off the module		1.8V power domain.
VOL_UP	146	DI	Volume up		The voltage is equal to the VBAT voltage.
VOL_DOWN	147	DI	Volume down		1.8V power domain.
SENSOR_I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SENSOR_I2C_SCL	131	OD	I2C clock signal of external sensors		1.8V power domain. Cannot be multiplexed into general-purpose GPIOs.
SENSOR_I2C_SDA	132	OD	I2C data signal of external sensors		
Sensor Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ACCL_INT	252	IO	Interrupt signal of proximity sensor		1.8V power domain. Can be configured as a general-purpose GPIO.
GYRO_INT	255	IO	Interrupt signal of gyroscopic sensor		
MAG_INT	254	IO	Interrupt signal of geomagnetic sensor		
ALPS_INT	253	IO	Interrupt signal of optical sensor		
HALL_INT	218	IO	Interrupt signal of Hall sensor		
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

ADC0	151	AI	General purpose ADC interface		Max input voltage: 1.8V.
ADC1	153	AI	General purpose ADC interface		Max input voltage: 1.8V.
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	19	AI/ AO	Main antenna interface		50Ω impedance.
ANT_DRX	149	AI	Diversity antenna interface		
ANT_GNSS	134	AI	GNSS antenna interface		
ANT_WIFI/BT	129	AI/ AO	Wi-Fi/BT antenna interface		
ANT_WIFI_ MIMO	324	AI/ AO	Wi-Fi MIMO antenna interface		50Ω impedance; SC66-CE and SC66-W do not support this function.
FM_ANT	244	AI	FM antenna interface		FM function is still under development.
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO_21	231	IO	GPIO	V_{IL}max=0.63V V_{IH}min=1.17V V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain.
GPIO_34	236	IO	GPIO		1.8V power domain.
GPIO_40	238	IO	GPIO		1.8V power domain.
GPIO_41	237	IO	GPIO		1.8V power domain.
GPIO_55	178	IO	GPIO		1.8V power domain.
GPIO_56	177	IO	GPIO		1.8V power domain.
GPIO_72	239	IO	GPIO		1.8V power domain.
GPIO_73	59	IO	GPIO		1.8V power domain.
GPIO_74	58	IO	GPIO		1.8V power domain.
GPIO_76	232	IO	GPIO		1.8V power domain.

GPIO_77	240	IO	GPIO		1.8V power domain.
GPIO_12	228	IO	GPIO		1.8V power domain.
GPIO_13	227	IO	GPIO		1.8V power domain.
GPIO_14	230	IO	GPIO		1.8V power domain.
GPIO_15	229	IO	GPIO		1.8V power domain.
GPIO_61	234	IO	GPIO		1.8V power domain.
GPIO_03B	11	IO	GPIO		1.8V power domain.
GPIO_08B	13	IO	GPIO		1.8V power domain.
GPIO_04B	14	IO	GPIO		1.8V power domain.
GPIO_05B	15	IO	GPIO		1.8V power domain.
GPIO_11A	211	IO	GPIO		1.8V power domain.
GPIO_13A	233	IO	GPIO		1.8V power domain.
GRFC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC_19	242	IO	GRFC~~Dedicated GPIO~~		Only for RF debug. It should not be pulled up. Cannot be multiplexed into general-purpose GPIOs.
GRFC_18	241	IO			
SPI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI3_CS	201	DO	Chip selection signal		1.8V power domain. Only support master mode.
SPI3_CLK	200	DO	Clock signal		
SPI3_MOSI	248	DO	Master out slave in		
SPI3_MISO	247	DI	Master in salve out		
I2S Interfaces					

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Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
MI2S_2_WS	203	DO	I2S word select signal		1.8V power domain.
MI2S_2_DATA0	249	IO	I2S DATA0 signal		1.8V power domain.
MI2S_2_SCK	250	DO	I2S serial clock signal		1.8V power domain.
MI2S_2_DATA1	251	IO	I2S DATA1 signal		1.8V power domain.
MI2S_2_MCLK	114	DO	I2S main clock signal		1.8V power domain.
LPI_MI2S_SCLK	212	DO	LPI_I2S serial clock signal		1.8V power domain. Cannot be multiplexed into a general-purpose GPIO.
LPI_MI2S_WS	156	DO	LPI_I2S word select		
LPI_MI2S_DATA0	154	IO	LPI_I2S signal data0		
LPI_MI2S_DATA1	155	IO	LPI_I2S signal data1		
Emergency Download Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	57	DI	Force the module to enter emergency download mode		Pulled up to LDO13A_1P8 during power-up will force the module to enter emergency download mode.
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BAT_PLUS	27	AI	Battery voltage detection differential input (+)		Must be connected.
BAT_MINUS	28	AI	Battery voltage detection differential input (-)		Must be connected.
BAT_THERM	29	AI	Battery temperature detection		Internally pulled up. Externally connected to GND via a 47KΩ NTC resistor.
GNSS_PPS_OUT	202	DO	LNA enable control		1.8V power domain; It should not be pulled up.

CBL_PWR_N	22	DI	Used for configuring auto power-on		If customers require automatic power-on, this pin should be shorted-to-ground.
DP_AUX_P	221	AI/ AO	DisplayPort auxiliary channel (+)		
DP_AUX_N	220	AI/ AO	DisplayPort auxiliary channel (-)		
Reserved pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	17, 213, 214, 215, 216, 217, 222, 235		Reserved pins		Keep these pins open.

NOTE

[1] uUSB refers to any USB interface except for USB Type-C.

3.4. Power Supply

3.4.1. Power Supply Pins

SC66 provides three VBAT pins, two VDD_RF pins and one VPH_PWR pin. VBAT pins must be connected to an external power supply. VDD_RF pins are used to connect bypass capacitors of external RF Power supply, so as to eliminate voltage fluctuation of RF part. VPH_PWR is used for powering other devices.

3.4.2. Decrease Voltage Drop

The power supply range of the module is from 3.55V to 4.4V, and the recommended value is 4.0V. The power supply performance, such as load capacity, voltage ripple, etc. directly influences the module’s performance and stability. Under ultimate conditions, the module may have a transient peak current up to 3A. If the power supply capability is not sufficient, there will be voltage drops, and if the voltage drops below 2.85V, the module will be powered off automatically. Therefore, please make sure the input voltage will never drop below 2.85V.

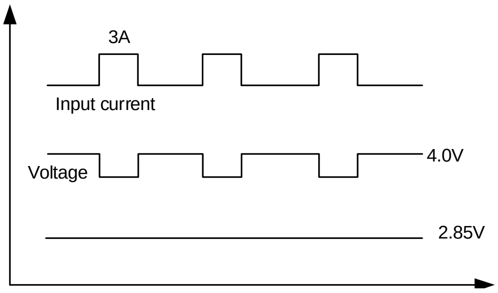


Figure 3: Voltage Drop Sample

To prevent the voltage from dropping below 2.85V, a bypass capacitor of about 100µF with low ESR (ESR=0.7Ω) should be used, and a multi-layer ceramic chip capacitor (MLCC) array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100nF, 33pF, 10pF) for composing the MLCC array, and place these capacitors close to VBAT/VDD_RF pins. The width of VBAT trace should be no less than 3mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to get a stable power source, it is suggested to use a 0.5W TVS and place it as close to the VBAT pins as possible to increase voltage surge withstand capability. The following figure shows the structure of the power supply.

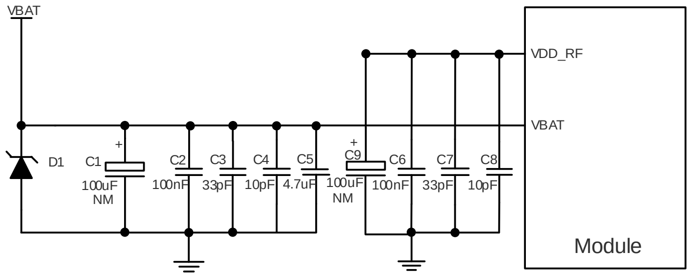


Figure 4: Structure of Power Supply

3.4.3. Reference Design for Power Supply

The power design for the module is very important, as the performance of module largely depends on the power source. The power supply of SC66 should be able to provide sufficient current up to 3A at least. By default, it is recommended to use a battery to supply power for SC66. But if battery is not intended to be used, it is recommended to use a regulator for SC66. If the voltage difference between the input and output is not too high, it is suggested to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5V input power source which adopts an LDO (MIC29502WU) from MICROCHIP. The typical output voltage is 4.0V and the maximum rated current is 5.0A.

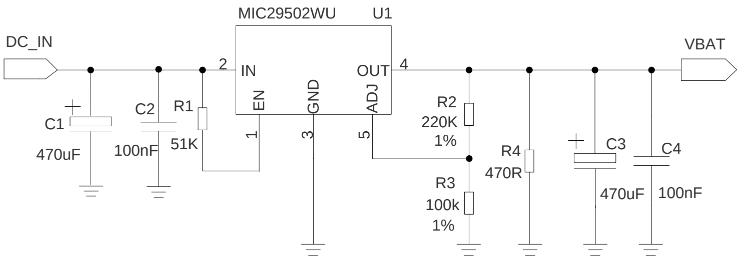


Figure 5: Referfence Circuit of Power Supply

NOTES

1. It is recommended to switch off the power supply when the module is in abnormal state, and then switch on the power to restart the module.
2. The module supports battery charging function by default. If the above power supply design is adopted, please make sure the charging function is disabled by software, or connect VBAT to Schottky diode in series to avoid the reverse current to the power supply chip.
3. When the battery power is reduced to 0%, the system will trigger automatic shutdown, so the design of power supply should be consistent with the configuration of fuel gauge driver.

3.5. Turn on and off Scenarios

3.5.1. Turn on the Module Using PWRKEY

The module can be turned on by driving PWRKEY pin to a low level for at least 3ms. PWRKEY pin is pulled to 1.8V internally. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

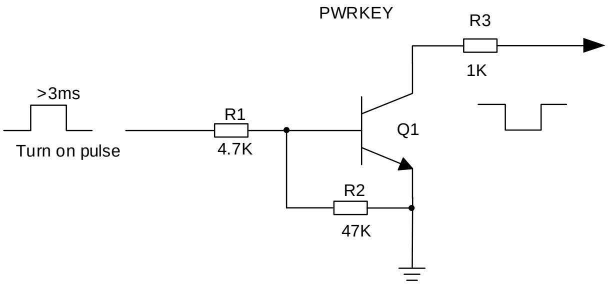


Figure 6: Turn on the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. For ESD protection, A TVS component placed near the button and a 1kΩ resistor connected to the PWRKEY in series are indispensable. A reference circuit is shown in the following figure:

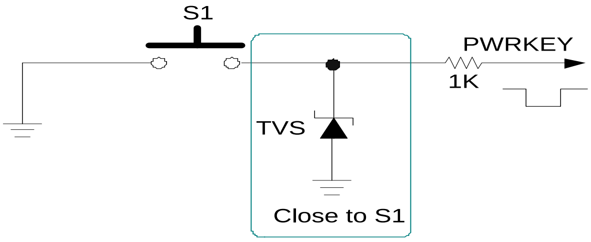


Figure 7: Turn on the Module Using Keystroke

The timing of turning on Module is illustrated in the following figure.

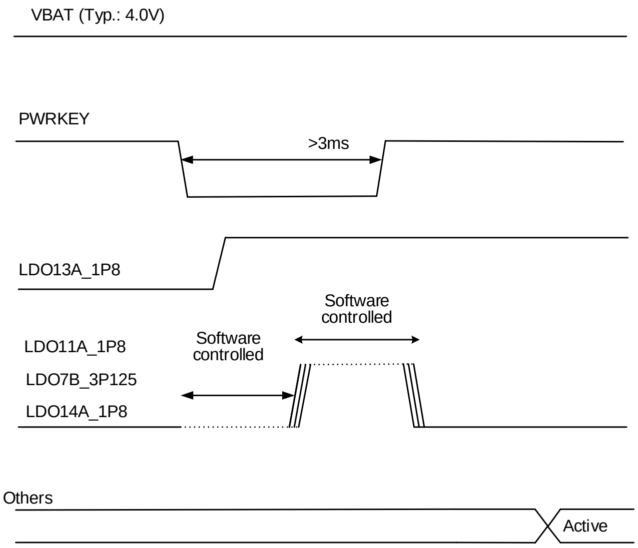


Figure 8: Timing of Turning on Module

NOTE

Make sure that VBAT is stable before pulling down PWRKEY pin. The recommended time between them is no less than 30ms. PWRKEY cannot be pulled down all the time.

3.5.2. Turn on the Module Automatically

The module can be turned on automatically with CBL_PWR_N. A reference circuit is shown below:

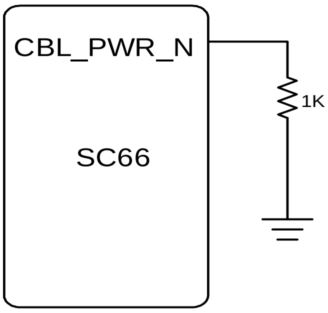


Figure 9: Turn on the Module Automatically

NOTE

If the module is turned on automatically through CBL_PWR_N, then it cannot be turned off unless the battery is removed.

3.5.3. Reboot/Turn off the Module

Pull down PWRKEY for at least 1s, and then choose to turn off or reboot the module when the prompt window comes up.

Another way to reboot the module is to drive PWRKEY to a low level for at least 8s. The restart scenario is illustrated in the following figure.

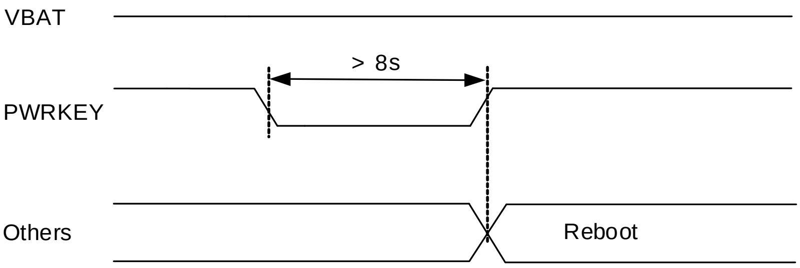


Figure 10: Timing of Rebooting Module

3.6. VRTC Interface

The RTC (Real Time Clock) can be powered by an external power source through VRTC when the module is powered down and there is no power supply for the VBAT. The external power source can be a rechargeable battery (such as a button cell battery) according to application demands. A reference circuit design is shown .

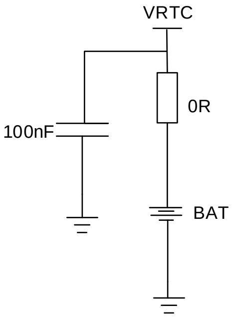


Figure 11: RTC Powered by a Rechargeable Button Cell Battery

NOTES

1. When VBAT is disconnected, the recommended input voltage range for VRTC is 2.1V~3.25V and the recommended typical value is 3.0V.
2. When powered by VBAT, the RTC error is 100ppm. When powered by VRTC, the RTC error is about 200ppm.
3. If a rechargeable battery is used, the ESR of battery should be less than 2KΩ, and it is recommended to use the MS621FE FL11E of SEIKO.
4. If RTC function is not needed, then it is recommended to connect a 47uF capacitor to the VRTC interface.

3.7. Power Output

SC66 supports output of regulated voltages for peripheral circuits. During application, it is recommended to connect a 33pF and a 10pF capacitor in parallel in the circuit to suppress high frequency noise.

Table 10: Power Description

Pin Name	Default Voltage (V)	Drive Current (mA)	Idle
LDO13A_1P8	1.8	20	Keep
LDO11A_1P8	1.8	150	/
LDO3B_2P8	2.8	600	/
LDO7B_3P125	3.125	150	/
LDO14A_1P8	1.8	150	Keep
SD_VDD	2.95	600	/
SD_PU_VDD	2.95	50	/
USIM1_VDD	1.8/2.95	150	/
USIM2_VDD	1.8/2.95	150	/
VPH_PWR	Equal to VBAT voltage	1000	Keep

3.8. Battery Charge and Management

SC66 module supports a fully programmable switch-mode Li-ion battery charge function. It can charge single-cell Li-ion and Li-polymer batteries. Switching charging with Quick Charge 3.0 and 4.0 supports up to 3.0A. The battery charger of SC66 module supports trickle charging, pre-charge, constant current charging and constant voltage charging modes, which optimize the charging procedure for Li-ion and Li-polymer batteries.

- **Trickle charging:** When the battery voltage is below 2.1V, a 45mA trickle charging current is applied to the battery.
- **Pre-charge:** When the battery voltage is charged up and is between 2.4V and 3.0V (the maximum pre-charge voltage is 2.4V~3.0V programmable, 3.0V by default), the system will enter pre-charge mode. The charging current is 500mA (100mA~1500mA programmable, 500mA by default).

- **Constant current mode (CC mode):** When the battery voltage is increased to between the maximum pre-charge voltage and 4.35V (3.6V~4.5V programmable, 4.35V by default), the system will switch to CC mode. The charging current is programmable from 0mA~3000mA. The default charging current is 500mA for USB charging and 2A for adapter.
- **Constant voltage mode (CV mode):** When the battery voltage reaches the final value 4.35V, the system will switch to CV mode and the charging current will decrease gradually. When the charging current reduces to about 100mA, the charging is completed.

Table 11: Pin Definition of Charging Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	41, 42	PI/PO	Charging power input. Power supply output for OTG device. USB/charger insertion detection.	Vmax=10V Vmin=3.6V Vnorm=5.0V
VBAT	36, 37, 38	PI/PO	Power supply for the module	Vmax=4.4V Vmin=3.55V Vnorm=4.0V
BAT_PLUS	27	AI	Differential input signal of battery voltage detection (+)	Must be connected
BAT_MINUS	28	AI	Differential input signal of battery voltage detection (-)	Must be connected
BAT_THERM	29	AI	Battery temperature detection	Internally pulled up. Externally connected to GND via a 47KΩ NTC resistor.

SC66 module supports battery temperature detection in the condition that the battery integrates a thermistor (47K 1% NTC thermistor with B-constant of 4050K by default; SDNT1608X473F4050FTF of SUNLORD is recommended) and the thermistor is connected to VBAT_THERM pin. If VBAT_THERM pin is not connected, there will be malfunctions such as boot error, battery charging failure, battery level display error, etc.

A reference design for battery charging circuit is shown below.

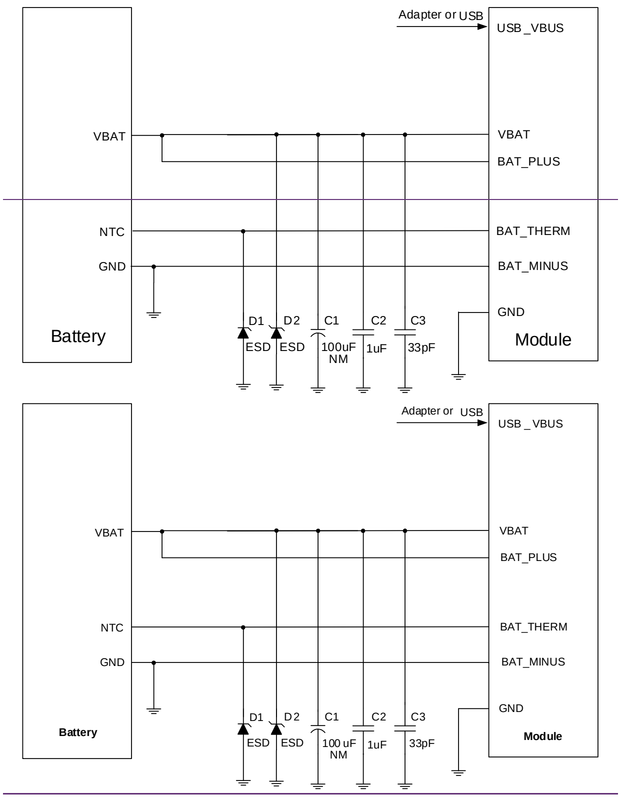


Figure 12: Reference Design for Battery Charging Circuit

SC66 offers a fuel gauge algorithm that is able to accurately estimate the battery's state by current and voltage monitor techniques. Using precise measurements of battery voltage, current, and temperature, the fuel gauge provides a dependable state of charge estimate throughout the entire life of the battery and across a broad range of operating conditions. It effectively protects the battery from over-discharging, and also allows users to estimate the battery life based on the battery level so as to timely save important data before completely power-down.

Mobile devices such as mobile phones and handheld POS systems are powered by batteries. When different batteries are utilized, the charging and discharging curve has to be modified correspondingly so as to achieve the best effect.

If thermistor is not available in the battery, or adapter is utilized for powering the module, then there is only a need for VBAT and GND connection. In this case, the system may be unable to detect the battery, which will cause power-on failure. In order to avoid this, VBAT_THERM should be connected to GND with a 47KΩ resistor. BAT_PLUS and BAT_MINUS must be connected, otherwise there may be abnormalities in use of the module. Among them, BAT_PLUS and BAT_MINUS are used for battery level detection, and they should be routed as differential pair to ensure accuracy.

USB_VBUS can be powered by external power or USB adapter, mainly used for USB detection and battery charging. The input of USB_VBUS is 3.6V~10V, and the typical working voltage is 5V. The SC66 module supports the charge management of Li-ion and Li-polymer batteries, but different types or capacities of batteries require different charging parameters, and the maximum charging current can reach 3A.

3.9. USB Interfaces

SC66 provides two USB interfaces which comply with the USB 3.1/2.0 specifications and support super speed (5Gbps) on USB 3.1, high speed (480Mbps) on USB 2.0 and full speed (12Mbps) modes. These USB interfaces can be used for AT command transmission, data transmission, software debugging and software upgrading.

3.9.1. Type-C Interface

3.9.1.1. USB Type-C Mode

The Type-C interface has one USB 2.0 compliant high-speed differential data pair (USB1_HS_DP/M) and two USB 3.1 compliant super-speed differential data pairs (USB_SS1_RX_P/M, USB_SS1_TX_P/M and USB_SS2_RX_P/M, USB_SS2_TX_P/M).

When Type-C is plugged in right-side up, USB_CC1 will detect the external device, and the data will be transmitted through USB_SS1; when it is plugged in upside down, USB_CC2 will detect the external device, and the data will be transmitted through USB_SS2.

The following table shows the pin definition of USB Type-C interface.

Table 12: Pin Definition of Type-C Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	41, 42	PI/PO	Charging power input; Power supply output for OTG device; USB/Charger insertion detection.	Vmax=10V Vmin=4.0V Vnorm=5.0V
USB1_HS_DM	33	IO	USB 2.0 differential data bus (-)	90Ω differential impedance.

USB1_HS_DP	32	IO	USB 2.0 differential data bus (+)	
USB_SS1_RX_P	171	AI	USB 3.1 differential receive (+)	
USB_SS1_RX_M	172	AI	USB 3.1 differential receive (-)	
USB_SS1_TX_P	174	AO	USB 3.1 channel 1 differential transmit (+)	
USB_SS1_TX_M	175	AO	USB 3.1 channel 1 differential transmit (-)	
USB_SS2_RX_M	161	AI	USB 3.1 channel 2 differential receive (-)	
USB_SS2_RX_P	162	AI	USB 3.1 channel 2 differential receive (+)	
USB_SS2_TX_M	164	AO	USB 3.1 channel 2 differential transmit (-)	
USB_SS2_TX_P	165	AO	USB 3.1 channel 2 differential transmit (+)	
UUSB_TYPEC	23	DI	uUSB & USB Type-C configuration selection pin	When USB Type-C is used, it should be connected to VPH_PWR through a 10KΩ resistor. When uUSB is used, it should be connected to GND through a 10KΩ resistor. Cannot be multiplexed into a general-purpose GPIO.
USB_CC2	223	AI	USB Type-C control detection pin 2	
USB_CC1	224	AI	USB Type-C control detection pin 1	When Micro USB is used, it can be used as USB_ID pin.
SS_DIR_IN	21	DI	CC status detection pin	When Type-C is used, it should be connected to SS_DIR_OUT; When uUSB is used, it should be connected to GND.

				Cannot be multiplexed into a general-purpose GPIO.
SS_DIR_OUT	226	DO	CC status output pin	

The following is a reference design for Type-C interface:

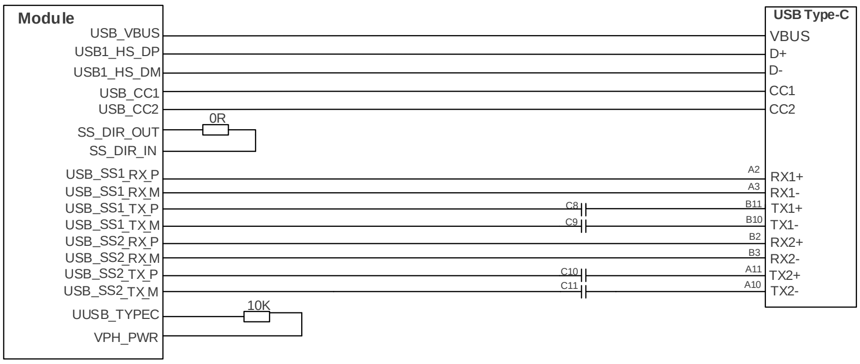


Figure 13: USB Type-C Interface Reference Design

3.9.1.2. DisplayPort Mode

SC66 supports DisplayPort mode with 4 lanes up to 4K@30ps over USB Type-C. The DisplayPort mode and USB Type-C mode cannot operate simultaneously. In the DisplayPort Mode, USB2.0 can be supported simultaneously and USB 3.1 cannot be supported simultaneously. The pin descriptions in USB Type-C/DisplayPort mode is listed below:

Table 13: Pin Descriptions in USB/DisplayPort Mode

Pin Name	USB Type-C Mode	DisplayPort Mode
USB_SS2_RX_P/M	USB_SS2_RX_P/M	DP_LANE0_P/M
USB_SS2_TX_P/M	USB_SS2_TX_P/M	DP_LANE1_P/M
USB_SS1_RX_P/M	USB_SS1_RX_P/M	DP_LANE3_P/M
USB_SS1_TX_P/M	USB_SS1_TX_P/M	DP_LANE2_P/M
DP_AUX_P/N	SBU1/2	AUX_P/N

USB1_HS_DP/DM	USB1_HS_DP/DM	USB1_HS_DP/M
USB_CC1/CC2	USB_CC1/CC2	HOTPLUG_DET/Vconn
USB_VBUS	USB_VBUS	USB_VBUS
GND	GND	GND

The reference design of DisplayPort is shown below:

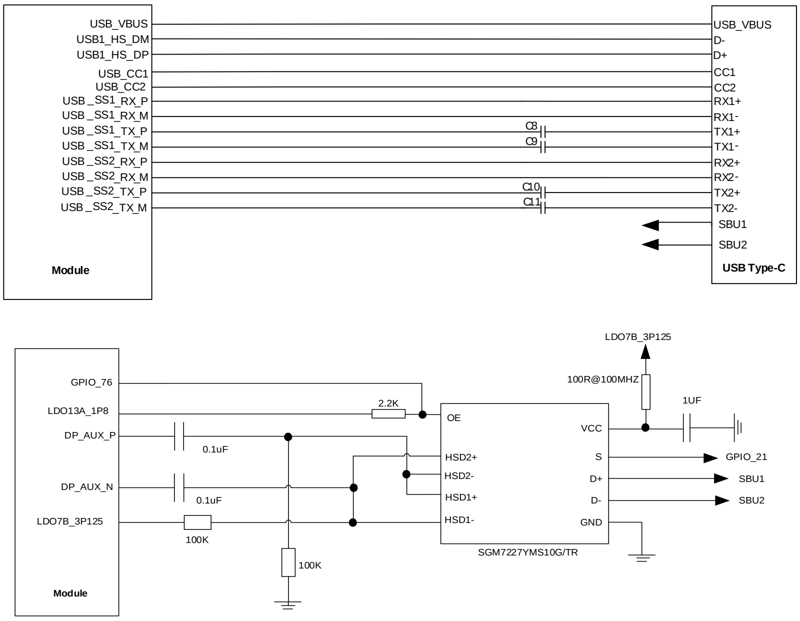


Figure 14: DisplayPort Reference Design

3.9.2. Micro USB Interface

SC66 supports USB Type-C interface by default. Micro USB can be used via software configuration.

Micro-USB interface can be supported through USB1_HS_DP/M or USB2_HS_DP/M. Micro-USB interface configured by USB1_HS_DP/M supports OTG and that configured by USB2_HS_DP/M only supports Host mode.

Table 14: USB1 & USB2 Pin Description

Pin Name	Pin No.	I/O	Description	Comment
USB1_HS_DM	33	IO	USB 2.0 differential data bus (-)	USB 2.0 standard compliant; Support OTG.
USB1_HS_DP	32	IO	USB 2.0 differential data bus (+)	
USB2_HS_DM	25	IO	USB 2.0 differential data bus (-)	USB 2.0 standard compliant; Only support host mode.
USB2_HS_DP	26	IO	USB 2.0 differential data bus (+)	

The reference circuit of Micro USB interface configured by using USB1:

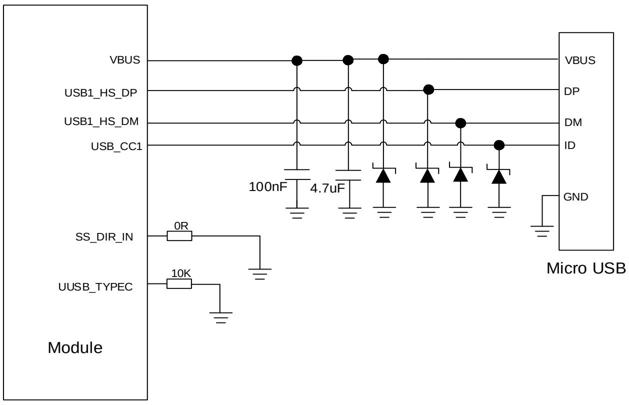


Figure 15: Micro USB Interface

The reference circuit of Host mode configured by USB2:

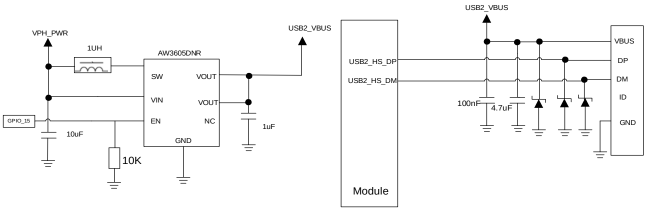


Figure 16: USB2 Host

3.9.3. USB Interface Design Considerations

Table 15: USB Trace Length Inside the Module

Pin No.	Signal	Length (mm)	Length Difference (DP-DM)
32	USB1_HS_DP	46.15	1.20
33	USB1_HS_DM	44.95	
171	USB_SS1_RX_P	39.75	0.00
172	USB_SS1_RX_M	39.75	
174	USB_SS1_TX_P	35.75	0.00
175	USB_SS1_TX_M	35.75	
162	USB_SS2_RX_P	31.6	0.16
161	USB_SS2_RX_M	31.6	
165	USB_SS2_TX_P	37.7	0.40
164	USB_SS2_TX_M	37.3	
26	USB2_HS_DP	40.75	-0.20
25	USB2_HS_DM	40.95	
221	DP_AUX_P	41.95	0.90
220	DP_AUX_N	41.05	

In order to ensure USB performance, please follow the following principles while designing USB interface.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90Ω.
- The ground reference plane must be continuous, without any cuts or any holes under the USB signals, to ensure impedance continuity.
- Pay attention to the influence of junction capacitance of ESD protection devices on USB data lines. Typically, the capacitance value should be less than 2pF for USB 2.0 and less than 0.2pF for USB 3.1 besides. Keep the ESD protection devices as close as possible to the USB connector.
- Do not route signal traces under crystals, oscillators, magnetic devices, audio signal, and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- USB 3.1 signal line should not be routed under the RF signal line. Crossing and parallel with RF signal line is forbidden. The signal isolation between USB3.0 signal and RF signal should be＞90db, otherwise, the RF signal will be seriously affected.
- Make sure the trace length difference between USB 3.1 RX and USB 3.1 TX differential pairs do not exceed 0.7mm.
- Make sure the trace length difference between USB 2.0 DP and USB 2.0 DM differential pairs do not exceed 2mm.
- For USB 3.1, the spacing between Rx and Tx signal traces should be three times the signal trace width. The spacing between USB 3.1 signal trace and other signal lines should be four times the signal trace width. For USB 2.0, the spacing between DP and DM signal traces should be three times the signal trace width and the spacing between USB 2.0 signal trace and other signal lines should be four times the signal trace width.
- For DisplayPort, the routing length difference between DP_AUX_N and DP_AUX_P should be less than 7mm.

3.10. UART Interfaces

The module provides the following four UART interfaces:

- UART6: 4-wire UART interface, hardware flow control supported.
- DEBUG UART: 2-wire UART interface, used for debugging by default.
- UART1: 2-wire UART interface.
- LPI_ UART _2: 2-wire low power UART interface.

The following table shows the pin definition of UART interfaces.

Table 16: Pin Definition of UART Interfaces

Pin Name	Pin No.	I/O	Description	Comment
DEBUG_TXD	5	DO	DEBUG UART transmit	1.8 power domain.

			data	
DEBUG_RXD	6	DI	DEBUG UART receive data	1.8 power domain.
UART1_TXD	7	DO	UART1 transmit data	1.8 power domain.
UART1_RXD	8	DI	UART1 receive data	1.8 power domain.
UART6_RXD	198	DI	UART6 receive data	1.8 power domain.
UART6_TXD	199	DO	UART6 transmit data	1.8 power domain.
UART6_CTS	246	DI	UART6 clear to send	1.8 power domain.
UART6_RTS	245	DO	UART6 request to send	1.8 power domain.
LPI_UART_2_TXD	60	DO	LPI_UART_2 transmit data	1.8 power domain. Cannot be multiplexed into general-purpose GPIOs..
LPI_UART_2_RXD	61	DI	LPI_UART_2 receive data	

UART6 is a 4-wire UART interface with 1.8V power domain. A level translator chip should be used if customers' application is equipped with a 3.3V UART interface. A level translator chip TXS0104EPWR provided by Texas Instruments is recommended.

The following figure shows a reference design.

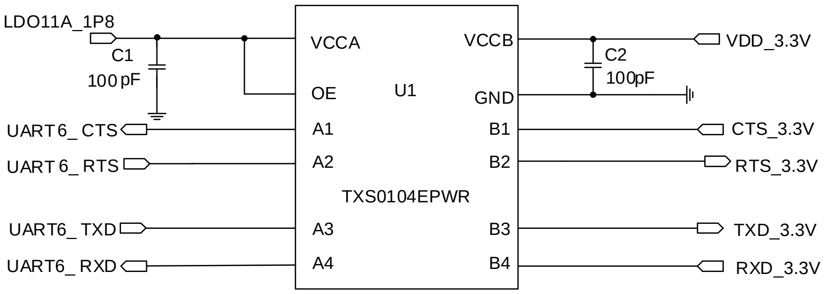


Figure 17: Reference Circuit with Level Translator Chip (for UART6)

The following figure is an example of connection between SC66 and PC. A voltage level translator and a RS-232 level translator chip are recommended to be added between the module and PC, as shown below:

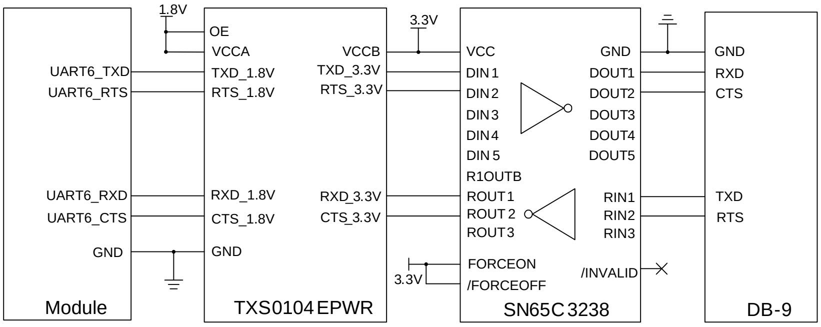


Figure 18: RS232 Level Match Circuit (for UART5)

NOTE

Debug UART, UART1, LPI_UART_2 are similar to UART6. Please refer to UART6 reference circuit design for DEBUG UART, UART1, LPI_UART_2.

3.11. (U)SIM Interfaces

SC66 provides two (U)SIM interfaces which both meet ETSI and IMT-2000 requirements. Dual SIM Dual Standby is supported by default. Both 1.8V and 2.95V (U)SIM cards are supported, and the (U)SIM interfaces are powered by the dedicated low dropout regulators in SC66 module.

Table 17: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_DET	145	DI	(U)SIM1 card insertion detection	Active low. Need external pull-up to 1.8V. If unused, keep this pin open. Disabled by default, and can be enabled through software configuration.
USIM1_RST	144	DO	(U)SIM1 card reset signal	Cannot be multiplexed into general-purpose GPIOs.
USIM1_CLK	143	DO	(U)SIM1 card clock signal	
USIM1_DATA	142	IO	(U)SIM1 card data signal	Pull up to USIM1 with a 10KΩ resistor.

				Cannot be multiplexed into a general-purpose GPIO.
USIM1_VDD	141	PO	(U)SIM1 card power supply	Either 1.8V or 2.95V (U)SIM card is supported.
USIM2_DET	256	DI	(U)SIM2 card insertion detection	Active low. Need external pull-up to1.8V. If unused, keep this pin open.
USIM2_RST	207	DO	(U)SIM2 card reset signal	Cannot be multiplexed into a general-purpose GPIO.
USIM2_CLK	208	DO	(U)SIM2 card clock signal	Cannot be multiplexed into a general-purpose GPIO.
USIM2_DATA	209	IO	(U)SIM2 card data signal	Pull up to USIM2 with a 10KΩ resistor. Cannot be multiplexed into a general-purpose GPIO.
USIM2_VDD	210	PO	(U)SIM2 card power supply	Either 1.8V or 2.95V (U)SIM card is supported.

SC66 supports (U)SIM card hot-plug via the USIM_DET pin, which is disabled by default and can be enabled through software configuration. A reference circuit for (U)SIM interface with an 8-pin (U)SIM card connector is shown below.

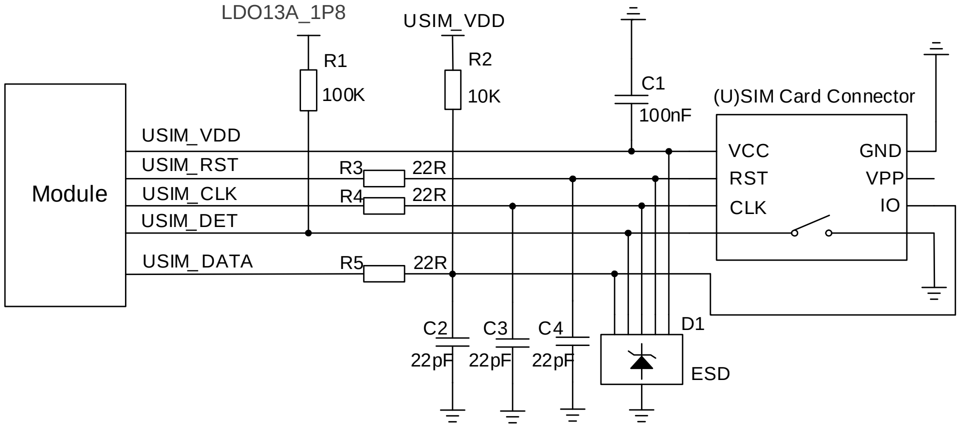


Figure 19: Reference Circuit for (U)SIM Interface with an 8-pin (U)SIM Card Connector

If there is no need to use USIM_DET, please keep it open. The following is a reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector.

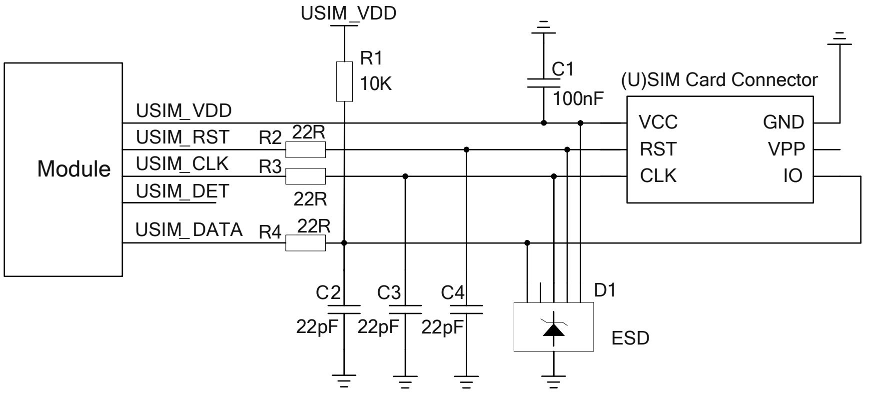


Figure 20: Reference Circuit for (U)SIM Interface with a 6-pin (U)SIM Card Connector

In order to ensure good performance and avoid damage of (U)SIM cards, please follow the criteria below in (U)SIM circuit design:

- Keep placement of (U)SIM card connector as close to the module as possible. Keep the trace length of (U)SIM card signals as less than 200mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- A filter capacitor shall be reserved for USIM_VDD, and its maximum capacitance should not exceed 1uF. The capacitor should be placed near to (U)SIM card.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with ground. USIM_RST also needs ground protection.
- In order to offer good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 50pF. The 22Ω resistors should be added in series between the module and (U)SIM card so as to suppress EMI spurious transmission and enhance ESD protection. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The 22pF capacitors should be added in parallel on USIM_DATA, USIM_VDD, USIM_CLK and USIM_RST signal lines so as to filter RF interference, and they should be placed as close to the (U)SIM card connector as possible.

3.12. SD Card Interface

SC66 module supports SD 3.0 specifications. The pin definition of the SD card interface is shown below.

Table 18: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment

SD_VDD	63	PO	Power supply for SD card	Vnorm=2.95V $I_O$max=600mA
SD_PU_VDD	179	PO	SD card pull-up power supply	Support 1.8V/2.95V power supply; The maximum drive current is 50mA.
SD_CLK	70	DO	High speed digital clock signal of SD card	Control characteristic impedance as 50Ω.
SD_CMD	69	IO	Command signal of SD card	
SD_DATA0	68	IO	High speed bidirectional digital signal lines of SD card	
SD_DATA1	67	IO		
SD_DATA2	66	IO		
SD_DATA3	65	IO		
SD_DET	64	DI	SD card insertion detection	Active low.

A reference circuit for SD card interface is shown below.

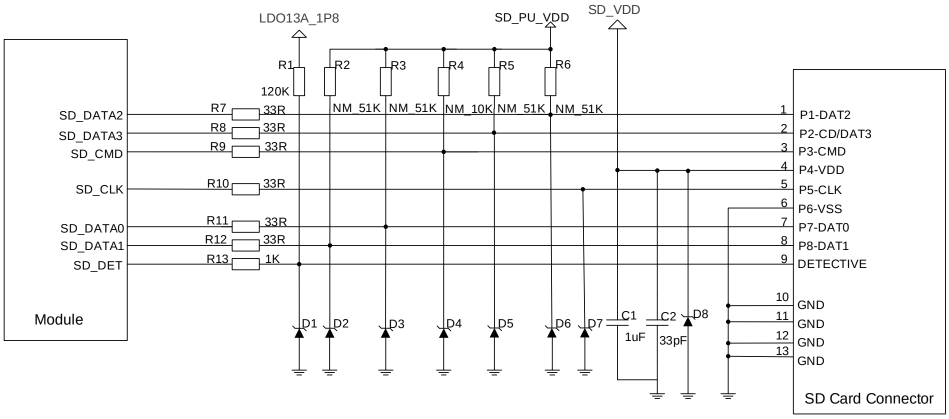


Figure 21: Reference Circuit for SD Card Interface

SD_VDD is a peripheral driver power supply for SD card. The maximum drive current is 600mA. Because of the high drive current, it is recommended that the trace width is 0.5mm or above. In order to ensure the stability of drive power, a 1uF and a 33pF capacitor should be added in parallel near the SD card connector.

CMD, CLK, DATA0, DATA1, DATA2 and DATA3 are all high speed signal lines. In PCB design, please control the characteristic impedance of them as 50Ω, and do not cross them with other traces. It is recommended to route the trace on the inner layer of PCB, and keep the same trace length for CLK, CMD, DATA0, DATA1, DATA2 and DATA3. CLK needs separate ground shielding.

Layout guidelines:

- Control impedance to 50Ω±10%, and ground shielding is required.
- The difference in trace lengths among the clock, data, and command signals should be less than 2 mm.
- The bus length should be less than 50mm.
- The spacing between signal lines should be 1.5 times the line width.
- The capacitive reactance of data signal line should be < 8 pF.

Table 19: SD Card Signal Trace Length Inside the Module

Pin No.	Signal	Length (mm)
70	SD_CLK	24.35
69	SD_CMD	24.30
68	SD_DATA0	24.30
67	SD_DATA1	24.30
66	SD_DATA2	24.25
65	SD_DATA3	24.30

3.13. GPIO Interfaces

SC66 has abundant GPIO interfaces with power domain of 1.8V. The pin definition is listed below.

Table 20: Pin Definition of GPIO Interfaces

Pin Name	Pin No.	GPIO	Default Status	Comment
GPIO_21	231	GPIO_21	B-PD:nppukp(1)	Wakeup (2)
GPIO_34	236	GPIO_34	B-PD:nppukp	
GPIO_40	238	GPIO_40	B-PD:nppukp	Wakeup

GPIO_41	237	GPIO_41	B-PD:nppukp	Wakeup
GPIO_55	178	GPIO_55	B-PD:nppukp	Wakeup
GPIO_56	177	GPIO_56	B-PD:nppukp	Wakeup
GPIO_72	239	GPIO_72	B-PD:nppukp	Wakeup
GPIO_73	59	GPIO_73	B-PD:nppukp	Wakeup
GPIO_74	58	GPIO_74	B-PD:nppukp	Wakeup
GPIO_76	232	GPIO_76	B-PD:nppukp	Wakeup
GPIO_77	240	GPIO_77	B-PD:nppukp	Wakeup
GPIO_12	228	GPIO_12	B-PD:nppukp	
GPIO_13	227	GPIO_13	B-PD:nppukp	Wakeup
GPIO_14	230	GPIO_14	B-PD:nppukp	
GPIO_15	229	GPIO_15	B-PD:nppukp	
GPIO_61	234	GPIO_61	B-PD:nppukp	
GPIO_03B	11	GPIO_03B	B-PD:nppukp	
GPIO_08B	13	GPIO_08B	B-PD:nppukp	
GPIO_04B	14	GPIO_04B	B-PD:nppukp	
GPIO_05B	15	GPIO_05B	B-PD:nppukp	
GPIO_11A	211	GPIO_11A	B-PD:nppukp	
GPIO_13A	233	GPIO_13A	B-PD:nppukp	

NOTES

1. 1) B: Bidirectional digital with CMOS input; PD:nppukp = Contains an internal pull-down.
2. 2) Wakeup: interrupt pins that can wake up the system.
3. More details about GPIO configuration, please refer to the *Quectel_SC66_GPIO_Configuration*.

3.14. I2C Interfaces

SC66 can provide up to five I2C Interfaces. As an open drain output, each I2C interface should be pulled up to 1.8V voltage. The SENSOR_I2C interface only supports sensors of the aDSP architecture. CAM_I2C bus is controlled by Linux Kernel code and supports connection to video output related devices.

Table 21: Pin Definition of I2C Interfaces

Pin Name	Pin No	I/O	Description	Comment
TP0_I2C_SCL	140	OD	TP I2C clock	Used for TP0.
TP0_I2C_SDA	206	OD	TP I2C data	
CAM_I2C_SCL0	75	OD	CAM I2C clock	Used for rear and front camera.
CAM_I2C_SDA0	76	OD	CAM I2C data	
CAM_I2C_SCL1	196	OD	CAM I2C clock	Used for depth camera.
CAM_I2C_SDA1	197	OD	CAM I2C data	
SENSOR_I2C_SCL	131	OD	Sensor I2C clock	Used for sensor. Cannot be multiplexed into general-purpose GPIOs.
SENSOR_I2C_SDA	132	OD	Sensor I2C data	
TP1_I2C_SCL	205	OD	TP I2C clock	Used for TP1.
TP1_I2C_SDA	204	OD	TP I2C data	

3.15. I2S Interfaces

SC66 provides two I2S interfaces with one of them is a low-power I2S. The reference power domain of the interface is 1.8V.

Table 22: Pin Definition of I2S Interfaces

Pin Name	Pin No	I/O	Description	Comment
MI2S_2_WS	203	DO	I2S word select (L/R)	
MI2S_2_DATA0	249	IO	I2S serial data0 channel	
MI2S_2_SCK	250	DO	I2S serial clock	

MI2S_2_DATA1	251	IO	I2S serial data1 channel	
MI2S_2_MCLK	114	DO	I2S main clock	
LPI_MI2S_SCLK	212	DO	LPI_I2S serial clock signal	Cannot be multiplexed into general-purpose GPIOs.
LPI_MI2S_WS	156	DO	LPI_I2S word select	
LPI_MI2S_DATA0	154	IO	LPI_I2S signal data0	
LPI_MI2S_DATA1	155	IO	LPI_I2S signal data1	

3.16. SPI Interface

SC66 provides one SPI interface which only supports master mode.

Table 23: Pin Definition of SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI3_MOSI	248	DO	Master out slave in of SPI interface	
SPI3_MISO	247	DI	Master in salve out of SPI interface	
SPI3_CS	201	DO	Chip selection signal of SPI interface	
SPI3_CLK	200	DO	Clock signal of SPI interface	

3.17. ADC Interfaces

SC66 provides two analog-to-digital converter (ADC) interfaces, and the pin definition is shown below.

Table 24: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	151	AI	Universal ADC interface	The maximum input voltage is 1.8V.
ADC1	153	AI	Universal ADC interface	The maximum input voltage is 1.8V.

The resolution of the ADC is up to 15 bits.

3.18. LCM Interfaces

SC66 video output interface (LCM interface) is based on MIPI_DSI standard and supports 8 groups of high-speed differential data transmission and WQXGA display (resolution: 2560 × 1600), Support dual display, default DSI+DP (Type-C), optional DSI0+DSI1. Note that DSI1 does not support screens with command mode.

Table 25: Pin Definition of LCM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
LDO11A_1P8	10	PO	1.8V output power supply for LCM logic circuit and DSI	
LDO3B_2P8	12	PO	2.8V output power supply for LCM analog circuits	
PWM	152	DO	PWM signal output	Cannot be multiplexed into a general-purpose GPIO.
LCD0_RST	127	DO	LCD0 reset signal	It should not be pulled up.
LCD0_TE	126	DI	LCD0 tearing effect signal	
DSI0_CLK_N	116	AO	LCD0 MIPI clock signal (-)	
DSI0_CLK_P	115	AO	LCD0 MIPI clock signal (+)	
DSI0_LN0_N	118	AO	LCD0 MIPI lane 0 data signal (-)	
DSI0_LN0_P	117	AO	LCD0 MIPI lane 0 data signal (+)	
DSI0_LN1_N	120	AO	LCD0 MIPI lane 1 data signal (-)	
DSI0_LN1_P	119	AO	LCD0 MIPI lane 1 data signal (+)	
DSI0_LN2_N	122	AO	LCD0 MIPI lane 2 data	

			signal (-)	
DSI0_LN2_P	121	AO	LCD0 MIPI lane 2 data signal (+)	
DSI0_LN3_N	124	AO	LCD0 MIPI lane 3 data signal (-)	
DSI0_LN3_P	123	AO	LCD0 MIPI lane 3 data signal (+)	
DSI1_CLK_N	103	AO	LCD1 MIPI clock signal (-)	
DSI1_CLK_P	102	AO	LCD1 MIPI clock signal (+)	
DSI1_LN0_N	105	AO	LCD1 MIPI lane 0 data signal (-)	
DSI1_LN0_P	104	AO	LCD1 MIPI lane 0 data signal (+)	
DSI1_LN1_N	107	AO	LCD1 MIPI lane 1 data signal (-)	
DSI1_LN1_P	106	AO	LCD1 MIPI lane 1 data signal (+)	
DSI1_LN2_N	109	AO	LCD1 MIPI lane 2 data signal (-)	
DSI1_LN2_P	108	AO	LCD1 MIPI lane 2 data signal (+)	
DSI1_LN3_N	111	AO	LCD1 MIPI lane 3 data signal (-)	
DSI1_LN3_P	110	AO	LCD1 MIPI lane 3 data signal (+)	
LCD1_RST	113	DO	LCD1 reset signal	V_{OL}max=0.45V V_{OH}min=1.35V 1.8V power domain.

GPIO_40	238	DO	LCD1 PWM output	Used as a GPIO by default

The following are the reference designs for LCM interfaces. LCM can use external backlight drive circuit according to customer requirement. The reference design of the external backlight drive circuit is shown in the figure below, in which pins PWM (Pin 152 & Pin 238) can be used for backlight brightness adjustment.

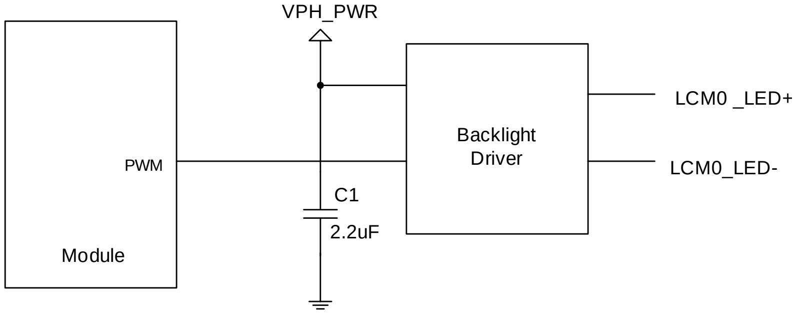


Figure 22: LCM0 External Backlight Driver Reference Circuit

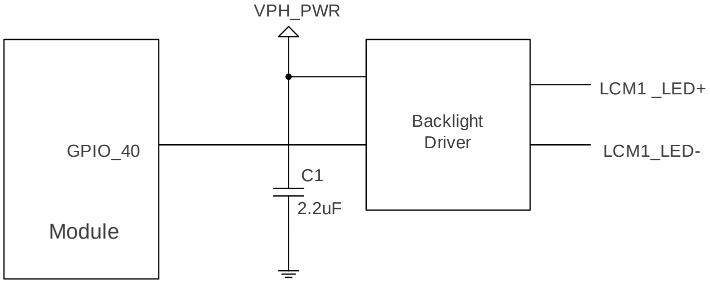


Figure 23: Reference Circuit Design for LCM1 Interface

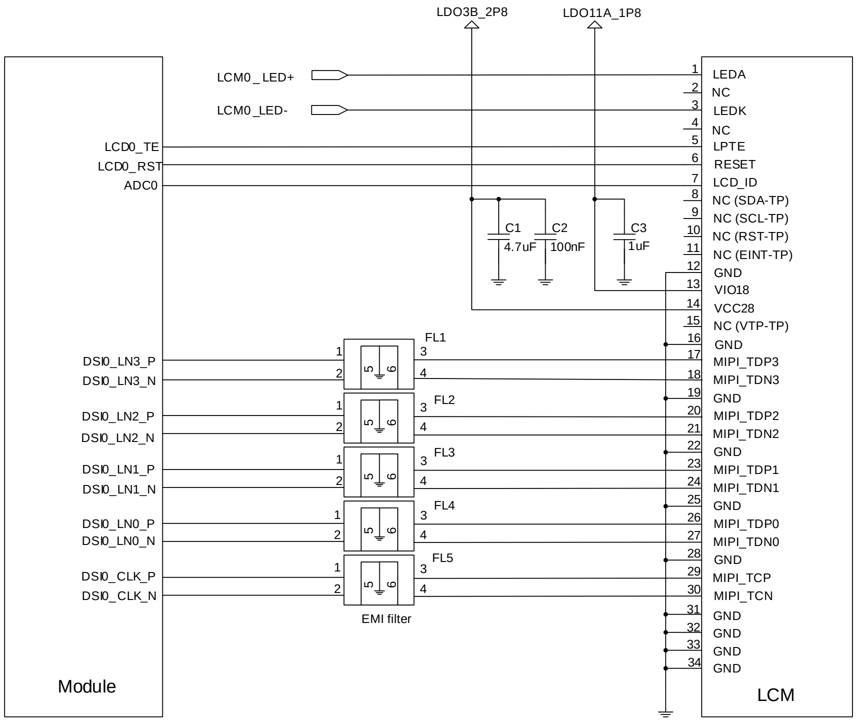


Figure 24: Reference Circuit Design for LCM0 Interface

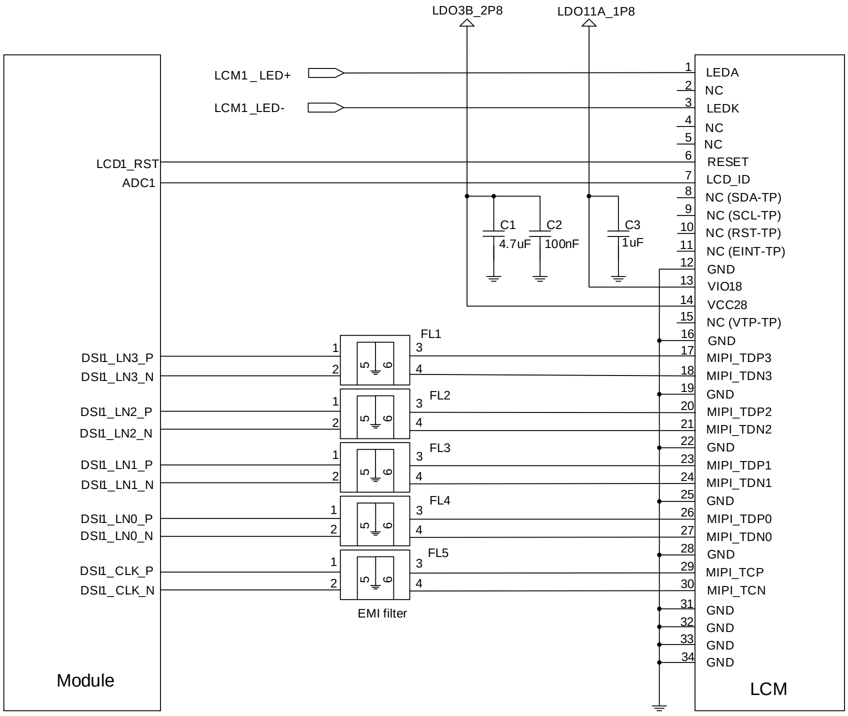


Figure 25: Reference Circuit Design for LCM1 Interface

MIPI are high speed signal lines. It is recommended that common-mode filters should be added in series near the LCM connector, so as to improve protection against electromagnetic radiation interference. ICMEF112P900MFR using ICT is recommended.

It is recommended to read the LCM ID register through MIPI when compatible design with other displays is required. If several LCM models share the same IC, it is recommended that LCM module factory burn the OTP register to distinguish different screens. Customers can also select the LCD_ID pin of LCM to connect the ADC pin of the SC66 module, but it should be noted that the output voltage of LCD_ID should not exceed the voltage range of the ADC pin.

3.19. Touch Panel Interfaces

SC66 provides two I2C interfaces for connection with Touch Panel (TP), and also provides the corresponding power supply and interrupt pins. The pin definition of touch panel interfaces is illustrated below.

Table 26: Pin Definition of Touch Panel Interfaces

Pin Name	Pin No	I/O	Description	Comment
LDO11A_1P8	10	PO	1.8V output power supply	Pull-up power supply of I2C Vnorm=1.8V $I_O$max=300mA
LDO3B_2P8	12	PO	2.8V output power supply for TP	TP power supply Vnom=2.8V Iomax=600mA
TP0_INT	139	DI	Interrupt signal of touch panel (TP0)	
TP0_RST	138	DO	Reset signal of touch panel (TP0)	
TP0_I2C_SCL SCL	140	OD	I2C clock signal of touch panel (TP0)	
TP0_I2C_SDA	206	OD	I2C data signal of touch panel (TP0)	
TP1_RST	136	DO	Reset signal of touch panel (TP1)	
TP1_INT	137	DI	Interrupt signal of touch panel (TP1)	
TP1_I2C_SCL	205	OD	I2C clock signal of touch panel (TP1)	
TP1_I2C_SDA	204	OD	I2C data signal of touch panel (TP1)	

A reference design for TP0 interface is shown below.

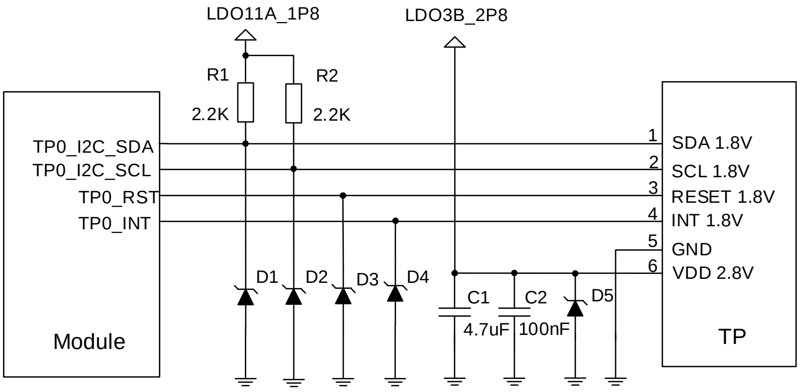


Figure 26: Reference Circuit Design for TP0 Interface

NOTE

The reference circuit design of TP1 is similar to that of TP0. Please refer to TP0 reference circuit design for TP1.

3.20. Camera Interfaces

Based on standard MIPI CSI input interface, SC66 module supports 3 cameras (4-lane + 4-lane + 4-lane) or 4 cameras (4-lane + 4-lane + 2-lane + 1-lane), with maximum pixels up to 24MP for SC66. The video and photo quality are determined by various factors such as camera sensor, camera lens quality, etc.

Table 27: Pin Definition of Camera Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GPIO_08B	13	DO	Rear camera DVDD power LDO enable pin	
GPIO_05B	15	IO	Front camera DVDD power LDO enable pin	
LDO11A_1P8	10	PO	1.8V output power supply Power for DOVDD	Vnorm=1.8V $I_O$max=150mA
LDO3B_2P8	12	PO	2.8V output power supply	Vnorm=2.8V $I_O$max=600mA

GPIO_04B	14	DO	Camera AVDD power LDO enable pin
CSI0_CLK_N	78	AI	MIPI clock signal of front camera (-)
CSI0_CLK_P	77	AI	MIPI clock signal of front camera (+)
CSI0_LN0_N	80	AI	MIPI lane 0 data signal of front camera (-)
CSI0_LN0_P	79	AI	MIPI lane 0 data signal of front camera (+)
CSI0_LN1_N	82	AI	MIPI lane 1 data signal of front camera (-)
CSI0_LN1_P	81	AI	MIPI lane 1 data signal of front camera (+)
CSI0_LN2_N	84	AI	MIPI lane 2 data signal of front camera (-)
CSI0_LN2_P	83	AI	MIPI lane 2 data signal of front camera (+)
CSI0_LN3_N	86	AI	MIPI lane 3 data signal of front camera (-)
CSI0_LN3_P	85	AI	MIPI lane 3 data signal of front camera (+)
CSI1_CLK_N	89	AI	MIPI clock signal of rear camera (-)
CSI1_CLK_P	88	AI	MIPI clock signal of rear camera (+)
CSI1_LN0_N	91	AI	MIPI data0 signal of rear camera (-)
CSI1_LN0_P	90	AI	MIPI data0 signal of rear camera (+)
CSI1_LN1_N	93	AI	MIPI data 1 signal of rear camera (-)
CSI1_LN1_P	92	AI	MIPI data 1 signal of rear camera (+)
CSI1_LN2_N	95	AI	MIPI data 2 signal of rear camera (-)
CSI1_LN2_P	94	AI	MIPI data 2 signal of rear camera (+)
CSI1_LN3_N	97	AI	MIPI data 3 signal of rear camera (-)
CSI1_LN3_P	96	AI	MIPI data 3 signal of rear camera (+)
CSI2_CLK_N	184	AI	MIPI clock signal of depth camera (-)
CSI2_CLK_P	183	AI	MIPI clock signal of depth camera (+)

CSI2_LN0_N	186	AI	MIPI data 0 signal of depth camera (-)
CSI2_LN0_P	185	AI	MIPI data 0 signal of depth camera (+)
CSI2_LN1_N	188	AI	MIPI lane 1 data signal of depth camera (-)
CSI2_LN1_P	187	AI	MIPI lane 1 data signal of depth camera (+)
CSI2_LN2_N	190	AI	MIPI lane 2 data signal of depth camera (-)
CSI2_LN2_P	189	AI	MIPI lane 2 data signal of depth camera (+)
CSI2_LN3_N	192	AI	MIPI lane 3 data signal of depth camera (-)
CSI2_LN3_P	191	AI	MIPI lane 3 data signal of depth camera (+)
MCAM_MCLK	99	DO	Rear camera clock signal
SCAM_MCLK	100	DO	Front camera clock signal
DCAM_MCLK	194	DO	Depth camera clock signal
MCAM_RST	74	DO	Rear camera reset signal
SCAM_RST	72	DO	Front camera reset signal
DCAM_RST	180	DO	Depth camera reset signal
MCAM_PWDN	73	DO	Rear camera PWDN signal
SCAM_PWDN	71	DO	Front camera PWDN signal
DCAM_PWDN	181	DO	Depth camera PWDN signal
CAM_I2C_SCL0	75	OD	I2C clock signal for rear and front cameras
CAM_I2C_SDA0	76	OD	I2C data signal for rear and front camera
CAM_I2C_SCL1	196	OD	I2C clock signal for depth camera
CAM_I2C_SDA1	197	OD	I2C data signal for depth camera

The following is a reference circuit design for dual camera applications:

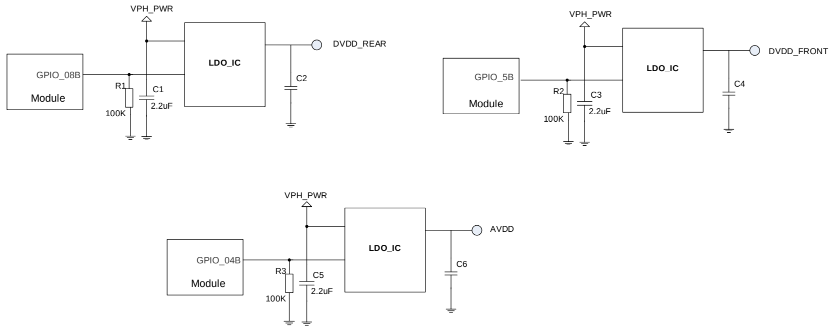


Figure 27: Reference Circuit Design for Dual Camera Applications

The following is a reference circuit design for dual camera applications.

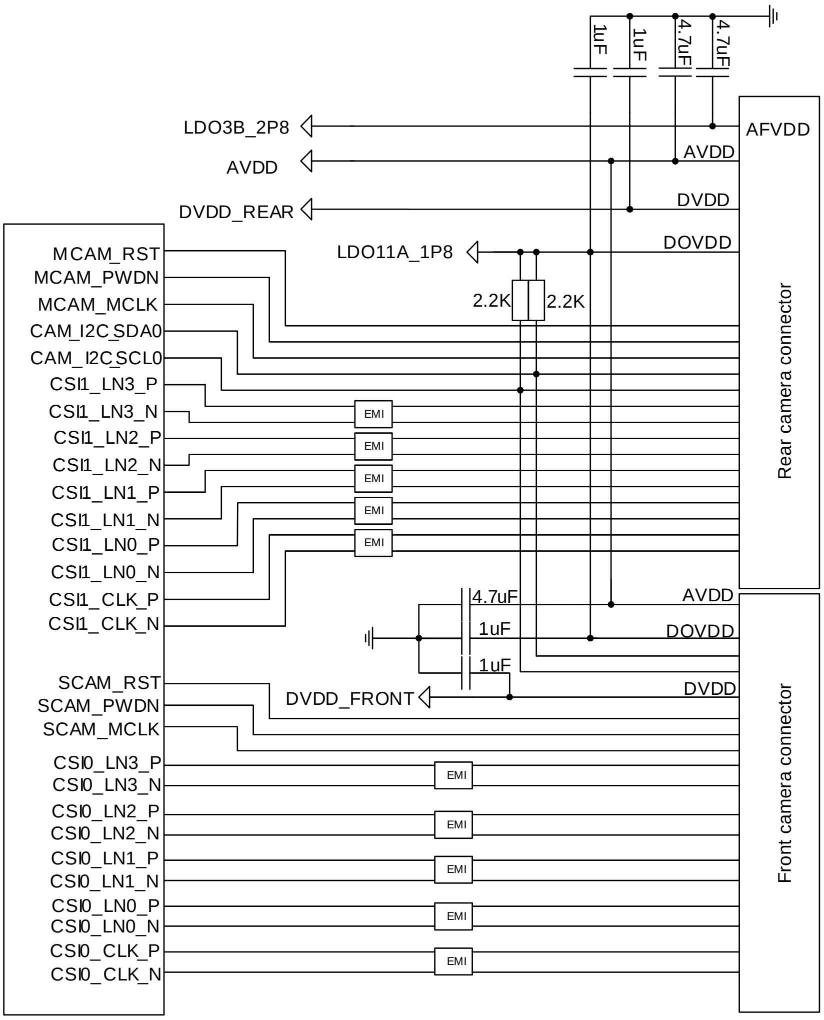


Figure 28: Reference Circuit Design for Two-Camera Applications

The following is a reference circuit design for three-camera applications.

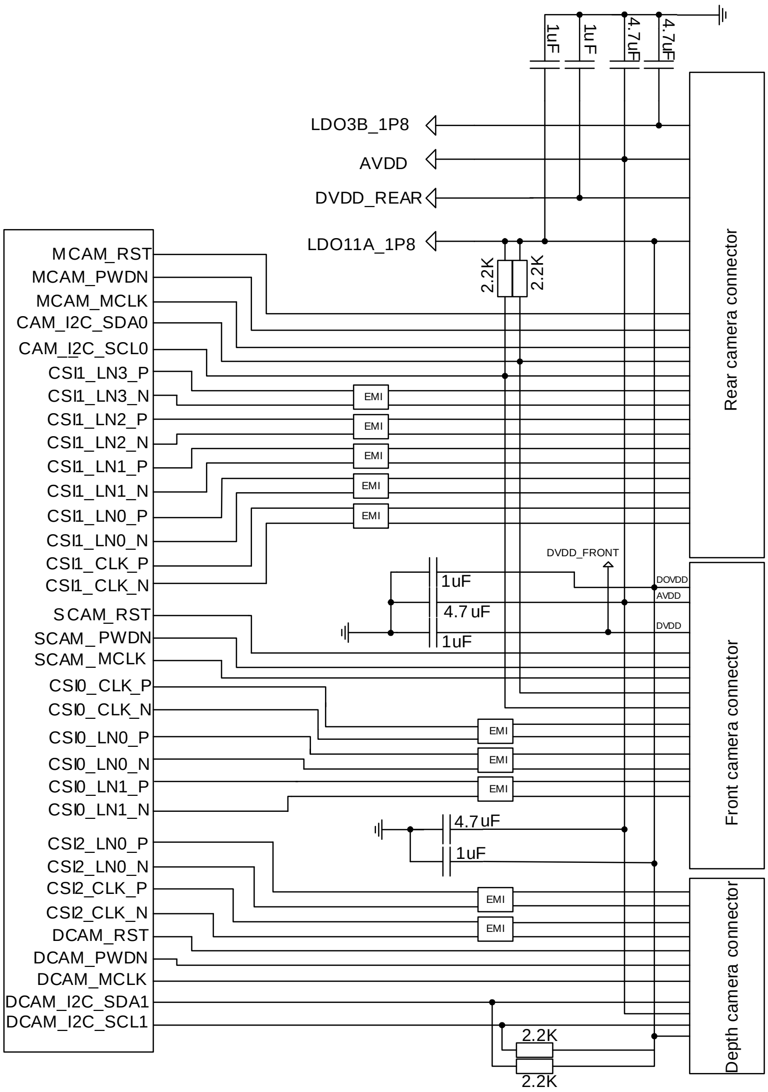


Figure 29: Reference Circuit Design for Three-Camera Applications

NOTES

1. CSI2_LN2_P/N, CSI2_LN3_P/N can be multiplexed into MIPI signal lines of the fourth camera.
2. LN2 can be configured as DATA, LN3 as CLK and GPIO_34 as MCLK.
3. I2C interfaces are connected with CAM_I2C_SDA1 and CAM_I2C_SCL1.
4. Reset and PWDN signals are configured by using general-purpose GPIOs.

3.20.1. Design Considerations

- Special attention should be paid to the pin definition of LCM/camera connectors. Assure the SC66 and the connectors are correctly connected.
- MIPI are high speed signal lines, supporting maximum data rate up to 2.1Gbps. The differential impedance should be controlled to 85Ω. Additionally, it is recommended to route the trace on the inner layer of PCB, and do not cross it with other traces. For the same group of DSI or CSI signals, all the MIPI traces should keep the same length.
- Be assure the reference ground plane for CSI/DSI is complete and integral, without any cut or void.
- Route the camera CLK signal in the inner layer of the PCB between ground fills
- Route CSI and DSI traces according to the following rules:
  a) The intra-pair spacing should be one-time the trace width
  b) The inter-pair spacing should be 1.5 times the trace width
  c) The spacing to other signal lines should be 2.5 times the trace width
- Route MIPI traces according to the following rules:
  a) The CSI trace length should not exceed 170mm and the DSI trace length should not exceed 110mm;
  b) Control the differential impedance to 85Ω±10%;
  c) Control intra-lane length difference within 0.7mm;
  d) Control inter-lane length difference within 1.4mm.

Table 28: Trace Length of MIPI Differential Pairs Inside the Module

Pin No.	Signal	Length (mm)	Length Difference (P-N)
116	DSI0_CLK_N	27.35	-0.05
115	DSI0_CLK_P	27.30	
118	DSI0_LN0_N	27.00	0.00
117	DSI0_LN0_P	27.00	
120	DSI0_LN1_N	26.65	-0.05
119	DSI0_LN1_P	26.60	

122	DSI0_LN2_N	26.55	0.00
121	DSI0_LN2_P	26.55	
124	DSI0_LN3_N	27.30	0.00
123	DSI0_LN3_P	27.30	
103	DSI1_CLK_N	23.20	0.30
102	DSI1_CLK_P	23.50	
105	DSI1_LN0_N	28.00	0.00
104	DSI1_LN0_P	28.00	
107	DSI1_LN1_N	30.00	0.00
106	DSI1_LN1_P	30.00	
109	DSI1_LN2_N	33.50	0.00
108	DSI1_LN2_P	33.50	
111	DSI1_LN3_N	37.50	0.00
110	DSI1_LN3_P	37.50	
89	CSI1_CLK_N	16.00	0.00
88	CSI1_CLK_P	16.00	
91	CSI1_LN0_N	15.00	0.00
90	CSI1_LN0_P	15.00	
93	CSI1_LN1_N	12.20	-0.10
92	CSI1_LN1_P	12.10	
95	CSI1_LN2_N	10.70	-0.00
94	CSI1_LN2_P	10.70	
97	CSI1_LN3_N	9.40	0.00
96	CSI1_LN3_P	9.40	
184	CSI2_CLK_N	17.50	0.20
183	CSI2_CLK_P	17.70	

186	CSI2_LN0_N	15.30	0.00
185	CSI2_LN0_P	15.30	
188	CSI2_LN1_N	7.40	0.00
187	CSI2_LN1_P	7.40	
190	CSI2_LN2_N	4.05	0.20
189	CSI2_LN2_P	4.25	
192	CSI2_LN3_N	7.05	0.00
191	CSI2_LN3_P	7.05	
78	CSI0_CLK_N	25.35	0.00
77	CSI0_CLK_P	25.35	
80	CSI0_LN0_N	23.35	-0.10
79	CSI0_LN0_P	23.25	
82	CSI0_LN1_N	22.20	0.25
81	CSI0_LN1_P	22.45	
84	CSI0_LN2_N	20.05	0.00
83	CSI0_LN2_P	20.05	
86	CSI0_LN3_N	18.35	-0.30
85	CSI0_LN3_P	18.05	

3.21. Sensor Interfaces

SC66 module supports communication with sensors via I2C interfaces, and it supports various sensors such as acceleration sensor, gyroscopic sensor, compass, optical sensor, temperature sensor.

Table 29: Pin Definition of Sensor Interfaces

Pin Name	Pin No.	I/O	Description	Comment

SENSOR_I2C_SCL	131	OD	I2C clock signal of external sensor	Dedicated used for sensors. It cannot be used for touch panel, NFC, I2C keyboard etc. Cannot be multiplexed into general-purpose GPIOs.
SENSOR_I2C_SDA	132	OD	I2C data signal of external sensor	
ALPS_INT	253	DI	Interrupt signal of optical sensor	
MAG_INT	254	DI	Interrupt signal of geomagnetic sensor	
ACCL_INT	252	DI	Interrupt signal of acceleration sensor	
GYRO_INT	255	DI	Interrupt signal of gyroscopic sensor	
HALL_INT	218	DI	Interrupt signal of Hall sensor	

3.22. Audio Interfaces

SC66 module provides three analog input channels and three analog output channels. The following table shows the pin definition.

Table 30: Pin Definition of Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MIC1_P	44	AI	Microphone input for channel 1 (+)	
MIC1_M	45	AI	Microphone input for channel 1 (-)	
MIC_GND	168		Microphone reference ground	If unused, connect to the ground.
MIC2_P	46	AI	Microphone input for headset (+)	Headset microphone input.
MIC3_P	169	AI	Microphone input for secondary microphone (+)	Secondary microphone input.
MIC_BIAS	167	AO	Microphone bias voltage	

EAR_P	53	AO	Earpiece output (+)	
EAR_M	52	AO	Earpiece output (-)	
SPK_P	55	AO	Speaker output (+)	
SPK_M	54	AO	Speaker output (-)	
HPH_R	51	AO	Headphone right channel output	
HPH_REF	50	AI	Headphone reference ground	It should be connected to main GND
HPH_L	49	AO	Headphone left channel output	
HS_DET	48	AI	Headset insertion detection	High level by default.

- The module offers three audio input channels, including one differential input pair and two single-ended channels. The three sets of MICs are integrated with internal bias voltage.
- The output voltage range of MIC_BIAS is programmable between 1.6V and 2.9V, and the maximum output current is 3mA.
- The earpiece interface uses differential output.
- The loudspeaker interface uses differential output as well. The output channel is available with a Class-D amplifier whose maximum output power is 1.5W when the load is 8Ω.
- The headphone interface features stereo left and right channel output, and headphone insertion detection function is supported.

3.22.1. Reference Circuit Design for Microphone Interface

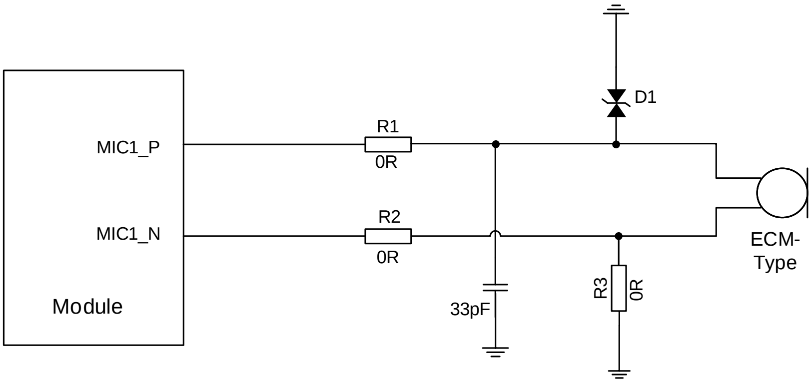


Figure 30: Reference Circuit Design for Analog ECM-type Microphone

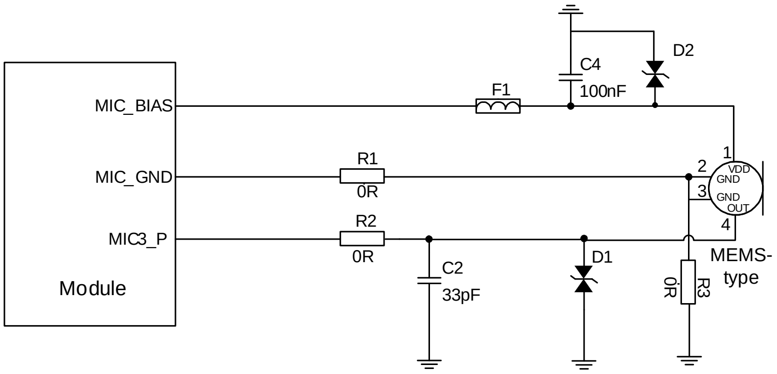


Figure 31: Reference Circuit Design for MEMS-type Microphone

3.22.2. Reference Circuit Design for Earpiece Interface

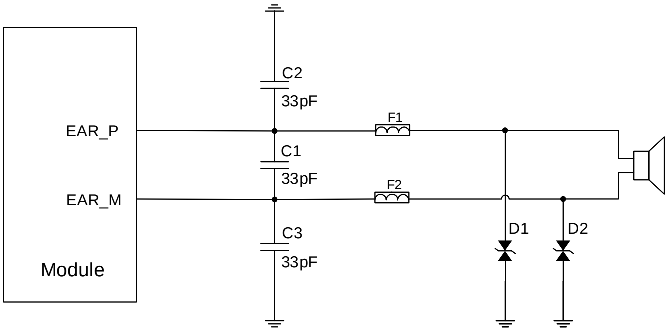


Figure 32: Reference Circuit Design for Earpiece Interface

3.22.3. Reference Circuit Design for Headphone Interface

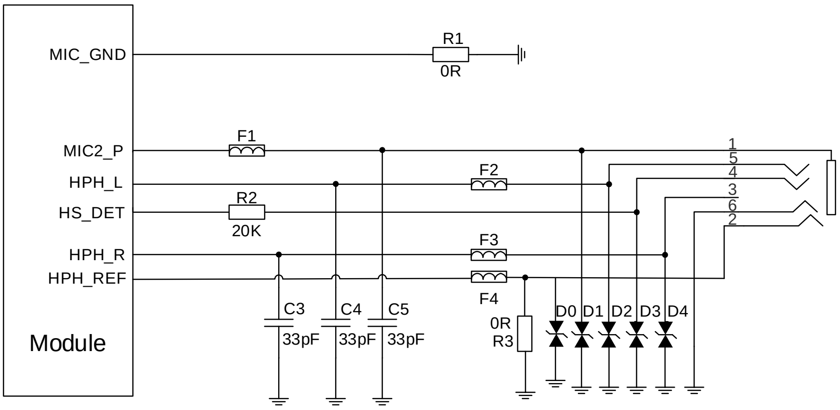


Figure 33: Reference Circuit Design for Headphone Interface

3.22.4. Reference Circuit Design for Loudspeaker Interface

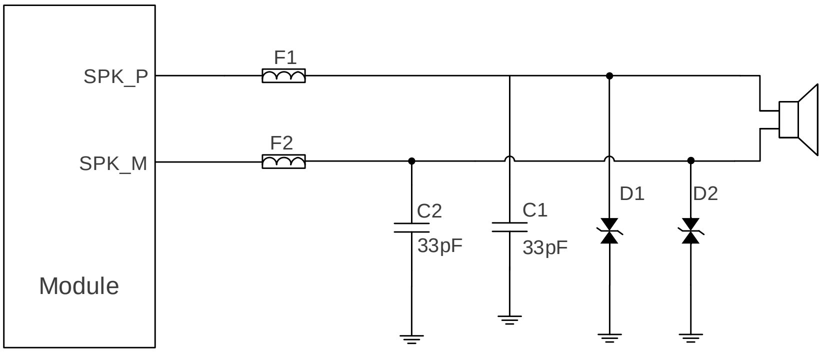


Figure 34: Reference Circuit Design for Loudspeaker Interface

3.22.5. Audio Interfaces Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10pF and 33pF) for filtering out RF interference, thus reducing TDD noise. The 33pF capacitor is applied for filtering out RF interference when the module is transmitting at EGSM900. Without placing this capacitor, TDD noise could be heard. The 10pF capacitor here is used for filtering out RF interference at DCS1800. Please note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, customers would have to discuss with their capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

The severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. In some cases, EGSM900 TDD noise is more severe; while in other cases, DCS1800 TDD noise is more obvious. Therefore, a suitable capacitor can be selected based on the test results. Sometimes, even no RF filtering capacitor is required.

In order to decrease radio or other signal interference, RF antennas should be placed away from audio interfaces and audio traces. Power traces cannot be parallel with and also should be far away from the audio traces.

The differential audio traces must be routed according to the differential signal layout rule.

3.23. Emergency Download Interface

USB_BOOT is an emergency download interface. Pulling up LDO13A_1P8 during power-up will force the module into emergency download mode. This is an emergency option when there are failures such as abnormal startup or operation. For convenient future firmware upgrade and debugging in the future, please reserve the reference circuit design shown below.

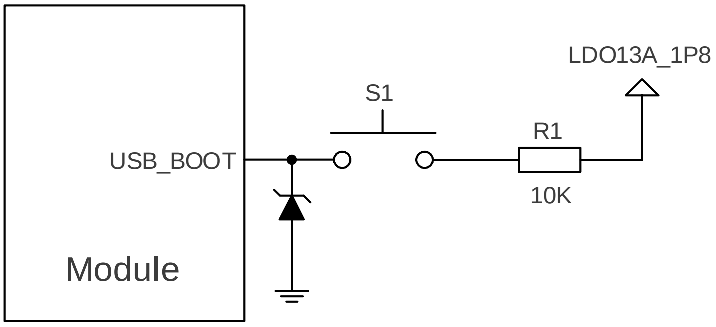


Figure 35: Reference Circuit Design for Emergency Download Interface

4 Wi-Fi and BT

SC66 module provides a shared antenna interface ANT_WIFI/BT for Wi-Fi and Bluetooth (BT) functions. The interface impedance is 50Ω. External antennas such as PCB antenna, sucker antenna and ceramic antenna can be connected to the module via these interfaces, so as to achieve Wi-Fi and BT functions. In addition, SC66-A*, SC66-J*, SC66-E* and SC66-MW* also support ANT_WIFI_MIMO antenna interface to achieve higher Wi-Fi performance.

4.1. Wi-Fi Overview

SC66 module supports 2.4GHz and 5GHz dual-band WLAN wireless communication based on IEEE 802.11a/b/g/n/ac standard protocols. The maximum data rate is up to 433Mbps. The features are below:

- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode
- Support WAPI SMS4 hardware encryption
- Support AP mode
- Support Wi-Fi Direct
- Support MCS 0-7 for HT20 and HT40
- Support MCS 0-8 for VHT20
- Support MCS 0-9 for VHT40 and VHT80

4.1.1. Wi-Fi Performance

The following table lists the Wi-Fi transmitting and receiving performance of SC66 module.

Table 31: Wi-Fi Transmitting Performance

	Standard	Rate	Output Power
2.4GHz	802.11b	1Mbps	16dBm±2.5dB
	802.11b	11Mbps	16dBm±2.5dB
	802.11g	6Mbps	16dBm±2.5dB
	802.11g	54Mbps	14dBm±2.5dB

	802.11n HT20	MCS0	15dBm±2.5dB
	802.11n HT20	MCS7	13dBm±2.5dB
	802.11n HT40	MCS0	14dBm±2.5dB
	802.11n HT40	MCS7	13dBm±2.5dB
5GHz	802.11a	6Mbps	15dBm±2.5dB
	802.11a	54Mbps	13dBm±2.5dB
	802.11n HT20	MCS0	15dBm±2.5dB
	802.11n HT20	MCS7	13dBm±2.5dB
	802.11n HT40	MCS0	15dBm±2.5dB
	802.11n HT40	MCS7	13dBm±2.5dB
	802.11ac VHT20	MCS0	14dBm±2.5dB
	802.11ac VHT20	MCS8	13dBm±2.5dB
	802.11ac VHT40	MCS0	13dBm±2.5dB
	802.11ac VHT40	MCS9	12dBm±2.5dB
	802.11ac VHT80	MCS0	13dBm±2.5dB
	802.11ac VHT80	MCS9	12dBm±2.5dB

Table 32: Wi-Fi Receiving Performance

	Standard	Rate	Sensitivity
2.4GHz	802.11b	1Mbps	-96dBm
	802.11b	11Mbps	-87dBm
	802.11g	6Mbps	-91dBm
	802.11g	54Mbps	-73dBm
	802.11n HT20	MCS0	-90dBm
	802.11n HT20	MCS7	-72dBm

	802.11n HT40	MCS0	-87dBm
	802.11n HT40	MCS7	-68dBm
5GHz	802.11a	6Mbps	-90dBm
	802.11a	54Mbps	-70dBm
	802.11n HT20	MCS0	-88dBm
	802.11n HT20	MCS7	-69dBm
	802.11n HT40	MCS0	-86dBm
	802.11n HT40	MCS7	-66dBm
	802.11ac VHT20	MCS8	-68dBm
	802.11ac VHT40	MCS9	-64dBm
	802.11ac VHT80	MCS9	-60dBm

Reference specifications are listed below:

- IEEE 802.11n WLAN MAC and PHY, October 2009+IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- IEEE Std 802.11b, IEEE Std 802.11d, IEEE Std 802.11e, IEEE Std 802.11g, IEEE Std 802.11i: IEEE 802.11-2007 WLAN MAC and PHY, June 2007

4.1.2. Wi-Fi MIMO Design Guidelines

Bad design of DSI trace and layout may cause reduced Wi-Fi MIMO receiving sensitivity. In order to avoid this, please follow the design rules listed below:

- Control the impedance of either feeder line or PCB trace in Wi-Fi MIMO part to 50Ω, and keep the trace length as short as possible;
- Maximize the distance between Wi-Fi MIMO antenna and DSI trace (including trace routing and antenna layout) to avoid mutual interference.
- Space for locating EMI filter should be reserved in DSI trace.

4.2. BT Overview

SC66 module supports BT5.0 (BR/EDR+BLE) specifications, as well as GFSK, 8-DPSK, π/4-DQPSK modulation modes.

- Maximally support up to 7 wireless connections.
- Maximally support up to 3.5 piconets at the same time.
- Support one SCO or eSCO (Extended Synchronous Connection Oriented) connection.

The BR/EDR channel bandwidth is 1MHz, and can accommodate 79 channels. The BLE channel bandwidth is 2MHz, and can accommodate 40 channels.

Table 33: BT Data Rate and Versions

Version	Data rate	Maximum Application Throughput	Comment
1.2	1Mbit/s	> 80Kbit/s	
2.0+EDR	3Mbit/s	> 80Kbit/s	
3.0+HS	24Mbit/s	Reference to 3.0+HS	
4.0	24Mbit/s	Reference to 4.0 LE	
5.0	48Mbit/S	Reference to 5.0	

Reference specifications are listed below:

- Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0+EDR/2.1/2.1+EDR/3.0/3.0+HS, August 6, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009
- Bluetooth 5.0 RF-PHY Cover Standard: RF-PHY.TS.5.0.0, December 06, 2016

4.2.1. BT Performance

The following table lists the BT transmitting and receiving performance of SC66 module.

Table 34: BT Transmitting and Receiving Performance

Transmitter Performance			
Packet Types	DH5	2-DH5	3-DH5
Transmitting Power	10dBm±2.5dB	8dBm±2.5dB	8dBm±2.5dB
Receiver Performance			
Packet Types	DH5	2-DH5	3-DH5
Receiving Sensitivity	-92dBm	-91dBm	-83dBm

5 GNSS

SC66 module integrates a Qualcomm IZat™ GNSS engine (Gen 9) which supports multiple positioning and navigation systems including GPS, GLONASS and BeiDou. With an embedded LNA, the module provides greatly improved positioning accuracy.

5.1. GNSS Performance

The following table lists the GNSS performance of SC66 module in conduction mode.

Table 35: GNSS Performance

Parameter	Description	Typ.	Unit
Sensitivity (GNSS)	Cold start	-144	dBm
	Reacquisition	-157	dBm
	Tracking	-157	dBm
TTFF (GNSS)	Cold start	32	s
	Warm start	30	s
	Hot start	5	s
Static Drift (GNSS)	CEP-50	10	m

5.2. GNSS RF Design Guidelines

Bad design of antenna and layout may cause reduced GNSS receiving sensitivity, longer GNSS positioning time, or reduced positioning accuracy. In order to avoid these, please follow the design rules listed below:

- Maximize the distance among GNSS antenna, main antenna, Rx-diversity/MIMO antenna, Wi-Fi/BT antenna, FM antenna and Wi-Fi MIMO antenna (including trace routing and antenna layout) to avoid mutual interference.
- In user systems, GNSS RF signal lines and RF components should be placed far away from high speed circuits, switched-mode power supplies, power inductors, the clock circuit of single-chip microcomputers, etc.
- For applications with harsh electromagnetic environment or high ESD-protection requirements, it is recommended to add ESD protective diodes for the antenna interface. Only diodes with ultra-low junction capacitance such as 0.5pF can be selected. Otherwise, there will be effects on the impedance characteristic of RF circuit loop, or attenuation of bypass RF signal may be caused.
- Control the impedance of either feeder line or PCB trace to 50Ω, and keep the trace length as short as possible.
- Refer to ***Chapter 6.3*** for GNSS antenna reference circuit designs.

6 Antenna Interfaces

SC66 provides six antenna interfaces for main antenna, Rx-diversity/MIMO antenna, GNSS antenna, Wi-Fi/BT antenna, FM antenna and Wi-Fi MIMO antenna, respectively. The antenna interfaces have an impedance of 50Ω.

6.1. Main/Rx-diversity Antenna Interfaces

The pin definition of main/Rx-diversity antenna interfaces is shown below.

Table 36: Pin Definition of Main/Rx-diversity Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	19	IO	Main antenna interface	50Ω impedance
ANT_DRX	149	AI	Diversity antenna interface	50Ω impedance

The operating frequencies of SC66 module are listed in the following tables.

Table 37: SC66-CE* Operating Frequencies

3GPP Band	Receive	Transmit	Unit
EGSM900	925~960	880~915	MHz
DCS1800	1805~1880	1710~1785	MHz
WCDMA B1	2110~2170	1920~1980	MHz
WCDMA B8	925~960	880~915	MHz
EVDO/CDMA BC0	869~894	824~849	MHz
TD-SCDMA B34	2010~2025	2010~2025	MHz

TD-SCDMA B39	1880~1920	1880~1920	MHz
LTE-FDD B1	2110~2170	1920~1980	MHz
LTE-FDD B3	1805~1880	1710~1785	MHz
LTE-FDD B5	869~894	824~849	MHz
LTE-FDD B8	925~960	880~915	MHz
LTE-TDD B34	2010~2025	2010~2025	MHz
LTE-TDD B38	2570~2620	2570~2620	MHz
LTE-TDD B39	1880~1920	1880~1920	MHz
LTE-TDD B40	2300~2400	2300~2400	MHz
LTE-TDD B41 1)	2555~2655	2555~2655	MHz

Table 38: SC66-A* Operating Frequencies

3GPP Band	Receive	Transmit	Unit
WCDMA B2	1930~1990	1850~1910	MHz
WCDMA B4	2110~2155	1710~1755	MHz
WCDMA B5	869~894	824~849	MHz
LTE-FDD B2	1930~1990	1850~1910	MHz
LTE-FDD B4	2110~2155	1710~1755	MHz
LTE-FDD B5	869~894	824~849	MHz
LTE-FDD B7	2620~2690	2500~2570	MHz
LTE-FDD B12	729~746	699~716	MHz
LTE-FDD B13	746~756	777~787	MHz
LTE-FDD B14	758~768	788~798	MHz
LTE-FDD B17	734~746	704~716	MHz
LTE-FDD B25	1930~1995	1850~1915	MHz

LTE-FDD B26	859~894	814~849	MHz
LTE-FDD B66	2110~2200	1710~1780	MHz
LTE-FDD B71	617~652	663~698	MHz
LTE-TDD B41 2)	2496~2690	2496~2690	MHz

Table 39: SC66-J* Operating Frequencies

3GPP Band	Receive	Transmit	Unit
WCDMA B1	2110~2170	1920~1980	MHz
WCDMA B6	875~885	830~840	MHz
WCDMA B8	925~960	880~915	MHz
WCDMA B19	875~890	830~845	MHz
LTE-FDD B1	2110~2170	1920~1980	MHz
LTE-FDD B3	1805~1880	1710~1785	MHz
LTE-FDD B5	869~894	824~849	MHz
LTE-FDD B8	925~960	880~915	MHz
LTE-FDD B11	1476~1496	1428~1448	MHz
LTE-FDD B18	860~875	815~830	MHz
LTE-FDD B19	875~890	830~845	MHz
LTE-FDD B21	1496~1511	1448~1463	MHz
LTE-FDD B26	859~894	814~849	MHz
LTE-FDD B28 (A+B)	758~803	703~748	MHz
LTE-TDD B41 1)	2535~2655	2535~2655	MHz

Table 40: SC66-E* Operating Frequencies

3GPP Band	Receive	Transmit	Unit
GSM850	869~894	824~849	MHz
EGSM900	925~960	880~915	MHz
DCS1800	1805~1880	1710~1785	MHz
PCS1900	1930~1990	1850~1910	MHz
WCDMA B1	2110~2170	1920~1980	MHz
WCDMA B2	1930~1990	1850~1910	MHz
WCDMA B4	2110~2155	1710~1755	MHz
WCDMA B5	869~894	824~849	MHz
WCDMA B8	925~960	880~915	MHz
LTE-FDD B1	2110~2170	1920~1980	MHz
LTE-FDD B2	1930~1990	1850~1910	MHz
LTE-FDD B3	1805~1880	1710~1785	MHz
LTE-FDD B4	2110~2155	1710~1755	MHz
LTE-FDD B5	869~894	824~849	MHz
LTE-FDD B7	2620~2690	2500~2570	MHz
LTE-FDD B8	925~960	880~915	MHz
LTE-FDD B20	791~821	832~862	MHz
LTE-FDD B28 (A+B)	758~803	703~748	MHz
LTE-TDD B38	2570~2620	2570~2620	MHz
LTE-TDD B39	1880~1920	1880~1920	MHz
LTE-TDD B40	2300~2400	2300~2400	MHz
LTE-TDD B41 2)	2496~2690	2496~2690	MHz

NOTES

1. [1] The bandwidth of LTE-TDD B41 for SC66-CE* and SC66-J* is 120MHz (2535MHz~2655MHz), and the corresponding channel ranges from 40040 to 41240.
2. [2] The bandwidth of LTE-TDD B41 for SC66-A and SC66-E is 200MHz (2496MHZ~2690MHz), and the corresponding channel ranges from 39650 to 41589.
3. “*” means under development.

6.1.1. Main and Rx-diversity Antenna Interfaces Reference Design

A reference circuit design for main and Rx-diversity antenna interfaces is shown below. A π-type matching circuit for each antenna should be reserved for better RF performance, and the π-type matching components (R1/C1/C2, R2/C3/C4) should be placed as close to the antennas as possible. The capacitors are not mounted by default and resistors are 0Ω.

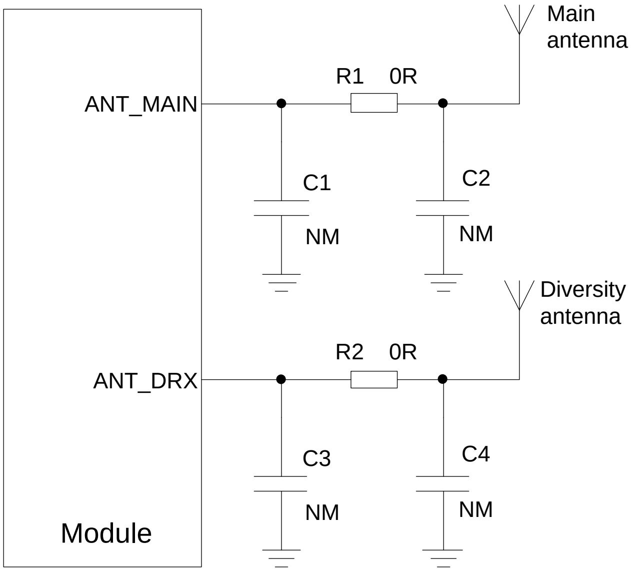


Figure 36: Reference Circuit Design for Main and Rx-diversity Antenna Interfaces

6.1.2. Reference Design of RF Layout

For user’s PCB, the characteristic impedance of all RF traces should be controlled to 50Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials’ dielectric constant, height from the reference ground to the signal layer (H), and the clearance between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip line or coplanar waveguide with different PCB structures.

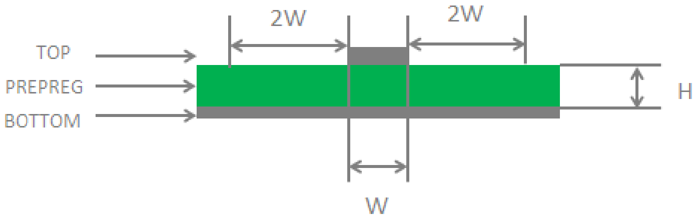


Figure 37: Microstrip Design on a 2-layer PCB

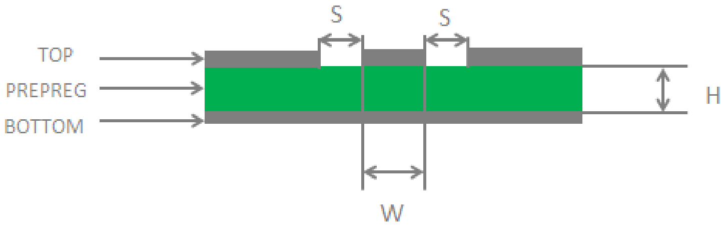


Figure 38: Coplanar Waveguide Design on a 2-layer PCB

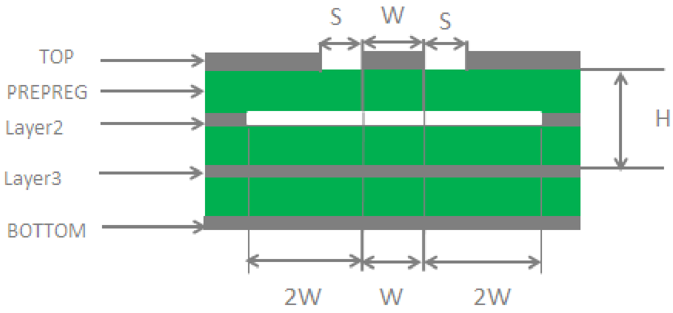


Figure 39: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

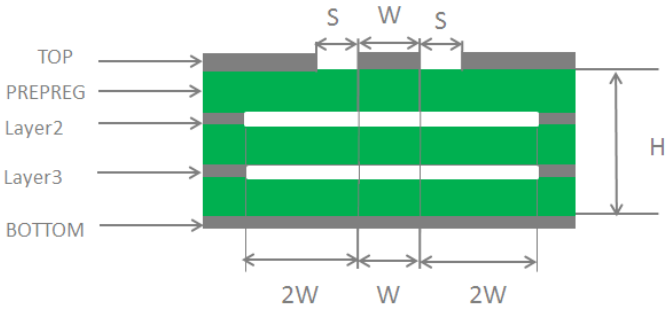


Figure 40: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right angle traces should be changed to curved ones.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times as wide as RF signal traces (2*W).

For more details about RF layout, please refer to ***document [3]***.

6.2. Wi-Fi/BT Antenna Interface

Table 41: Pin Definition of Wi-Fi/BT Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_WIFI/BT	129	IO	Wi-Fi/BT antenna interface	50Ω impedance
ANT_WIFI_	324	IO	Wi-Fi MIMO antenna interface	50Ω impedance

MIMO[1]	

NOTE

[1] SC66-CE and SC66-W do not support Wi-Fi MIMO function.

Table 42: Wi-Fi/BT Frequency

Type	Frequency	Unit
802.11a/b/g/n/ac	2402~2482 5180~5825	MHz
BT5.0	2402~2480	MHz

A reference circuit design for Wi-Fi/BT antenna interface is shown below. A π-type matching circuit is recommended to be reserved for better RF performance. The capacitors are not mounted by default and resistors are 0Ω.

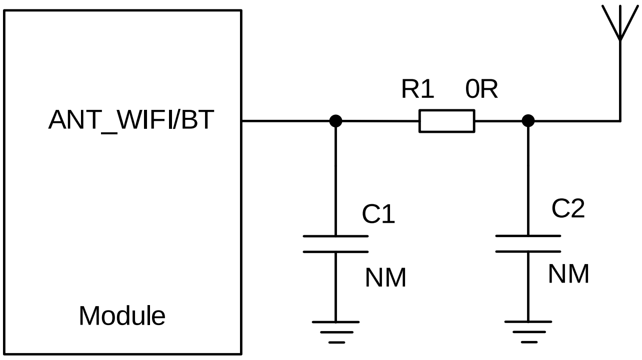


Figure 41: Reference Circuit Design for Wi-Fi/BT Antenna Interface

A reference circuit design for Wi-Fi MIMO antenna interface is shown below. A π-type matching circuit is recommended to be reserved for better RF performance. The capacitors are not mounted by default and resistors are 0Ω.

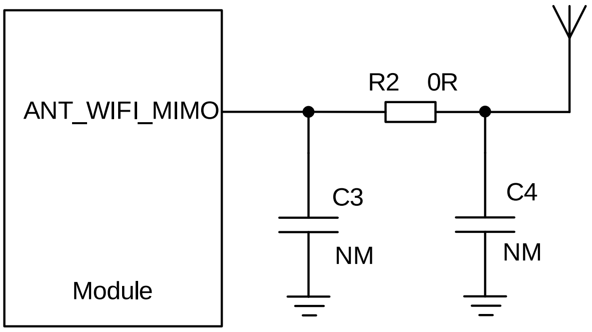


Figure 42: Reference Circuit Design for Wi-Fi MINO Antenna Interface

6.3. GNSS Antenna Interface

Table 43: Pin Definition of GNSS Antenna

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	134	AI	GNSS antenna Interface	50Ω impedance
GNSS_PPS_OUT	202	DO	LNA enable control	For test purpose only. If unused, keep it open. Cannot be pulled up.

Table 44: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42±1.023	MHz
GLONASS	1597.5~1605.8	MHz
BeiDou	1561.098±2.046	MHz

6.3.1. Recommended Circuit for Passive Antenna

GNSS antenna interface supports passive ceramic antennas and other types of passive antennas. A reference circuit design is given below.

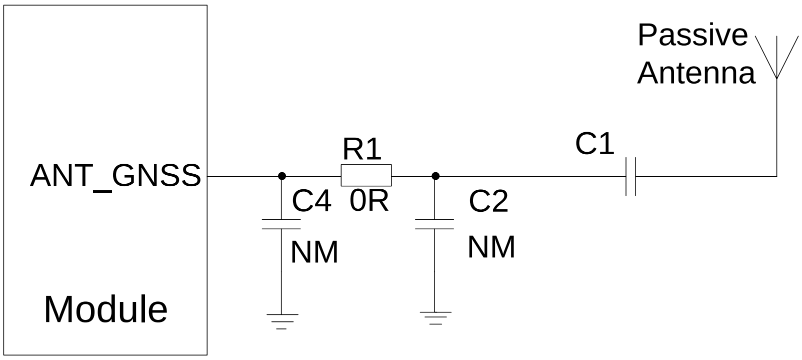


Figure 43: Reference Circuit Design for GNSS Passive Antenna

NOTE

When the passive antenna is placed far away from the module (that is, the antenna trace is long) and the external loss is more than 2dB, it is recommended to add an external LNA circuit for better GNSS receiving performance, and the LNA should be placed close to the antenna.

6.3.2. Recommended Circuit for Active Antenna

The active antenna is powered by a 56nH inductor through the antenna's signal path. The common power supply voltage ranges from 3.3V to 5.0V. Although featuring low power consumption, the active antenna still requires stable and clean power supplies. It is recommended to use high performance LDO as the power supply. A reference design of GNSS active antenna is shown below.

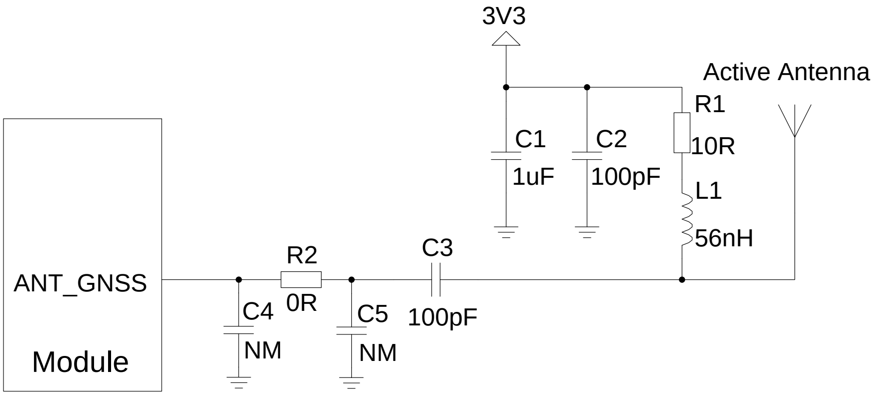


Figure 44: Reference Circuit Design for GNSS Active Antenna

6.4. Antenna Installation

6.4.1. Antenna Requirements

The following table shows the requirements on main antenna, Rx-diversity, Wi-Fi/BT antenna and GNSS antenna.

Table 45: Antenna Requirements

Antenna Type	Requirements
GSM/WCDMA/TD-SCDMA/ LTE	VSWR: ≤ 2 Gain (dBi): 1 Max Input Power (W): 50 Input Impedance (Ω): 50 Polarization Type: Vertical Cable Insertion Loss: < 1dB (frequency: 663-960 MHz) Cable Insertion Loss: < 1.5dB (frequency: 1427-2200 MHz) Cable Insertion Loss: < 2dB (frequency: 2300-2690 MHz)
Wi-Fi/BT	VSWR: ≤ 2 Gain (dBi): 1 Max Input Power (W): 50 Input Impedance (Ω): 50 Polarization Type: Vertical Cable Insertion Loss: < 1dB
GNSS [1]	Frequency range: 1559MHz~1609MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive Antenna Gain: > 0dBi Active Antenna Noise Figure: < 1.5dB (Typ.) Active Antenna Gain: > -2dBi Active Antenna Embedded LNA Gain: < 17dB (Typ.) Active Antenna Total Gain: < 17dBi (Typ.)

NOTE

[1] It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

6.4.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by HIROSE.

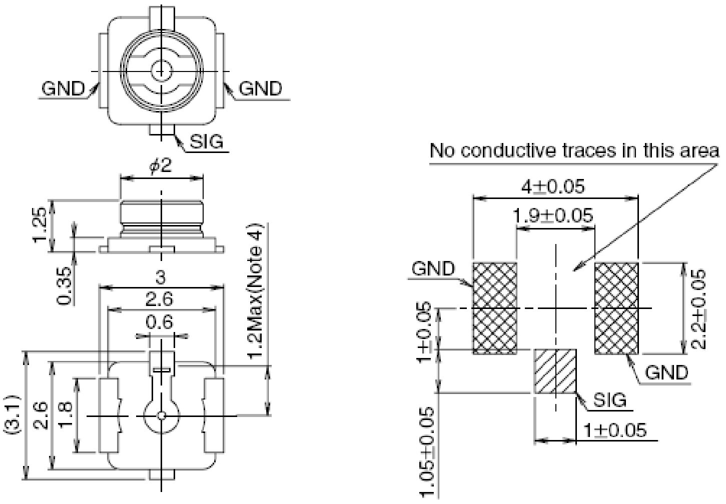


Figure 45: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

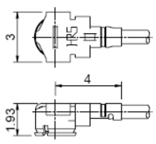
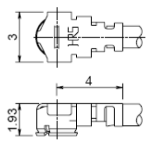
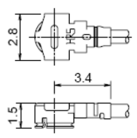
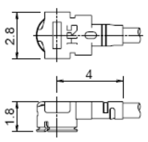
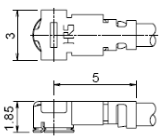
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 46: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

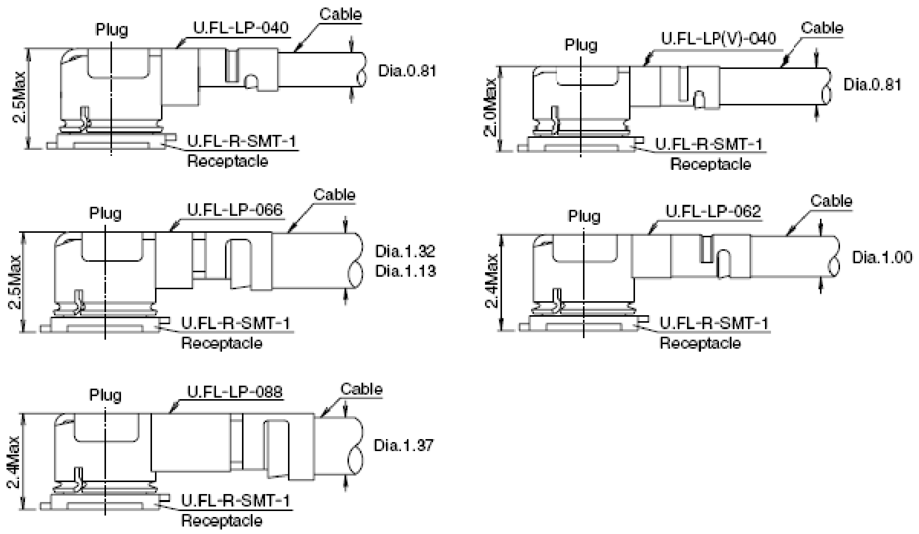


Figure 47: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://www.hirose.com.

7 Electrical, Reliability and Radio Characteristics

7.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 46: Absolute Maximum Ratings

Parameter	Min	Max	Unit
VBAT	-0.5	6	V
USB_VBUS	-0.5	16	V
Current on VBAT	0	3	A
Voltage on Digital Pins	-0.3	2.09~~3~~	V

7.2. Power Supply Ratings

Table 47: SC66 Module Power Supply Ratings

Parameter	Description	Conditions	Min	Typ.	Max	Unit
VBAT	VBAT	The actual input voltages must stay between the minimum and maximum values	3.55	4.0	4.4	V
	Voltage drop during transmitting burst	Maximum power control level at EGSM900			400	mV

I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level at EGSM900		1.8	3.0	A
USB_VBUS			3.6	5.0	10	V
VRTC	Power supply voltage of backup battery		2.1	3.0	3.25	V

7.3. Operation and Storage Temperatures

The operation and storage temperatures are listed in the following table.

Table 48: Operation and Storage Temperatures

Parameter	Min	Typ.	Max	Unit
Operating temperature range 1)	-35	+25	+65	°C
Extended temperature range 2)	-40		+75	°C
Storage temperature range	-40		+90	°C

NOTES

1. 1) Within operation temperature range, the module is 3GPP compliant.
2. 2) Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.

7.4. Current Consumption

Table 49: SC66-CE* Current Consumption

Parameter	Description	Conditions	Min	Typ.	Max	Unit
I_{VBAT}	OFF state	Power down	TBD	TBD	TBD	uA
	GSM/GPRS supply current	Sleep (USB disconnected) @DRX=2	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=5	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=9	TBD	TBD	TBD	mA
	WCDMA supply current	Sleep (USB disconnected) @DRX=6	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=8	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=9	TBD	TBD	TBD	mA
	CDMA supply current	BC0 CH283 @Slot Cycle Index=1	TBD	TBD	TBD	mA
		BC0 CH283 @Slot Cycle Index=7	TBD	TBD	TBD	mA
	TD-SCDMA supply current	Sleep (USB disconnected) @DRX=6	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=8	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=9	TBD	TBD	TBD	mA
	LTE-FDD supply current	Sleep (USB disconnected) @DRX=6	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=8	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=9	TBD	TBD	TBD	mA
	LTE-TDD supply current	Sleep (USB disconnected) @DRX=6	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=8	TBD	TBD	TBD	mA

		Sleep (USB disconnected) @DRX=9	TBD	TBD	TBD	mA
	GSM voice call	EGSM900 @PCL 5	TBD	TBD	TBD	mA
		EGSM900 @PCL 12	TBD	TBD	TBD	mA
		EGSM900 @PCL 19	TBD	TBD	TBD	mA
		DCS1800 @PCL 0	TBD	TBD	TBD	mA
		DCS1800 @PCL 7	TBD	TBD	TBD	mA
		DCS1800 @PCL 15	TBD	TBD	TBD	mA
	WCDMA voice call	B1 @max power	TBD	TBD	TBD	mA
		B8 @max power	TBD	TBD	TBD	mA
	GPRS data transfer	EGSM900 (1UL/4DL) @PCL 5	TBD	TBD	TBD	mA
		EGSM900 (2UL/3DL) @PCL 5	TBD	TBD	TBD	mA
		EGSM900 (3UL/2DL) @PCL 5	TBD	TBD	TBD	mA
		EGSM900 (4UL/1DL) @PCL 5	TBD	TBD	TBD	mA
		DCS1800 (1UL/4DL) @PCL 0	TBD	TBD	TBD	mA
		DCS1800 (2UL/3DL) @PCL 0	TBD	TBD	TBD	mA
		DCS1800 (3UL/2DL) @PCL 0	TBD	TBD	TBD	mA
		DCS1800 (4UL/1DL) @PCL 0	TBD	TBD	TBD	mA
	EDGE data transfer	EGSM900 (1UL/4DL) @PCL 8	TBD	TBD	TBD	mA
		EGSM900 (2UL/3DL) @PCL 8	TBD	TBD	TBD	mA
		EGSM900 (3UL/2DL) @PCL 8	TBD	TBD	TBD	mA
		EGSM900 (4UL/1DL) @PCL 8	TBD	TBD	TBD	mA
		DCS1800 (1UL/4DL) @PCL 2	TBD	TBD	TBD	mA
		DCS1800 (2UL/3DL) @PCL 2	TBD	TBD	TBD	mA
		DCS1800 (3UL/2DL) @PCL 2	TBD	TBD	TBD	mA
		DCS1800 (4UL/1DL) @PCL 2	TBD	TBD	TBD	mA

	WCDMA data transfer	B1 (HSDPA) @max power	TBD	TBD	TBD	mA
		B8 (HSDPA) @max power	TBD	TBD	TBD	mA
		B1 (HSUPA) @max power	TBD	TBD	TBD	mA
		B8 (HSUPA) @max power	TBD	TBD	TBD	mA
	EVDO/CDMA data transfer	BC0 @max power	TBD	TBD	TBD	mA
	TD-SCDMA data transfer	TD-SCDMA B34 @max power	TBD	TBD	TBD	mA
		TD-SCDMA B39 @max power	TBD	TBD	TBD	mA
	LTE data transfer	LTE-FDD B1 @max power	TBD	TBD	TBD	mA
		LTE-FDD B3 @max power	TBD	TBD	TBD	mA
		LTE-FDD B5 @max power	TBD	TBD	TBD	mA
		LTE-FDD B8 @max power	TBD	TBD	TBD	mA
		LTE-TDD B34 @max power	TBD	TBD	TBD	mA
		LTE-TDD B38 @max power	TBD	TBD	TBD	mA
		LTE-TDD B39 @max power	TBD	TBD	TBD	mA
		LTE-TDD B40 @max power	TBD	TBD	TBD	mA
		LTE-TDD B41 @max power	TBD	TBD	TBD	mA

Table 50: SC66-A* Current Consumption

Parameter	Description	Conditions	Min	Typ.	Max	Unit
I_{VABT}	Power down	OFF state	TBD	TBD	TBD	uA
	WCDMA supply current	Sleep (USB disconnected) @DRX=6	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=8	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=9	TBD	TBD	TBD	mA
	LTE-FDD supply current	Sleep (USB disconnected) @DRX=6	TBD	TBD	TBD	mA

		Sleep (USB disconnected) @DRX=8	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=9	TBD	TBD	TBD	mA
	LTE-TDD supply current	Sleep (USB disconnected) @DRX=6	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=8	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=9	TBD	TBD	TBD	mA
	WCDMA voice call	B2 @max power	TBD	TBD	TBD	mA
		B4 @max power	TBD	TBD	TBD	mA
		B5 @max power	TBD	TBD	TBD	mA
	WCDMA data transfer	B2 (HSDPA) @max power	TBD	TBD	TBD	mA
		B4 (HSDPA) @max power	TBD	TBD	TBD	mA
		B5 (HSDPA) @max power	TBD	TBD	TBD	mA
		B2 (HSUPA) @max power	TBD	TBD	TBD	mA
		B4 (HSUPA) @max power	TBD	TBD	TBD	mA
		B5(HSUPA) @max power	TBD	TBD	TBD	mA
	LTE data transfer	LTE-FDD B2 @max power	TBD	TBD	TBD	mA
		LTE-FDD B4 @max power	TBD	TBD	TBD	mA
		LTE-FDD B5 @max power	TBD	TBD	TBD	mA
		LTE-FDD B7 @max power	TBD	TBD	TBD	mA
		LTE-TDD B12 @max power	TBD	TBD	TBD	mA
		LTE-TDD B13 @max power	TBD	TBD	TBD	mA
		LTE-TDD B14 @max power	TBD	TBD	TBD	mA
		LTE-TDD B17 @max power	TBD	TBD	TBD	mA
		LTE-TDD B25 @max power	TBD	TBD	TBD	mA
		LTE-FDD B26 @max power	TBD	TBD	TBD	mA

		LTE-FDD B66 @max power	TBD	TBD	TBD	mA
		LTE-TDD B71 @max power	TBD	TBD	TBD	mA
		LTE-TDD B41 @max power	TBD	TBD	TBD	mA

Table 51: SC66-J* Current Consumption

Parameter	Description	Conditions	Min	Typ.	Max	Unit
I_{VBAT}	Power down	OFF state	TBD	TBD	TBD	uA
	WCDMA supply current	Sleep (USB disconnected) @DRX=6	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=8	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=9	TBD	TBD	TBD	mA
	LTE-FDD supply current	Sleep (USB disconnected) @DRX=6	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=8	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=9	TBD	TBD	TBD	mA
	LTE-TDD supply current	Sleep (USB disconnected) @DRX=6	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=8	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=9	TBD	TBD	TBD	mA
	WCDMA voice call	B1 @max power	TBD	TBD	TBD	mA
		B6 @max power	TBD	TBD	TBD	mA
		B8 @max power	TBD	TBD	TBD	mA
		B19 @max power	TBD	TBD	TBD	mA
	WCDMA data transfer	B1 (HSDPA) @max power	TBD	TBD	TBD	mA
		B6 (HSDPA) @max power	TBD	TBD	TBD	mA
		B8 (HSDPA) @max power	TBD	TBD	TBD	mA

		B19 (HSDPA) @max power	TBD	TBD	TBD	mA
		B1 (HSUPA) @max power	TBD	TBD	TBD	mA
		B6 (HSUPA) @max power	TBD	TBD	TBD	mA
		B8 (HSUPA) @max power	TBD	TBD	TBD	mA
		B19 (HSUPA) @max power	TBD	TBD	TBD	mA
	LTE data transfer	LTE-FDD B1 @max power	TBD	TBD	TBD	mA
		LTE-FDD B3 @max power	TBD	TBD	TBD	mA
		LTE-FDD B5 @max power	TBD	TBD	TBD	mA
		LTE-FDD B8 @max power	TBD	TBD	TBD	mA
		LTE-FDD B11 @max power	TBD	TBD	TBD	mA
		LTE-FDD B18 @max power	TBD	TBD	TBD	mA
		LTE-FDD B19 @max power	TBD	TBD	TBD	mA
		LTE-FDD B21 @max power	TBD	TBD	TBD	mA
		LTE-FDD B26 @max power	TBD	TBD	TBD	mA
		LTE-FDD B28 (A+B) @max power	TBD	TBD	TBD	mA
		LTE-TDD B41 @max power	TBD	TBD	TBD	mA

Table 52: SC66-E* Current Consumption

Parameter	Description	Conditions	Min	Typ.	Max	Unit
I_{VBAT}	Power down	OFF state	TBD	TBD	TBD	uA
	GSM/GPRS supply current	Sleep (USB disconnected) @DRX=2	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=5	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=9	TBD	TBD	TBD	mA
	WCDMA supply current	Sleep (USB disconnected) @DRX=6	TBD	TBD	TBD	mA

		Sleep (USB disconnected) @DRX=8	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=9	TBD	TBD	TBD	mA
	LTE-FDD supply current	Sleep (USB disconnected) @DRX=6	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=8	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=9	TBD	TBD	TBD	mA
	LTE-TDD supply current	Sleep (USB disconnected) @DRX=6	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=8	TBD	TBD	TBD	mA
		Sleep (USB disconnected) @DRX=9	TBD	TBD	TBD	mA
	GSM voice call	GSM850 @PCL 5	TBD	TBD	TBD	mA
		GSM850 @PCL 12	TBD	TBD	TBD	mA
		GSM850 @PCL 19	TBD	TBD	TBD	mA
		EGSM900 @PCL 5	TBD	TBD	TBD	mA
		EGSM900 @PCL 12	TBD	TBD	TBD	mA
		EGSM900 @PCL 19	TBD	TBD	TBD	mA
		DCS1800 @PCL 0	TBD	TBD	TBD	mA
		DCS1800 @PCL 7	TBD	TBD	TBD	mA
		DCS1800 @PCL 15	TBD	TBD	TBD	mA
		PCS1900 @PCL 0	TBD	TBD	TBD	mA
		PCS1900 @PCL 7	TBD	TBD	TBD	mA
		PCS1900 @PCL 15	TBD	TBD	TBD	mA
	WCDMA voice call	B1 @max power	TBD	TBD	TBD	mA
		B2 @max power	TBD	TBD	TBD	mA
		B4 @max power	TBD	TBD	TBD	mA
		B5 @max power	TBD	TBD	TBD	mA

		B8 @max power	TBD	TBD	TBD	mA
	GPRS data transfer	GSM850 (1UL/4DL) @PCL 5	TBD	TBD	TBD	mA
		GSM850 (2UL/3DL) @PCL 5	TBD	TBD	TBD	mA
		GSM850 (3UL/2DL) @PCL 5	TBD	TBD	TBD	mA
		GSM850 (4UL/1DL) @PCL 5	TBD	TBD	TBD	mA
		EGSM900 (1UL/4DL) @PCL 5	TBD	TBD	TBD	mA
		EGSM900 (2UL/3DL) @PCL 5	TBD	TBD	TBD	mA
		EGSM900 (3UL/2DL) @PCL 5	TBD	TBD	TBD	mA
		EGSM900 (4UL/1DL) @PCL 5	TBD	TBD	TBD	mA
		DCS1800 (1UL/4DL) @PCL 0	TBD	TBD	TBD	mA
		DCS1800 (2UL/3DL) @PCL 0	TBD	TBD	TBD	mA
		DCS1800 (3UL/2DL) @PCL 0	TBD	TBD	TBD	mA
		DCS1800 (4UL/1DL) @PCL 0	TBD	TBD	TBD	mA
		PCS1900 (1UL/4DL) @PCL 0	TBD	TBD	TBD	mA
		PCS1900 (2UL/3DL) @PCL 0	TBD	TBD	TBD	mA
		PCS1900 (3UL/2DL) @PCL 0	TBD	TBD	TBD	mA
		PCS1900 (4UL/1DL) @PCL 0	TBD	TBD	TBD	mA
	EDGE data transfer	GSM850 (1UL/4DL) @PCL 8	TBD	TBD	TBD	mA
		GSM850 (2UL/3DL) @PCL 8	TBD	TBD	TBD	mA
		GSM850 (3UL/2DL) @PCL 8	TBD	TBD	TBD	mA
		GSM850 (4UL/1DL) @PCL 8	TBD	TBD	TBD	mA
		EGSM900 (1UL/4DL) @PCL 8	TBD	TBD	TBD	mA
		EGSM900 (2UL/3DL) @PCL 8	TBD	TBD	TBD	mA
		EGSM900 (3UL/2DL) @PCL8	TBD	TBD	TBD	mA
		EGSM900 (4UL/1DL) @PCL 8	TBD	TBD	TBD	mA

	DCS1800 (1UL/4DL) @PCL 2	TBD	TBD	TBD	mA
	DCS1800 (2UL/3DL) @PCL 2	TBD	TBD	TBD	mA
	DCS1800 (3UL/2DL) @PCL 2	TBD	TBD	TBD	mA
	DCS1800 (4UL/1DL) @PCL 2	TBD	TBD	TBD	mA
	PCS1900 (1UL/4DL) @PCL 2	TBD	TBD	TBD	mA
	PCS1900 (2UL/3DL) @PCL 2	TBD	TBD	TBD	mA
	PCS1900 (3UL/2DL) @PCL 2	TBD	TBD	TBD	mA
	PCS1900 (4UL/1DL) @PCL 2	TBD	TBD	TBD	mA
WCDMA data transfer	B1 (HSDPA) @max power	TBD	TBD	TBD	mA
	B2 (HSDPA) @max power	TBD	TBD	TBD	mA
	B4 (HSDPA) @max power	TBD	TBD	TBD	mA
	B5 (HSDPA) @max power	TBD	TBD	TBD	mA
	B8 (HSDPA) @max power	TBD	TBD	TBD	mA
	B1 (HSUPA) @max power	TBD	TBD	TBD	mA
	B2 (HSUPA) @max power	TBD	TBD	TBD	mA
	B4 (HSUPA) @max power	TBD	TBD	TBD	mA
	B5 (HSUPA) @max power	TBD	TBD	TBD	mA
	B8 (HSUPA) @max power	TBD	TBD	TBD	mA
LTE data transfer	LTE-FDD B1 @max power	TBD	TBD	TBD	mA
	LTE-FDD B2 @max power	TBD	TBD	TBD	mA
	LTE-FDD B3 @max power	TBD	TBD	TBD	mA
	LTE-FDD B4 @max power	TBD	TBD	TBD	mA
	LTE-FDD B5 @max power	TBD	TBD	TBD	mA
	LTE-FDD B7 @max power	TBD	TBD	TBD	mA
	LTE-FDD B8 @max power	TBD	TBD	TBD	mA

	LTE-FDD B20 @max power	TBD	TBD	TBD	mA
	LTE-FDD B28 (A+B) @max power	TBD	TBD	TBD	mA
	LTE-TDD B41 @max power	TBD	TBD	TBD	mA

NOTE

"*" means under development.

7.5. RF Output Power

The following table shows the RF output power of SC66 module.

Table 53: SC66-CE* RF Output Power

Frequency	Max	Min
EGSM900	33dBm±2dB	5dBm±5dB
DCS1800	30dBm±2dB	0dBm±5dB
WCDMA B1	24dBm+1/-3dB	<-49dBm
WCDMA B8	24dBm+1/-3dB	<-49dBm
EVDO/CDMA BC0	24dBm+3/-1dB	<-49dBm
TD-SCDMA B34	24dBm+1/-3dB	<-49dBm
TD-SCDMA B39	24dBm+1/-3dB	<-49dBm
LTE-FDD B1	23dBm±2dB	<-39dBm
LTE-FDD B3	23dBm±2dB	<-39dBm
LTE-FDD B5	23dBm±2dB	<-39dBm
LTE-FDD B8	23dBm±2dB	<-39dBm
LTE-FDD B34	23dBm±2dB	<-39dBm

LTE-TDD B38	23dBm±2dB	<-39dBm
LTE-TDD B39	23dBm±2dB	<-39dBm
LTE-TDD B40	23dBm±2dB	<-39dBm
LTE-TDD B41	23dBm±2dB	<-39dBm

Table 54: SC66-A* RF Output Power

Frequency	Max	Min
WCDMA B2	24dBm+1/-3dB	<-49dBm
WCDMA B4	24dBm+1/-3dB	<-49dBm
WCDMA B5	24dBm+1/-3dB	<-49dBm
LTE-FDD B2	23dBm±2dB	<-39dBm
LTE-FDD B4	23dBm±2dB	<-39dBm
LTE-FDD B5	23dBm±2dB	<-39dBm
LTE-FDD B7	23dBm±2dB	<-39dBm
LTE-FDD B12	23dBm±2dB	<-39dBm
LTE-FDD B13	23dBm±2dB	<-39dBm
LTE-FDD B14	23dBm±2dB	<-39dBm
LTE-FDD B17	23dBm±2dB	<-39dBm
LTE-FDD B25	23dBm±2dB	<-39dBm
LTE-FDD B26	23dBm±2dB	<-39dBm
LTE-FDD B66	23dBm±2dB	<-39dBm
LTE-TDD B71	23dBm±2dB	<-39dBm
LTE-TDD B41	23dBm±2dB	<-39dBm

Table 55: SC66-J* RF Output Power

Frequency	Max	Min
WCDMA B1	24dBm+1/-3dB	<-49dBm
WCDMA B6	24dBm+1/-3dB	<-49dBm
WCDMA B8	24dBm+1/-3dB	<-49dBm
WCDMA B19	24dBm+1/-3dB	<-49dBm
LTE-FDD B1	23dBm±2dB	<-39dBm
LTE-FDD B3	23dBm±2dB	<-39dBm
LTE-FDD B5	23dBm±2dB	<-39dBm
LTE-FDD B8	23dBm±2dB	<-39dBm
LTE-FDD B11	23dBm±2dB	<-39dBm
LTE-FDD B18	23dBm±2dB	<-39dBm
LTE-FDD B19	23dBm±2dB	<-39dBm
LTE-FDD B21	23dBm±2dB	<-39dBm
LTE-FDD B26	23dBm±2dB	<-39dBm
LTE-FDD B28 (A+B)	23dBm±2dB	<-39dBm
LTE-TDD B41	23dBm±2dB	<-39dBm

Table 56: SC66-E* RF Output Power

Frequency	Max	Min
GSM850	33dBm±2dB	5dBm±5dB
EGSM900	33dBm±2dB	5dBm±5dB
DCS1800	30dBm±2dB	0dBm±5dB
PCS1900	30dBm±2dB	0dBm±5dB
WCDMA B1	24dBm+1/-3dB	<-49dBm

WCDMA B2	24dBm+1/-3dB	<-49dBm
WCDMA B4	24dBm+1/-3dB	<-49dBm
WCDMA B5	24dBm+1/-3dB	<-49dBm
WCDMA B8	24dBm+1/-3dB	<-49dBm
LTE-FDD B1	23dBm±2dB	<-39dBm
LTE-FDD B2	23dBm±2dB	<-39dBm
LTE-FDD B3	23dBm±2dB	<-39dBm
LTE-FDD B4	23dBm±2dB	<-39dBm
LTE-FDD B5	23dBm±2dB	<-39dBm
LTE-FDD B7	23dBm±2dB	<-39dBm
LTE-FDD B8	23dBm±2dB	<-39dBm
LTE-FDD B20	23dBm±2dB	<-39dBm
LTE-FDD B28 (A+B)	23dBm±2dB	<-39dBm
LTE-TDD B38	23dBm±2dB	<-39dBm
LTE-TDD B39	23dBm±2dB	<-39dBm
LTE-TDD B40	23dBm±2dB	<-39dBm
LTE-TDD B41	23dBm±2dB	<-39dBm

NOTES

1. In GPRS 4 slots TX mode, the maximum output power is reduced by 3dB. This design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.
2. "*" means under development.

7.6. RF Receiving Sensitivity

The following table shows the conducted RF receiving sensitivity of SC66 module.

Table 57: SC66-CE* RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
EGSM900	-109dBm	/	/	-102.4dBm
DCS1800	-108dBm	/	/	-102.4dBm
WCDMA B1	-110dBm	/	/	-106.7dBm
WCDMA B8	-110dBm	/	/	-103.7dBm
EVDO/CDMA BC0	-109dBm	/	/	-104dBm
TD-SCDMA B34	-109dBm	/	/	-108dBm
TD-SCDMA B39	-109dBm	/	/	-108dBm
LTE-FDD B1 (10M)	-98dBm	-98.5dBm	-101.2dBm	-96.3dBm
LTE-FDD B3 (10M)	-98dBm	-98.5dBm	-101.2dBm	-93.3dBm
LTE-FDD B5 (10M)	-98dBm	-99dBm	-101.5dBm	-94.3dBm
LTE-FDD B8 (10M)	-98dBm	-99dBm	-101.5dBm	-93.3dBm
LTE-TDD B34 (10M)	-98dBm	-98dBm	-101dBm	-96.3dBm
LTE-TDD B38 (10M)	-97.5dBm	-98dBm	-100.5dBm	-96.3dBm
LTE-TDD B39 (10M)	-98dBm	-98dBm	-101dBm	-96.3dBm
LTE-TDD B40 (10M)	-97.5dBm	-98dBm	-100.5dBm	-96.3dBm
LTE-TDD B41 (10M)	-97.5dBm	-98dBm	-100.5dBm	-94.3dBm

Table 58: SC66-A* RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
WCDMA B2	/	/	/	-104.7dBm
WCDMA B4	/	/	/	-106.7dBm
WCDMA B5	/	/	/	-104.7dBm
LTE-FDD B2 (10M)	/	/	/	-94.3dBm
LTE-FDD B4 (10M)	/	/	/	-96.3dBm
LTE-FDD B5 (10M)	/	/	/	-94.3dBm
LTE-FDD B7 (10M)	/	/	/	-94.3dBm
LTE-FDD B12 (10M)	/	/	/	-93.3dBm
LTE-FDD B13 (10M)	/	/	/	-93.3dBm
LTE-FDD B14 (10M)	/	/	/	-93.3dBm
LTE-FDD B17 (10M)	/	/	/	-93.3dBm
LTE-FDD B25 (10M)	/	/	/	-92.8dBm
LTE-FDD B66 (10M)	/	/	/	-95.8dBm
LTE-TDD B71 (10M)	/	/	/	-93.5dBm
LTE-TDD B41 (10M)	/	/	/	-94.3dBm

Table 59: SC66-J* RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
WCDMA B1	/	/	/	-106.7dBm
WCDMA B6	/	/	/	-106.7dBm
WCDMA B8	/	/	/	-103.7dBm
WCDMA B19	/	/	/	-106.7dBm
LTE-FDD B1 (10M)	/	/	/	-96.3dBm

LTE-FDD B3 (10M)	/	/	/	-93.3dBm
LTE-FDD B5 (10M)	/	/	/	-94.3dBm
LTE-FDD B8 (10M)	/	/	/	-93.3dBm
LTE-FDD B11 (10M)	/	/	/	-96.3dBm
LTE-FDD B18 (10M)	/	/	/	-96.3dBm
LTE-FDD B19 (10M)	/	/	/	-96.3dBm
LTE-FDD B21 (10M)	/	/	/	-96.3dBm
LTE-FDD B26 (10M)	/	/	/	-93.8dBm
LTE-FDD B28 (A+B) (10M)	/	/	/	-94.8dBm
LTE-TDD B41 (10M)	/	/	/	-94.3dBm

Table 60: SC66-E* RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
GSM850	/	/	/	-102.4dBm
EGSM900	/	/	/	-102.4dBm
DCS1800	/	/	/	-102.4dBm
PCS1900	/	/	/	-102.4dBm
WCDMA B1	/	/	/	-106.7dBm
WCDMA B2	/	/	/	-104.7dBm
WCDMA B4	/	/	/	-106.7dBm
WCDMA B5	/	/	/	-104.7dBm
WCDMA B8	/	/	/	-103.7dBm
LTE-FDD B1 (10M)	/	/	/	-96.3dBm
LTE-FDD B2 (10M)	/	/	/	-94.3dBm

LTE-FDD B3 (10M)	/	/	/	-93.3dBm
LTE-FDD B4 (10M)	/	/	/	-96.3dBm
LTE-FDD B5 (10M)	/	/	/	-94.3dBm
LTE-FDD B7 (10M)	/	/	/	-94.3dBm
LTE-FDD B8 (10M)	/	/	/	-93.3dBm
LTE-FDD B20 (10M)	/	/	/	-93.3dBm
LTE-FDD B28 (A+B) (10M)	/	/	/	-94.8dBm
LTE-TDD B38 (10M)	/	/	/	-96.3dBm
LTE-TDD B39 (10M)	/	/	/	-96.3dBm
LTE-TDD B40 (10M)	/	/	/	-96.3dBm
LTE-TDD B41 (10M)	/	/	/	-94.3dBm

NOTE

"*" means under development.

7.7. Electrostatic Discharge

The module is not protected against electrostatic discharge (ESD) in general. Consequently, it should be subject to ESD handling precautions that are typically applied to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the electrostatic discharge characteristics of SC66 module.

Table 61: ESD Characteristics (Temperature: 25°C, Humidity: 45%)

Test Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	+/-5	+/-10	KV
All Antenna Interfaces	+/-5	+/-10	KV
Other Interfaces	+/-0.5	+/-1	KV

8 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.05mm unless otherwise specified.

8.1. Mechanical Dimensions of the Module

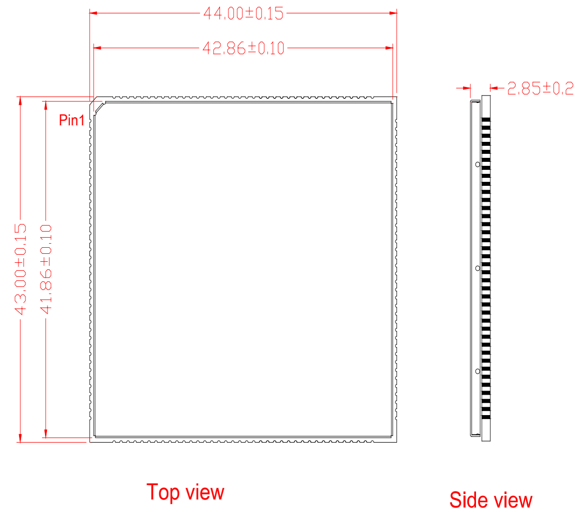


Figure 48: Module Top and Side Dimensions

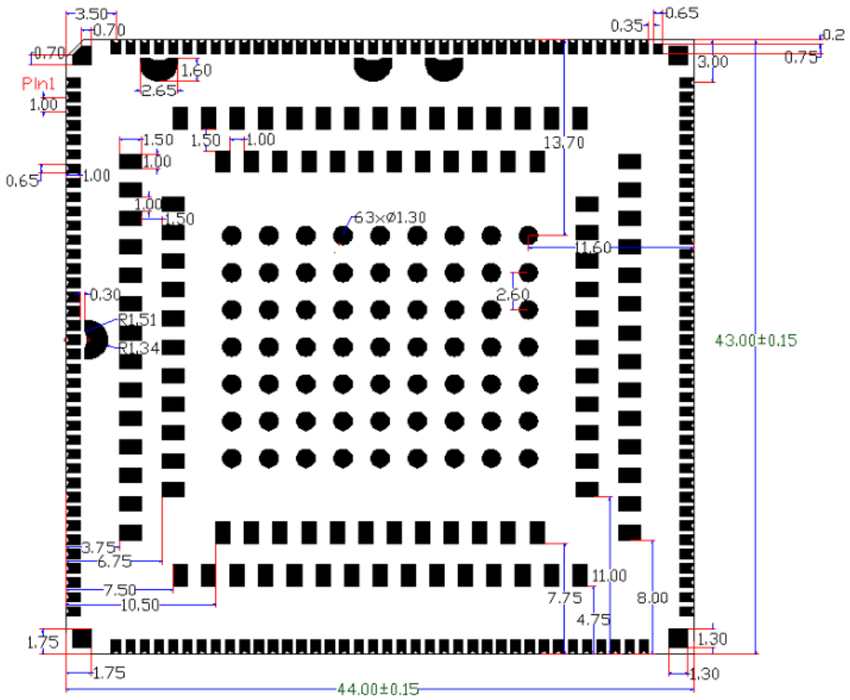


Figure 49: Module Bottom Dimensions (Top View)

8.2. Recommended Footprint

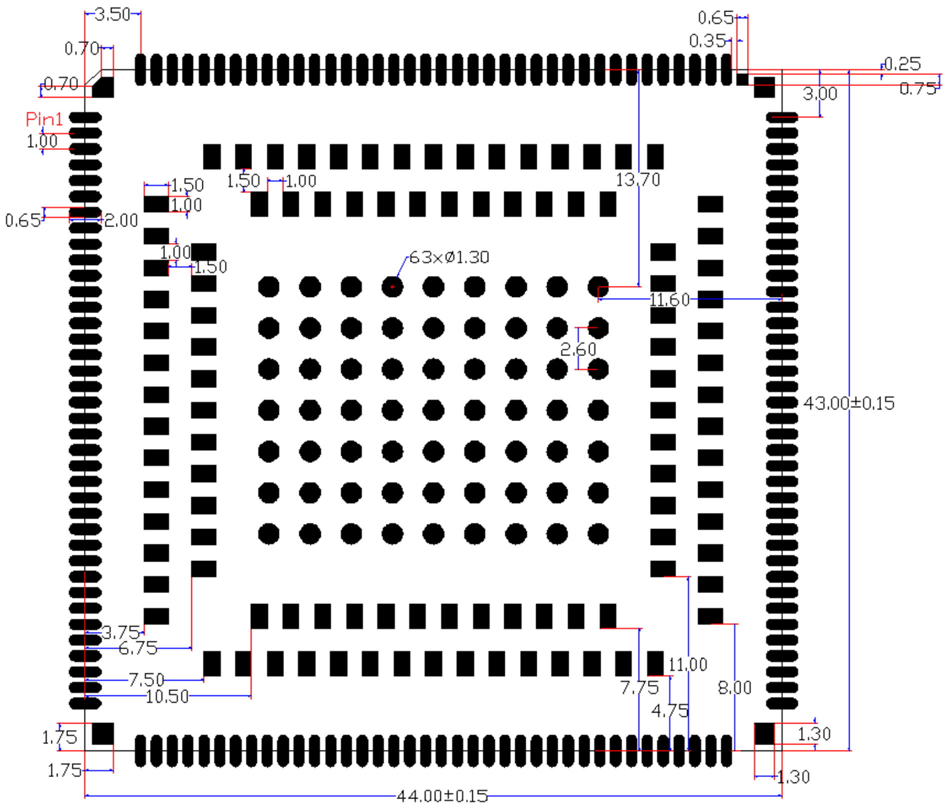


Figure 50: Recommended Footprint (Top View)

NOTES

1. For easy maintenance of the module, keep about 3mm between the module and other components on host PCB.
2. All RESERVED pins should be kept open and MUST NOT be connected to ground.

8.3. Top and Bottom View of the Module

Figure 51: Top View of the Module

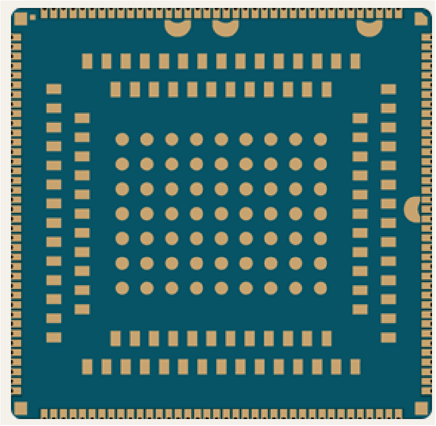


Figure 52: Bottom View of the Module

NOTE

These are renderings of SC66 module. For authentic dimension and appearance, please refer to the module that you receive from Quectel.

9 Storage, Manufacturing and Packaging

9.1. Storage

SC66 is stored in a vacuum-sealed bag. It is rated at MSL 3, and its storage restrictions are shown below.

1. Shelf life in the vacuum-sealed bag: 12 months at <40ºC/90%RH.

2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:
   - Mounted within 168 hours at the factory environment of ≤30ºC/60%RH.
   - Stored at <10%RH.

3. Devices require baking before mounting, if any circumstance below occurs.
   - When the ambient temperature is 23ºC±5ºC and the humidity indication card shows the humidity is >10% before opening the vacuum-sealed bag.
   - Device mounting cannot be finished within 168 hours at factory conditions of ≤30ºC/60%.

4. If baking is required, devices may be baked for 8 hours at 120ºC±5ºC.

NOTE

As the plastic package cannot be subjected to high temperature, it should be removed from devices before high temperature (120ºC) baking. If shorter baking time is desired, please refer to IPC/JEDECJ-STD-033 for baking procedure.

9.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18mm~0.20mm. It is recommended to slightly reduce the amount of solder paste for LGA pads, thus avoiding short-circuit. For more details, please refer to ***document [4]***.

It is suggested that the peak reflow temperature is 238~245ºC, and the absolute maximum reflow temperature is 245ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

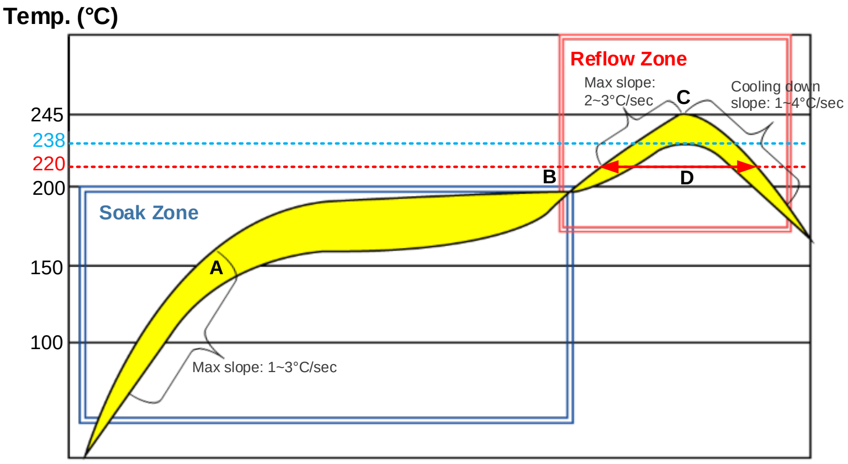


Figure 53: Recommended Reflow Soldering Thermal Profile

Table 62: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1 to 3°C/sec
Soak time (between A and B: 150°C and 200°C)	60 to 120 sec

Reflow Zone	
Max slope	2 to 3°C/sec
Reflow time (D: over 220°C)	40 to 60 sec
Max temperature	238°C ~ 245°C
Cooling down slope	1 to 4°C/sec
Reflow Cycle	
Max reflow cycle	1

9.3. Packaging

SC66 is packaged in tape and reel carriers. Each reel is 330mm in diameter and contains 200 modules. The following figures show the package details, measured in mm.

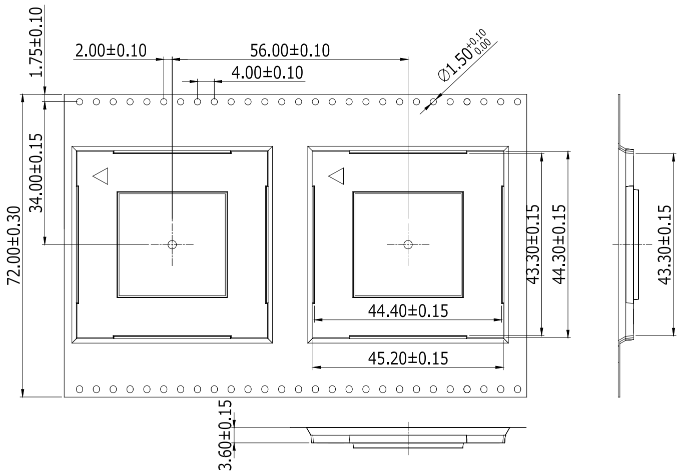


Figure 54: Tape Dimensions

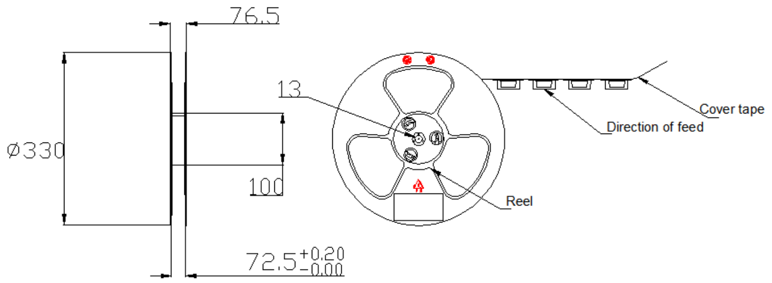


Figure 55: Reel Dimensions

Table 63: Reel Packaging

Model Name	MOQ for MP	Minimum Package: 200pcs	Minimum Package×4=800pcs
SC66	200	Size: 398mm × 383mm × 83mm N.W: 1.92kg G.W: 3.67kg	Size: 420mm × 350mm × 405mm N.W: 8.18kg G.W: 15.18kg

10 Appendix A References

Table 64: Related Documents

SN	Document Name	Remark
[1]	Quectel_Smart_EVB-G2_User_Guide	EVB User Guide for SC66
[2]	Quectel_SC66_GPIO_Configuration	GPIO Configuration of SC66
[3]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[4]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide
[5]	Quectel_SC66_Reference_Design	Reference Design for SC66

Table 65: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-rate
bps	Bits per Second
CC	Configuration Channel
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear to Send
DP	DisplayPort
DRX	Discontinuous Reception
EFR	Enhanced Full Rate
EGSM	Extended GSM900 band (includes standard GSM900 band)

ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate
GMSK	Gaussian Minimum Shift Keying
GPS	Global Positioning System
GPU	Graphics Processing Unit
GSM	Global System for Mobile Communications
HR	Half Rate
HSDPA	High Speed Down Link Packet Access
HSPA	High Speed Packet Access
I/O	Input/Output
IQ	Inphase and Quadrature
LCD	Liquid Crystal Display
LCM	LCD Module
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LRA	Linear Resonant Actuator
LTE-TDD	Long-Term Evolution Time-Division Duplex
MIPI	Mobile Industry Processor Interface
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PMI	Power Management Interface
PMU	Power Management Unit
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation

QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RH	Relative Humidity
RHCP	Right Hand Circularly Polarized
RTC	Real Time Clock
Rx	Receive
SMS	Short Message Service
TDD	Time Division Distortion
TE	Terminal Equipment
TX	Transmitting Direction
UART	Universal Asynchronous Receiver & Transmitter
UMTS	Universal Mobile Telecommunications System
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_I	Voltage Input
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_O	Voltage Output
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

11 Appendix B GPRS Coding Schemes

Table 66: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

12 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 67: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
13	3	3	NA

14	4	4	NA
15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6

13 Appendix D EDGE Modulation and Coding Schemes

Table 68: EDGE Modulation and Coding Schemes

Coding Schemes	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1:	GMSK	/	9.05kbps	18.1kbps	36.2kbps
CS-2:	GMSK	/	13.4kbps	26.8kbps	53.6kbps
CS-3:	GMSK	/	15.6kbps	31.2kbps	62.4kbps
CS-4:	GMSK	/	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.60kbps	35.20kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps

IC & FCC Requirement

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FCC Certification Requirements.

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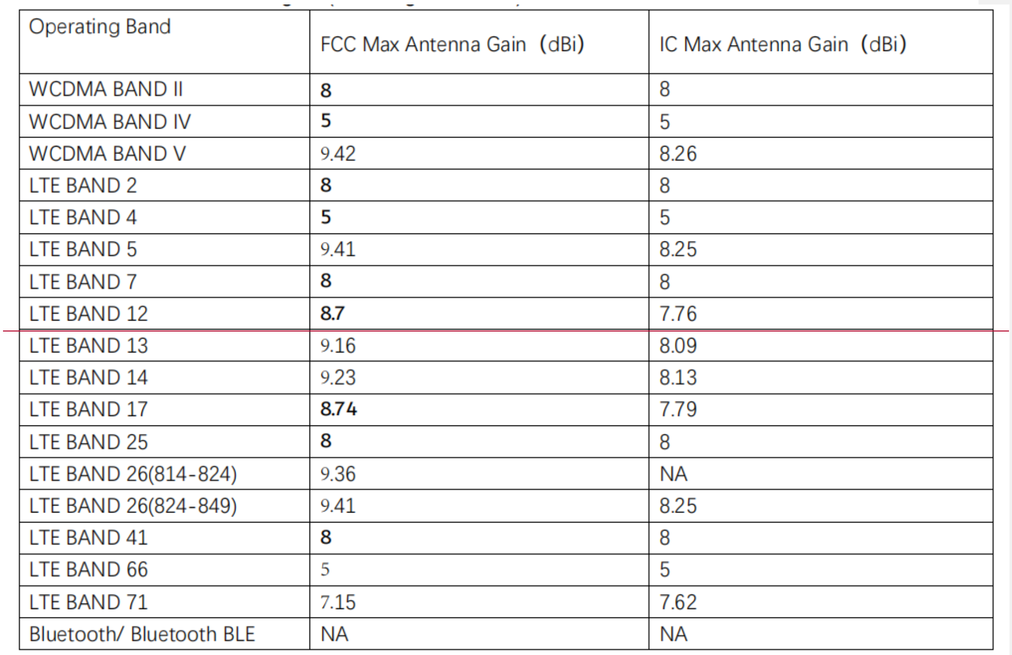
According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device. And the following conditions must be met:

1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based timeaveraging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.

2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user’s body and must not transmit simultaneously with any other antenna or transmitter.

3.A label with the following statements must be attached to the host end product: This device contains FCC ID: XMR2019SC66A

4.To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:



Operating Band	FCC Max Antenna Gain（dBi）	IC Max Antenna Gain（dBi）
WCDMA BAND II	8	8
WCDMA BAND IV	5	5
WCDMA BAND V	9.42	8.26
LTE BAND 2	8	8
LTE BAND 4	5	5
LTE BAND 5	9.41	8.25
LTE BAND 7	8	8
LTE BAND 12	8.7	7.76
LTE BAND 13	9.16	8.09
LTE BAND 14	9.23	8.13
LTE BAND 17	8.74	7.79
LTE BAND 25	8	8
LTE BAND 26(814-824)	9.36	NA
LTE BAND 26(824-849)	9.41	8.25
LTE BAND 41	8	8
LTE BAND 66	5	5
LTE BAND 71	7.15	7.62
Bluetooth/ Bluetooth BLE	NA	NA

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Operating Band	FCC Max Antenna Gain（dBi）	IC Max Antenna Gain（dBi）
WCDMA BAND II		
WCDMA BAND IV		
WCDMA BAND V		

LTE BAND 2		
LTE BAND 4		
LTE BAND 5		
LTE BAND 7		
LTE BAND 12		
LTE BAND 13		
LTE BAND 14		
LTE BAND 17		
LTE BAND 25		
LTE BAND 26(814-824)		
LTE BAND 26(824-849)		
LTE BAND 41		
LTE BAND 66		
LTE BAND 71		
Bluetooth/ Bluetooth BLE		
WIFI 2.4G/5G		

~~WIFI 2.4G/5G~~	~~NA~~	~~NA~~

5. This module must not transmit simultaneously with any other antenna or transmitter
6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

For this device, OEM integrators must be provided with labeling instructions of finished products. Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:

A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).

For a host using a certified modular with a standard fixed label, if (1) the module’s FCC ID is not visible

when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module:“Contains Transmitter Module FCC ID: XMR2019SC66A” or “Contains FCC ID: XMR2019SC66A” must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.
The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.
The user’s manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
Changes or modifications not expressly approved by the manufacturer could void the user’s authority to operate the equipment.
To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Supplier’s Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements.

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Manual Information To the End User

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The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

IC Statement
IRSS-GEN
"This device complies with Industry Canada’s licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device." or "Le présent appareil est conforme aux CNR d’Industrie Canada applicables aux appareils radio exempts de licence. L’exploitation est autorisée aux deux conditions suivantes :
1) l’appareil ne doit pas produire de brouillage; 2) l’utilisateur de l’appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d’en compromettre le fonctionnement."
Déclaration sur l'exposition aux rayonnements RF
L'autre utilisé pour l'émetteur doit être installé pour fournir une distance de séparation d'au moins 20 cm

de toutes les personnes et ne doit pas être colocalisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.

The host product shall be properly labeled to identify the modules within the host product.

The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word “Contains” or similar wording expressing the same meaning, as follows: “Contains IC: 10224A-2019SC66A” or “where: 10224A-2019SC66A is the module’s certification number”.

Le produit hôte doit être correctement étiqueté pour identifier les modules dans le produit hôte.

L'étiquette de certification d'Innovation, Sciences et Développement économique Canada d'un module doit être clairement visible en tout temps lorsqu'il est installédans le produit hôte; sinon, le produit hôte doit porter une étiquette indiquant le numéro de certification d'Innovation, Sciences et Développement économique Canada pour le module, précédé du mot «Contient» ou d'un libellé semblable exprimant la même signification, comme suit:

"Contient IC: 10224A-2019SC66A " ou "où: 10224A-2019SC66A est le numéro de certification du module".