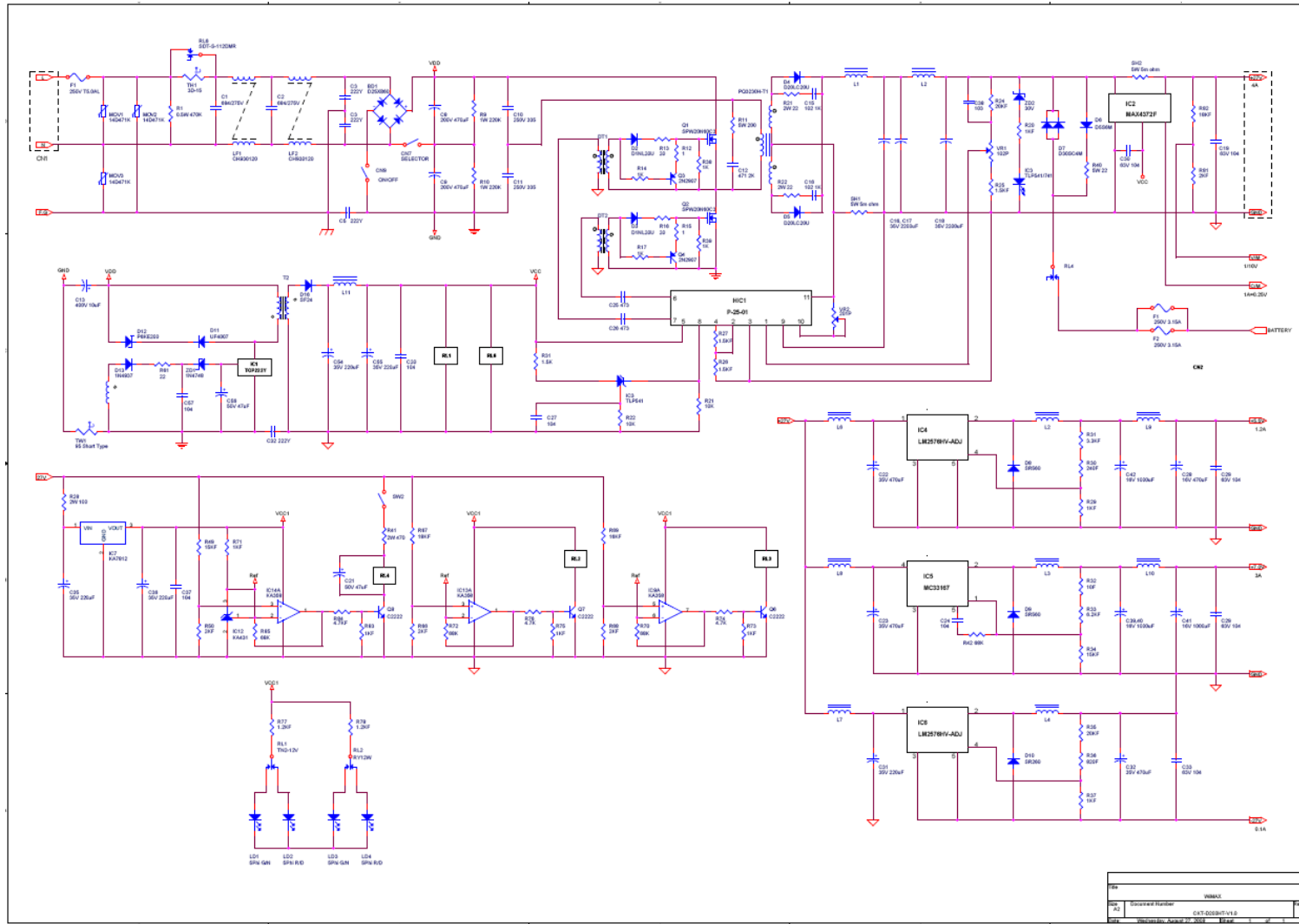


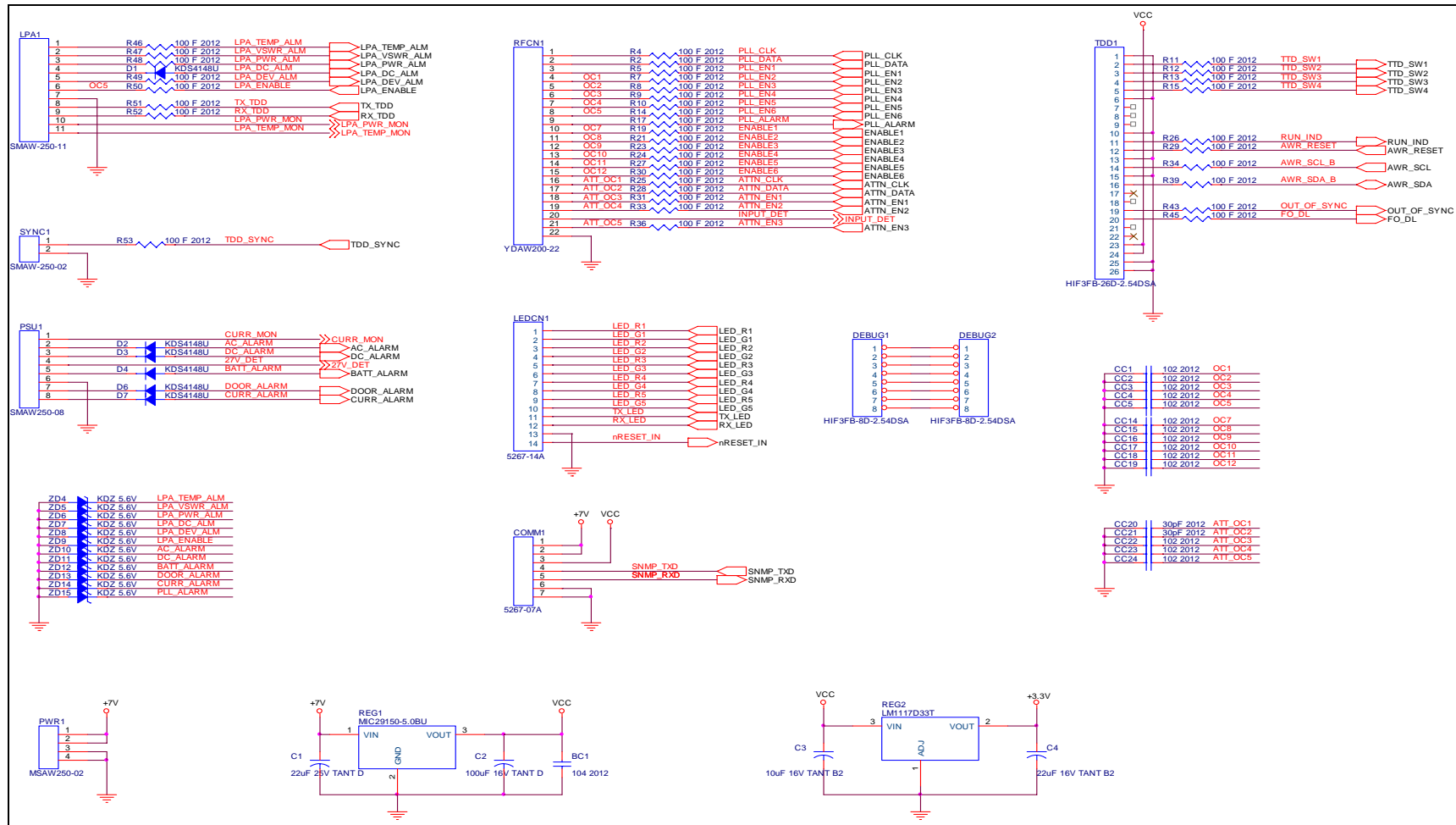
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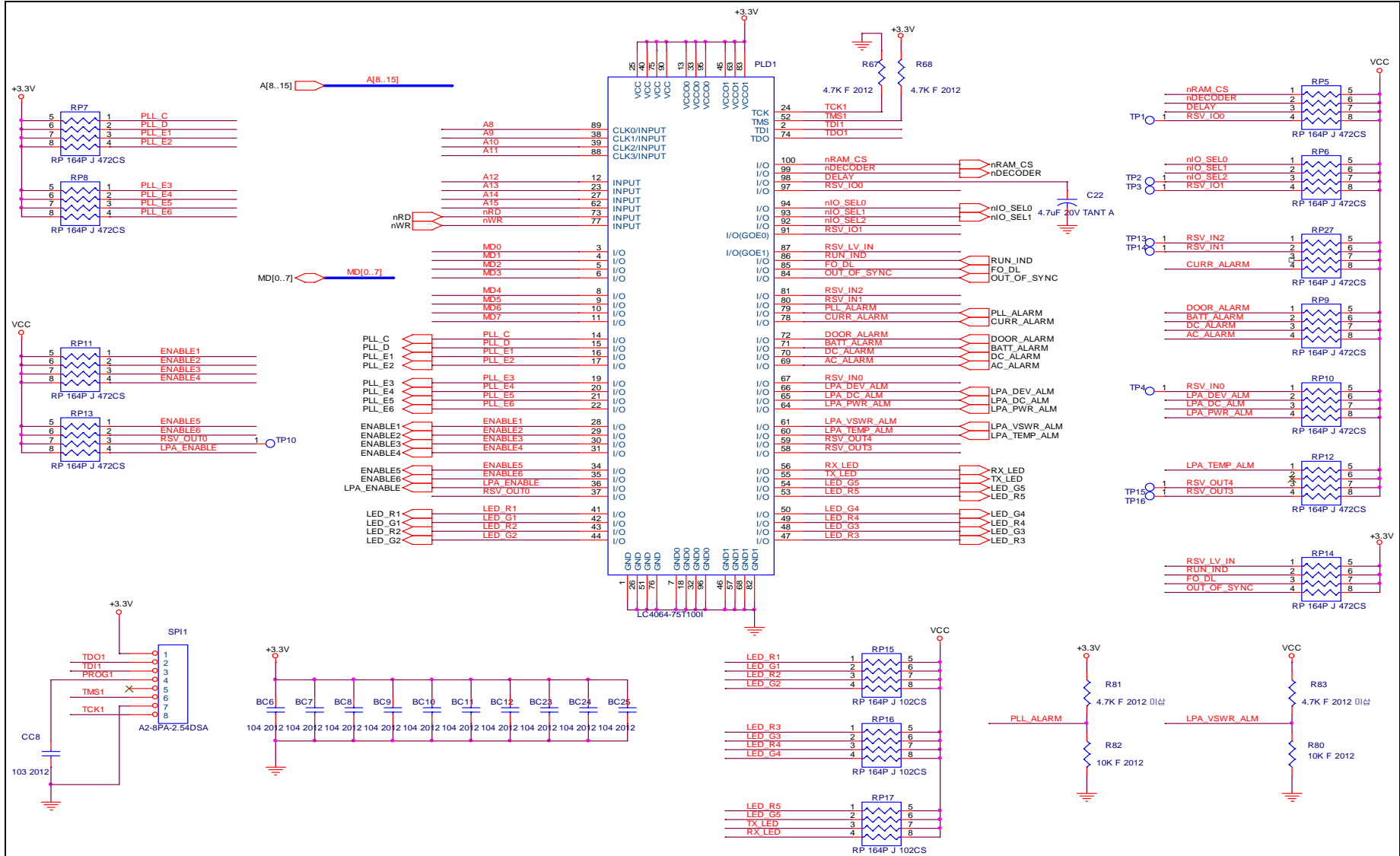
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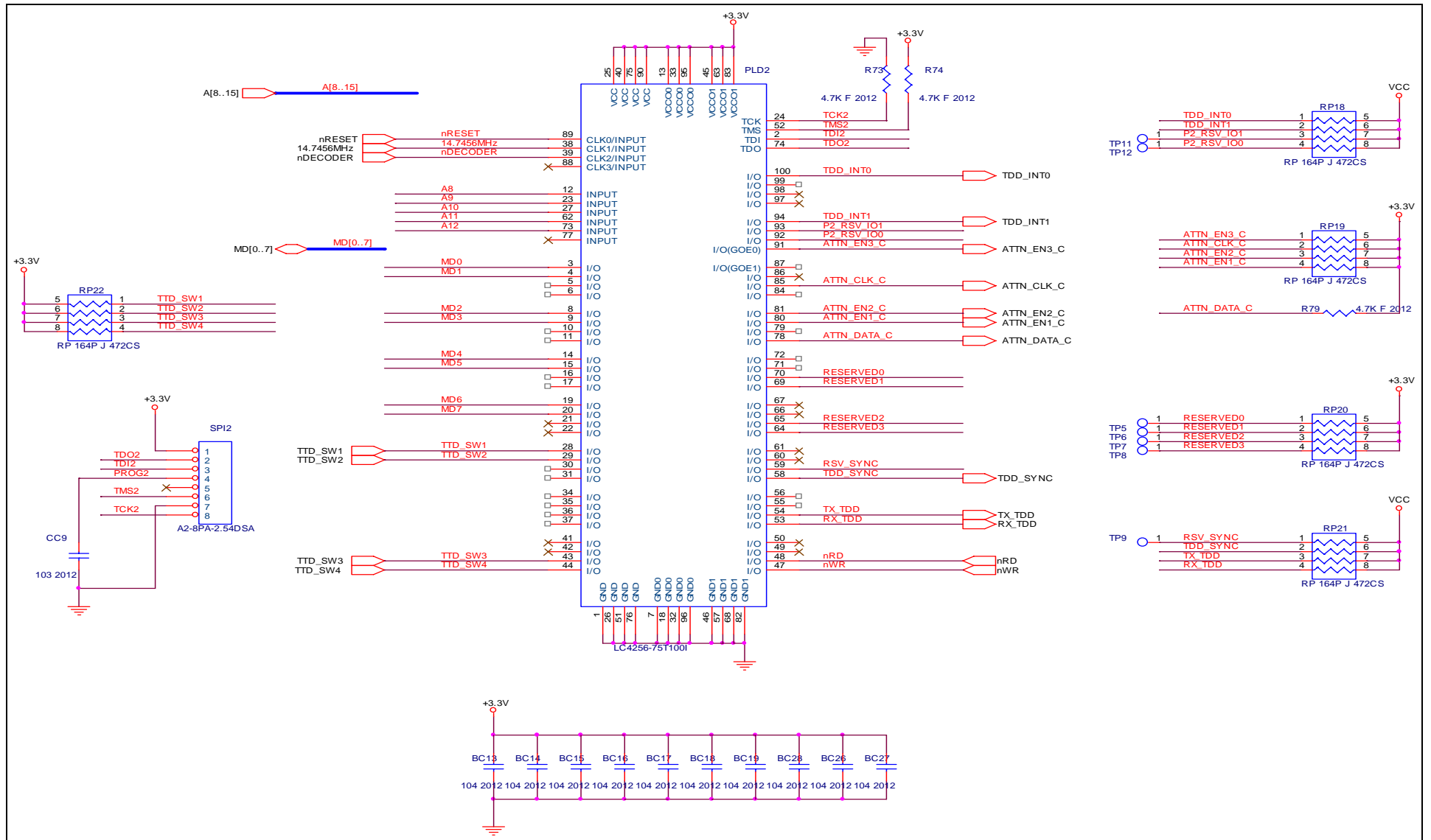


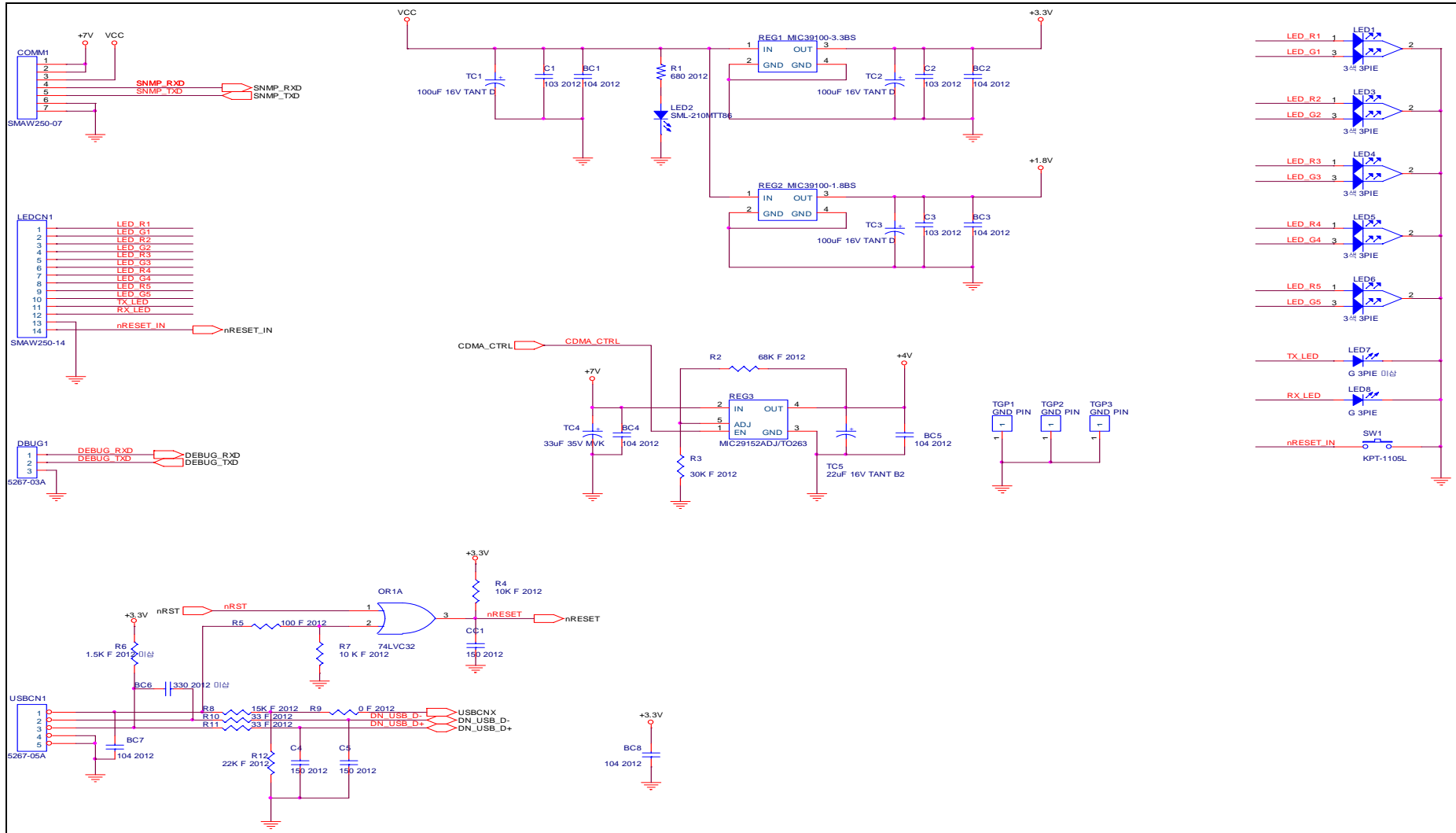
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Rev	Issue Date	2008/07/01	Rev

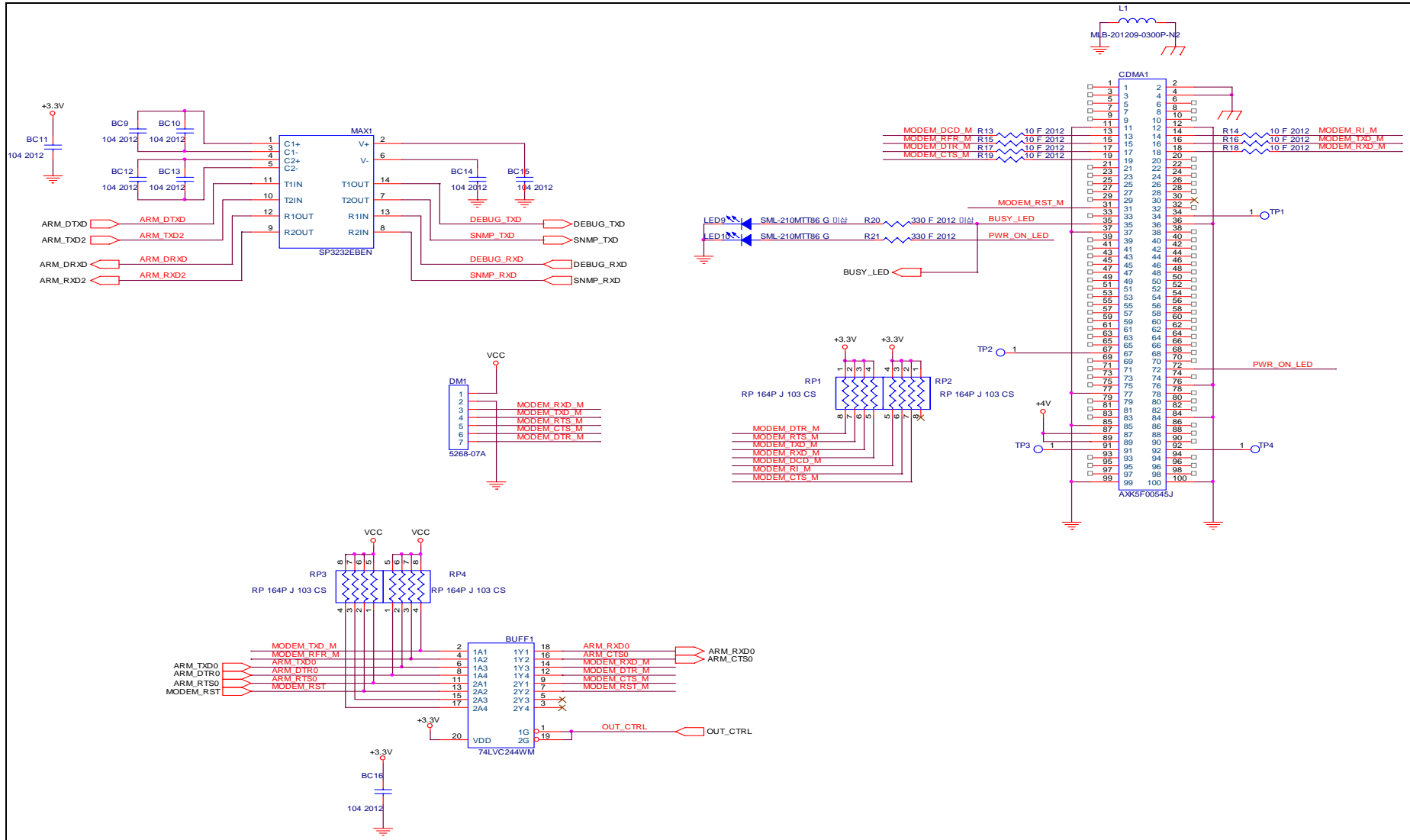
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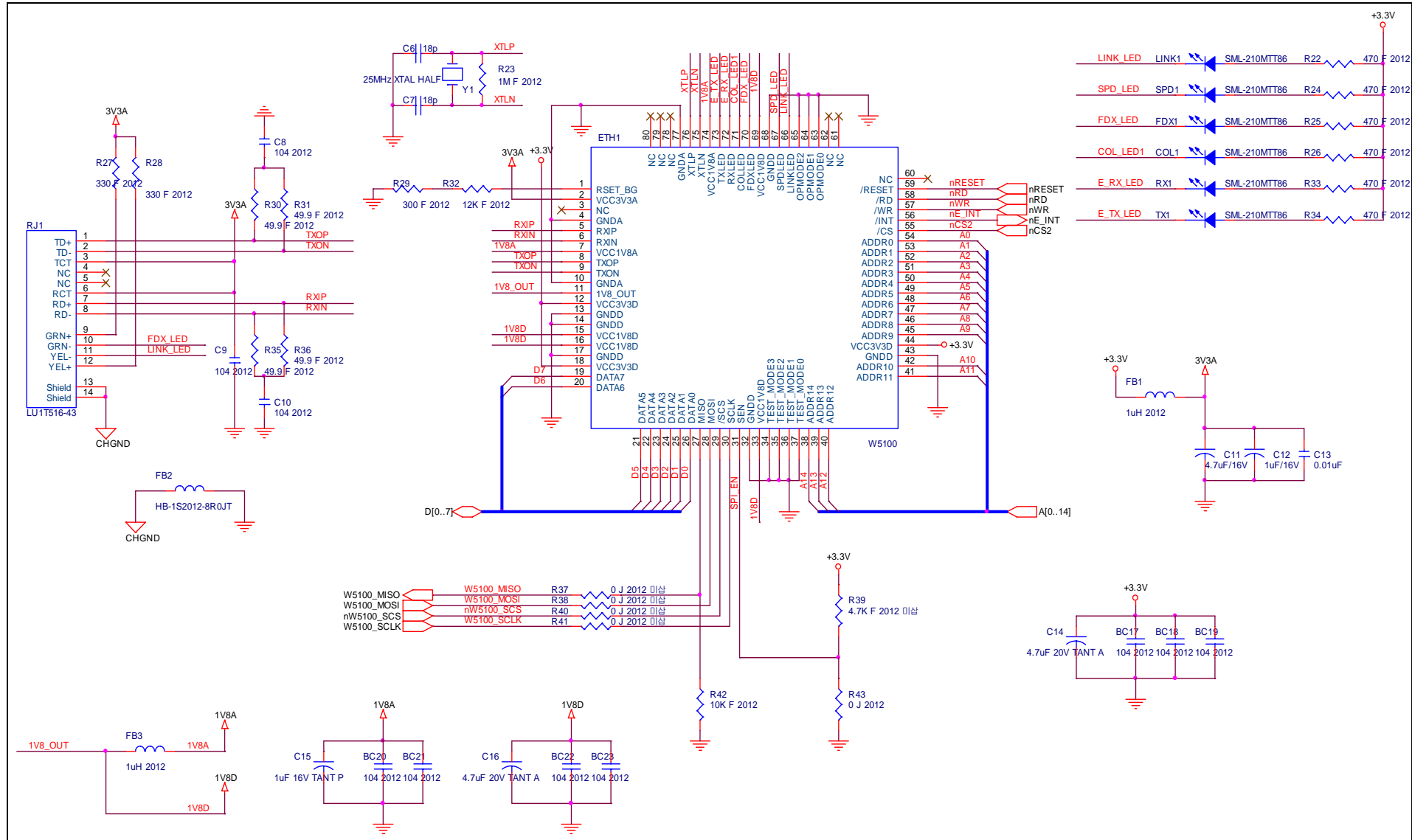


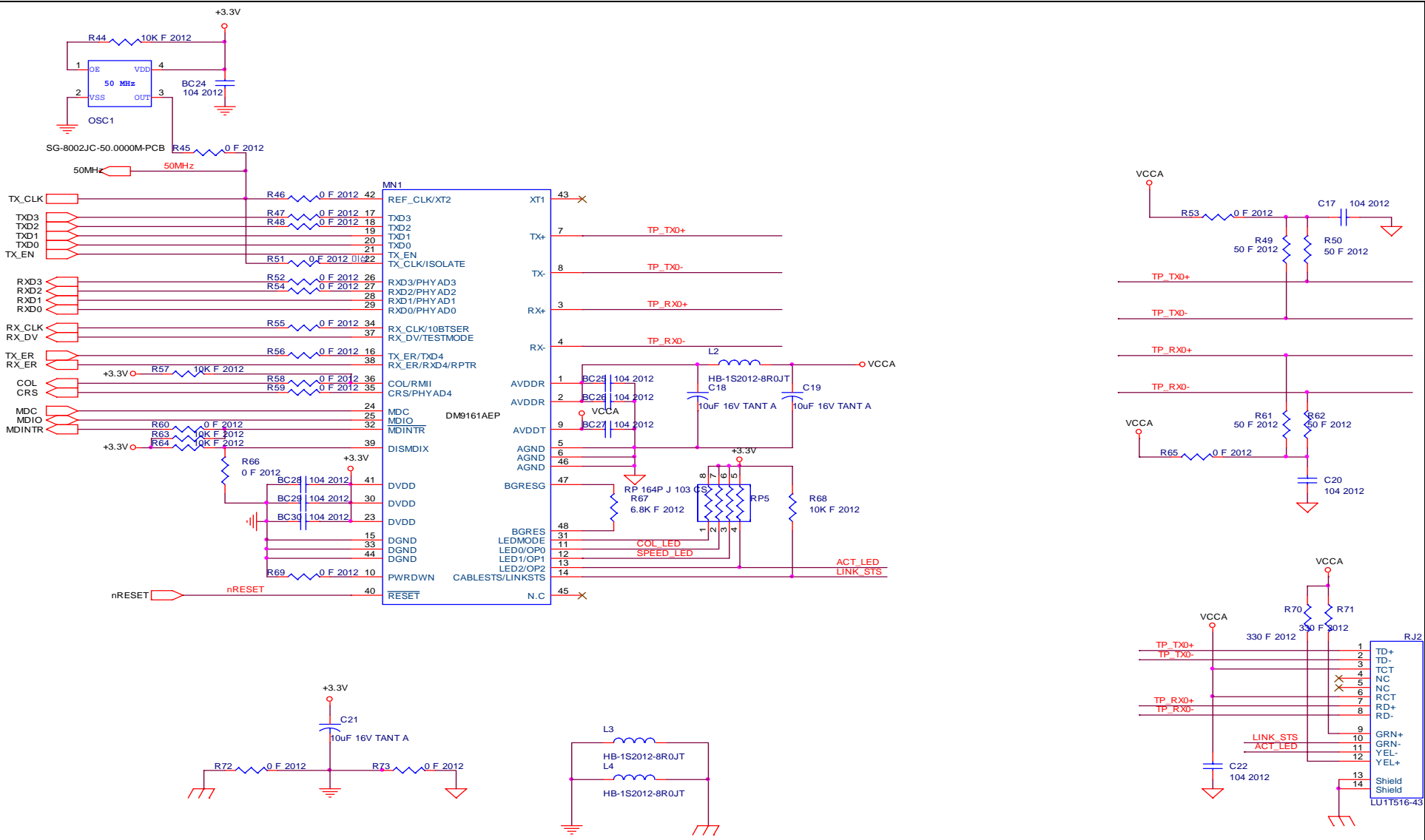


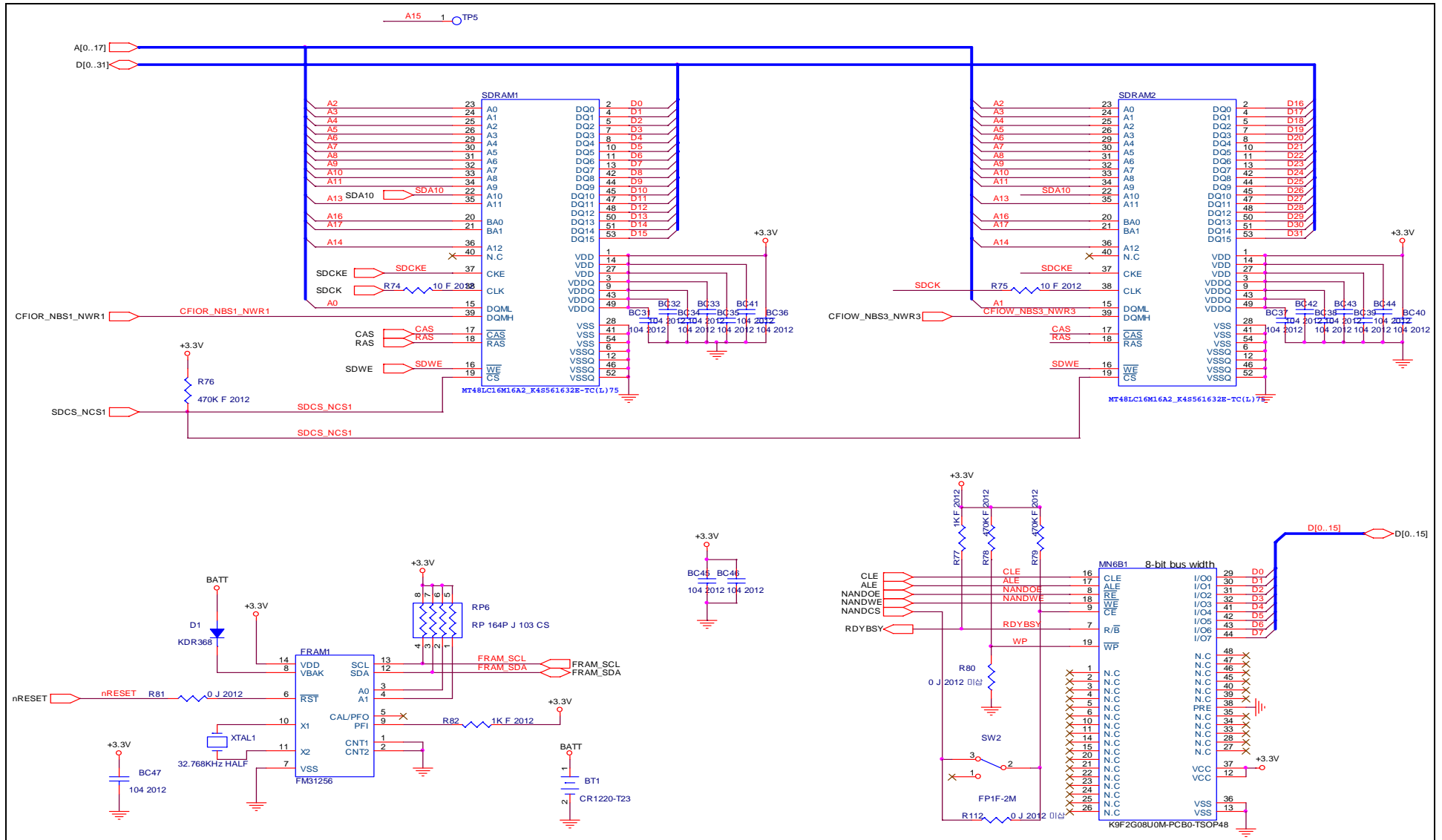




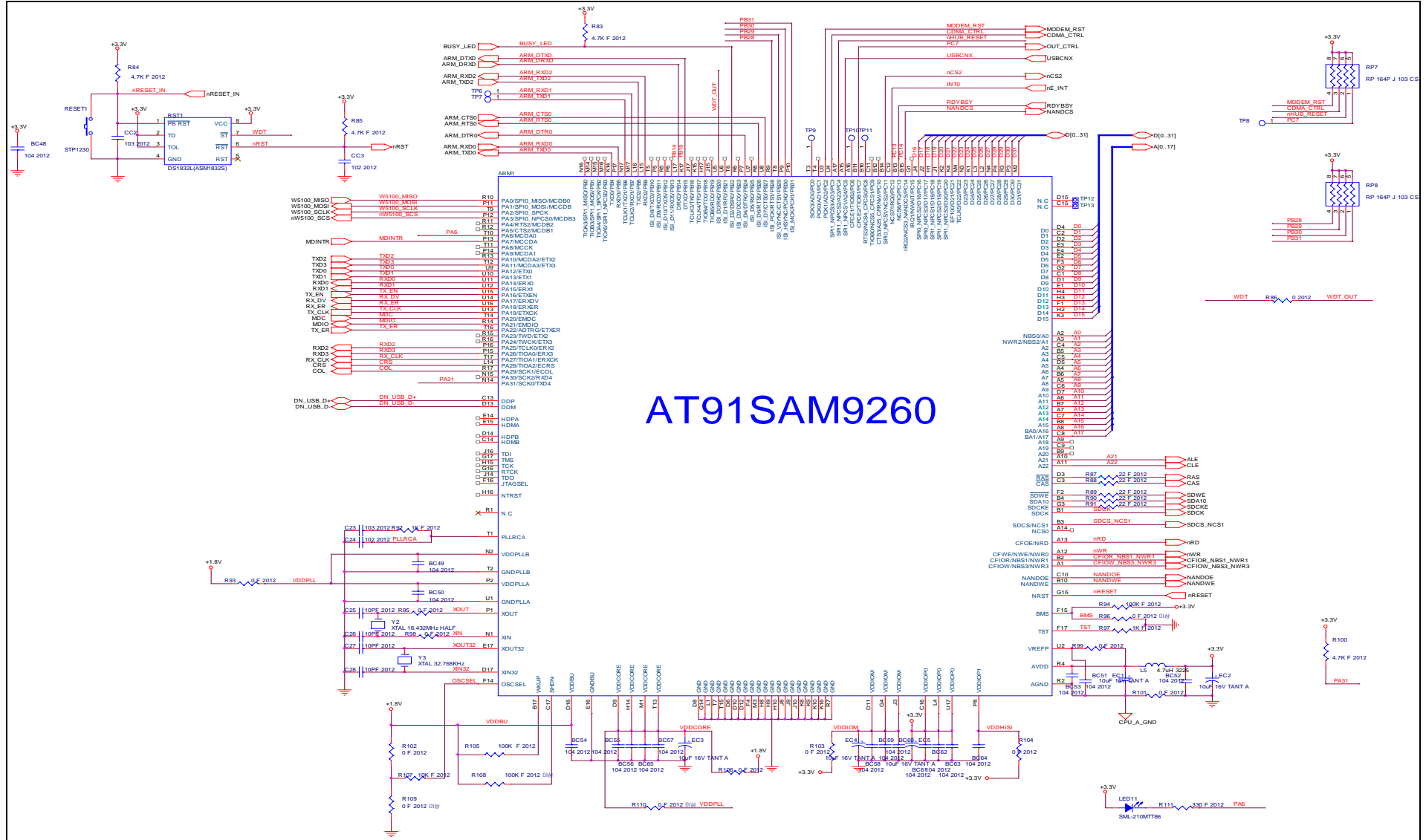




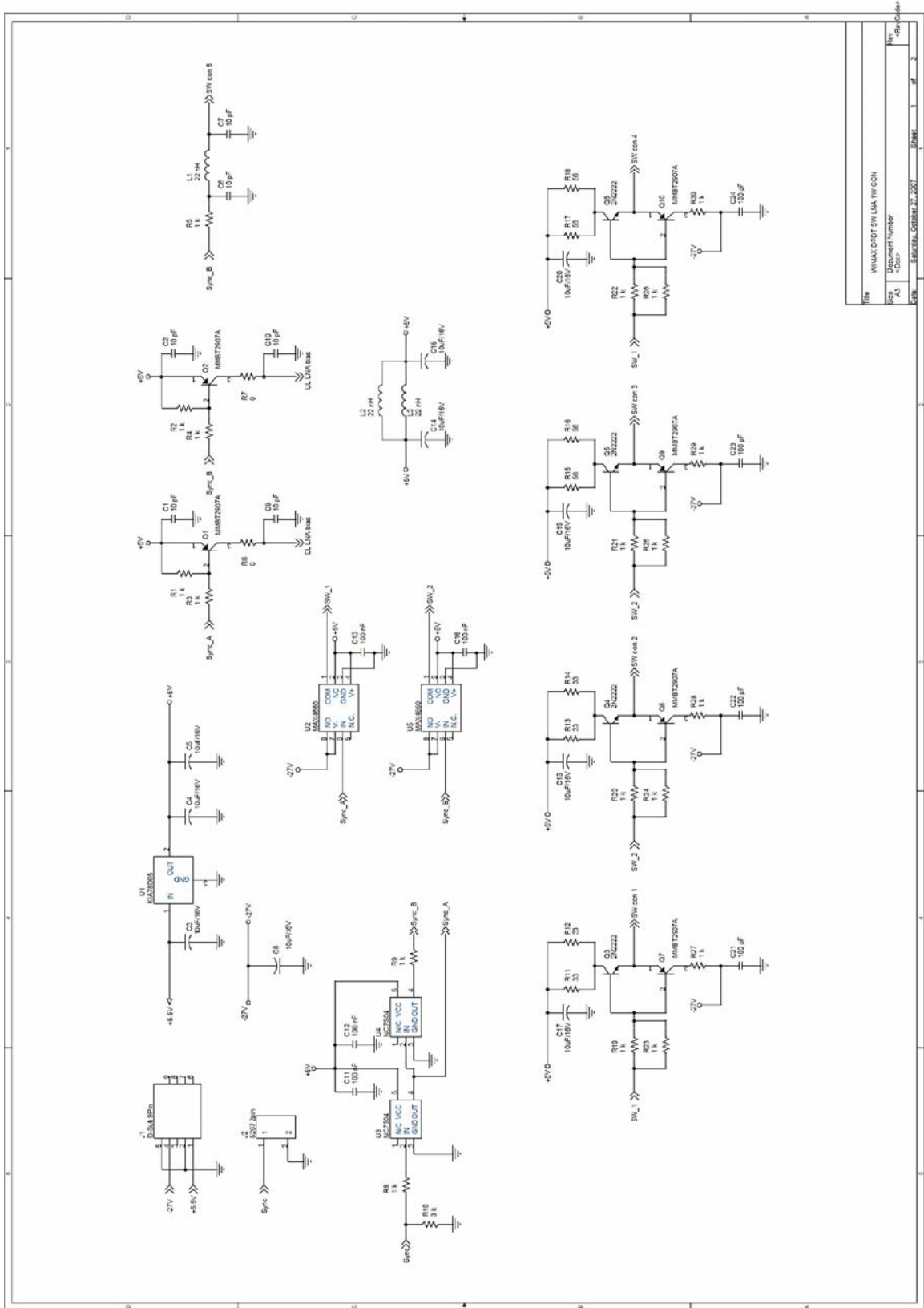




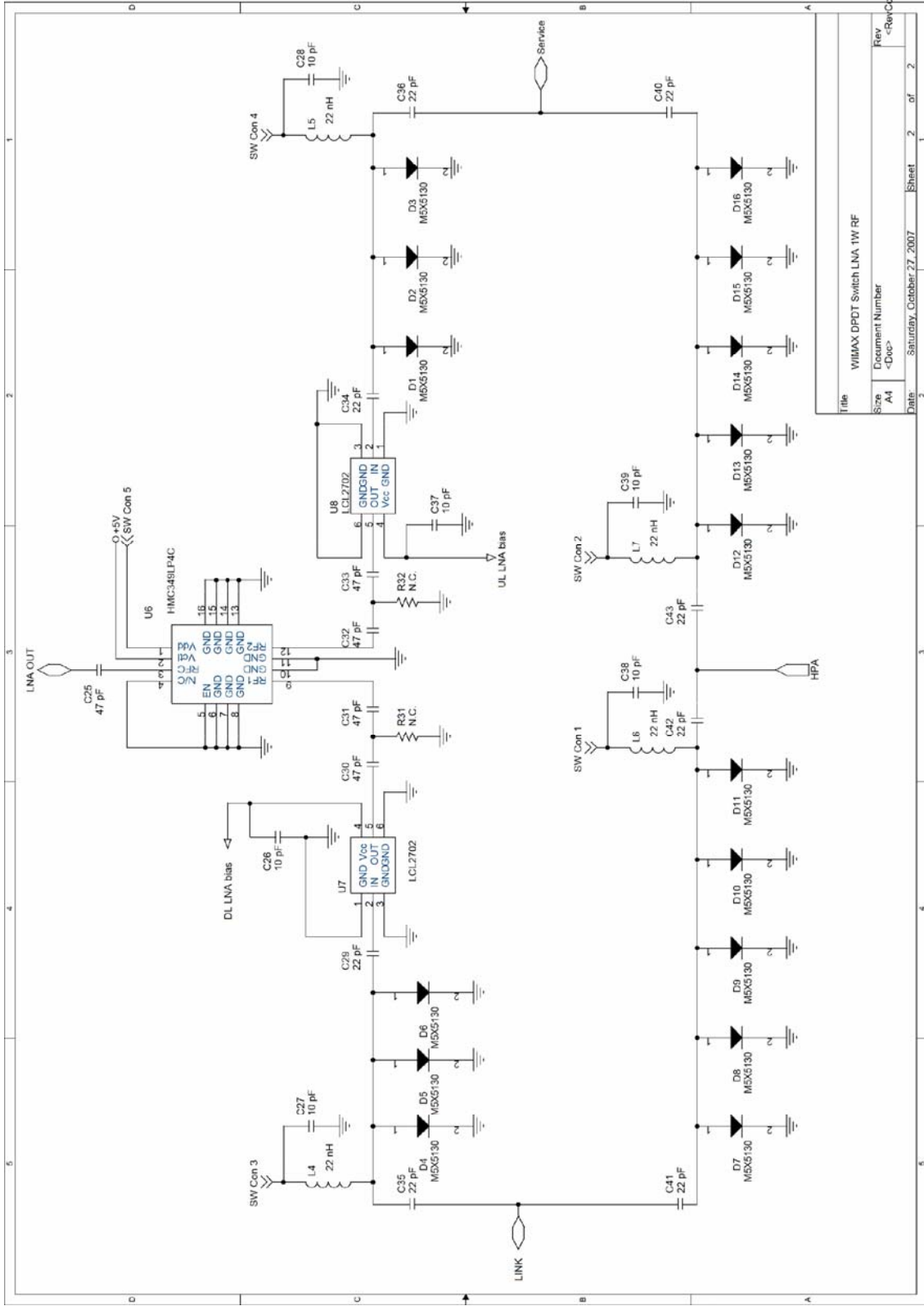
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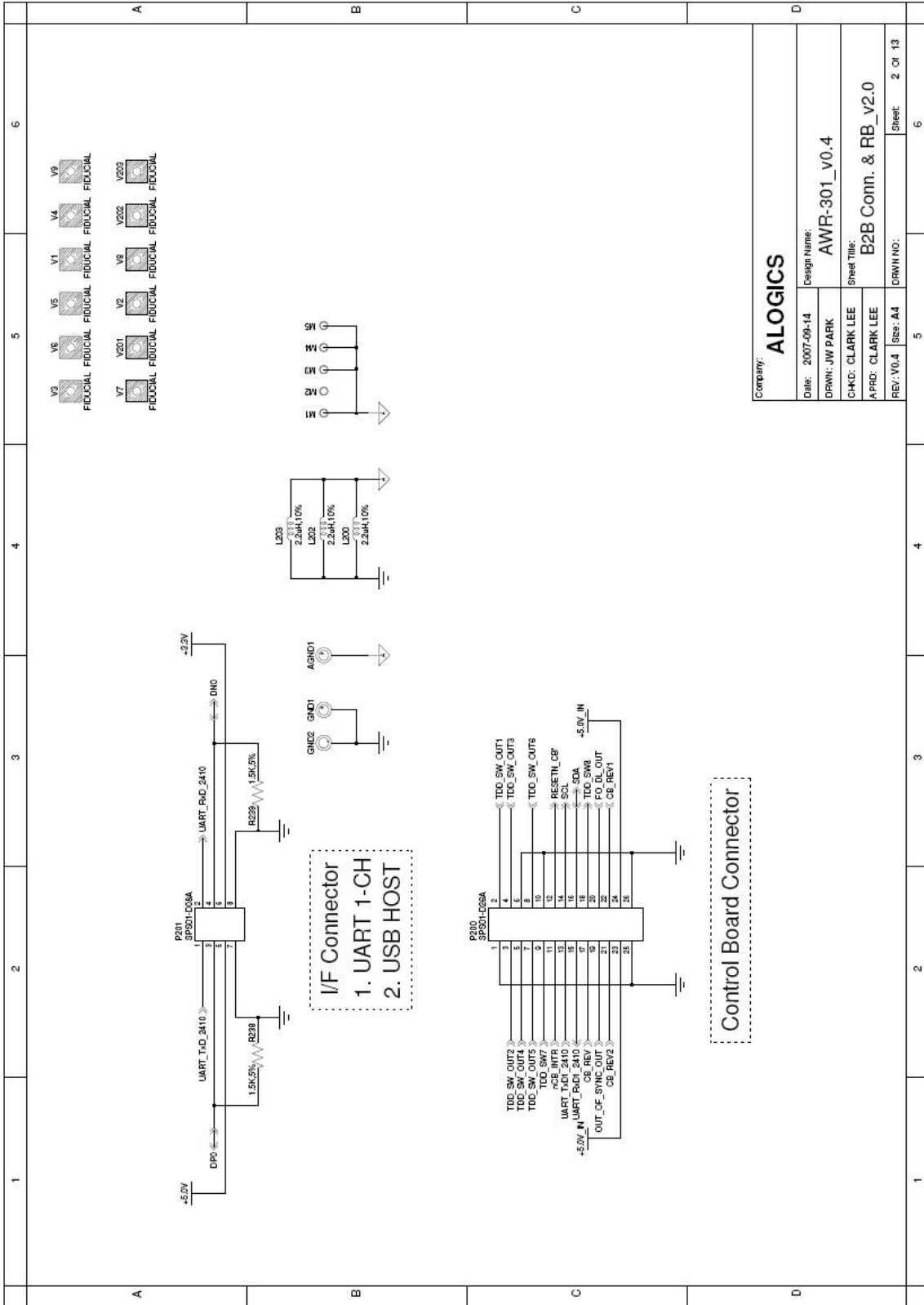
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WINAX-DPOT SW LNA 1W CON	A3	-Doc-	2



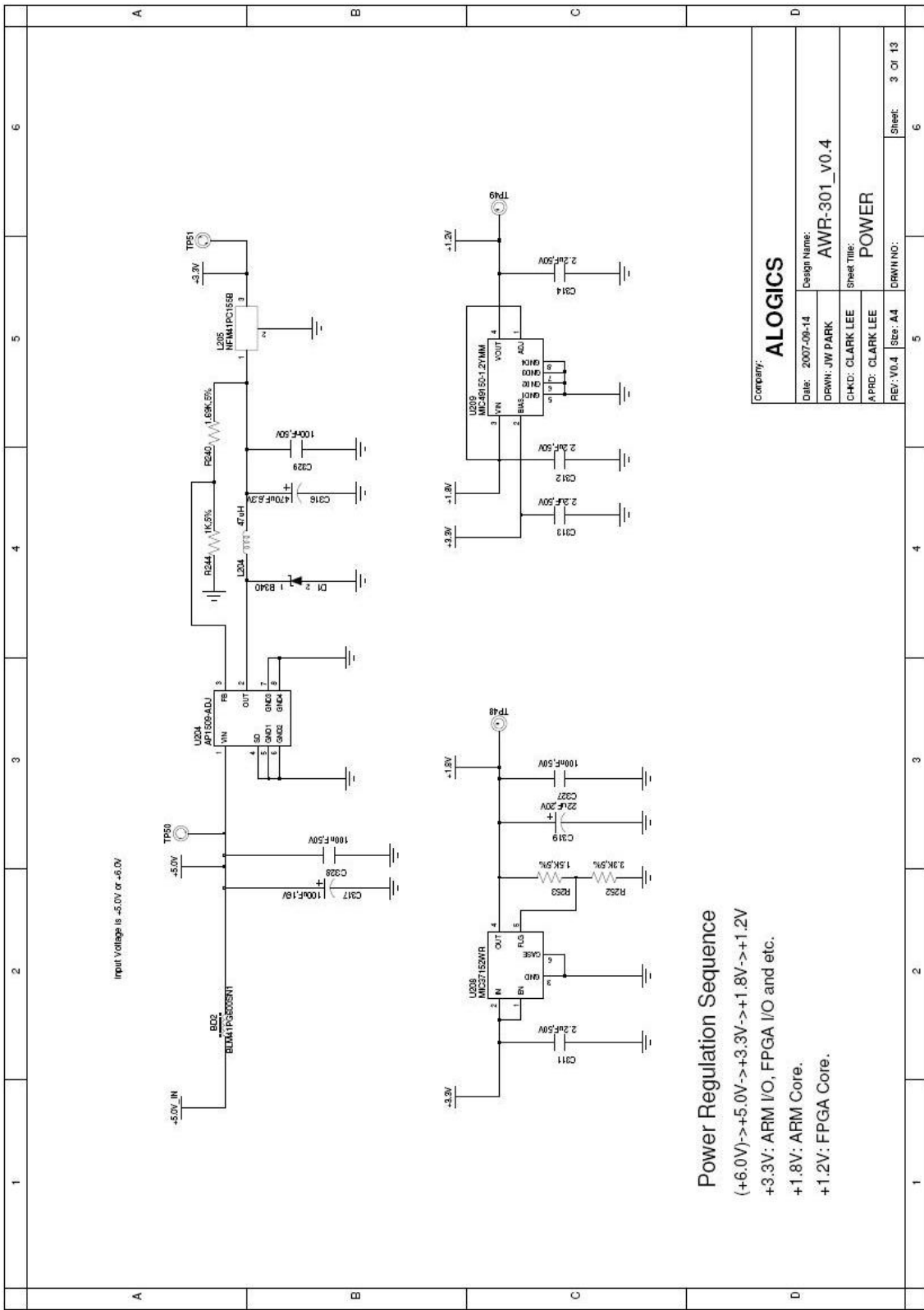
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Size	Document Number	Rev	<RevCode>
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Date	Saturday, October 7, 2007	Sheet	2 of 2



Company: **ALOGICS**

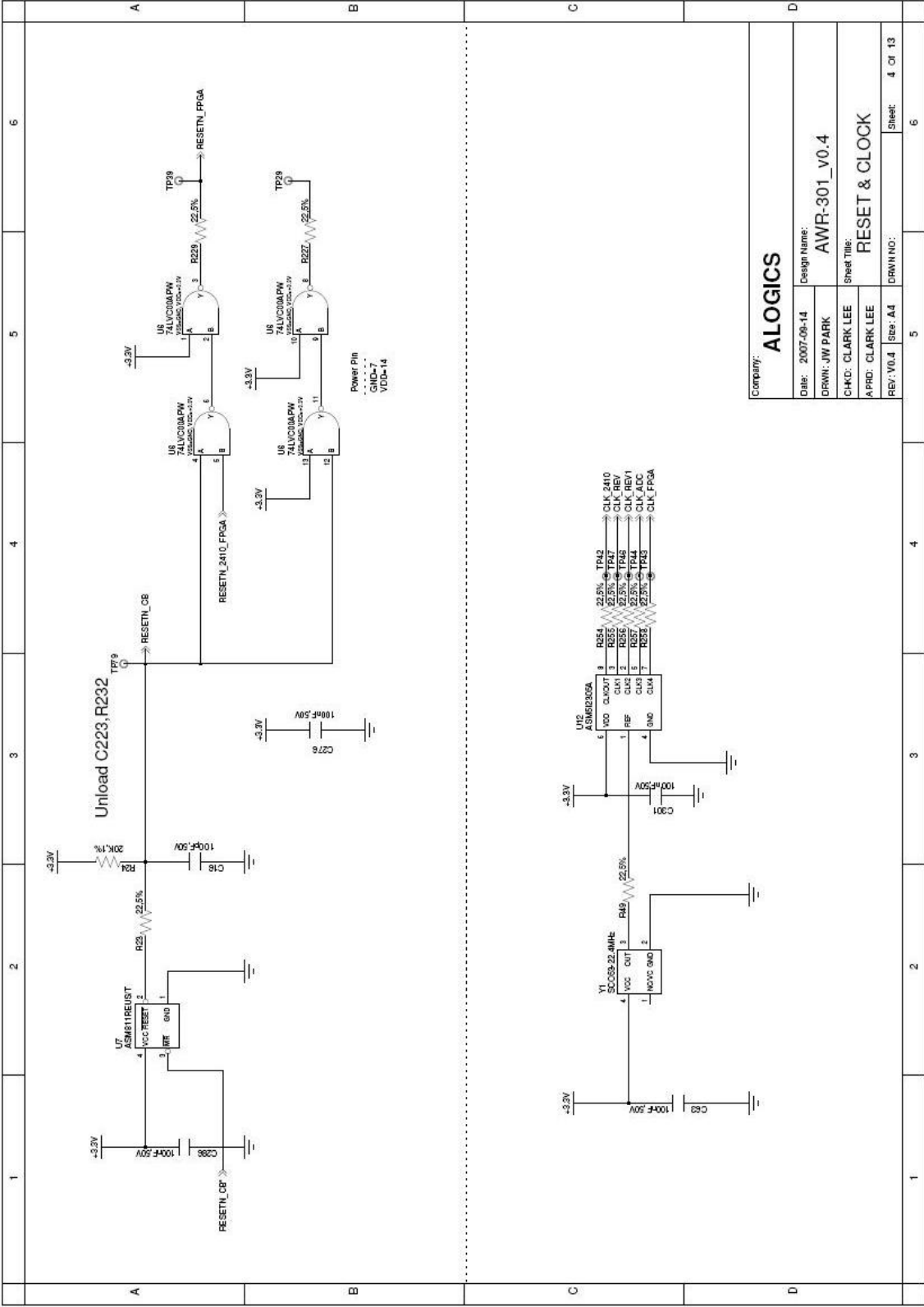
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CHKD: CLARK LEE	APRD: CLARK LEE
REV: V0.4 Ser: A4	DRWN NO:

Sheet: 2 of 13



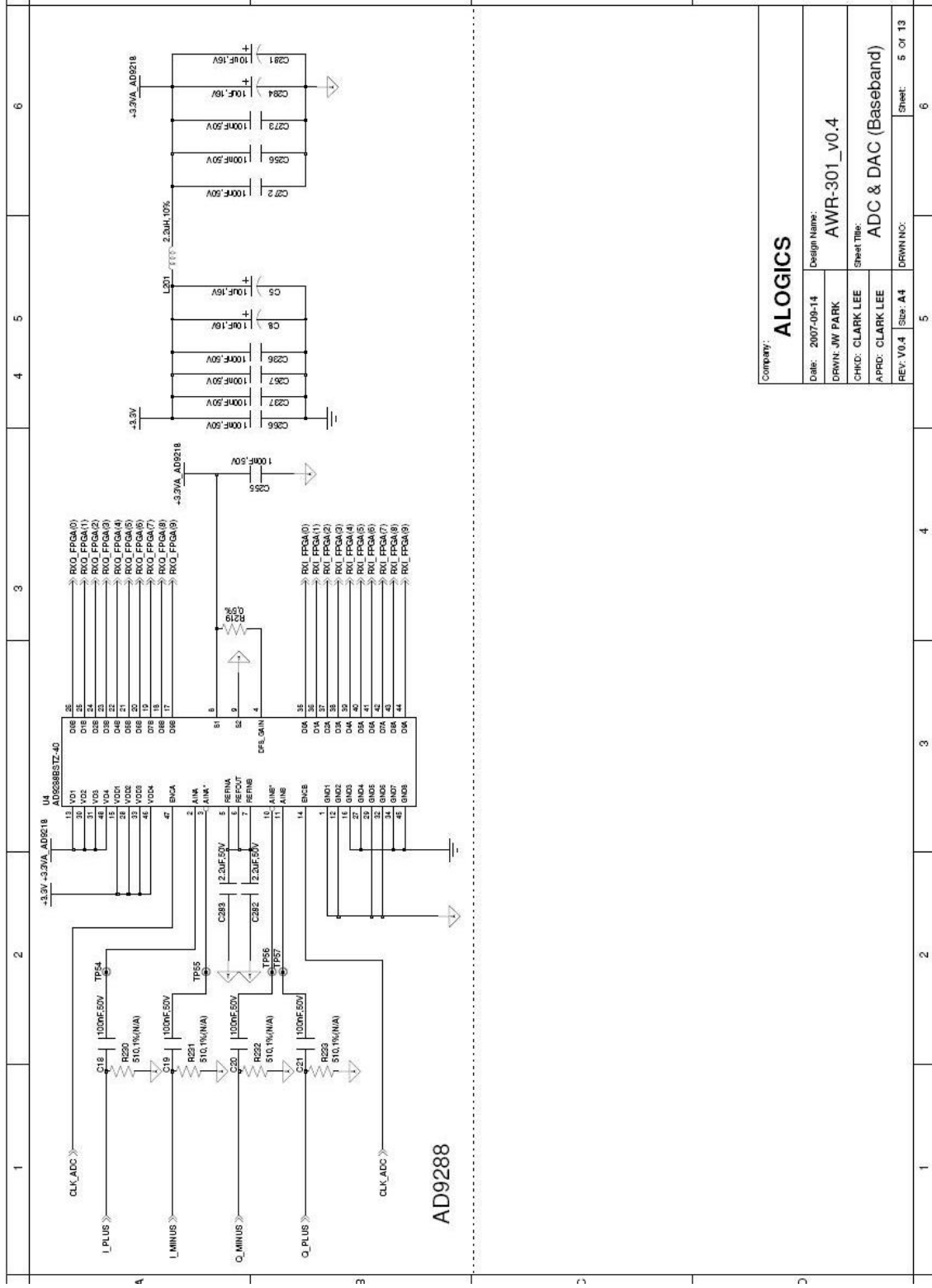
Power Regulation Sequence
 (+6.0V)->+5.0V->+3.3V->+1.8V->+1.2V
 +3.3V: ARM I/O, FPGA I/O and etc.
 +1.8V: ARM Core.
 +1.2V: FPGA Core.

Company: ALOGICS	
Date: 2007-09-14	Design Name: AWR-301_v0.4
DRWN: JW PARK	Sheet Title: POWER
CHKD: CLARK LEE	APRD: CLARK LEE
REV: V0.4	Size: A4
Sheet: 3	Of 13

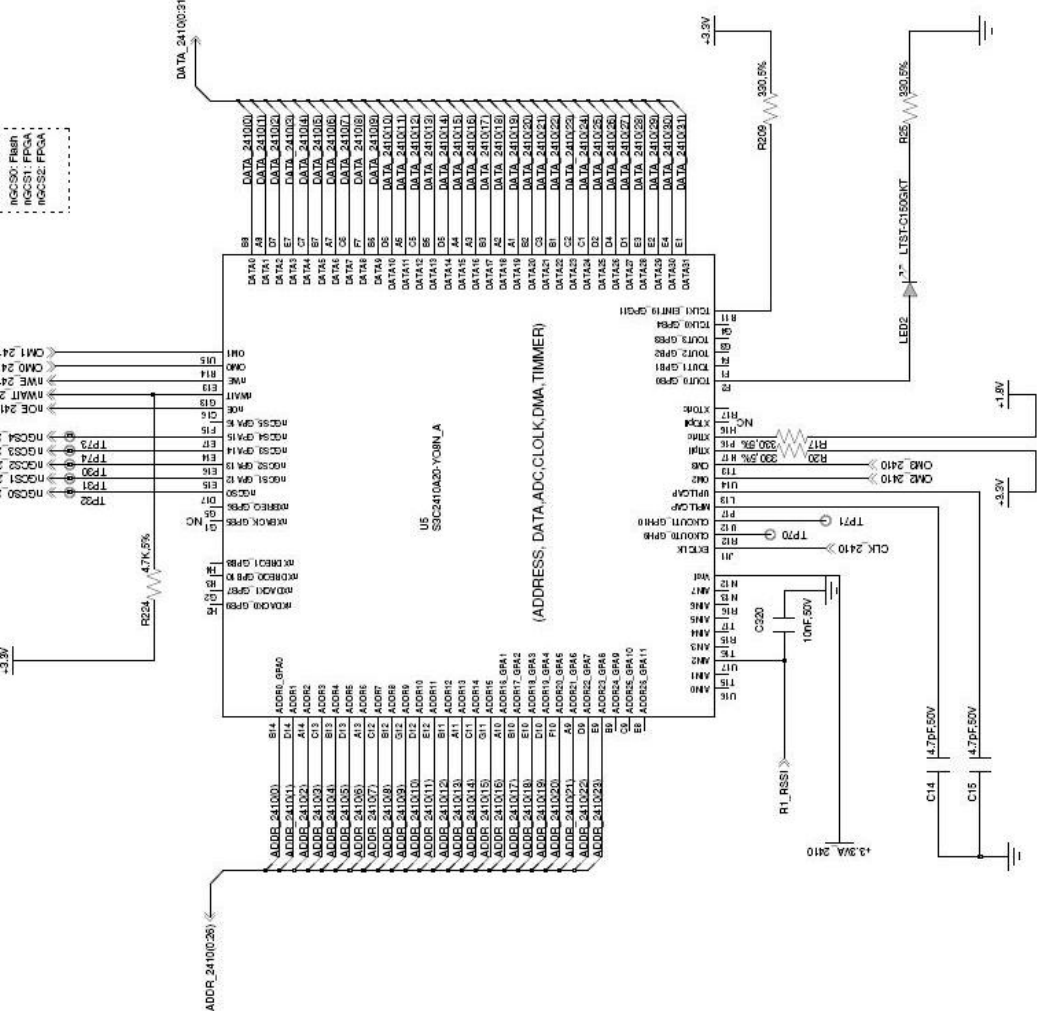
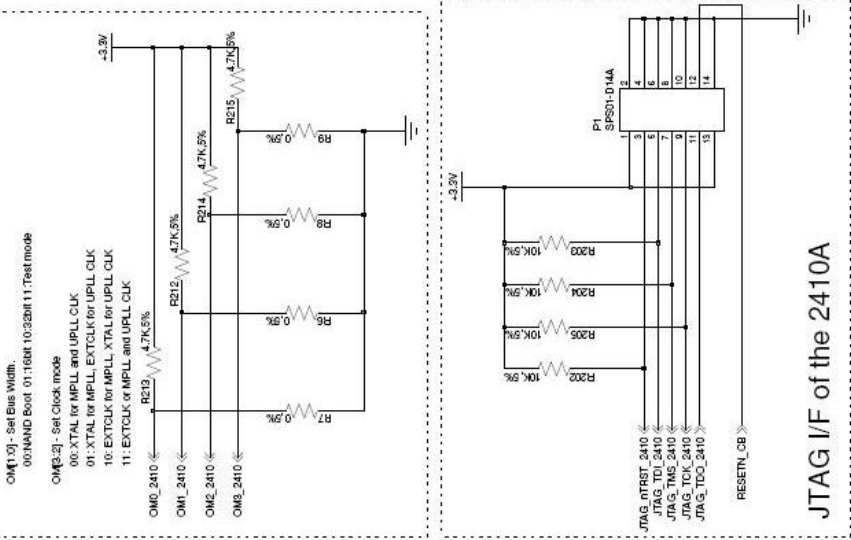


Company: **ALOGICS**

Date:	2007-08-14	Design Name:	AWR-301_v0.4
Drawn:	JW PARK	Sheet Title:	RESET & CLOCK
Checked:	CLARK LEE	Drawn No.:	4 Of 13
Approved:	CLARK LEE	Sheet:	4 Of 13
Rev:	V0.4	Spec:	A4

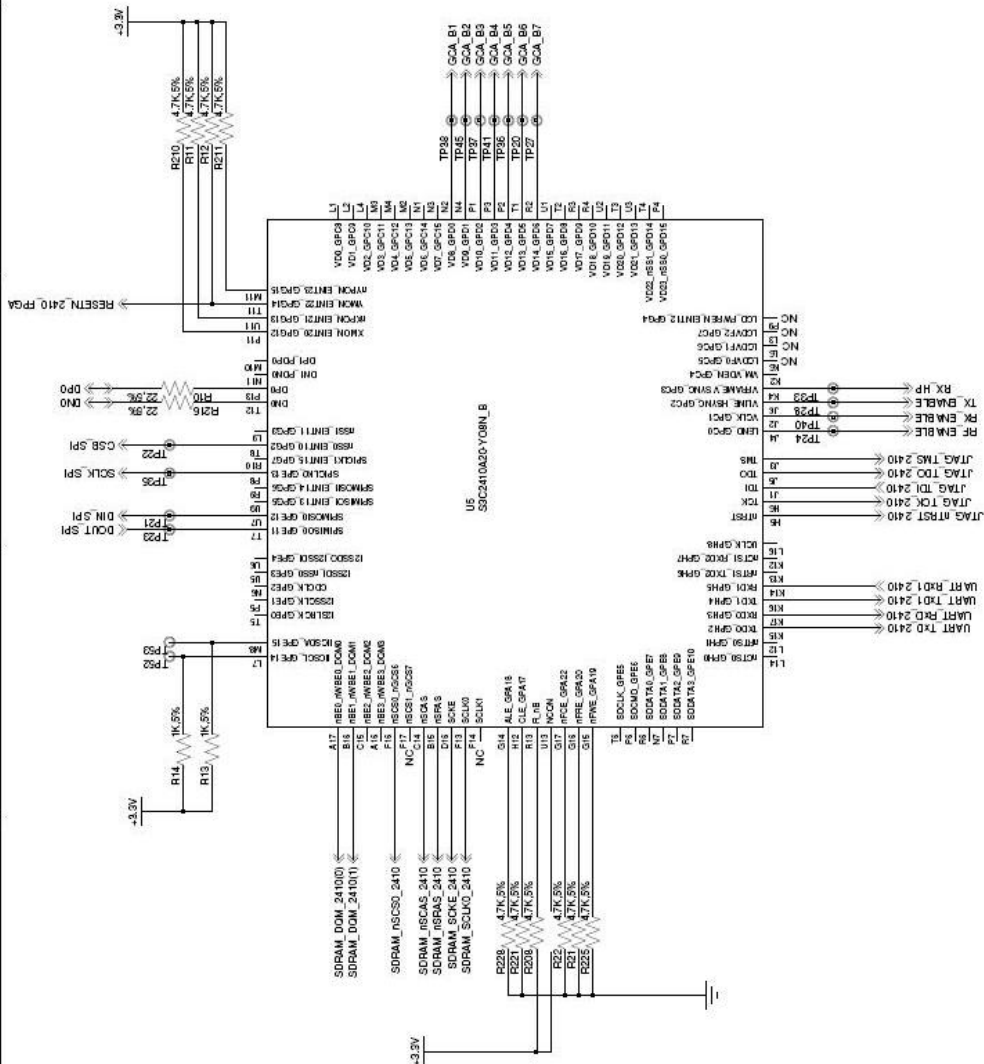


Company: ALOGICS	
Date: 2007-09-14	Design Name: AWR-301_v0.4
DRWN: JW PARK	Sheet Title: ADC & DAC (Baseband)
CHKD: CLARK LEE	Size: A4
APRD: CLARK LEE	DRWN NO: 5 of 13
REV: V0.4	Sheet: 5 of 13



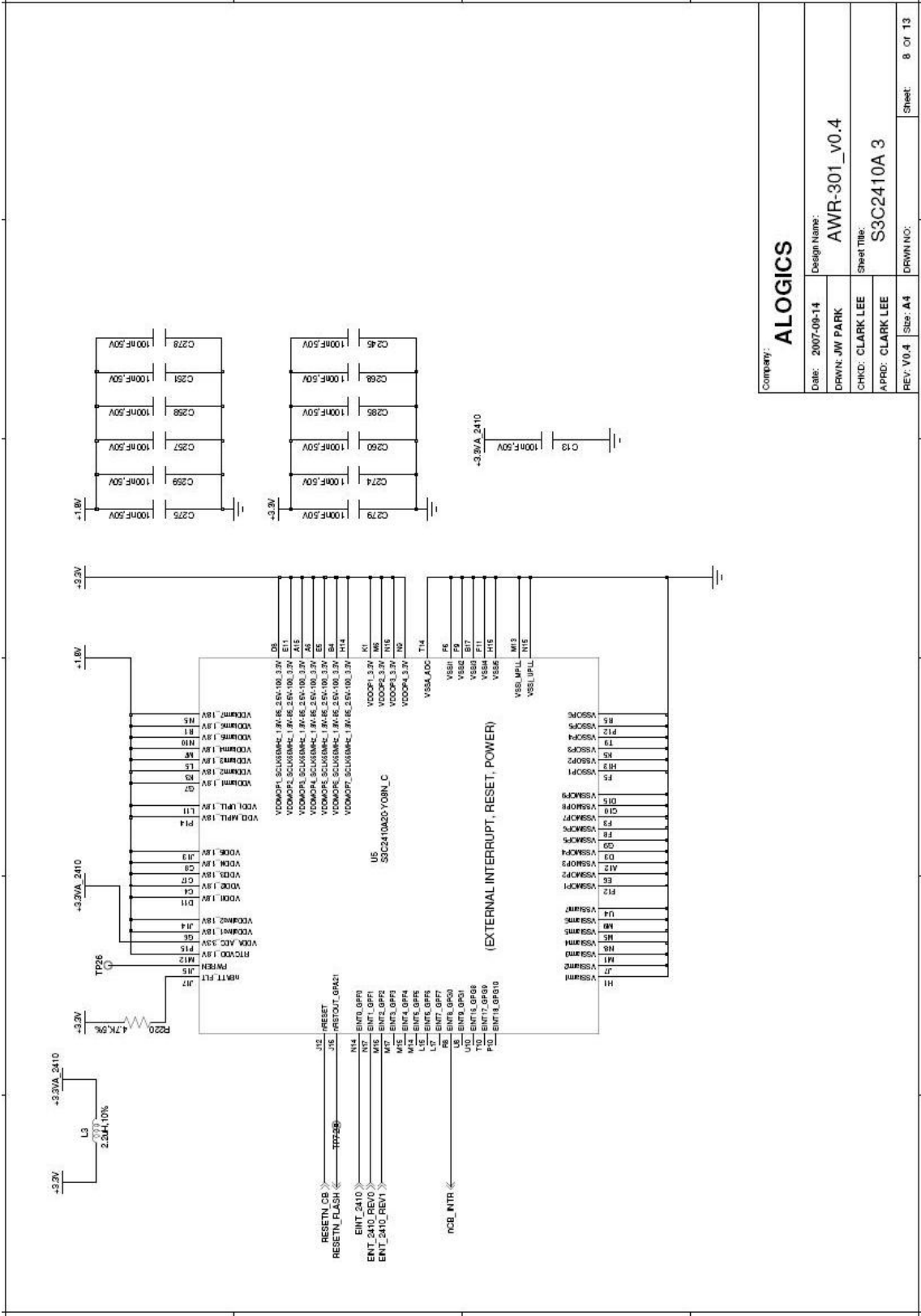
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2	JTAG_TMS_2410	JTAG Test Mode Select
3	JTAG_TCK_2410	JTAG Test Clock
4	JTAG_TDO_2410	JTAG Test Data Out
5	RESETN_CB	Reset (Active Low)

DN0/DP0: USB HOST
 DN1/DP1: USB Device

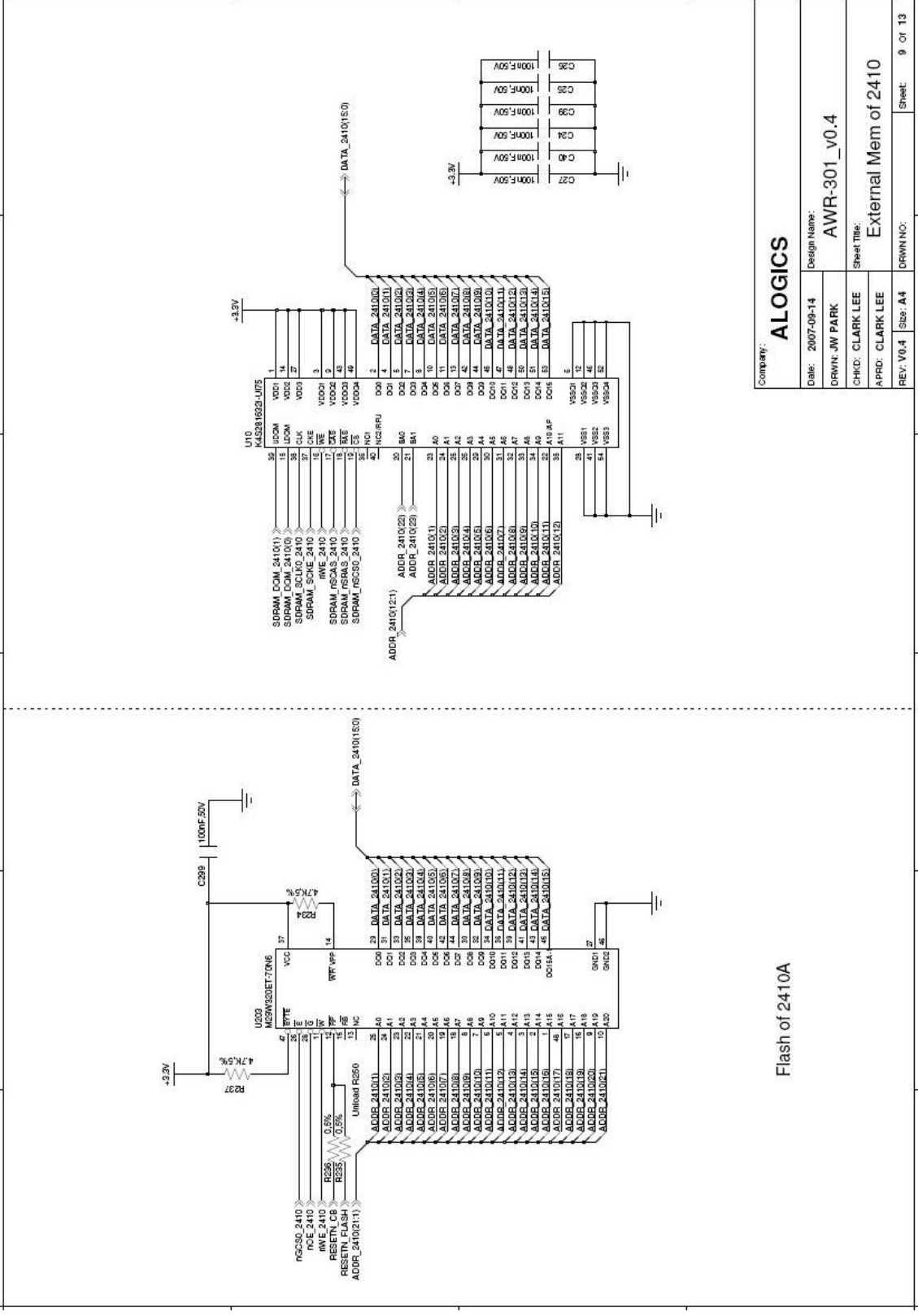


ALOGICS

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Sheet Title:		S3C2410A 2 & FRAM	
CHKD: CLARK LEE	APPR: CLARK LEE	Sheet No:	DRWN NO:
Size: A4	Sheet: 7 of 13		



Company: ALOGICS	
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DRWN: JW PARK	Sheet Title: S3C2410A 3
CHKD: CLARK LEE	APRD: CLARK LEE
REV: V0.4	Sheet: 8 of 13



Flash of 2410A

Company: **ALOGICS**

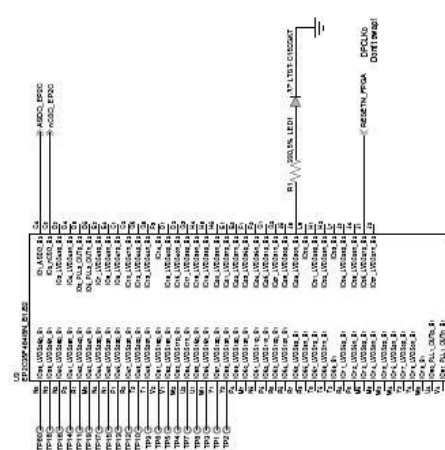
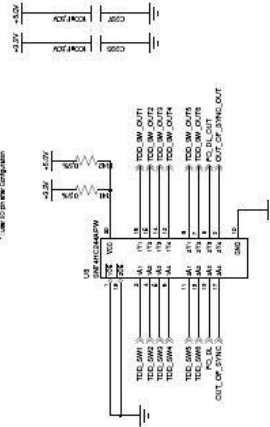
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Size:	A4
DRWING:	Sheet: 9 of 13

External Mem of 2410

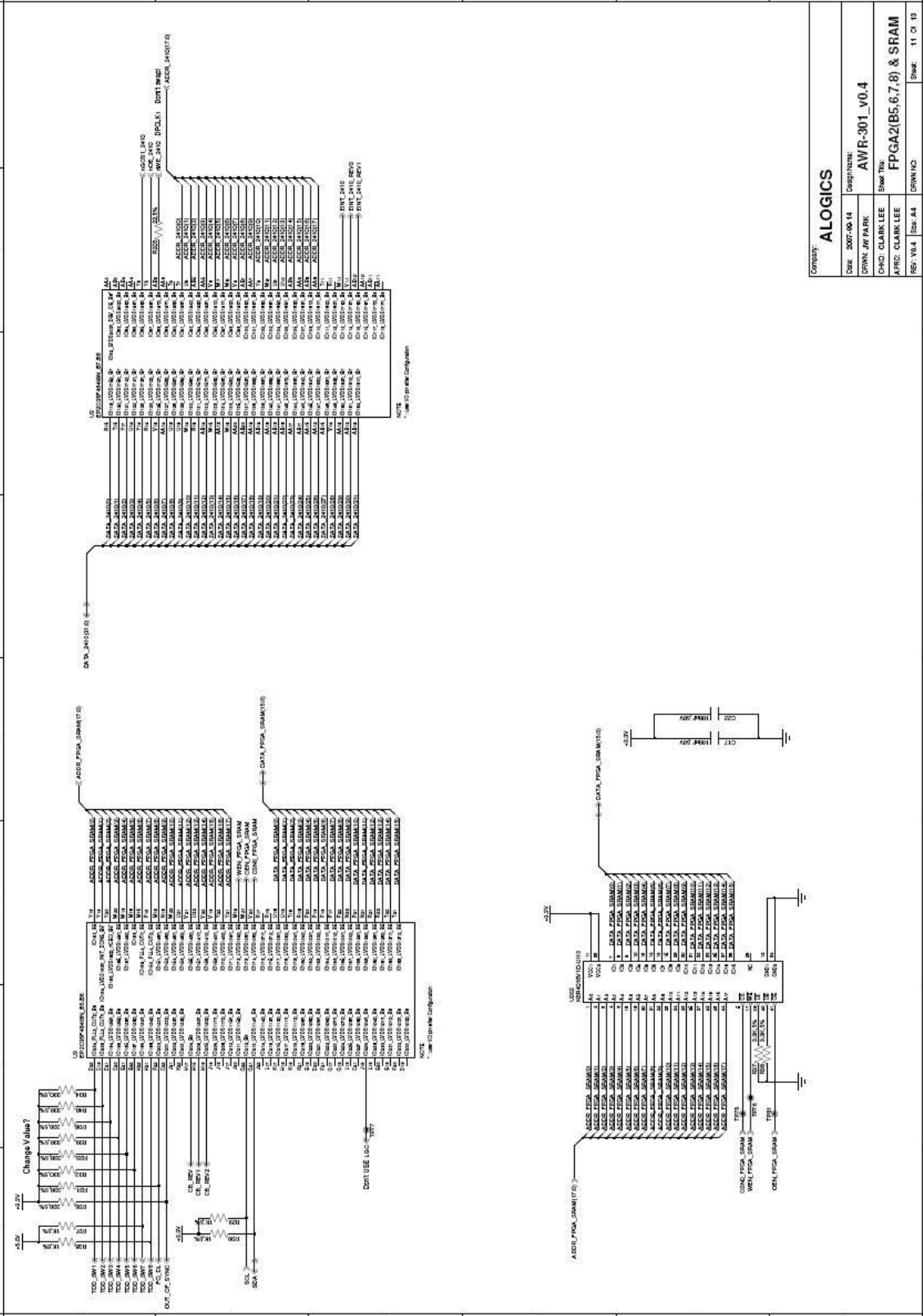
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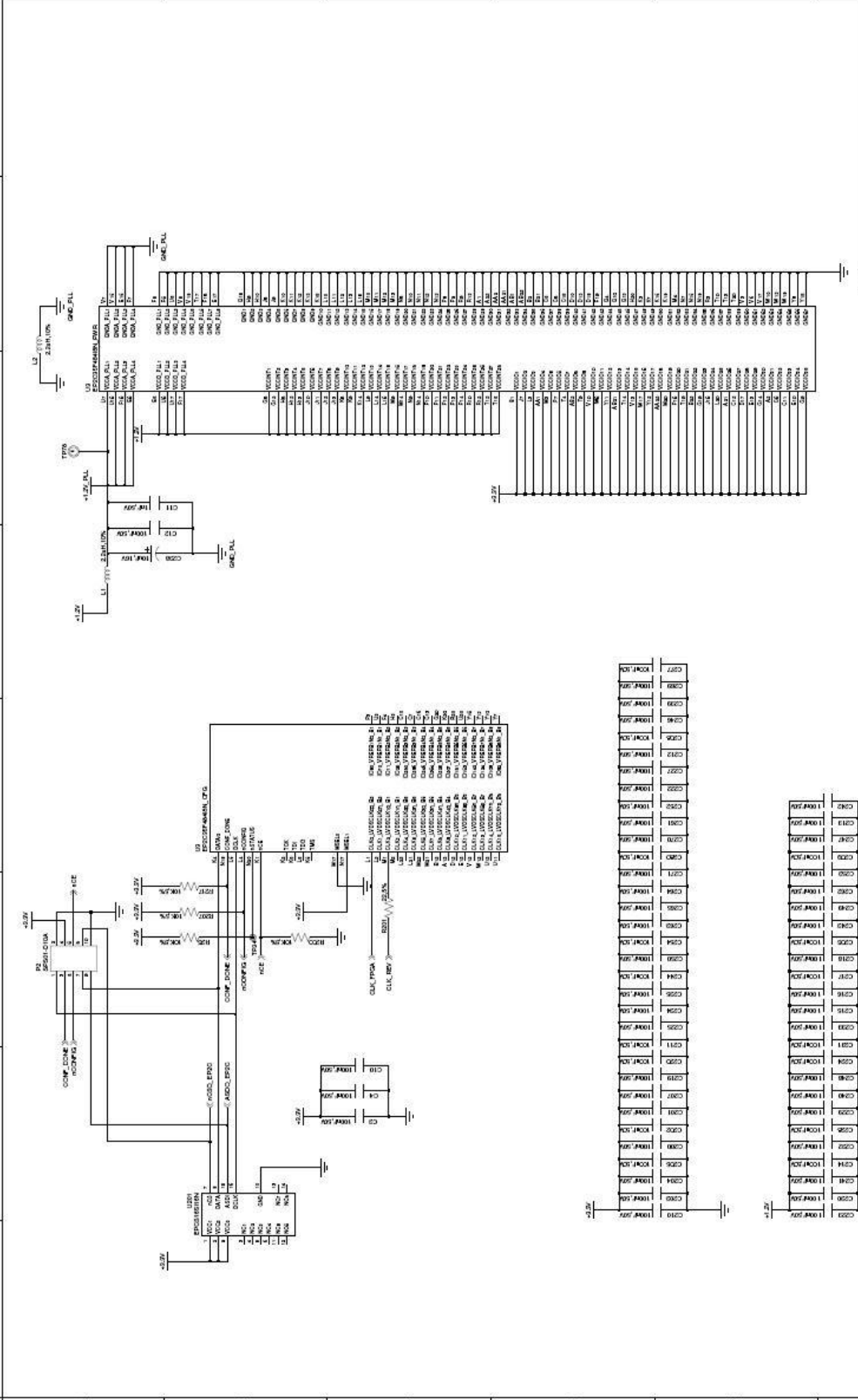
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5	10M	U1000A00	14	10M	U1000A00
6	10M	U1000A00	15	10M	U1000A00
7	10M	U1000A00	16	10M	U1000A00
8	10M	U1000A00	17	10M	U1000A00
9	10M	U1000A00	18	10M	U1000A00
10	10M	U1000A00	19	10M	U1000A00
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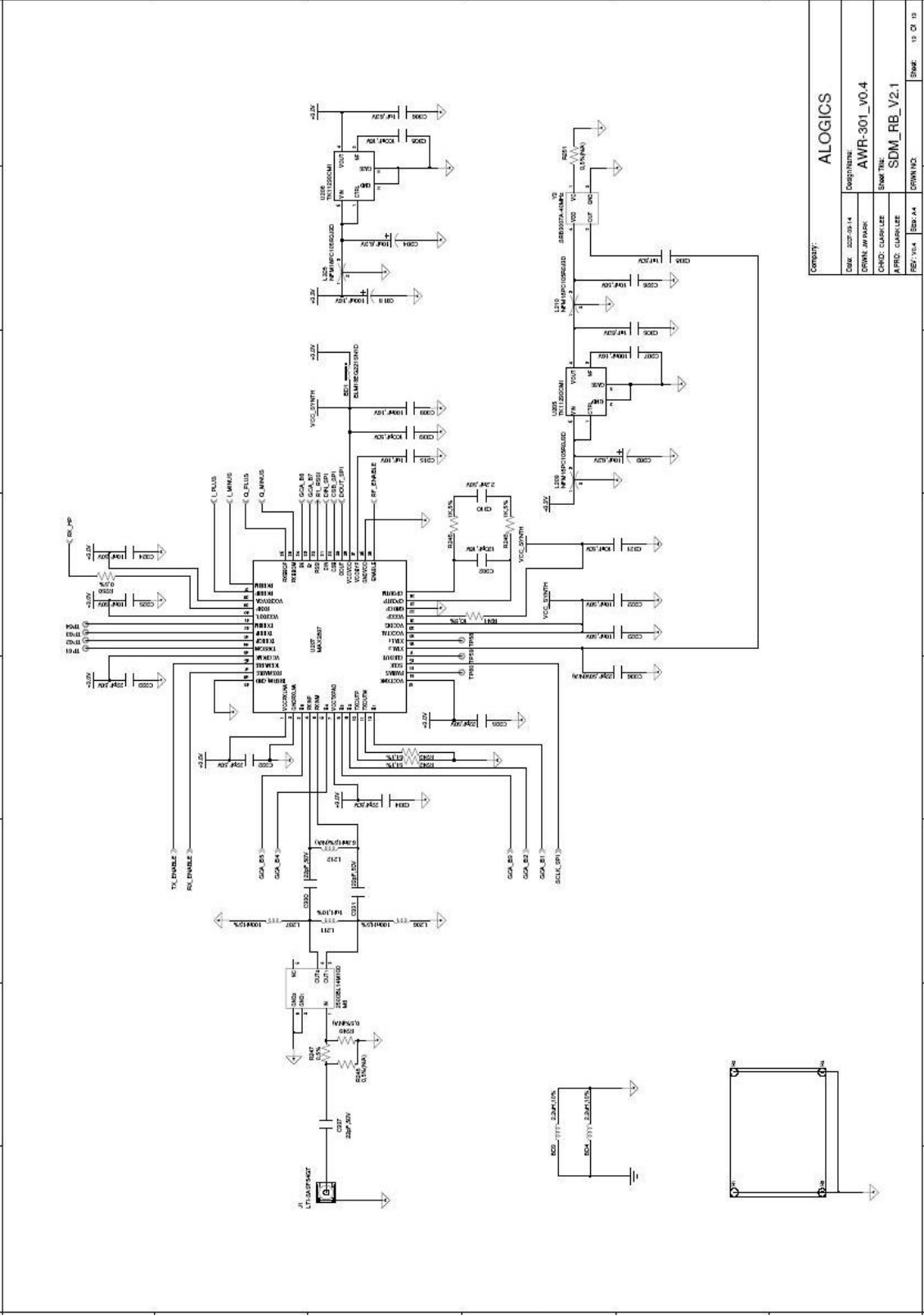
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Checked: CLARK LEE	Drawn: CLARK LEE
Rev: V0.4	Sheet: 10 Of 13





Company: **ALOGICS**
 Date: 2007-06-15 Design Name: **AWR-301_v0.4**
 Drawn By: PARK
 Checked By: CLARK LEE
 Approved By: CLARK LEE
 Rev: V0.4 Rev: A4
 Sheet: 12 of 13

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ALOGICS

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REVNO	001

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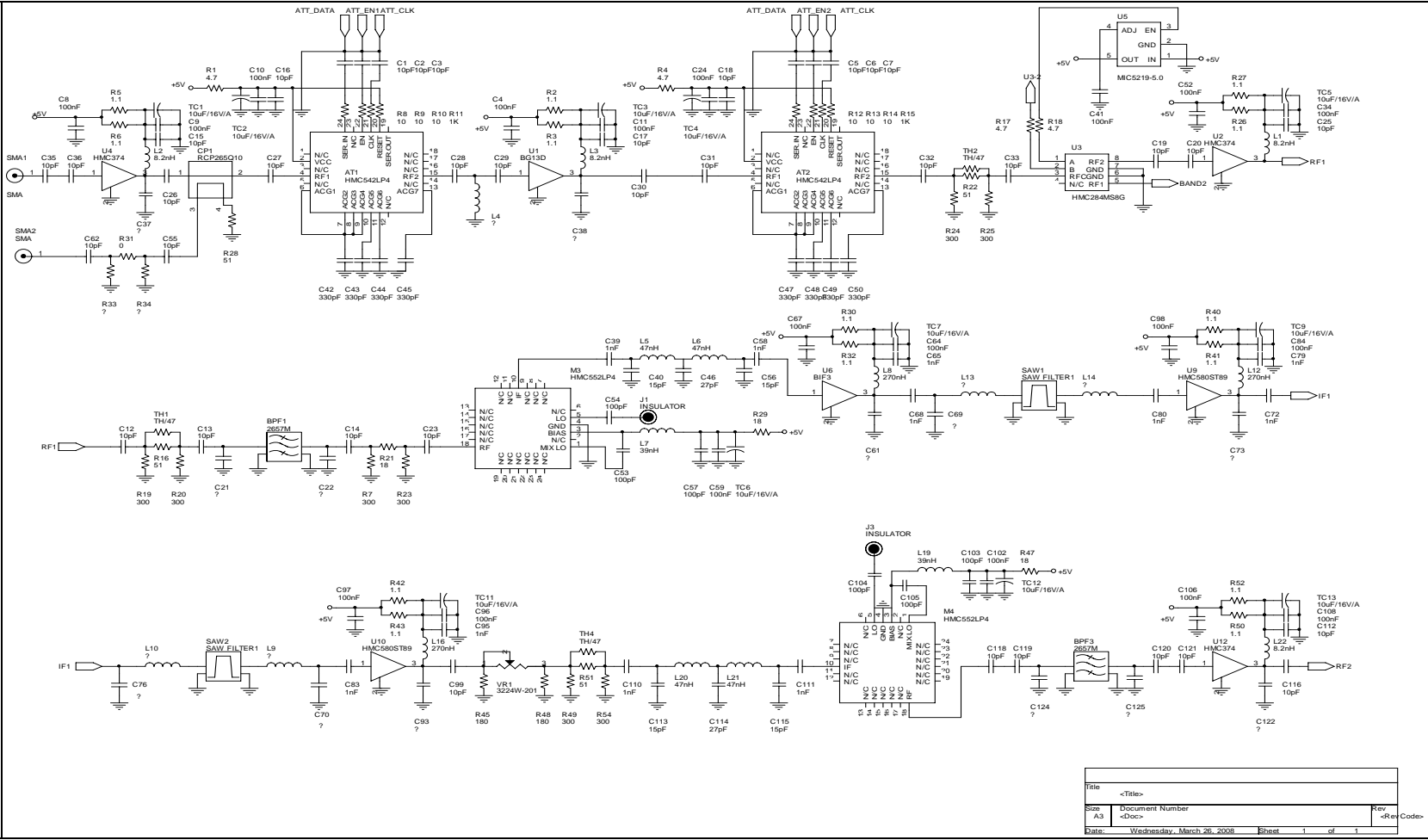
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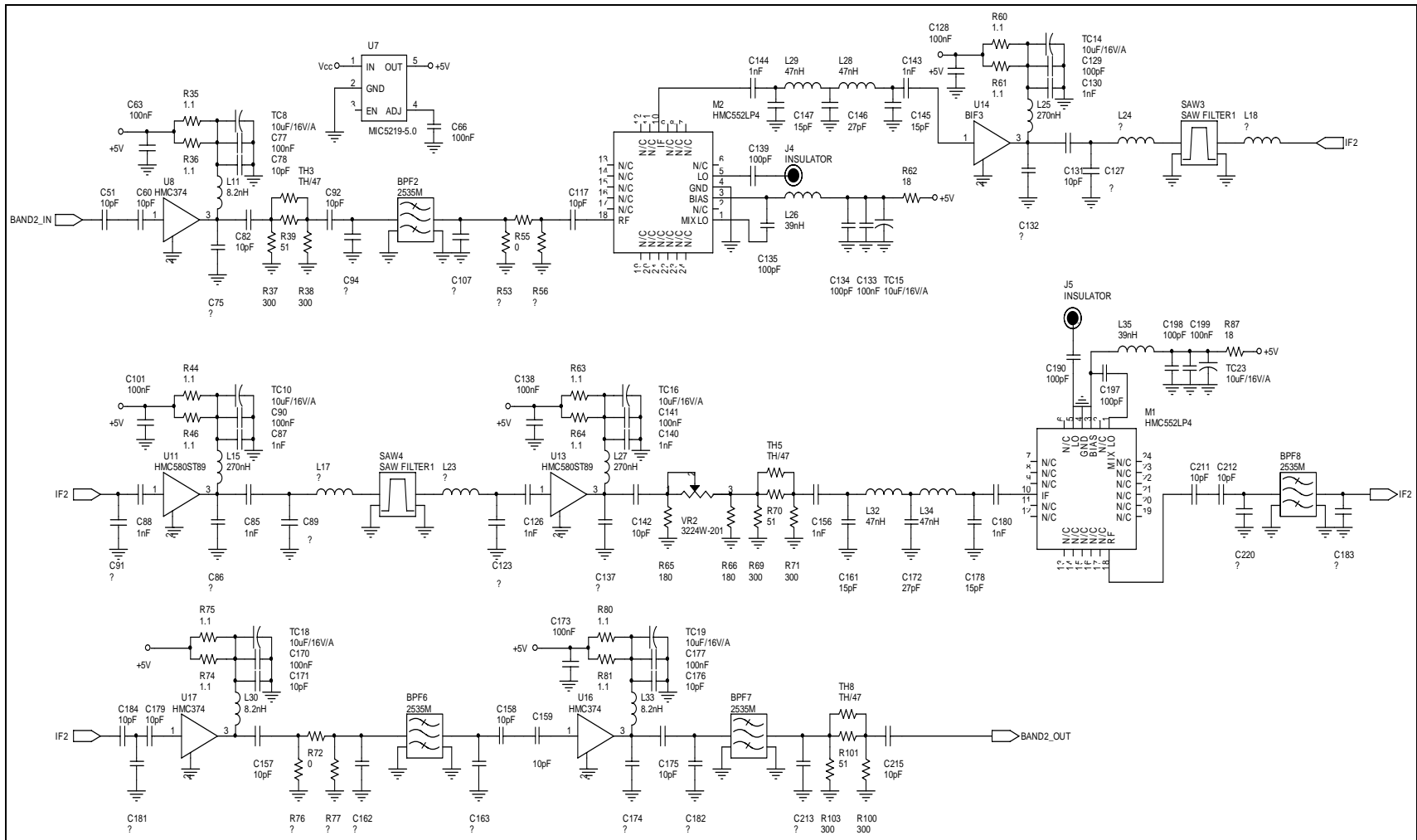
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RF module

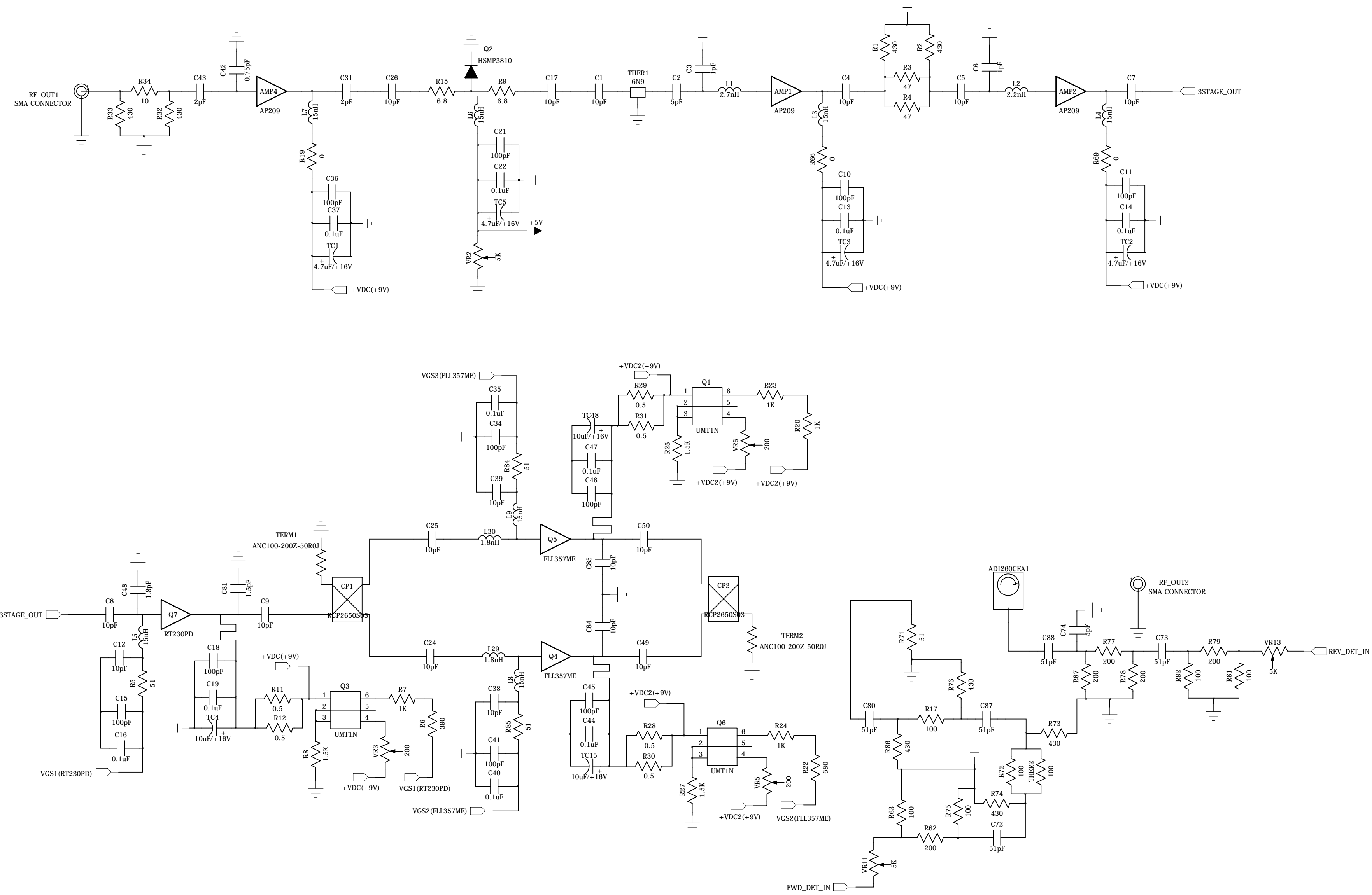


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Date	Wednesday, March 26, 2008	Sheet 1 of 1



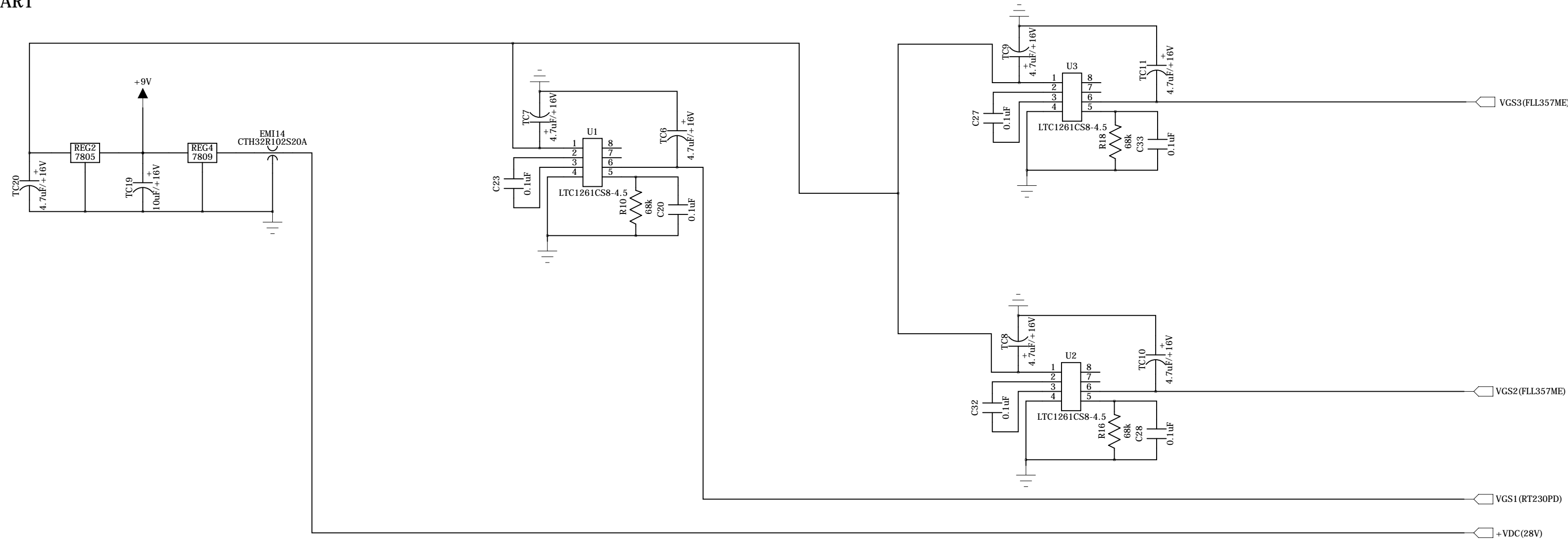
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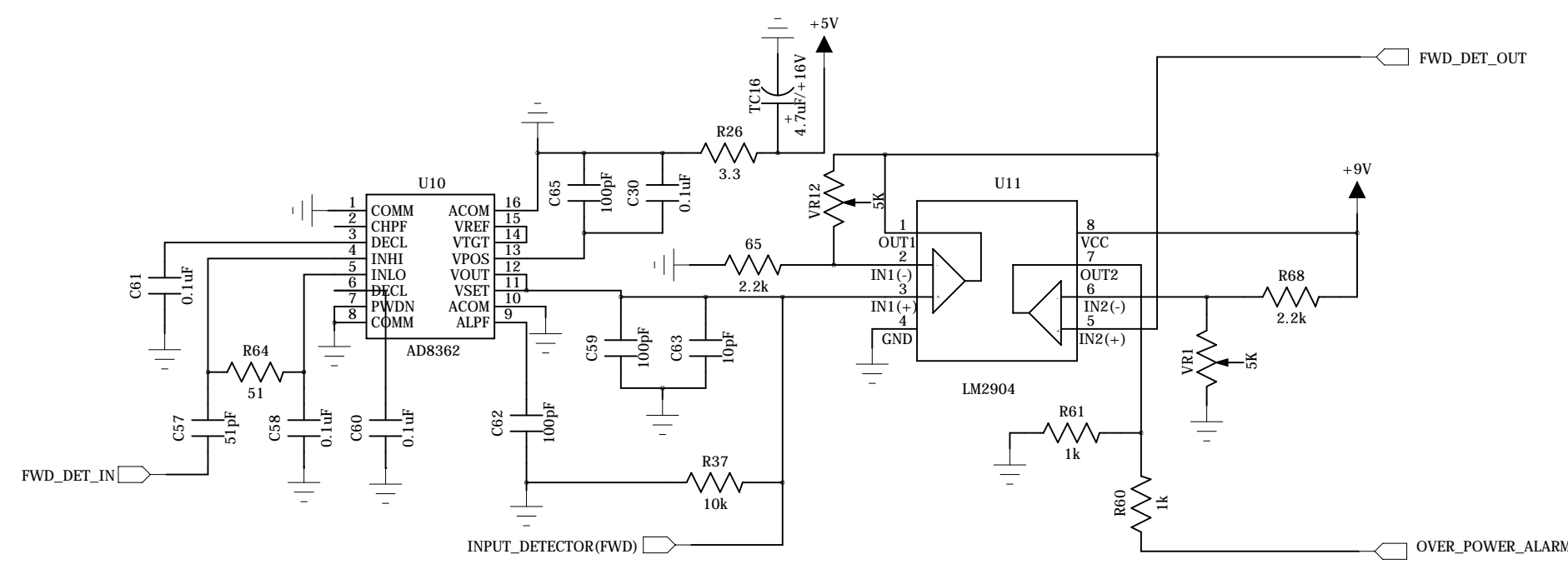


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				DATED: 2008.02.29 SIZE: A1 REVISION: 1.0 SHEET: 1 OF 2

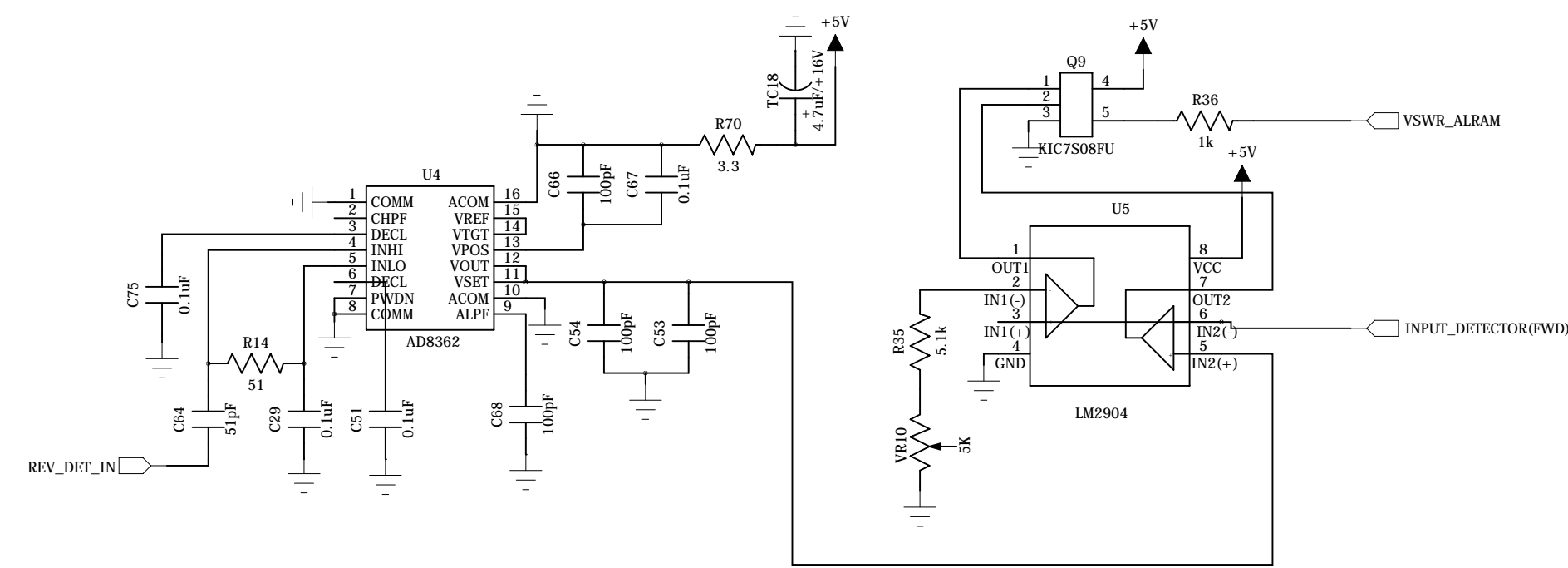
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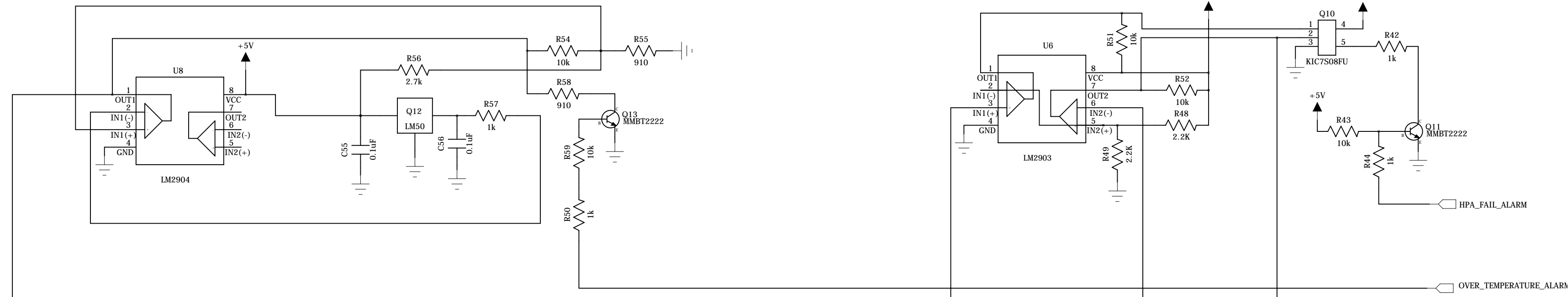
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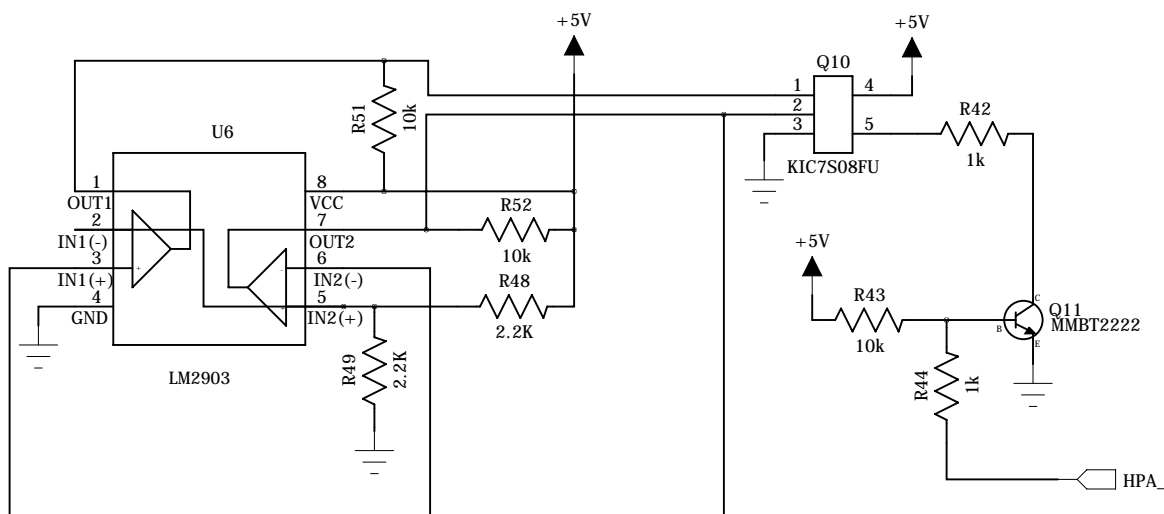
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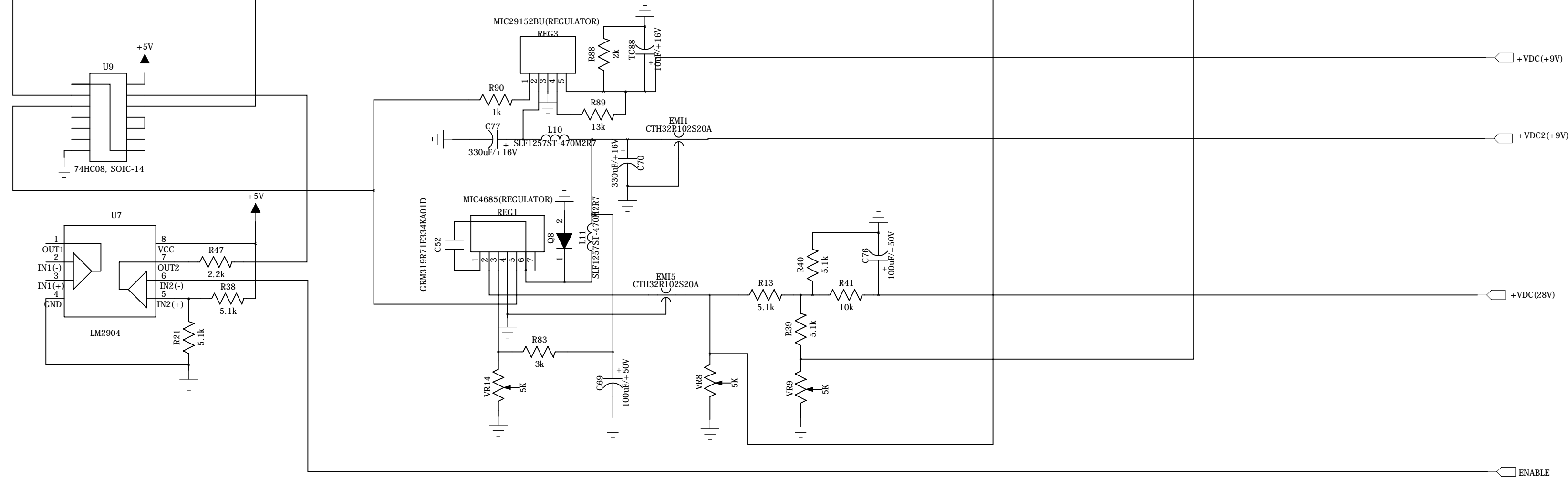
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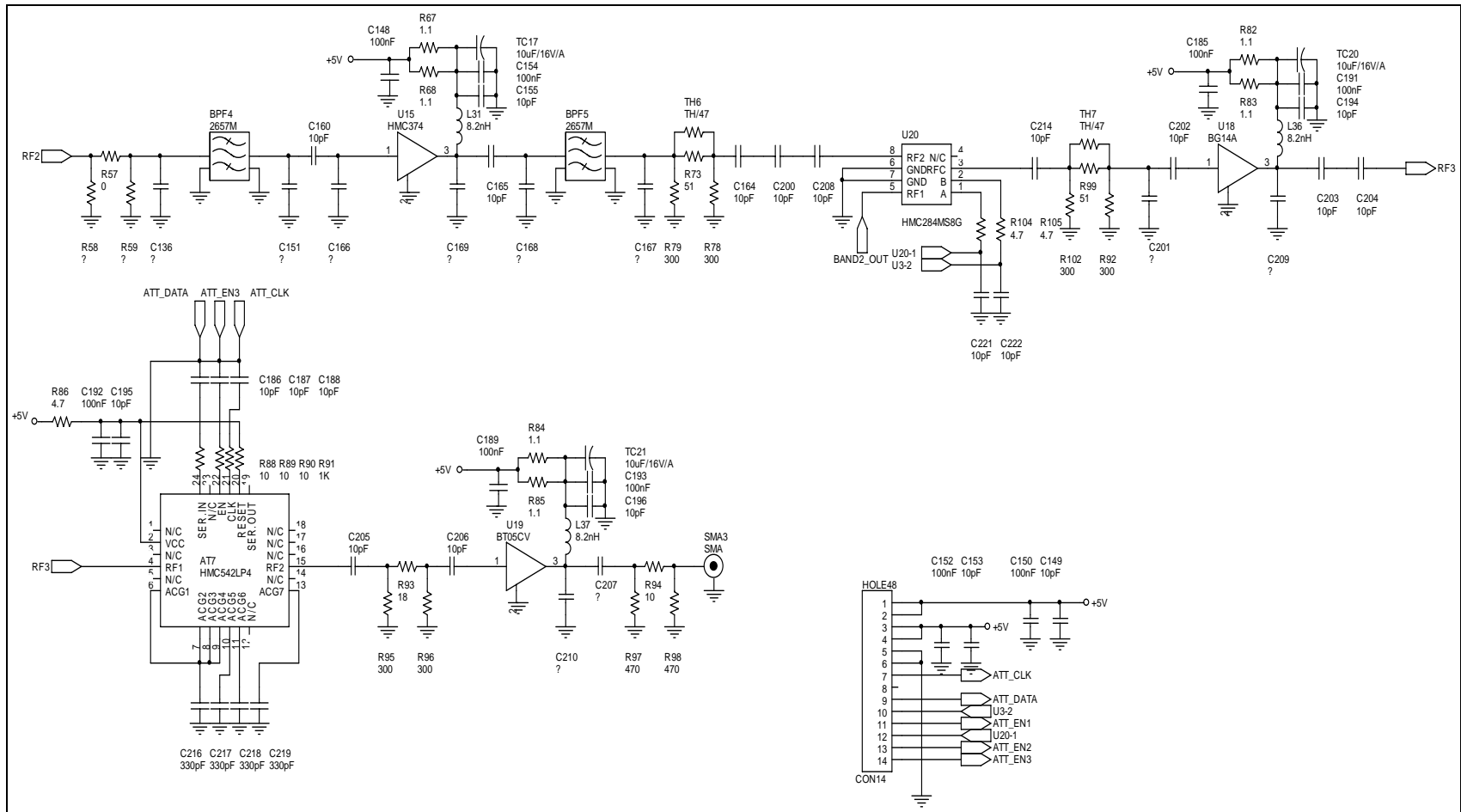
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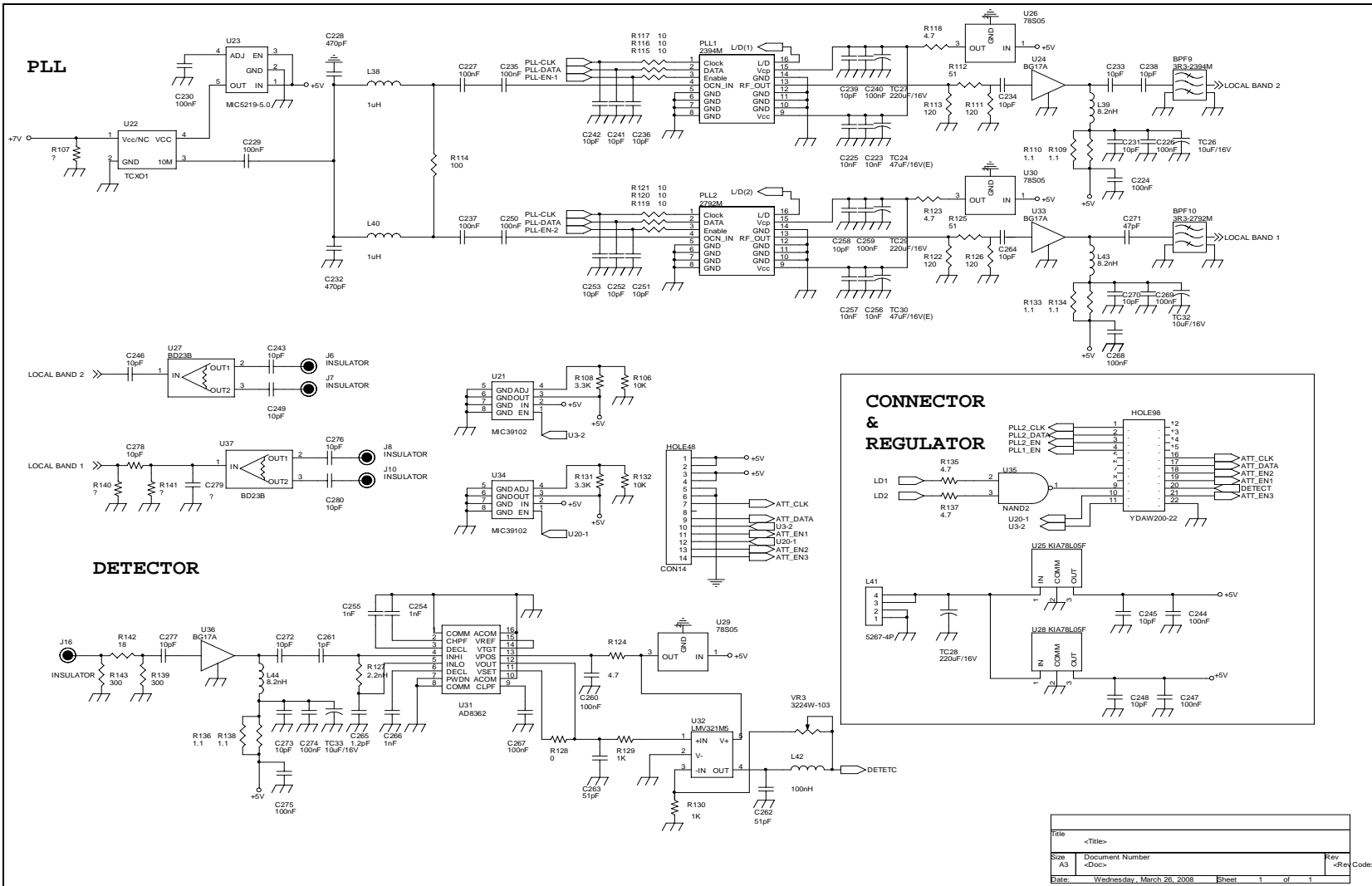


ENABLE PART



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				Designed by: N. I. LEE Drawn By: N. I. LEE CON PART
				DATED: 2007.08.20 SIZE: A1 REVISION: 1.0 SHEET: 2 OF 2





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