ZR36474BGCF

COACH-9e

Camera-On-A-Chip

Digital Camera Processor

Preliminary
Data Book

Proprietary and Confidential

Version 0.14

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COACH-9e Data Sheet v.0.14

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CHAPTER 1 INTRODUCTION

1.1 ABOUT THIS DOCUMENT

This document provides a detailed description of the COACH-9e Digital Still Camera (DSC) processor arranged to guide the system designer through the design process. By referring to this document, the designer will gain a thorough understanding of the chip and wil be able to develop a camera with a wide range of features. Each interface is explained along with specific connection information for every pin. Electrical specifications and recommendations are provided to ease the implementation of the COACH-9e in a system design. And finally, mechanical specifications provide layout information.

1.2 TERMINOLOGY

A pound sign (#) after a signal name refers to an active low signal, indicating a signal is in the asserted state when driven to a low level. For example, when Reset# is low, a reset condition occurs. PU refers to a pull-up resistor, and PD refers to a pull-down resistor. NC is an abbreviation for no connect. Bus signals are grouped in brackets and the sequence is defined with a colon such as DVDAT[7:0].

Terms appearing throughout this document are defined as follows:

- **COACH** ? 擧amera-On-A-Chip?device (includes hardware and firmware)
- **COACHWARE** ? COACH firmware library provided by Zoran that runs on the COACH embedded CPU processor and implements camera functionality.
- **HCE** (Host COACH Embedded) ? Embedded host functionality in the COACH that resides in the customer担software layer. HCE interfaces COACHWARE via dedicated API commands.
- **COACHWARE API** ? API layer through which the host or HCE communicates with COACHWARE.

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CHAPTER 2 FUNCTIONAL OVERVIEW

The COACH-9e is a low system cost, highly integrated device. The following list illustrates the features of the COACH-9e.

2.1 SYSTEM FEATURES

- A 32-bit MIPS 4kem CPU allows easy development and porting of SW applications.
- Up to 8Mega pixels (MPx) image capture resolution.
- Click-to-Click timing of less than 250 mSec with 4MPx resolution.
- High quality 16x to 1/16x scaler.
- Embedded CD quality audio codec.
- Micro controller functionality integration includes:-

  ? input (3 external) 12-bit successive approximation register (SAR) ADC with a sample rate of 100 Ks/sec.
  岩 mbedded Real time clock (RTC).
  昉 attern generator for motor control support with 16 pulse width modulated (PWM) outputs.
  ? general purpose pulse width modulated (PWM) outputs.
  盼 W download support from USB, NAND, NOR, SD and MMC.
  盼 pecial power control (PWRC) block for cost-effective camera power supply design with direct connection to a 1.5-3.6V battery. Control mechanisms for power ON/OFF and low battery detect.
  盼 upport for flash light control including red-eye reduction.

2.2 DISPLAY FEATURES

- 64 color on screen display (OSD) with 4 transparency levels.
- 4 display highlight rectangles.
- Quantization Noise reduction filter for 6-bit DLCDs.
- Embedded TV encoder for direct output to TV monitor (CVBS format). No need for off-chip NTSC/PAL encoder or video DAC.

2.3 VIDEO PROCESSING FEATURES:

- Advanced 10-bit CCD signal processing unit that performs:

昀 dvanced Anti Lens Shading filtering (Patent pending)
昊 hite Balance Correction
昉 rogrammable Gamma look up table (LUT)
旰 ayer Grid Color Filter Array (CFA) reconstruction
昀 utomatic real time peak noise and defective pixel correction (Patent pending)
昆 CD noise suppression:
- CFA grid noise reduction
- Black noise compensation
- Color aliasing suppression, including special filter for video modes.
- Blemish column noise correction
- Advanced random noise suppression

昆 olor matching and advanced color space conversion
昄 uminance Correction
昀 utomatic Focusing (AF)
昀 utomatic White Balance (AWB)
昀 utomatic Exposure (AE)
昅 ore Zoran patent-pending technology is employed

- Image enhancement and manipulation effects for better viewing and printing.
- Black frame noise reduction for enhanced long exposure image quality.
- 27 MPx/sec high speed JPEG compression/decompression engine.
- Smooth, high quality 16x to 1/16x scaler. Allows zero overhead smooth up to 16x digital zoom in:

昉 review
昤 till/Clip Capture
昉 C Video
旧 eal time L/R, U/D image flip

2.4 AUDIO PROCESSING FEATURES:

- Embedded CD quality audio codec supporting 32, 44.1, and 48 KHz sampling rates and up to 84dB SNR.
- Auto Level Control (ALC).
- Stereo audio playback output to headphones.
- Microphone, line out and speaker amplifiers provide a glueless interface external audio I/O devices.

2.5 INTERFACE FEATURES:

- Digital video output to interface AU, Casio, Epson, Sanyo, Sony and Toppoly LCDs including an on-chip programmable controller.
- Sensor support:

  喜 nterface to industry standard CCD sensor arrays from Sony, Sharp, and Panasonic (progressive and

interlaced) and popular CMOS sensors.
昅 ulti-field modern CCD sensor types.
昇 ew "VGA" mode for Panasonic, Sony, and Sharp sensors.
昅 lueless interface to an external TG and 10-bit CCD analog front end (CDS-AFE).

- Direct interface to resident flash memory (NAND or NOR type) and/or removable memory cards such as Secure Digital (SD) and MultimediaCard (MMC) .
- Supports single 16-bit data width DDR -SDRAM of 128Mbit and 256Mbit.
- General Interface Ports:

  昨 ^{2}C (Zoran serial bus)
  昀 ynchronous Serial Port (SP)
  昨 S-232 Serial Communication Port
  昔 JTAG port for debugging probe
  昀 SB 2.0 High-Speed interface.

- Over 100 general purpose I/O (GPIO). Some GPIO signals are multiplexed with unused pins. Many GPIO pins can also be used as interrupt pins.

2.6 FIRMWARE (COACHWARE) FEATURES:

- Embedded host control (**HCE**) software architecture allows the creation of DSC applications with minimum effort.
- Reusable COACH software API set (**COACHWARE API)**. Backward compatibility with previous generations.
- Open firmware architecture allows easy modification to implement customer software modules.
- Advanced bit rate control (BRC) guarantees the size of the Video compressed clips at maximum visual quality.
- All standard camera operating modes including live preview, still image capture, MJPEG video capture, image and video playback, thumbnails playback, menu mode, and others.
- DCF image and audio file format, with FlashPix? ready compliance. Full performance and easily customized DCF library.
- Fully customizable EXIF 2.2 library.
- Fully customizable DPOF 1.1 support.
- Image Editing.
- Image playback allows up to 16x digital zoom, accelerated playback and image rotation.
- Advanced GUI support including:

  脊 UV 4:2:2 and 6-bit OSD color spaces
  昨 esizable, multi-color fonts

盼 hapes and image drawing including circles, rectangles, bitmaps, JPEGs and others
盻 irtual mode, for automatic fitting of the customer graphics to actual display size, thus significantly decreasing the effort of the GUI developer.
眄 icture-in-Picture support for creating multiple image layers in image playback and live preview. For example, implements panoramic support mode.

- Audio support:

  昅 ultiple formats support including MP3, MPEG-1 layer 2, ADPCM, uLaw and others
  盱 ptional audio annotation of pictures
  眄 layback and recording of sound in AVI clips
  盼 ound effects such as shutter effects
  旸 ictaphone feature

- Support for a variety of USB interface protocols including:

  眄 C Video Capture mode for capturing real time video (MJPEG compressed) to PC.
  昊 IA, Twain, and Twain 2 protocols for direct retrieval of images and live video.
  旰 ulk-Only mass storage to recognize a camera as a PC drive. No drivers required for most operating systems.
  眄 icture Transfer Protocol (PTP)
  眄 ictbridge for direct printing to all printers supporting the Pictbridge interface.

2.7 SOFTWARE FEATURES:

- Extensive set of PC tools and drivers.

2.8 TECHNOLOGY:

- COACH-9e is available in a 293-pin RoHS compliant BGA package.
- Required power supply voltages:

  ? .3V peripheral I/O
  ? .5V DDR SDRAM I/O
  ? .8V Core
  ? .5V-3.6V battery

CHAPTER 3 PIN LIST

3.1 PIN DIAGRAM ? 293 BGA

Figure 3-1 is the pin diagram of the COACH-9e.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	
19	DV DAT5	DV DAT7	DVCLK	DV CNTL1	DV CNTL8	NC	VID2	VID8	FLSH TRIG	CCLK	M4C / GSI2	M4A / GSI0	M3C	M2A	TG VAL	AFEVAL	RAM ADD4	RAM ADD5	RAM ADD2	19
18	DV DAT2	DV DAT4	DV DAT3	DV CNTL7	NC	VID0	VID3	SUB CNTL	VID7	CCLK OUT	FPDIN	SCL	M3D	M2B	M1C	SPCLK	RAM ADD3	RAM ADD6	RAM ADD1	18
17	HPR	HPL	DV DAT0					DV CNTL9	VID1	VID6	VDD CORE	M4D / GSI3				XL GPIO1	SP DATA	RAM ADD7	RAM ADD0	17
16	SPKRP	GND SPKR	DV DAT1														GND	RAM ADD8	RAM ADD10	16
15	SPKRN	VDD SPKR	LINE OUT		DV DAT6	DV CNTL3	DV CNTL5	VDDP	VIS	SDA	VDDP	M2C	M1B	VDDP	VDD RAM		GND	RAM ADD9	RAM BA1	15
14	MICN	GND AUD	VDD AUD		AREF	DV CNTL0	DV CNTL4	VDD CORE	VID4	HIS	M4B / GSI1	M3A	M1D	XL GPIO2	VDD RAM		XL GPIO0	RAM ADD11	RAM BA0	14
13	MICP	GND PWR	MIC ENB		VCM	RESET #	DV CNTL2	DV CNTL6	VID5	VID9	EXP CNTL	M3B	M2D	GND	VDD CORE		GND	RAM ADD12	RAM CS#	13
12	RTCXI	RTCXO	VDD PWR		PDE TECT	PWR ON0	PWR ON2	GND	GND	GND	GND	M1A	XL GPIO4	GND	GND		GND	RAM CKEN	RAM RAS#	12
11	USBDN	VDD USB			PWR ON1	VDD RTC	NC	GND	GND	GND	GND	GND	GND	GND	VDD RAM			RAM CLK	RAM CAS#	11
10	USBDP	GND USB			RSET	USB VBUS	CVBS	PWR ENB	GND	GND	GND	GND	GND	GND	RAM VREF			RAM WE#	RAM CLK#	10
9	VCLKO	USB RSET			VDD ADC	GP ADC0	GND ADC	GND	GND	GND	GND	GND	GND	GND	VDD CORE			RAM LDM	RAM UDM	9
8	VCLKI	VDD USBPLL	GND DAC		GP ADC4	NC	GND	GND	GND	GND	GND	EJTDI	EJTCK	GND	VDD RAM		GND	RAM UDQS	RAM LDQS	8
7	GND USBPLL	VDD PLL	VDD DAC		PWM5	PWM6 / GSI4	FA12	FA13	FA21	FD5	FD7	FGPIO 26	EJTMS	GND	VDD RAM		GND	RAM DAT8	RAM DAT7	7
6	NC	GND PLL	GP ADC1		VDD CORE	PWM2	FA11	FA18	FA23	FD6	FGPIO 1	FGPIO 28	FCD1#	GND	VDD RAM		GND	RAM DAT9	RAM DAT6	6
5	AUD GPIO1	AUD GPIO0	AUD GPIO2		PWM4	VDDP	FA14	VDDP	FRES BSY#	VDDP	FGPIO 29	VDDP	EJTDO	GND	VDD RAM		GND	RAM DAT10	RAM DAT5	5
4	PWM3	PWM7 / GSI5	AUD GPIO3														GND	RAM DAT11	RAM DAT4	4
3	PWM1	PWM0	AUD GPIO4					FA15	VDD CORE	FA20	FRES CE#	FGPIO 30				VDD CORE	GND	RAM DAT12	RAM DAT3	3
2	FA3	FA2	FA0	FGPIO 31	FA1	FA7	FA8	FA22	FWR#	FD0	FD2	FEXT BSY#	FCLK	GND	FGPIO 27	TXD	RAM DAT15	RAM DAT13	RAM DAT2	2
1	FA4	FA5	FA6	FA9	FA10	FA16	FA17	FA19	FOE#	FD4	FD1	FD3	FGPIO 25	GND	GND	RXD	RAM DAT0	RAM DAT14	RAM DAT1	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	

Figure 3-1: *Pin Diagram ? 293 BGA, COACH-9e*

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3.2 PIN LISTING BY PIN NUMBER

Table 3-1 contains a listing of the pins in pin-number order.

Table 3-1: Pin List

No.	Pin
A1	FA4
A2	FA3
A3	PWM1
A4	PWM3
A5	AUDGPIO1
A6	NC
A7	GNDUSBPLL
A8	VCLKI
A9	VCLKO
A10	USBDP
A11	USBDN
A12	RTCXI
A13	MICP
A14	MICN
A15	SPKRN
A16	SPKRP
A17	HPR
A18	DVDAT2
A19	DVDAT5
B1	FA5
B2	FA2
B3	PWM0

No.	Pin
B4	PWM7 / GSI5
B5	AUDGPIO0
B6	GNDPLL
B7	VDDPLL
B8	VDDUSBPLL
B9	USBRSET
B10	GNDUSB
B11	VDDUSB
B12	RTCXO
B13	GNDPWR
B14	GNDAUD
B15	VDDSPKR
B16	GNDSPKR
B17	HPL
B18	DVDAT4
B19	DVDAT7
C1	FA6
C2	FA0
C3	AUDGPIO4
C4	AUDGPIO3
C5	AUDGPIO2
C6	GPADC1

No.	Pin
C7	VDDDAC
C8	GNDDAC
C12	VDDPWR
C13	MICENB
C14	VDDAUD
C15	LINEOUT
C16	DVDAT1
C17	DVDAT0
C18	DVDAT3
C19	DVCLK
D1	FA9
D2	FGPIO31
D18	DVCNTL7
D19	DVCNTL1
E1	FA10
E2	FA1
E5	PWM4
E6	VDDCORE
E7	PWM5
E8	GPADC4
E9	VDDADC
E10	RSET
E11	PWRON1

No.	Pin
E12	PDETECT
E13	VCM
E14	AREF
E15	DVDAT6
E18	NC
E19	DVCNTL8
F1	FA16
F2	FA7
F5	VDDP
F6	PWM2
F7	PWM6 / GSI4
F8	NC
F9	GPADC0
F10	USBVBUS
F11	VDDRTC
F12	PWRON0
F13	RESET#
F14	DVCNTL0
F15	DVCNTL3
F18	VID0
F19	NC
G1	FA17
G2	FA8

No.	Pin
G5	FA14
G6	FA11
G7	FA12
G8	GND
G9	GNDADC
G10	CVBS
G11	NC
G12	PWRON2
G13	DVCNTL2
G14	DVCNTL4
G15	DVCNTL5
G18	VID3
G19	VID2
H1	FA19
H2	FA22
H3	FA15
H5	VDDP
H6	FA18
H7	FA13
H8	GND
H9	GND
H10	PWRENB
H11	GND
H12	GND
H13	DVCNTL6
H14	VDDCORE

No.	Pin
H15	VDDP
H17	DVCNTL9
H18	SUBCNTL
H19	VID8
J1	FOE#
J2	FWR#
J3	VDDCORE
J5	FRESBSY#
J6	FA23
J7	FA21
J8	GND
J9	GND
J10	GND
J11	GND
J12	GND
J13	VID5
J14	VID4
J15	VIS
J17	VID1
J18	VID7
J19	FLSHTRIG
K1	FD4
K2	FD0
K3	FA20
K5	VDDP
K6	FD6

No.	Pin
K7	FD5
K8	GND
K9	GND
K10	GND
K11	GND
K12	GND
K13	VID9
K14	HIS
K15	SDA
K17	VID6
K18	CCLKOUT
K19	CCLK
L1	FD1
L2	FD2
L3	FRESCE#
L5	FGPIO29
L6	FGPIO1
L7	FD7
L8	GND
L9	GND
L10	GND
L11	GND
L12	GND
L13	EXPCNTL
L14	M4B / GSI1
L15	VDDP

No.	Pin
L17	VDDCORE
L18	FPDIN
L19	M4C / GSI2
M1	FD3
M2	FEXTBSY#
M3	FGPIO30
M5	VDDP
M6	FGPIO28
M7	FGPIO26
M8	EJTDI
M9	GND
M10	GND
M11	GND
M12	M1A
M13	M3B
M14	M3A
M15	M2C
M17	M4D / GSI3
M18	SCL
M19	M4A / GSI0
N1	FGPIO25
N2	FCLK
N5	EJTDO
N6	FCD1#
N7	EJTMS
N8	EJTCK

No.	Pin
N9	GND
N10	GND
N11	GND
N12	XLGPIO4
N13	M2D
N14	M1D
N15	M1B
N18	M3D
N19	M3C
P1	GND
P2	GND
P5	GND
P6	GND
P7	GND
P8	GND
P9	GND
P10	GND
P11	GND
P12	GND
P13	GND
P14	XLGPIO2
P15	VDDP
P18	M2B
P19	M2A
R1	GND
R2	FGPIO27

No.	Pin
R5	VDDRAM
R6	VDDRAM
R7	VDDRAM
R8	VDDRAM
R9	VDDCORE
R10	RAMVREF
R11	VDDRAM
R12	GND
R13	VDDCORE
R14	VDDRAM
R15	VDDRAM
R18	M1C
R19	TGVAL
T1	RXD
T2	TXD
T3	VDDCORE
T17	XLGPIO1
T18	SPCLK
T19	AFEVAL
U1	RAMDAT0
U2	RAMDAT15
U3	GND
U4	GND
U5	GND
U6	GND
U7	GND

No.	Pin
U8	GND
U12	GND
U13	GND
U14	XLGPIO0
U15	GND
U16	GND
U17	SPDAT
U18	RAMADD3
U19	RAMADD4
V1	RAMDAT14
V2	RAMDAT13
V3	RAMDAT12
V4	RAMDAT11
V5	RAMDAT10
V6	RAMDAT9
V7	RAMDAT8
V8	RAMUDQS
V9	RAMLDM
V10	RAMWE#
V11	RAMCLK
V12	RAMCKEN
V13	RAMADD12
V14	RAMADD11
V15	RAMADD9
V16	RAMADD8
V17	RAMADD7

No.	Pin
V18	RAMADD6
V19	RAMADD5
W1	RAMDAT1
W2	RAMDAT2
W3	RAMDAT3
W4	RAMDAT4
W5	RAMDAT5
W6	RAMDAT6
W7	RAMDAT7
W8	RAMLDQS
W9	RAMUDM
W10	RAMCLK#
W11	RAMCAS#
W12	RAMRAS#
W13	RAMCS#
W14	RAMBA0
W15	RAMBA1
W16	RAMADD10
W17	RAMADD0
W18	RAMADD1
W19	RAMADD2

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CHAPTER 4 PIN DESCRIPTIONS

4.1 PIN FUNCTIONS

The following tables are grouped by function and describe each COACH pin. Some pins have dual functionality and can be configured as a dedicated signal or as a General Purpose I/O (GPIO). These pins are designated with a slash (/) between the respective names, such as SPDAT / CCDGPIO0?

The 摘irection?column shows which direction or combination of directions each pin is capable of supporting. The 捏O Buffer?column indicates the pin buffer type as shown in Table 4-1.

When configured as GPIO, many of the pins have interrupt capability. COACH-9e supports edge-triggered interrupts only. Each interrupt can be triggered by a rising edge, falling edge, or both edges

The initialization states of the PU/PD resistors are shown in Table 4-24 on page 4-18.

Table 4-1: Legend of I/O Buffer Types

I/O Buffer	Description
IO_XTL	Crystal Driver with High Enable
IOm	PAD3V_S ? 3.3V-tolerant tri-state Input/Output pad with a Schmitt trigger input and a medium drive strength output
IOs	PAD3V_S ? 3.3V-tolerant tri-state Input/Output pad with a Schmitt trigger input and a strong drive strength output
IOUm	PAD3V_S ? 3.3V-tolerant tri-state Input/Output pad with a Schmitt trigger input and a medium drive strength output Switchable PU resistor available
IOUs	PAD3V_S ? 3.3V-tolerant tri-state Input/Output pad with a Schmitt trigger input and a strong drive strength output Switchable PU resistor available
IODm	PAD3V_S ? 3.3V-tolerant tri-state Input/Output pad with a Schmitt trigger input and a medium drive strength output Switchable PU resistor available
IODs	PAD3V_S ? 3.3V-tolerant tri-state Input/Output pad with a Schmitt trigger input and a strong drive strength output Switchable PD resistor available
IOUD	PAD3V_S - 3.3v tolerant Tri-state input/output pad, with a Schmitt trigger, strong drive. PU or PD resistor can be enabled according to the SW configuration
SSTL21X	SSTL IO Driver for DDR-DRAM

Table 4-1: Legend of I/O Buffer Types *(continued)*

I/O Buffer	Description
USB	USB Transceiver Buffer
O_ANLG	Analog Output Pin
I_ANLG	Analog Input Pin
PWR	Power/Ground Pin

4.1.1 DDR INTERFACE

Table 4-2: DDR Interface (50 Pins)

Pin Name	Direction	I/O Buffer	Description
RAMDAT[15:0]	I/O	SSTL21X	Bi-directional data bus
RAMADD[12:0]	O	SSTL21X	Address Bus
RAMBA[1:0]	O	SSTL21X	Bank select
RAMRAS#	O	SSTL21X	Row Select (Active Low)
RAMCAS#	O	SSTL21X	Column Select (Active Low)
RAMCLK	O	SSTL21X	Clock Output ? RAMCLK and RAMCLK# are differential clocks
RAMCLK#	O	SSTL21X	Clock Output ? RAMCLK and RAMCLK# are differential clocks
RAMVREF	I	PWR1.25V	Comparators Reference Voltage ? Half of VDDRAM (~1.25V)
RAMLDM	O	SSTL21X	Low Byte Data Mask
RAMUDM	O	SSTL21X	Upper Byte Data Mask
RAMCS#	O	SSTL21X	Chip Select (Active Low)
RAMWE#	O	SSTL21X	Write Enable (Active Low)
RAMLDQS	I/O	SSTL21X	Data Strobe Lower Byte
RAMUDQS	I/O	SSTL21X	Data Strobe Upper Byte
RAMCKEN	O	SSTL21X	Clock Enable ? De-asserted for dynamic power saving
VDDRAM	PWR	PWR 2.5V	VDD (7 Pins) ? 2.5V

1. There are no internal termination resistors in the SSTL I/O buffer. A correct PCB layout will not require them.

4.1.2 CCD/CMOS SENSOR INTERFACE

Table 4-3: CCD/CMOS Sensor Interface (20 Pins)

Pin Name	Direction	I/O Buffer	Description
SPDAT / CCDGPIO0	I/O	IODm	Serial Port Data Output ? TG and CDS-AFE
SPCLK / CCDGPIO1	I/O	IODm	Serial Port Clock Output ? TG and CDS-AFE
AFEVAL / CCDGPIO2	I/O	IOUm	Serial Port CDS-AFE Strobe Output
TGVAL / CCDGPIO3	I/O	IOUm	Serial Port Timing Generator Strobe Output
VIS / CCDGPIO4	I/O	IODs	Vertical Sync Input/Output of Image Sensor Port
HIS / CCDGPIO5	I/O	IODs	Horizontal Sync Input/Output of Image Sensor Port
VID[9:0]	I	IODs	Input Video Data. Connect MSB to VID9
CCLK	I	IOs	CCD/CMOS Sensor Pixel Clock Can be used as crystal clock oscillator input if internal PLL is not used. Frequency should be pixel clock rate or half and multiplied internally.
CCLKOUT / CCDGPIO12	I/O	IODs	TG Clock ? Twice the Pixel Frequency
SUBCNTL / CCDGPIO13	I/O	IODm	Configurable Control Signal for SUB Pulses
EXPCNTL / CCDGPIO14	I/O	IODm	Configurable Control Signal for Exposure Pulses

Table Notes:

1. There is a gap in the CCDGPIO sequence (CCDGPIO[11:6]).

4.1.3 PHOTOFLASH INTERFACE

FSGPIO1 can be used as an interrupt.

Table 4-4: Photoflash Interface (2 Pins)

Pin Name	Direction	I/O Buffer	Description
FLSHTRIG / FSGPIO0	I/O	IODs	Trigger Pulse for Discharging Flash Strobe Circuit
FPDIN / FSGPIO1	I/O	IODs	Flash Strobe Photo Diode Input Output Signal of Photo Diode Comparator.

4.1.4 LCD DIGITAL VIDEO OUTPUT INTERFACE

Digital video pins can be configured as GPIOs (DVGPIO[18:5]). Note that DVGPO[4:0] act as outputs only as they are used as configuration pins at power-up. DVGPIO[18:16] can be used as interrupts.

Table 4-5: LCD Digital Video Output Interface (19 Pins)

Pin Name	Direction	I/O Buffer	Pin Name	SONY	AU Module	AU Panel	Casio Panel	Epson Panel
DVDAT0 / DVGPO0 / CFG1	O	IOm	DVDAT0	D0	DVDAT0	DVDAT0	DVDAT0	DA0
DVDAT1 / DVGPO1 / CFG2	O	IOm	DVDAT1	D1	DVDAT1	DVDAT1	DVDAT1	DA1
DVDAT2 / DVGPO2 /CFG4	O	IOm	DVDAT2	D2	DVDAT2	DVDAT2	DVDAT2	DA2
DVDAT3 / DVGPO3 / CFG7	O	IOm	DVDAT3	D3	DVDAT3	DVDAT3	DVDAT3	DA3
DVDAT4 / DVGPO4 / CFG0	O	IOm	DVDAT4	D4	DVDAT4	DVDAT4	DVDAT4	DA4
DVDAT[7:5] / DVGPIO[7:5]	I/O	IODm	DVDAT5	D5	DVDAT5	DVDAT5	DVDAT5	DA5
	I/O	IODm	DVDAT6	D6	DVDAT6	DVDAT6	GPCK	DYIO2
	I/O	IODm	DVDAT7	D7	DVDAT7	DVDAT7	CP	FRYS
DVCLK / DVGPIO8	I/O	IODm	DVCLK	CK	DVCLK	DVCLK	CLK	XSCL

Table 4-5: LCD Digital Video Output Interface (19 Pins) ***(continued)***

Pin Name	Direction	I/O Buffer	Pin Name	SONY	AU Module	AU Panel	Casio Panel	Epson Panel
DVCNTL[7:0] / DVGPIO[16:9]	I/O	IODm	DVCNTL0		DVALID	DVALID		YSCL
	I/O	IODm	DVCNTL1	VSYNC	DVVS	DVVS	VSYNC	YSCLD
	I/O	IODm	DVCNTL2	HSYNC	DVHS	DVHS	HSYNC	EIO1
	I/O	IODm	DVCNTL3					RES
	I/O	IODm	DVCNTL4					LP
	I/O	IODm	DVCNTL5	SEN				SHL
	I/O	IODm	DVCNTL6					FRYP
	I/O	IODm	DVCNTL7					GCP
DVCNTL[9:8] / DVGPIO[18:17]	I/O	IODm	DVCNTL8					DYIO1
	I/O	IODm	DVCNTL9					EIO2

4.1.5 TV MONITOR INTERFACE

Table 4-6: TV Monitor Interface (4 Pins)

Pin Name	Direction	I/O Buffer	Description
CVBS	O	O_ANLG	Composite Video Output ? Designed to drive a 37.5Ω equivalent load
RSET	I	I_ANLG	Reference load resistor for Video DAC Add a 392Ω +/-1% resistor between this pin and GNDDAC
VDDDAC	PWR 3.3v	PWR	video DAC vdd ? 3.3v
GNDDAC	PWR	PWR	video DAC ground

4.1.6 AUDIO PORT INTERFACE

Table 4-7: Audio Port Interface (19 Pins)

Pin Name	Direction	I/O Buffer	Description
AUDGPIO0	I/O	IODm	General Purpose I/O
AUDGPIO1	I/O	IODm	General Purpose I/O
AUDGPIO2	I/O	IODm	General Purpose I/O

Table 4-7: Audio Port Interface (19 Pins) ***(continued)***

Pin Name	Direction	I/O Buffer	Description
AUDGPIO3	I/O	IODm	General Purpose I/O
AUDGPIO4	I/O	IODm	General Purpose I/O
GNDAUD	PWR	PWR	Audio Ground
MICP	I	I_ANLG	Connected to the microphone positive terminal via coupling capacitor (differential)
MICN	I	I_ANLG	Connected to the microphone negative terminal via coupling capacitor (differential)
MICENB	O	O_ANLG	Enable Signal Microphone
VDDAUD	PWR 3.3V	PWR	Audio VDD ? 3.3V
GNDSPKR	PWR	PWR	Speaker Ground
SPKRP	O	0_ANLG	Positive Differential Output Signal for External Speaker
SPKRN	O	0_ANLG	Negative Differential Output Signal for External Speaker
LINEOUT	O	0_ANLG	Analog Output Signal for TV
VDDSPKR	PWR 3.3v	PWR	Speaker vdd ? 3.3v
VCM	O	0_ANLG	Common Mode Voltage Connect a capacitor from this pin to GNDAUD Select a value to minimize noise. Recommended value is 1μF
AREF	I	I_ANLG	Audio Reference Voltage Connect a capacitor from this pin to GNDAUD Select a value to minimize noise. Recommended value is 1μF
HPL	O	0_ANLG	Analog headphones, left side audio output
HPR	O	0_ANLG	Analog headphones, right side audio output

AUDGPIO[4:0] can be used as interrupts

4.1.7 PWM PORT INTERFACE.

Table 4-8: PWM Port Interface (8 Pins)

Pin Name	Direction	I/O Buffer	Description
PWM[3:0] / PWMGPIO[3:0]	I/O	IODm	General Purpose PWM Signal

Table 4-8: PWM Port Interface (8 Pins) ***(continued)***

Pin Name	Direction	I/O Buffer	Description
PWM[5:4] / PWMGPIO[5:4]	I/O	IODm	General Purpose PWM Signal
PWM[7:6] / GSI[5:4] PWMGPIO[7:6]	I/O	IODm	General Purpose PWM Signal

4.1.8 USB PORT INTERFACE

Table 4-9: USB Port Interface (8 Pins)

Pin Name	Direction	I/O Buffer	Description
GNDUSB	PWR	PWR	USB Ground
USBDP	I/O	USB	Positive Lead of Differential USB Signal USB specified PU/PD and series termination resistors are internal to the COACH.
USBDN	I/O	USB	Negative Lead of Differential USB Signal USB specified PU/PD and series termination resistors are internal to the COACH.
VDDUSB	PWR 3.3V	PWR	USB VDD ? 3.3V
GNDUSBPLL	PWR	PWR	USB Ground
VDDUSBPLL	PWR 1.8V	PWR	USB VDDPLL ? 1.8V
USBVBUS	I	I_ANLG	USB Vbus with an internal voltage divider
USBRSET	I	I_ANLG	USB Reference Voltage Connect a 6.19kΩ (1%) resistor between this pin and GND

4.1.9 UART PORT INTERFACE

Table 4-10: UART Port Interface (2 Pins)

Pin Name	Direction	I/O Buffer	Description
TXD / URTGPIO0	I/O	IODm	Logic level transmit data output of the UART
RXD / URTGPIO1	I/O	IODm	Logic level receive data input of the UART

4.1.10 FLASH / ROM MEMORY INTERFACE.

Table 4-11: Flash / ROM Memory Interface (47 Pins)

Pin Name	Direction	I/O Buffer	Description
FRESCE#	O	Os	The FCU supports the following protocols: Resident devices 昇 AND, NOR. External devices 盼 D, MMC.
FGPIO1	I/O	IOUs	
FWR#	I/O	IOUs	
FOE#	O	Os	
FD0	I/O	IODs	
FD1	I/O	IODs	
FD2	I/O	IODs	
FD3	I/O	IODs	
FD4	I/O	IODs	
FD5	I/O	IODs	
FD6	I/O	IODs	
FD7	I/O	IODs	
FA0	O	Os	
FA1	O	Os	
FA2 / FGPIO0	I/O	IODs	
FA3	I/O	IODs	
FA4 / FGPIO2	I/O	IOUs	

Table 4-11: Flash / ROM Memory Interface (47 Pins) ***(continued)***

Pin Name	Direction	I/O Buffer	Description
FA5 / FGPIO3	I/O	IOUs	The FCU supports the following protocols: Resident devices 昇 AND, NOR. External devices 盼 D, MMC.
FA6 / FGPIO4	I/O	IOUs	
FA7 / FGPIO5	I/O	IOUs	
FA8 / FGPIO6	I/O	IODs	
FA9 / FGPIO7	I/O	IODs	
A10 / FGPIO8	I/O	IODs	
FRESBSY#	I	IOUs	
FEXTBSY# / FGPIO9	I/O	IOUs	
FCD1# / FGPIO10	I/O	IOUs	
FCLK / FGPIO11	I/O	IOUs	
FA11 / FGPIO12	I/O	IODs	
FA12 / FGPIO13	I/O	IOUs	
FA13 / FGPIO14 / CFG5	O	Os	
FA14 / FGPIO15 / CFG6	O	Os	
FA15 / FGPIO16 / CFG12	O	Os	

Table 4-11: Flash / ROM Memory Interface (47 Pins) ***(continued)***

Pin Name	Direction	I/O Buffer	Description
FA16 / FGPIO17 / CFG13	O	Os	The FCU supports the following protocols: Resident devices 昇 AND, NOR. External devices 盼 D, MMC.
FA17 / FGPIO18 / CFG14	O	Os	
FA18 / FGPIO19 / CFG15	O	Os	
FA19 / FGPIO20 / CFG16	O	Os	
FA20 / FGPIO21	I/O	IOs	
FA21 / FGPIO22	I/O	IOs	
FA22 / FGPIO23	I/O	IOs	
FA23 / FGPIO24	I/O	IOs	
FGPIO25	I/O	IOUs	
FGPIO26	I/O	IODs	
FGPIO27	I/O	IOUs	
FGPIO28	I/O	IOUs	
FGPIO29	I/O	IOUs	
FGPIO30	I/O	IODs	
FGPIO31	I/O	IOUs	

Table Notes: Eight pins are used as configuration pins (CFG[16:12], CFG[6,5]) during the initialization period. See CFG assignments in the following pin name column. Also, thirty-two pins can be configured to operate as GPIOs. Note that FGPIO[20:13] are used as outputs only. FGPIO[24:21], FGPIO[8:6], and FGPIO0 can be used as interrupts

4.1.11 PIN MODE MAP

Table 4-12: Flash Memory/ROM Interface Pin Map

Pin Name	Initialization State	CFG	Direction	GPIO	NAND	NOR	SD/MMC
FRESCE#	O, H		O		CE#(O)	CE#(O)	1
FGPIO1#	O, H		I/O	FGPIO1	1	1	1
FWR#	I, PU		I/O		WE#(O)	WE#(O)	0
FOE#	O, H		O		RE#(O)	OE#(O)	1
FD0	O, H		I/O		IO0(I/O)	DQ0(I/O)	0
FD1	O, H		I/O		IO1(I/O)	DQ1(I/O)	0
FD2	O, H		I/O		IO2(I/O)	DQ2(I/O)	0
FD3	O, H		I/O		IO3(I/O)	DQ3(I/O)	0
FD4	O, H		I/O		IO4(I/O)	DQ4(I/O)	0
FD5	O, H		I/O		IO5(I/O)	DQ5(I/O)	0
FD6	O, H		I/O		IO6(I/O)	DQ6(I/O)	0
FD7	O, H		I/O		IO7(I/O)	DQ7(I/O)	0
FA0	O, L		O		ALE(O)	A0(O)	0
FA1	O, L		O		CLE(O)	A1(O)	0
FA2	I, PD		I/O	FGPIO0	GPIO-I	A2(O)	GPIO-I
FA3	I, PD		I/O		SE#(O)	A3(O)	0
FA4	I, PU		I/O	FGPIO2	GPIO-I	A4(O)	DAT0(I/O)
FA5	I, PU		I/O	FGPIO3	GPIO-I	A5(O)	DAT2(I/O)
FA6	I, PU		I/O	FGPIO4	GPIO-I	A6(O)	DAT3(I/O)
FA7	I, PU		I/O	FGPIO5	GPIO-I	A7(O)	CMD(I/O)
FA8	I, PD		I/O	FGPIO6	GPIO-I	A8(O)	GPIO-I
FA9	I, PD		I/O	FGPIO7	GPIO-I	A9(O)	GPIO-I
FA10	I, PD		I/O	FGPIO8	GPIO-I	A10(O)	GPIO-I

Table 4-12: Flash Memory/ROM Interface Pin Map *(continued)*

Pin Name	Initialization State	CFG	Direction	GPIO	NAND	NOR	SD/MMC
FRESBSY#	I, PU		I		RY/BY#(I)	RY/BY#(I)	GPIO-I
FEXTBSY#	I, PU		I/O	FGPIO9	GPIO-I	GPIO-I	CD1#(I)
FCD1#	I, PU		I/O	FGPIO10	GPIO-I	GPIO-I	CD2#(I)
FCLK	O, L		I/O	FGPIO11	0	0	0
FA11	I, PD		I/O	FGPIO12	WP#(O)	A11(O)	GPIO-I
FA12			I/O	FGPIO13		A12(O)	DAT1(I/O)
FA13	I, CFG	CFG5	O	FGPIO14		A13(O)	
FA14	I, CFG	CFG6	O	FGPIO15		A14(O)	
FA15	I, xPD	CFG12	O	FGPIO16		A15(O)	
FA16	I, xPD	CFG13	O	FGPIO17		A16(O)	
FA17	I, CFG	CFG14	O	FGPIO18		A17(O)	
FA18	I, CFG	CFG15	O	FGPIO19		A18(O)	
FA19	I, CFG	CFG16	O	FGPIO20		A19(O)	
FA20	I[5]		I/O	FGPIO21	GPIO-I	A20(O)	GPIO-I
FA21	I[5]		I/O	FGPIO22	GPIO-I	A21(O)	GPIO-I
FA22	I[5]		I/O	FGPIO23	GPIO-I	A22(O)	GPIO-I
FA23	I[5]		I/O	FGPIO24	GPIO-I	A23(O)	GPIO-I
FGPIO25	O, H		I/O	FGPIO25	1	1	1
FGPIO26	O, H		I/O	FGPIO26	1	1	1
FGPIO27	O, H		I/O	FGPIO27	1	1	1
FGPIO28	O, H		I/O	FGPIO28	1	1	1
FGPIO29	O, L		I/O	FGPIO29	0	0	CLK(O)
FGPIO30	O, L		I/O	FGPIO30	0	0	0
FGPIO31	I, PU		I/O	FGPIO31	GPIO-I	GPIO-I	

Table 4-12: Flash Memory/ROM Interface Pin Map *(continued)*

Pin Name	Initialization State	CFG	Direction	GPIO	NAND	NOR	SD/MMC
Any other GPIO not specified above	O, L						

4.1.12 PIN MODE MAP

1. The 揑nitialization State?column indicates the state of each pin immediately after power up, before the COACH starts booting the firmware. See Table 4-24 for a description of the initialization states.
2. Cells with ? ?or ? ?indicate the output value of the pin during boot for the specific boot media. If the initialization state is (O,H) or (O,L), the system designer must ensure there are no contentions during boot. If the 揚IO?column declares the pin as 揋PIOx?and this pin is not required for accessing media, the pin can be used as GPIO after boot up. The notation ? ?means high and ? ?means low.
3. FA[23:20] are set to inputs during initialization. Since these pins have no PU/PD resistors enabled, the user should put PD resistors in case NOR is not used. This is to ensure these pins are not floating.
4. Cells marked with GPIO-I?mean the pins are inputs during boot and can be configured as GPIO afterwards.
5. xPU or xPD means an external pull-up or pull-down resistor should be used. Pull-up resistors must be used on SD DAT and CMD pins.
6. A signal name with the I/O direction in parentheses indicates the direction of this signal from the COACH point of view.
7. The pins will remain in the initialization state if not used to operate boot media and not set to ? ?or ? ?during boot.

4.1.13 Z^{2}C PORT INTERFACE

Table 4-13: Z^{2}C Port Interface (2 Pins)

Pin Name	Direction	I/O Buffer	Description
SDA / ICGPIO0	I/O	IOs	Data In/Out Pin
SCL / ICGPIO1	I/O	IOs	Clock ? Supports single master operation only

4.1.14 PLL PORT INTERFACE

Table 4-14: PLL Port Interface (4 Pins)

Pin Name	Direction	I/O Buffer	Description
VCLKI	I	IO_XTL	Main Input Clock Driven by 12MHz crystal or clock oscillator 30PPM
VCLKO	O	IO_XTL	Crystal Oscillator Driver Output Not connected if crystal oscillator not used

Table 4-14: PLL Port Interface (4 Pins) ***(continued)***

Pin Name	Direction	I/O Buffer	Description
VDDPLL	PWR 1.8V	PWR	PLL VDD ? 1.8V
GNDPLL	PWR	PWR	PLL Ground

4.1.15 RTC INTERFACE

Table 4-15: RTC Interface (3 Pins)

Pin Name	Direction	I/O Buffer	Description
RTCXI	I	IO_XTL	RTC Clock Input? Connect a 32.768kHz crystal If RTC not in use, connect this pin to GNDPWR
RTCXO	O	IO_XTL	RTC Clock Output? Connect a 32.768kHz crystal If RTC not in use, leave this pin open.
VDDRTC	PWR	PWR	Real Time Clock Power Connect a backup capacitor to this pin If RTC not in use, leave this pin open

4.1.16 PWRC INTERFACE

Table 4-16: PWRC Interface (8 Pins)

Pin Name	Direction	I/O Buffer	Description
PWRON[2:0]	I	I_ANLG	Camera power on and off signal. Active High
PWRENB	O	O_ANLG	Power Enable Signal ? Enables the main DCDC controller
PDETECT	I	I_ANLG	Battery Voltage Detect. PDETECT < VDDPWR Connect an RC delay circuit to this pin
RESET#	I	I_ANLG	Main reset
VDDPWR	PWR	PWR	PWRC supply voltage
GNDPWR	PWR	PWR	PWRC Ground

4.1.17 EJTAG INTERFACE

Table 4-17: EJTAG Interface (4 Pins)

Pin Name	Direction	I/O Buffer	Description
EJTMS / EJGPIO0	I	IOUm	Debug Port Mode
EJTCK / EJGPIO1	I	IOm	Debug Port Clock
EJTDI / EJGPIO2	I	IOUm	Debug Port Data In
EJTDO / EJGPIO3	O	IOm	Debug Port Data Out

4.1.18 ADC INTERFACE

Table 4-18: ADC Interface 5 Pins)

Pin Name	Direction	I/O Buffer	Description
GPADC[1:0]	I	I_ANLG	General Purpose ADC Input Pins
GPADC4	I	I_ANLG	General Purpose ADC Input Pin
VDDADC	PWR	PWR	ADC VDD
GNDADC	PWR	PWR	ADC Ground

4.1.19 LENS INTERFACE.

Table 4-19: LENS Interface (16 Pins)

Pin Name	Direction	I/O Buffer	Description
M1[D:A] / LGPIO[3:0]	I/O	IODm	Focus Motor Control
M2[D:A] / LGPIO[7:4]	I/O	IODm	Zoom Motor Control
M3[D:A] / LGPIO[11:8]	I/O	IODm	Iris/Shutter Motor Control
M4[D:A] / GSI[3:0] LGPIO[15:12]	I/O	IODm	Motor Control

LGPIO[11:8] can be used as interrupts

4.1.20 XLGPIO PINS.

Table 4-20: XLGPIO Pins (4 Pins)

Pin Name	Direction	I/O Buffer	Description
XLGPIO0	I/O	IODm	General Purpose I/O
XLGPIO1	I/O	IODm	General Purpose I/O Has a configurable counter used as zoom encoder counter input when applicable
XLGPIO2	I/O	IOm	General Purpose I/O
XLGPIO4	I/O	IODm	General Purpose I/O

XLGPIO4, XLGPIO1, and XLGPIO0 can be used as interrupts

4.1.21 GENERAL SERIAL INTERFACE (GSI)

The GSI pins are multiplexed with two PWM and four Lens interface signals. Please refer to that those pin description sections for details.

4.1.22 POWER PINS

Table 4-21: Power Pins (63 Pins)

Pin Name	Direction	I/O Buffer	Description
GND	PWR	PWR	Ground ? 49 Pins
VDDP	PWR 3.3V	PWR	3.3V Power Supply Pin for I/O Pads ? 7 Pins
VDDCORE	PWR 1.8V	PWR	1.8V Power Supply Pin for Core ? 7 Pins

4.2 CONFIGURATION PINS

The Flash Memory Interface Address bus pins, FA[19:13], and DLCD Data bus pins, DVDAT[4:0], are used as CFG[16:0] and are defined as inputs during reset. External pull-up/down resistors define the input value ? ?or ? ? respectively. Following de-assertion of RESET#, the CFG[16:0] values are sampled and the pin direction is switched to output to drive the Flash Memory and DLCD interfaces.

Table 4-22: Configuration Pin Values

Signal Name	Configuration Name	Description
CFG0 =DVDAT4	Reserved	Install a PD resistor
CFG[2:1] =DVDAT[1:0]	Reserved	Install a PD resistor
CFG4=DVDAT2	Reserved	Install a PD resistor
CFG5 = FA13	Reserved	Install a PD resistor
CFG6 =FA14	Boot speed/ NAND2K capacity	Boot speed for resident NOR or NAND with less than 2K page size: 0 - slow 1 - fast 2K page NAND capacity (always slow boot speed) 0 - 2Gb and up 1 - 1Gb
CFG7 =DVDAT3	Reserved	Install a PD resistor
CFG[16:12] =FA[19:15]	Boot Device	Selects the Primary Boot Source CCLKOUT = FA19 = MSB 00000 ? 2 KB page NANDs. 1Gb if CFG6 = 1, 2 Gb and up if CFG6 = 0. 00001 ? UART Command 00010 ? Resident NOR (INTEL and AMD types) 00011 ? 8 or 16 Mb resident NAND flash 00100 ? 32 or 64 Mb resident NAND flash 00101 ? 128 or 256 Mb resident NAND flash 00111 ? Reserved for internal use 01000 ? 4-bit SD card (all versions except SD 2.0) 01111 ? MMC 1bit

Table Notes:

1. Reserved CFG pins must be pulled down with a resistor and not be left floating during reset.
2. Ignore the gap in the number sequence.
3. **WARNING**: If any of the DVDAT configuration pins are set to value ? ? the LCD electronics (except LCD backlight) must be powered up during boot time.
4. The COACH cannot boot from an SD 2.0 card.

4.3 PIN INITIALIZATION STATES

During and after active reset, until the time firmware takes control, the COACH-9e pins are set to an initialization state, as defined in Table 4-24, 揑n Initialization State Values,?on page 4-18. Table 4-23 shows the state legend for the initialization states.

Most pins whose initial state is input are internally connected to pull-up or pull-down resistors, as indicated in Table 4-24. When the booted firmware takes control of the pins, it disables the pull-up and pull-down resistors, except as noted.

Table 4-23: Initialization State Legend

State	Description
I	Input without pull-up or pull-down (floating)
I,PD	Input with pull-down enabled
I,PU	Input with pull-up enabled
O	Output direction
O,Z	Output direction? Asserted by software
O,H	Output direction? Asserted by hardware to drive High; deasserted by software
O,L	Output direction? Asserted by hardware to drive Low; deasserted by software
I, CFG	Input direction? Used for configuration settings.
INOUT_S	Input or output, Software selectable

Table 4-24: Pin Initialization State Values

Pin Name	Initialization State
DDR	
RAMDAT[15:0]	O
RAMADD[12:0]	O, L
RAMBA[1:0]	O, L
RAMRAS#	O, H
RAMCAS#	O, H
RAMCLK	O
RAMCLK#	O

Table 4-24: Pin Initialization State Values *(continued)*

Pin Name	Initialization State
RAMLDM	O, H
RAMUDM	O, H
RAMCS#	O, H
RAMWE#	O, H
RAMLDQS	O, L
RAMUDQS	O, L
RAMCKEN	O, L
CCD	
SPDAT	I, PD
SPCLK	I, PD
AFEVAL	I, PU
TGVAL	I, PU
VIS	I, PD
HIS	I, PD
VID[9:0]	I, PD
CCLK	I
CCLKOUT	I, PD
SUBCNTL	I, PD
EXPCNTL	I, PD
FLASH STROBE	
FLSHTRIG	I, PD
FPDIN	I, PD
DLCD	
DVDAT[4:0]	I,CFG
DVDAT[7:5]	I, PD

Table 4-24: Pin Initialization State Values *(continued)*

Pin Name	Initialization State
DVCLK	I, PD
DVCNTL[9:0]	I, PD
AUDIO	
AUDGPIO0	I, PD
AUDGPIO1	I, PD
AUDGPIO2	I, PD
AUDGPIO3	I, PD
AUDGPIO4	I, PD
PWM	
PWM[7:0]	I, PD
UART	
TXD	I, PD
RXD	I, PD
FLASH	
FRESCE#	O, H
FGPIO1#	O, H
FWR#	I, PU
FOE#	O, H
FD[7:0]	O, H
FA0	O, L
FA1	O, L
FA2	I, PD
FA3	I, PD
FA[7:4]	I, PU
FA[11:8]	I, PD

Table 4-24: Pin Initialization State Values *(continued)*

Pin Name	Initialization State
FA12	I, PU
FRESBSY#[2]	I, PU
FEXTBSY#	I, PU
FCD1#	I, PU
FCLK	O, L
FA[19:13]	I, CFG
FA[23:20]	I[1]
FGPIO25	O, H
FGPIO26	O, H
FGPIO27	O, H
FGPIO28	O, H
FGPIO29	O, L
FGPIO30	O, L
FGPIO31	I, PU
ZI^{2}C	
SDA	I
SCL	I
EJTAG	
EJTMS[2]	I, PU (Permanent)
EJTCK	I
EJTDI[2]	I, PU (Permanent)
EJTDO	I
LENS	
M1[D:A]	I, PD

Table 4-24: Pin Initialization State Values *(continued)*

Pin Name	Initialization State
M2[D:A]	I, PD
M3[D:A]	I, PD
M4[D:A]	I, PD
GPIO	
XLGPIO[1:0]	I, PD
XLGPIO2	O, L
XLGPIO4	I, PD
ANALOG	
RAMVREF	I
VCLKI	I
VCLKO	O
RTCXI	I
RTCXO	O
PWRON0	I
PWRON1	I
PWRON2	I
PWRENB	O
PDETECT	I
RESET#	I
GPADC4, GPADC[1:0]	I
CVBS	O, Z
RSET	I
USBDN	O, Z
USBDP	O, Z
USBVBUS	I

Table 4-24: Pin Initialization State Values *(continued)*

Pin Name	Initialization State
USBRSET	I
MICP	I
MICN	I
MICENB	O, L
SPKRP	O, Z
SPKRN	O, Z
LINEOUT	O, Z
VCM	O
AREF	I
HPR	O
HPL	O

Table Notes:

1. The FA[23:20] lines are not connected to internal PU or PD resistors. For this reason, the user should put external PD resistors so the pins are not floating. If an MS/MSPro card is connected to these lines, the PD resistors are part of the MS/MSPro system configuration already.
2. The pins FRESBSY#, EJTMS, and EJTDI have permanent internal pull resistors (PU/PD as defined during initialization), even after software disabled the internal pull resistors.

4.4 I/O STRUCTURE DIAGRAMS

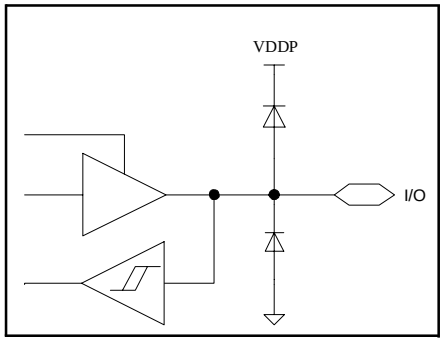

Figure 4-1: *IO Structure Diagram*

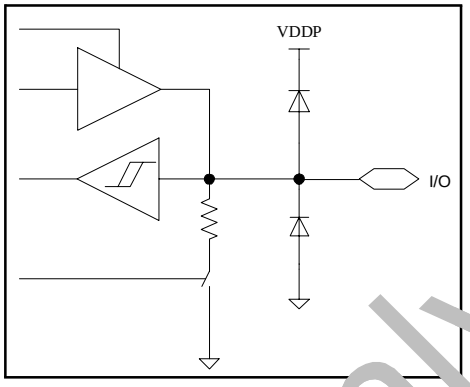

Figure 4-2: *IOD Structure Diagram*

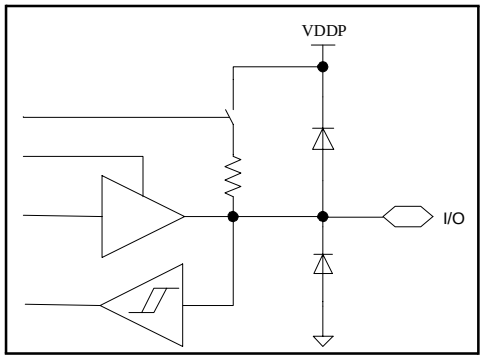

Figure 4-3: *IOU Structure Diagram*

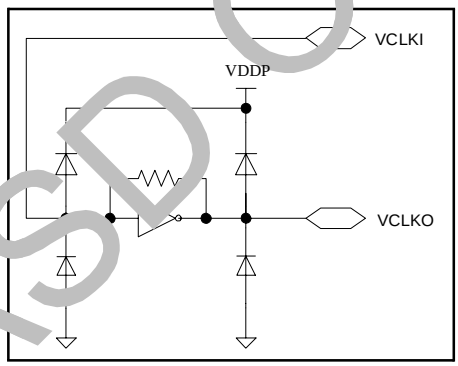

Figure 4-4: *IOCLK Structure Diagram*

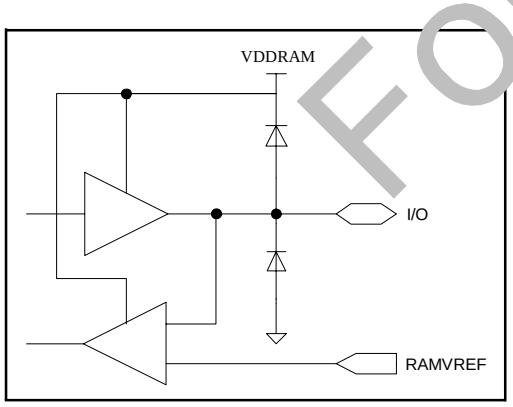

Figure 4-5: *SSTL_IO Structure Diagram*

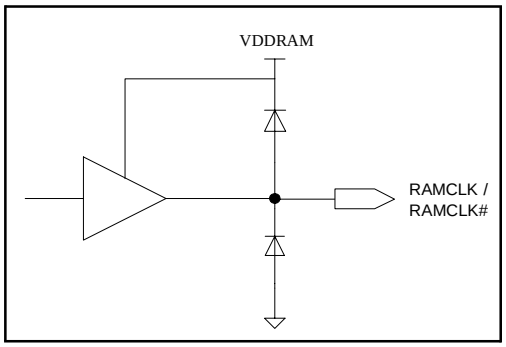

Figure 4-6: *SSTL_CLK Structure Diagram*

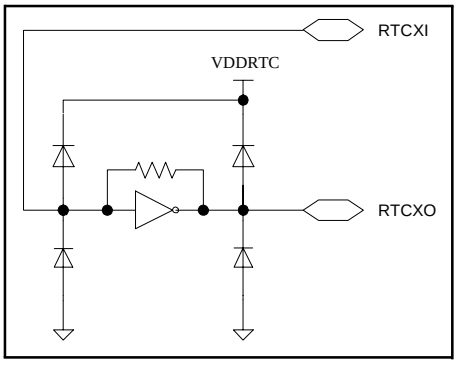

Figure 4-7: *IORTC Structure Diagram*

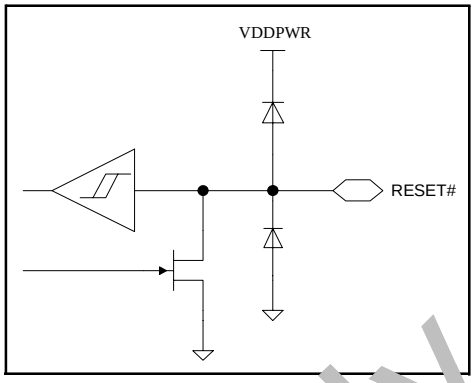

Figure 4-8: *IORESET# Structure Diagram*

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CHAPTER 5 INTERFACE DESCRIPTIONS

5.1 DDR

The COACH has an integrated DDR SDRAM controller with an SSTL_21x compatible interface. Termination resistors connected to a termination voltage (VTT) are unnecessary because of the point-to-point environment; however, it may be necessary to include series resistors in the clock and strobe lines to improve signal quality. PCB signal trace lengths can be very short, thus ensuring that the duration of undershoot or overshoot owing to impedance mismatch is negligibly short. If data and strobe trace lengths are made substantially equal, skew requirements can easily be satisfied: for write operations the setup and hold times have values guaranteed by design; for read operations, the delay locked loop (DLL) positions the internal read strobe optimally with respect to the external data strobe edges.

The controller supports industry standard JEDEC-compliant DDR memory chips and some non-compliant chips with a +2.5V nominal supply voltage (VDDRAM) with densities ranging from 128Mb to 256Mb. The interface supports 4 banks, 16 bit data bus width, 13 bit address bus width, and a 108MHz clock frequency. To allow users the flexibility to customize the interface for a particular DDR device, certain features of the DDR interface are parameterized in the controller design. By setting those parameter values, the controller will initialize the DDR in the required predefined manner and customize certain programmable timing constraints.

5.2 CCD/CMOS

The COACH provides a flexible interface to CMOS and CCD image sensor chipsets. It supports a variety of still mode and 30fps video mode sensors with up to 10-bit pixel depth. For CCD sensors, control signals are driven by the timing generator (TG) device while the image data is received from the analog front end (AFE) device. In addition, the COACH can trigger the mechanical shutter and provide optimal exposure control. Interface timing is configurable through firmware settings.

Synchronization signals and image data are synchronous to the pixel clock CCLK, which is always an input. The COACH has an optional clock generator (CCLKOUT), which can be used to provide a clock to the sensor chip set. CCLKOUT frequency is programmable in the range 10.0MHz to 80MHz; available frequencies are 648MHz/N for integer values of N. The internal synchronization signal generator can operate in master or slave mode.

5.3 SENSOR SERIAL PORT

The Sensor Serial Port (SP) interface is a flexible half-duplex, synchronous, serial communication channel. The SP is typically used to configure CCD sensor TG (Timing Generator) and AFE (Analog Front-End) chip-sets, as illustrated in Figure 5-1, *Serial Port Interface*. It is also possible to implement a communication channel with other compatible devices. SPCLK is the output clock, TGVAL is the timing generator data latch, AFEVAL is the analog front end data latch, and SPDAT is the bi-directional data.

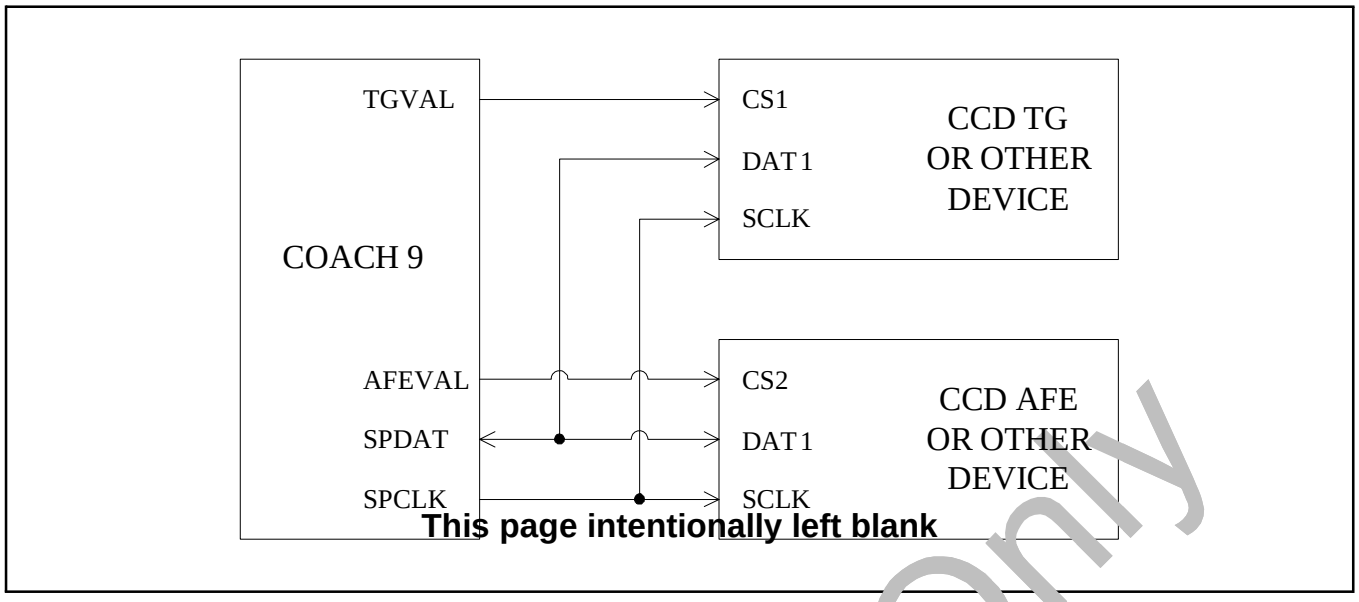

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Figure 5-1: *Serial Port Interface*

The protocol is controlled by software, so the user must refer to the appropriate documentation for configuration details. The SP interface includes two sets of control registers, one related to the TG and one to the AFE. The control registers define for each device the SPCLK rate, SPCLK sampling edge and the TGVAL/AFEVAL signal waveforms. These registers also select transmit or receive transactions with the TG or AFE devices, alternating between devices if desired, with programmable delay between each transaction.

Two modes of data transmission can be implemented; short data bursts with either device, and long data bursts reserved for TG transactions only. The protocol can transmit continuous short data bursts of up to 128 bits to the selected device at a clock frequency of 3.375 MHz or 421.875 KHz. Long data bursts can be transmitted only to the TG at the aforementioned clock frequencies plus an additional frequency setting of 27 MHz. In this mode, data is transmitted under DMA control and a CPU interrupt is generated at the end of transmission. To initiate receive mode, the COACH selects the TG or AFE by transmitting the device address and asserting the read bit. SPDAT changes direction from output to input and receives up to 128 bits of sequential data. Upon completion of data transfer, SPDAT reverts back to its default output direction. The clock frequency can be set to 3.375 MHz or 421.875 KHz in receive mode.

The following is a brief description of each SP signal:

- **SPDAT**奎 erial data I/O. The trigger event for data transmission and data delay from the trigger are programmable. The short data burst length is programmable through the API.
- **SPCLK**奎 erial clock output. SPCLK inactive level, active edge, and frequency are programmable through the API.
- **TGVAL**梶 G latch enable output. The polarity and active timing are programmable through the API.
- **AFEVAL**桝 FE latch enable output. The polarity and active timing are programmable through the API.

5.4 PHOTOFLASH

The COACH supports a variety of photoflash modes and timing parameters. The FLSHTRIG output drives the photoflash circuit and can operate in three primary modes; disabled under all lighting conditions, controlled by an auto exposure algorithm, or enabled under all lighting conditions. FLSHTRIG polarity, duration, and delay are programmable. The COACH also supports red eye reduction.

The COACH can control the duration of the photoflash time with a simple light detection circuit. A photo detector is used as a light sensitive element to sense the light reflected from the subject being photographed. The photo element generates a signal proportional to the amount of light it senses and the signal is fed to a comparator, which compares it to a dynamic reference voltage (Vref) generated by a COACH PWM output and an RC filter circuit. The required flash illumination level is determined prior to taking a picture by exposure metering algorithms running on the COACH that adjusts the reference voltage. During the photoflash illumination period, the reflected light level is compared with this reference level and the comparator signals the photoflash controller, through the FPDIN input, that enough illumination has been projected onto the subject. The flash trigger output (FLSHTRIG) then shuts down the photoflash discharge circuitry, turning off the flash output. The FPDIN polarity can be set to active high or low through the firmware. Figure 5-2, *Photoflash Control Configuration*, shows an example of the photoflash control circuit.

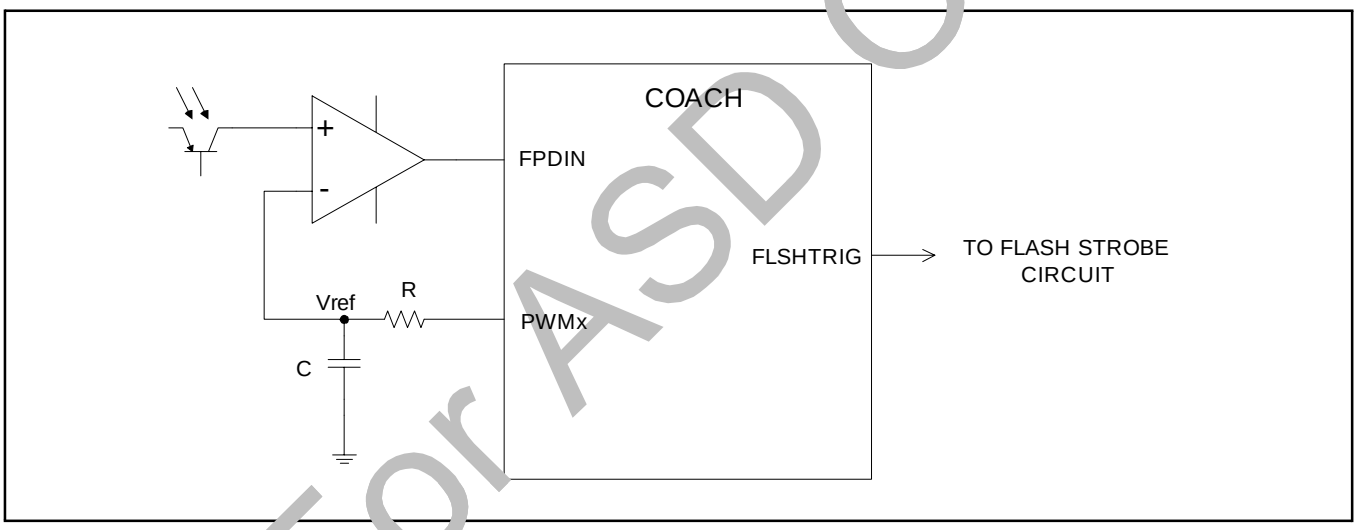

Figure 5-2: *Photoflash Control Configuration*

5.5 LCD CONTROLLER

The COACH LCD controller is a highly programmable interface with an 8-bit wide data bus and ten dedicated control signals. Its programmable timing generator can produce any desired pattern of sync and control signals. The phase of the data and control signals with respect to the clock is programmable in increments of one-half of the clock period for clock frequencies (f_{CLK}) in the range 13.5MHz < $f_{CLK} \leq$ 27.0MHz, one-quarter of the clock period for 6.75MHz < $f_{CLK} \leq$ 13.5MHz, and one-eighth of the clock period for 3.0MHz < $f_{CLK} \leq$ 6.75MHz. The clock frequency is programmable in the range 3.0MHz to 27.0MHz with available frequencies in this range expressed as 324/N MHz, where $12 \leq N \leq 108$.

The interface supports RGB and YUV4:2:2 formats in a variety of arrangements including RGB strip and RGB delta. Other features include programmable scan direction, interlaced and non-interlaced modes.

To make implementation easier and take advantage of established designs, it is advisable to assign DVCNTL1 as VSYNC and DVCNTL2 as HSYNC.

The LCD controller unit can be disabled by software for power savings.

5.6 TV MONITOR

The COACH outputs an analog composite video signal (CVBS) driven by a digital composite video encoder. The 10-bit, current-output video DAC is designed to drive a 37.5 ohm load consisting of a 75 ohm resistor connected to the COACH output in parallel with the 75 ohm input resistance of the TV. The DAC is clocked at 27MHz, so an LC-pi smoothing filter is typically used but may not be required. The video encoder clock is derived from the 12MHz main clock oscillator by an analog PLL, so the color sub-carrier frequency tolerance is the same as that of the 12MHz clock. The DAC current reference is set by a resistor connected to RSET. The resistor value is derived as follows:

RSET Resistor Value= (8.50 ∗ *Vref* ∗ *RL*) ÷ *Vfs*

where:

Vref = 1.235V (COACH internal reference voltage)

RL = DAC load resistance connected to the CVBS output pin (37.5Ω).

Vfs = full scale video voltage output (usually 1Vpp)

The closest 1% resistor value is 392 ohms.

The video signal can be encoded in either NTSC or PAL format. Black level, white level, blank level, Cb and Cr burst levels, and Cb and Cr gains are programmable while all video timing values are internally fixed.

The video encoder and DAC can be disabled for power savings.

5.7 AUDIO

5.7.1 AUDIO INTERFACE

COACH has a built-in linear audio codec (the ASC). At any time, the codec can be operating in recording (A/D) or playback (D/A) mode; simultaneous recording and playback is not supported. The master clock is generated by a discrete-time oscillator (DTO) at frequencies of 3200 ∗ fs. Sample rates of 32K, 44.1K and 48K samples/second are supported.

5.7.2 BUILT-IN ASC

The ASC block contains a mono ADC, stereo DAC, digital channel filters, differential-input microphone amplifier, and speaker/line/headphone drivers (refer to Figure 5-4, *ASC Structure,* on page 5-6).

The microphone amplifier gain control has a range of -26dB to +12dB in 0.5dB steps. The record channel also has programmable Automatic Level Control (ALC) to keep the recording level constant; for more details see the next section. (With microphone input, the ALC should be enabled and the amplifier gain would typically be set

to +12dB. With line input, the ALC should be disabled and the amplifier gain should be set to a level that supports the input signal swing.) The MICENB pin supplies power (VDDAUD) to the microphone when enabled. The firmware activates the MICENB signal prior to recording and recording begins after the reference voltage external capacitor is fully charged. AC coupling capacitors are required at the MICP and MICN inputs with recommended values of 2.2uF. A capacitor of a few hundred picofarads connected across the microphone may also be beneficial, to attenuate RF pickup.

The playback channel can drive stereo headphones, mono speaker connected to the differential-output speaker driver and mono line output. The differential speaker amplifier can drive 100mW into an 8-ohm speaker. Each headphone amplifier can drive 15mW into a 16-ohm headphone. Figure 5-3 shows the recommended circuit for headphone load.

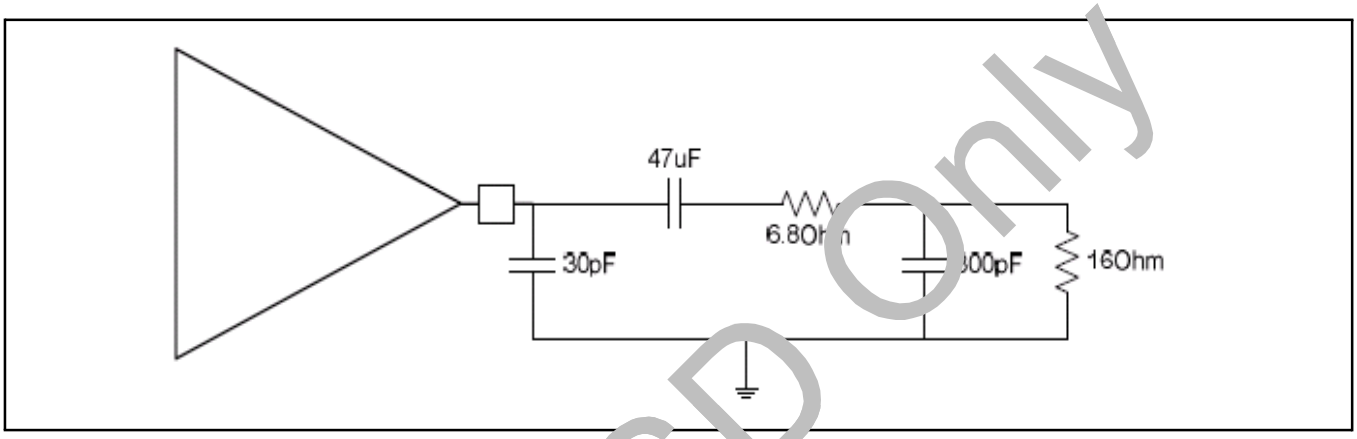

Figure 5-3: *Recommended Headphone Load Circuit*

VDDSPKR powers the speaker, headphones, and line output buffers. VDDAUD powers the remaining circuits (DAC, ADC, microphone amplifier, etc.). When the headphone amplifier is disabled, the left and right channel outputs remain biased to VDDSPKR/2, to minimize pop noise when the amplifier is enabled. The line output does not have a similar internal bias circuit; when disabled, it settles to 0 volts, and external means of minimizing pop noise must be used if this is a problem.

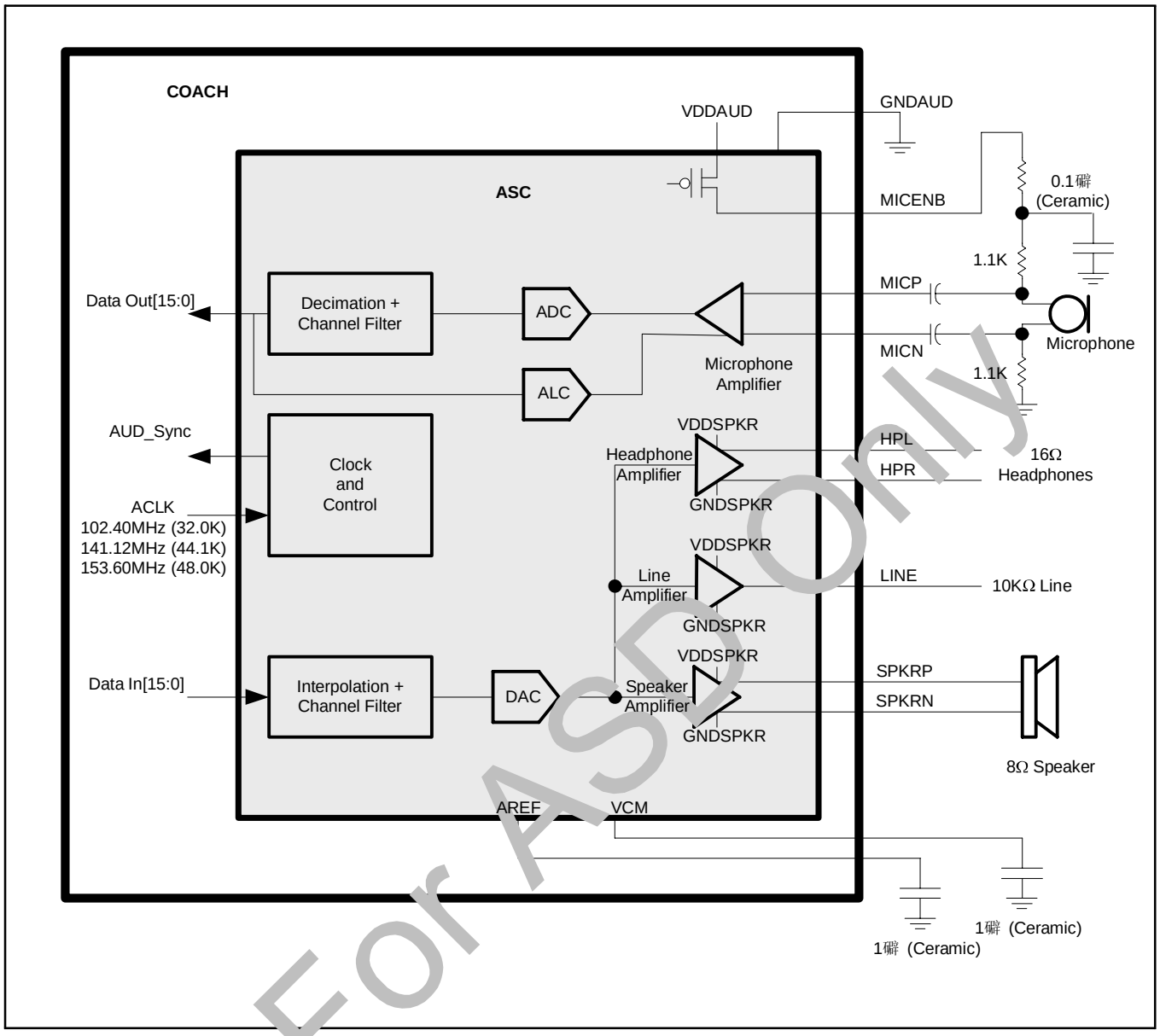

Figure 5-4: *ASC Structure*

5.7.3 AUTOMATIC LEVEL CONTROL

The ADC channel features automatic level control (ALC) which overrides the currently programmed input amplifier gain and automatically sets it to a value that tends to keep a -3dBFS constant recording level for varying input amplitudes. The ALC can be enabled or disabled through software settings. Figure 5-5, *ALC Operation*, illustrates how the ALC operates, including the delay associated with it.

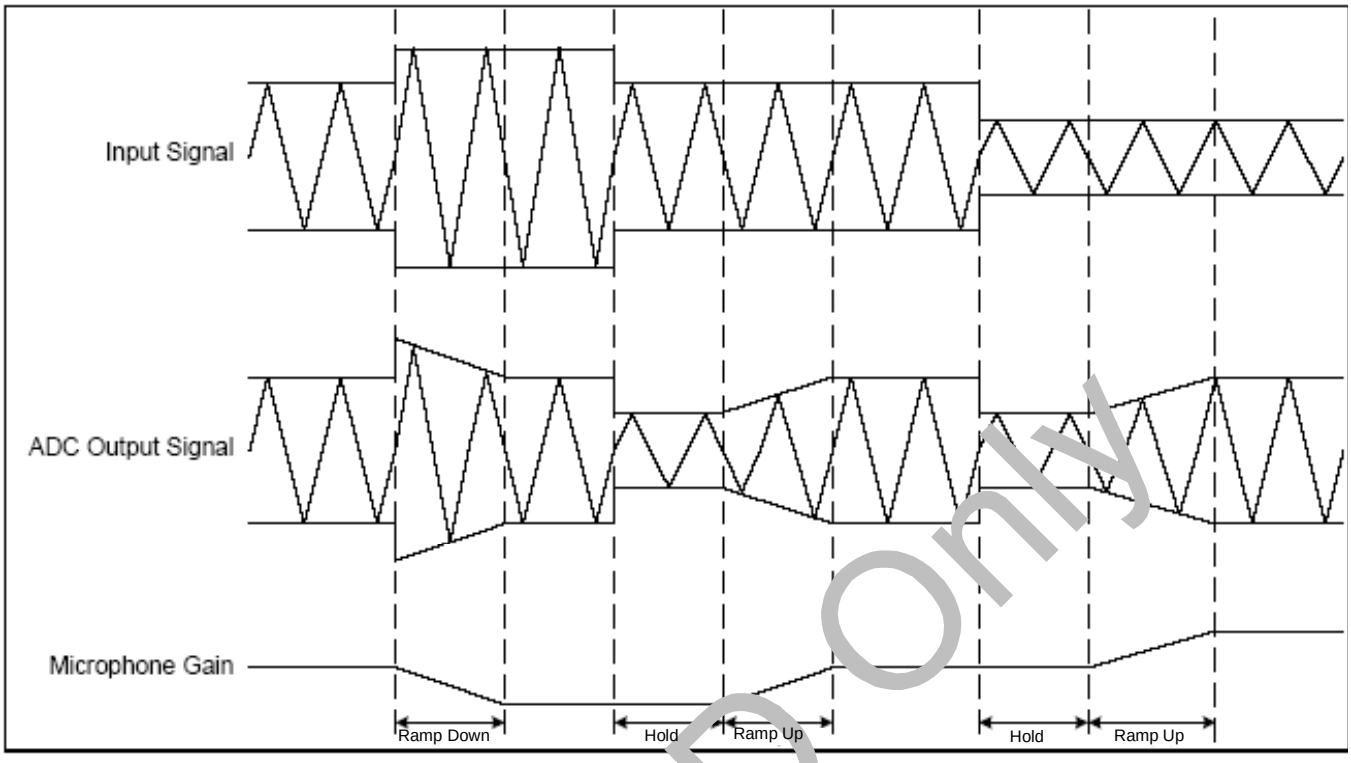

Figure 5-5: *ALC Operation*

The time response of the ALC to input amplitude variations are defined as follows:

- 昤 he ramp up interval is the time it takes the ALC to change gain from -24dB to +10dB (90% of the gain range).
- 昤 he ramp down interval is the time it takes the ALC to change gain from +10db to -24dB.
- 昤 he hold interval is the time the ALC waits before increasing the gain on low amplitude detection. This is useful for avoiding gain changes during short periods of intentional silence.

The ramp up and ramp down periods have a programmable range of 3ms to 24.576s and the hold period has a programmable range of 2.6ms to 87.4906s. The maximum input amplifier gain setting, when the ALC is active, is programmable from 0dB to +12dB in increments of 3dB.

During long periods of silence the ALC may erroneously increase the gain, so to ensure ambient noise isn't amplified, a noise gate is implemented in the codec that automatically mutes the digital signal. The noise gate threshold is -63dBFS and is enabled through software settings.

5.8 PWM

There are eight pulse width modulation (PWM) signal generators. Each can be independently programmed to operate in one of two modes:

- 昆 onstant duty cycle mode栝 enerates a constant-frequency, constant duty-cycle pulse train. Frequency

and duty cycle are software-specified.

- 旳 verage duty cycle mode栝 enerates a train of pulses with a software-specified average duty cycle. The pulse width is fixed, but the pulse period is variable. With an external lowpass filter, this mode is useful to implement a simple D/A converter to generate a DC voltage level.

In addition, there are two repeat modes: single mode and continuous mode. In single mode, a single cycle is generated. In continuous mode, a continuous stream of cycles is generated until stopped. Single mode is available only in constant duty cycle mode.

In constant duty cycle mode, the programmable frequency range is 824Hz to 1.6875MHz. The high and low times of the cycle are programmed as integer multiples of 1/27MHz, with all cycles having identical timing in continuous mode. High and low values must be multiples of 8 when configured for single cycle. Timing multiples can range from 8 (2^3) to 16384 (2^14). For example, to generate a 33.33% duty cycle set the high time integer multiple (NH) to 8, the low time integer multiple (NL) to 16, and calculate the frequency as follows:

$$\frac{27MHz}{NH+NL} \qquad \frac{27MHz}{24} \qquad 1.125MHz$$

In average duty cycle mode, the high and low times of the cycle are programmed in fixed-point resolution to provide better accuracy. Since the timing can vary from one cycle to the next, the frequency of each cycle is not important here. The maximum high and low timing multiples are set with an 8-bit integer plus 6-bit fraction. The minimum low and high time multiple is 8 in units of 64 ÷ 27MHz. The width of the active pulse is 8 units, and the inactive part of the cycle is specified by a 14-bit fixed-point number, interpreted as 8 integer bits and 6 fractional bits.This mode is best utilized for DC level generation with an external RC low-pass filter. In such an application, it is desirable to run at the highest available frequency to minimize ripple.

Figure 5-6, *PWM Outputs* shows an example output in each mode. The PWM generators can be independently enabled or disabled; if disabled, the output is held low. Each generator can also be programmed to issue an interrupt at the end of its cycle (high time plus low time).

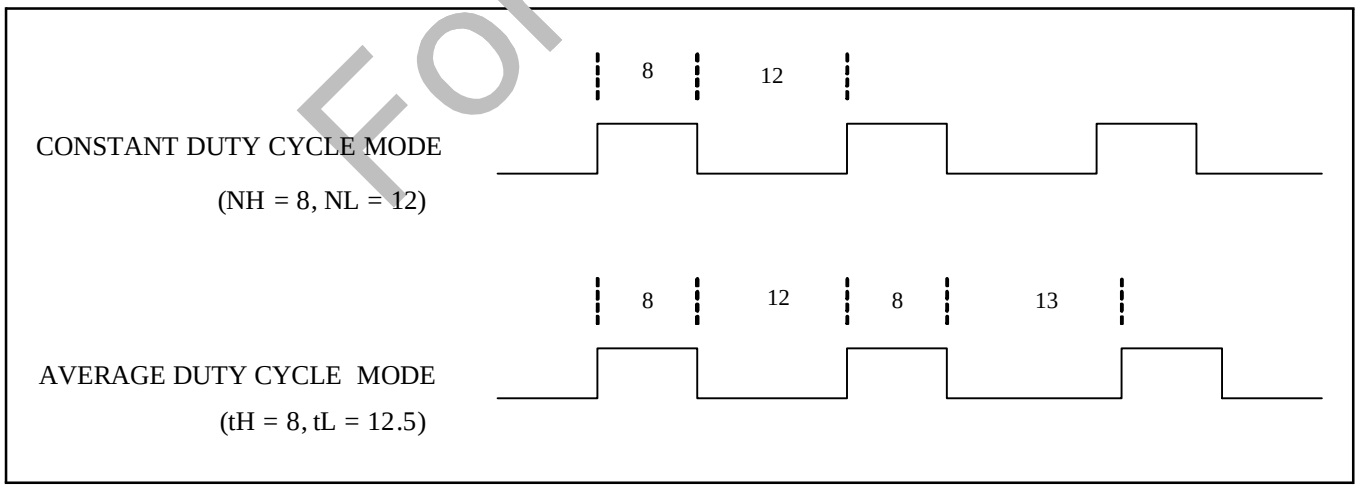

Figure 5-6: *PWM Outputs*

5.9 USB

The COACH features a fully compliant Universal Serial Bus (USB) 2.0 High Speed slave (device) interface. The COACH also supports full speed, making it compliant with USB 1.1. Software can disable USB operation for power savings.

This block has an integral PLL clock generator driven from the 12MHz main COACH oscillator. The USB block and the USB PLL clock generator are each powered from isolated supplies. All required pull-up, pull-down, and series termination resistors are internal to the COACH. Termination resistors are self-calibrated with an external resistor connected to USBRSET.

The COACH supports USB Suspend and Resume power control modes, when configured as slave, as defined in the USB 2.0 standard. The USB clock is disabled during suspend mode and enabled after resume mode is entered.

For correct operation in High Speed mode, the USB interface should not be connected to more than one USB connector.

5.10 UART

A universal asynchronous receiver transmitter (UART) port is integrated into the COACH. It can be used for any purpose, the most popular being software debugging. The UART supports full duplex, asynchronous, serial communication at programmable baud rates shown in Table 5-1 (*UART Baud Rates)*.

Table 5-1: UART Baud Rates

Baud Rate (bps)
9600
14400
19200
38400
57600
115200

It is based on the industry standard 16550 UART chip and includes a baud rate generator, first-in first-out (FIFO) buffer, serial-to-parallel converter, and parallel-to-serial converter. It is a highly programmable block with even, odd, or no parity generation and detection. A communication event consists of a start bit, 5 to 8 bit data stream, optional parity, followed by the stop bit.

The UART block can be disabled for power savings. For a production design where the interface is not utilized, all UART interface pins can be left open.

If a second UART is required, it is possible to implement one using the General Serial Interface.

5.11 FLASH CONTROL UNIT

The Flash memory Control Unit (FCU) is a flexible and highly programmable block that can implement a variety of flash memory interfaces and protocols. Pull-up and pull-down resistors on designated configuration pins to select the type of medium that the COACH will boot the firmware from. The COACH can boot from and communicate with any supported medium. The FCU supports one resident and up to two external media in a system design; however, only one can be active at a time. Some FCU pins can be shared between different media. See Table 3-1 on page -3 for detailed connection information. The following list shows supported devices and describes a few of the interface details.

- **NAND**泰 esident only. Single-Level Cell (SLC). Note that the NAND flash must support Sequential Row Read if the "Fast boot" configuration is used and the page size is 512+16 bytes or smaller.
- **8-bit NOR**泰 esident only. Intel and AMD type up to 16MB density.
- **Secure Digital (SD)**梁 xternal only. 1-bit and 4-bit SD mode. SPI mode is not supported. See Chapter 5, 揷C/DC Characteristics" for the maximum clock frequency supported.
- **Multi-Media Card (MMC)**梁 xternal only. 1-bit and 4-bit mode. MMC-HS is supported in 4-bit mode up to 25MHz.

5.12 Z^2C

The Z^2C interface is a serial bus master that implements industry-standard two-wire data communication between the chip and one or more compatible slave devices. The COACH Z^2C clock is programmable from 42.2KHz to 400KHz at discrete frequencies expressed as 108MHz ÷ 5N, where maximum N is 512. (If a slower speed is desired, the protocol is implemented in firmware with port pins defined as GPIO.) The Z^2C bus supports clock stretching.

The interface consists of two signals: SDA, the bidirectional serial data signal; and SCL, the clock, always driven by the COACH. Data transfer may consist of a single byte or several bytes in burst mode. The bytes within the address or data parts of the communication session are transmitted MSB first. SCL high time is two-fifths of a clock cycle. All setup and hold times are one-fifth of a clock cycle; the user must select the clock frequency such that the setup hold time specifications of the slave device are satisfied. The SDA and SCL I/O buffers emulate open-drain types and require external pull-up resistors to interface with slave devices. Pull-up resistor values of 10K satisfy the majority of applications. Note that variations in resistor value and circuit capacitance may affect actual setup and hold times.

5.13 PLL

The COACH phase locked loop (PLL) circuit requires a 12MHz reference, that can be supplied by an external oscillator or generated by an on-chip oscillator with an external 12MHz crystal. The external oscillator should be connected to VCLKI and drive a 3.3V signal. The crystal for the internal oscillator must be fundamental mode, parallel-resonant at the required frequency. Accuracy of the oscillator frequency mainly depends on crystal frequency tolerance and the match between the crystal's specified load capacitance and actual equivalent load capacitance of the circuit. Load capacitors used in the oscillator circuit of Figure 5-7, *PLL Interface*, CL1 and CL2, plus stray capacitance in the board layout, combine to create the equivalent load capacitance, CL, as in the following formula. In the calculation, CL1 and CL2 should include the external capacitors as well as stray

capacitance and capacitance of COACH pins VCLKI and VCLKO respectively; if the crystal and capacitors are located close to the COACH, a typical value for the additional capacitance for each pin is 2pF.

$$CL = [(CL1 \times CL2) \div (CL1 + CL2)]$$

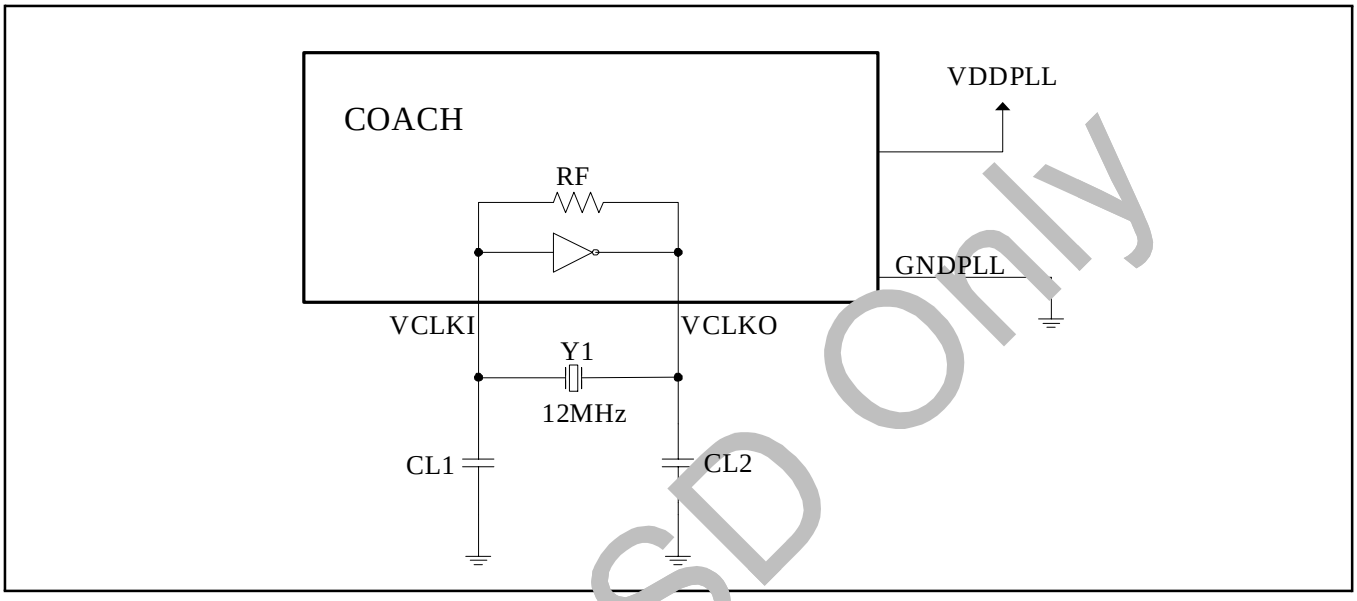

Figure 5-7: *PLL Interface*

5.14 RTC

The COACH real time clock (RTC) circuit provides a set of continuously running counters that can be used as a general time base or clock/calendar function. The count range is 136 years with one second resolution and the circuit can issue interrupts to the CPU every second. The RTC requires a 32.768KHz reference, supplied by a low-power on-chip oscillator with an external crystal. Time-keeping accuracy depends on the accuracy of the oscillator frequency, which in turn mainly depends on the crystal frequency tolerance and the match between crystal and oscillator capacitive load, the crystal's specified load capacitance and actual equivalent load capacitance of the circuit. Equivalent load capacitance, CL, is the capacitive load of the oscillating circuit seen from the crystal pins. Load capacitors used in the oscillator circuit of Figure 5-8, *RTC Interface*, CL1 and CL2, plus stray capacitance in the board layout and COACH capacitance, combine to create CL as in the following formula. In the calculation, CL1 and CL2 should include the external capacitors as well as stray capacitance and capacitance of COACH pins RTCXI and RTCXO respectively; if the crystal and capacitors are located close to the COACH, a typical value for the additional capacitance for each pin is 2pF.

$$CL = [(CL1 \times CL2) \div (CL1 + CL2)]$$

The RTC block is powered from VDDRTC as shown in Figure 5-8. Backup capacitor CBACKUP is charged from VDDP or VDDPWR, whichever is larger, minus a very small diode drop (approximately 0.2V). The value selected for CBACKUP depends on the amount of time sustained RTC operation is required when the battery is removed and VDDPWR and VDDP are not available. A current limiting resistor (RL) should be placed in series with the backup capacitor, large enough to limit the initial capacitor surge current to 20mA or less, yet small enough to allow a fully-discharged capacitor to charge in a reasonable time, and small enough to prevent a significant reduction in the operating voltage range due to quiescent voltage drop across it.

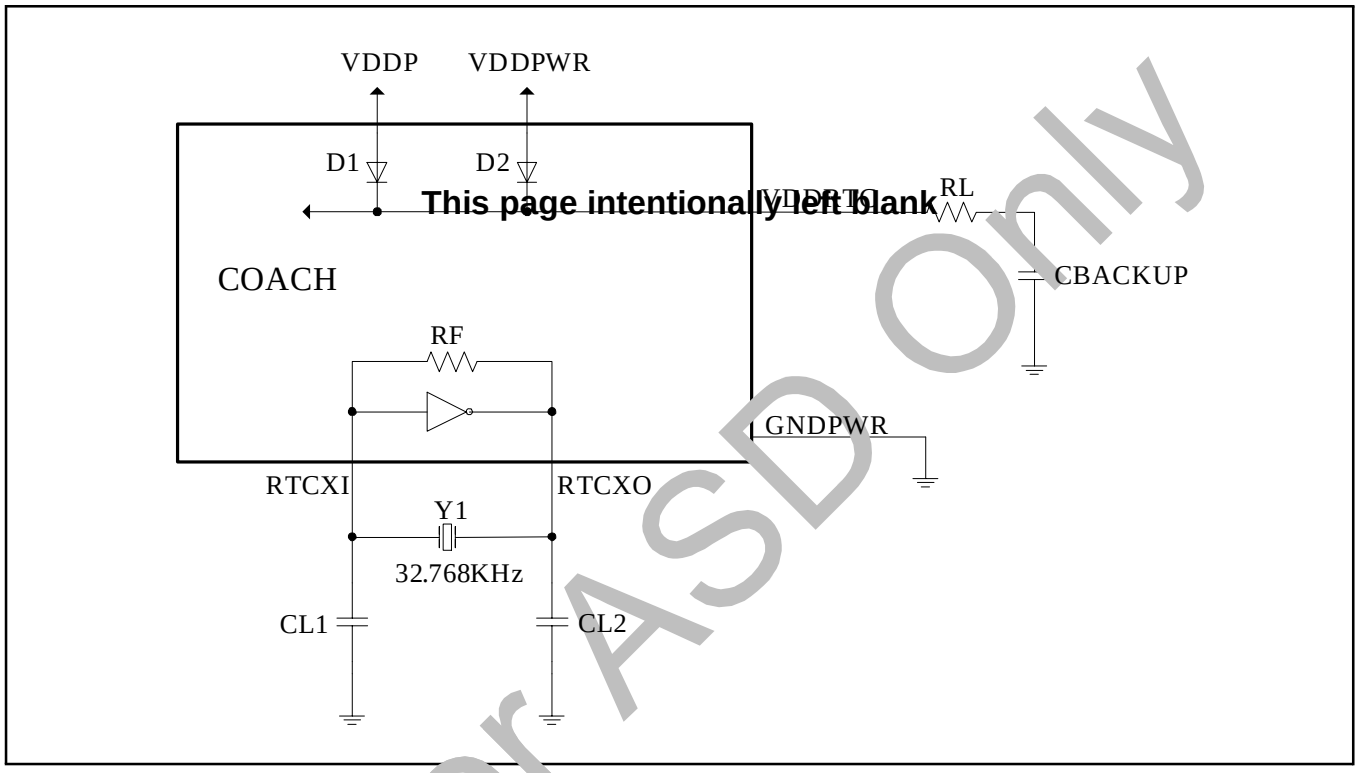

Figure 5-8: *RTC Interface*

5.15 PWRC

The power control block (PWRC) is a system power manager operating from an independent power source such as a battery or regulator. It also performs various control functions by transferring status information to and from the CPU and generates a COACH reset. The PWRC circuit is asynchronous, operating without a clock, and is designed to draw low quiescent current to maximize battery life. All inputs have Schmitt triggers to clean up slow, noisy signals. Figure 5-9 is a block diagram of the PWRC block including typical system connections.

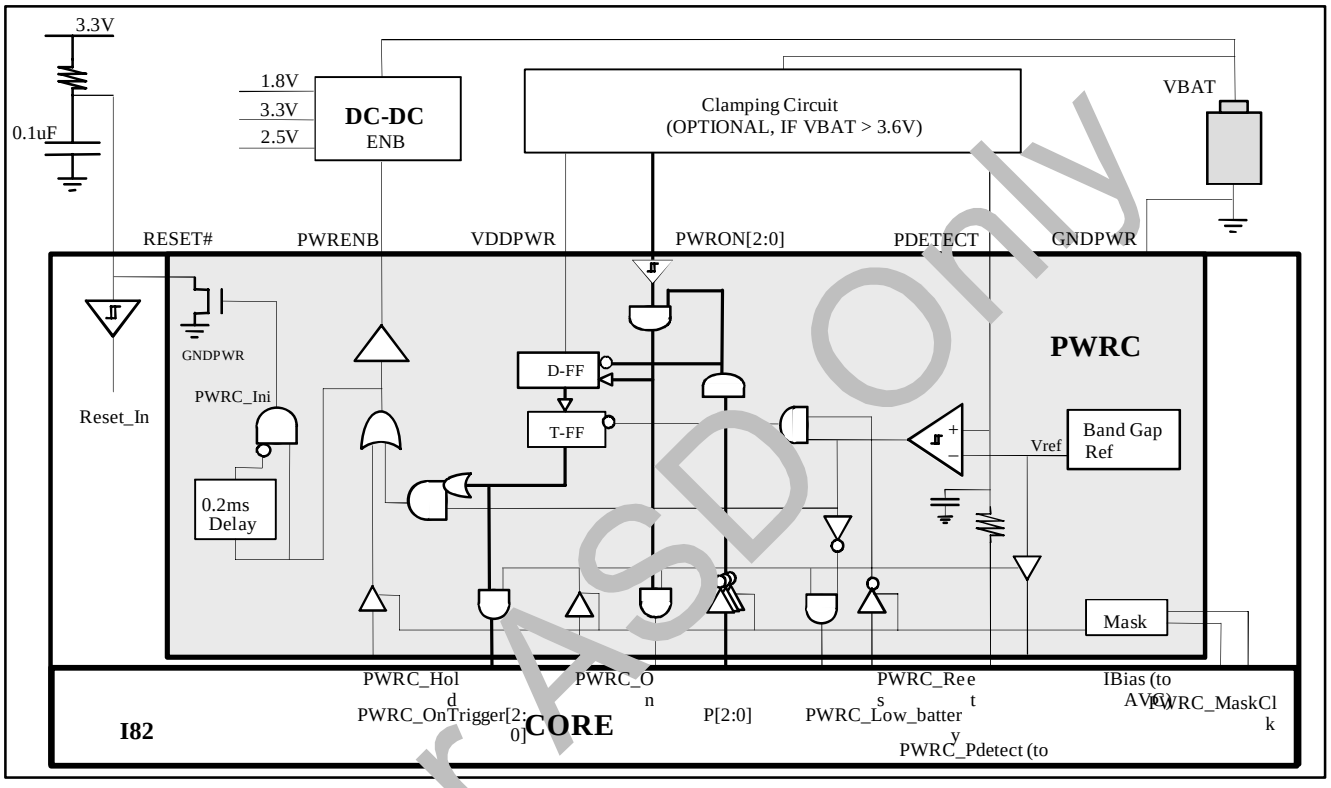

Figure 5-9: *PWRC Block Diagram*

5.15.1 PDETECT

The PWRC block has a battery level supervisory circuit to detect low battery before and after the DC/DC converters are enabled. A low power band-gap reference (see Chapter 5 for specifications) and comparator detect low battery voltage. Low battery voltage threshold is determined by applying a fraction of the battery voltage to PDETECT with an external resistor divider. As the battery voltage drops, the battery's lowest allowable voltage will equal the reference voltage at which time the comparator output goes low. The comparator has hysteresis to minimize false triggering during battery load transients. The resistors should be large enough to minimize power drain from the battery, but small enough to prevent the input resistance of PDETECT from affecting the threshold battery voltage significantly. If low battery indication is active before attempting to power on the system, the PWRC block is disabled and the system will not turn on until batteries are replaced. If low battery is activated during system operation, an interrupt is issued and the software will execute a power down routine.

A capacitor must also be connected from PDETECT to ground, to provide an RC delay of the voltage on PDETECT when the battery is inserted. This ensures that the comparator output will initially be low and clear the flip-flops. This is the only way to ensure that the flip-flops will be initialized in the correct state. The delay should be at least 2ms measured from the time VDDPWR reaches its minimum power-up voltage until PDETECT reaches the internal reference voltage.

5.15.2 POWER CYCLE

The system power ON time starts at the rising edge of at least one of the PWRON[2:0] inputs only if the battery voltage meets system requirements (see the previous section, 揚DETECT?on page 5-13). The system power switch should be momentary type, generating a pulse at power on and another pulse at power off. The PWRON[2:0] pins are connected in a wired "OR" configuration. The COACH can identify and store the source of power from each PWRON[2:0] pin. The PWRENB output is used to enable the system DC/DC converters. PWRENB is initially driven from VDDPWR and subsequently driven from VDDP (minus a diode voltage drop). This keeps the PWRENB voltage above the threshold voltage of the DC/DC converter and enables input during low battery voltage conditions. After boot, the COACH software takes control of the PWRC system functions and periodically monitors each PWRON[2:0] pin to detect a power off condition which occurs when all PWRON[2:0] pins are low. At this time, the software will execute a power down routine.

5.15.3 POWER SEQUENCE

The required power-up sequence is VDDRAM first, VDDCORE second, and finally VDDP. Note that if VDDCORE reaches the operating range while VDDP is still below 1V, there may be a glitch on some pins. If the system design is susceptible to glitches on some of the I/O (typically, FLSHTRIG is particularly sensitive to a glitch on power-up), it is recommended to install Schottky diode D2. This will cause VDDP to initially track VDDCORE and prevent glitches. If the power supply applies VDDCORE before VDDRAM and this sequence cannot be modified, it is recommended to include Schottky diode D1 connected as shown in Figure 5-10, *Power Supply Diodes*. This will force VDDCORE to pull up VDDRAM along with it, minus a diode drop.

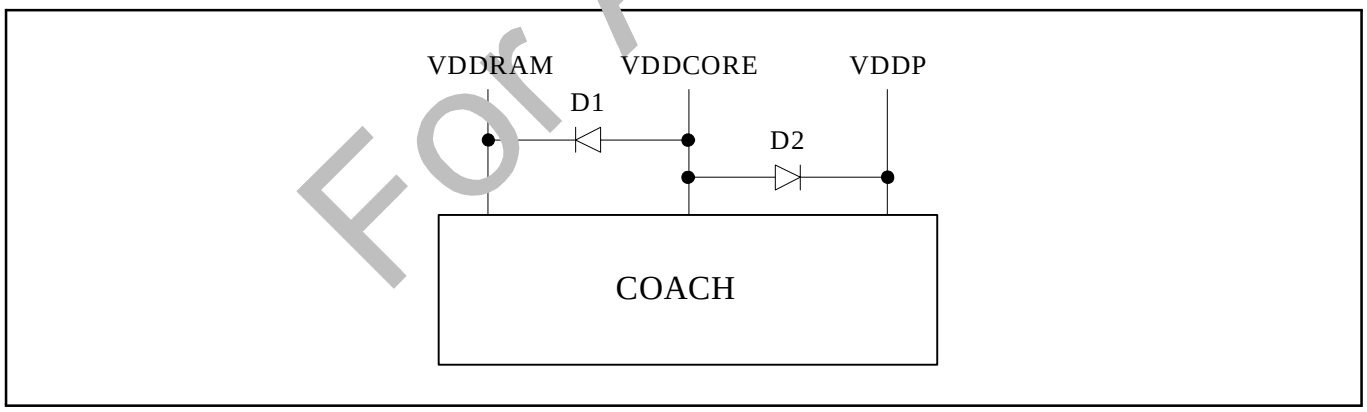

Figure 5-10: *Power Supply Diodes*

5.15.4 RESET

The PWRC asserts RESET# on the rising edge of any one of the first PWRON[2:0] signals for a duration of 0.2ms in order to guarantee the COACH wakes up in a known state. If a second PWRON[2:0] signal is subsequently activated, the RESET# is not asserted because the system is already active. An external RC delay

circuit should be connected to RESET# to ensure the COACH remains in a reset state until all power supplies settle to their final value.

5.16 EJTAG

The COACH supports a four pin version of the EJTAG interface defined in IEEE 1149.1 JTAG and referenced as a Test Access Port (TAP). he controller reset pin (TRST) is not used in this implementation; instead, a power up reset of the TAP provides reset functionality. This interface is a serial communications channel with frequencies up to 40MHz on EJTCK. The TAP controller uses the mode select (EJTMS) pin, which determines if instruction or data registers should be accessed in the EJTDI and EJTDO data path. EJTCK is independent of all other COACH clocks. EJTMS and EJTDI are sampled on the rising edge of EJTCK, while EJTDO is sampled on the falling edge. The COACH implementation meets all relevant AC/DC characteristics defined in the EJTAG specification.

When a system is designed to implement the EJTAG interface, strong pull-up resistors must be connected to all TAP lines. The recommended value is 1.0K Ω. A series resistor for EJTDO should be installed and adjusted to the specific design. A typical value for this is 33 Ω. For production designs that do not require EJTAG implementation, a pull-up resistor is only required on EJTCK since the other inputs, EJTMS and EJTDI, have permanent internal weak pull-ups.

5.17 ADC

The COACH has an integral eight input multiplexed 12-bit SAR ADC as illustrated in Figure 5-11, *ADC Interface*. The clock is programmable up to 2MHz and each conversion requires 26 clock cycles, producing a maximum sampling rate of 76.92KHz. The full scale input voltage range is 0 to VDDADC and the ADC reference voltage is also the power supply input, VDDADC. Three inputs are connected to external pins, one input internally connected to PDETECT to measure battery voltage, one input internally connected to the video DAC reference, one input connected to VDDADC and the remaining two connected to ground. All eight inputs can be individually enabled or disabled. The ADC can operate as a ratiometric ADC, returning a digitized value proportional to the ratio of input voltage and reference voltage or it can use VDACREF as an absolute reference to calibrate the ADC.

The ADC can operate in two modes: single-channel or multi-channel. In single-channel mode, only one input is sampled each conversion cycle. In multi-channel mode, the enabled inputs are scanned in a circular order at a programmable interval between conversions and programmable starting channel. Prompted by an end of conversion (EOC) interrupt, the CPU reads the digital value after every conversion. The ADC block can be disabled by software for power savings.

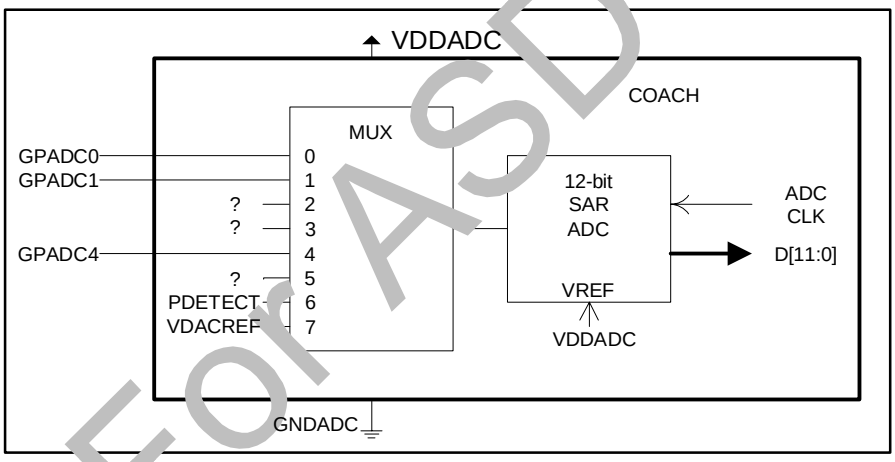

Figure 5-11: *ADC Interface*

5.18 LMC

The Lens Motor Controller (LMC) drives four separate ports, each port having four outputs, with only one port active at a time. Most lens assemblies have integral motors for zoom, auto focus (AF), shutter, and iris. The LMC is a versatile, programmable interface for the system designer to drive these various types of motors.

5.18.1 ARCHITECTURE

The COACH has four programmable ports, designated M1 through M4. Each port has four outputs designated A, B, C, and D, as shown in Figure 5-12, *LMC Port Outputs*. The LMC clock frequency is 100KHz. Each output, A through D, is driven by an 8-bit circular shift register (ring counter) that shifts to the left. The user can preset all 8 bits of each of the four shift registers to generate an 8-bit event sequence with 0.01ms resolution. This sequence can be repeated up to 4096 times (2^12). The user can choose to drive all outputs low at the end of a sequence, or remain in their final programmed state. The LMC can also generate an interrupt at the end of each sequence or end of each step. When motor timing is not critical, software can activate the LMC sequencer. In critical timing situations, an integral hardware timing generator can activate the sequencer.

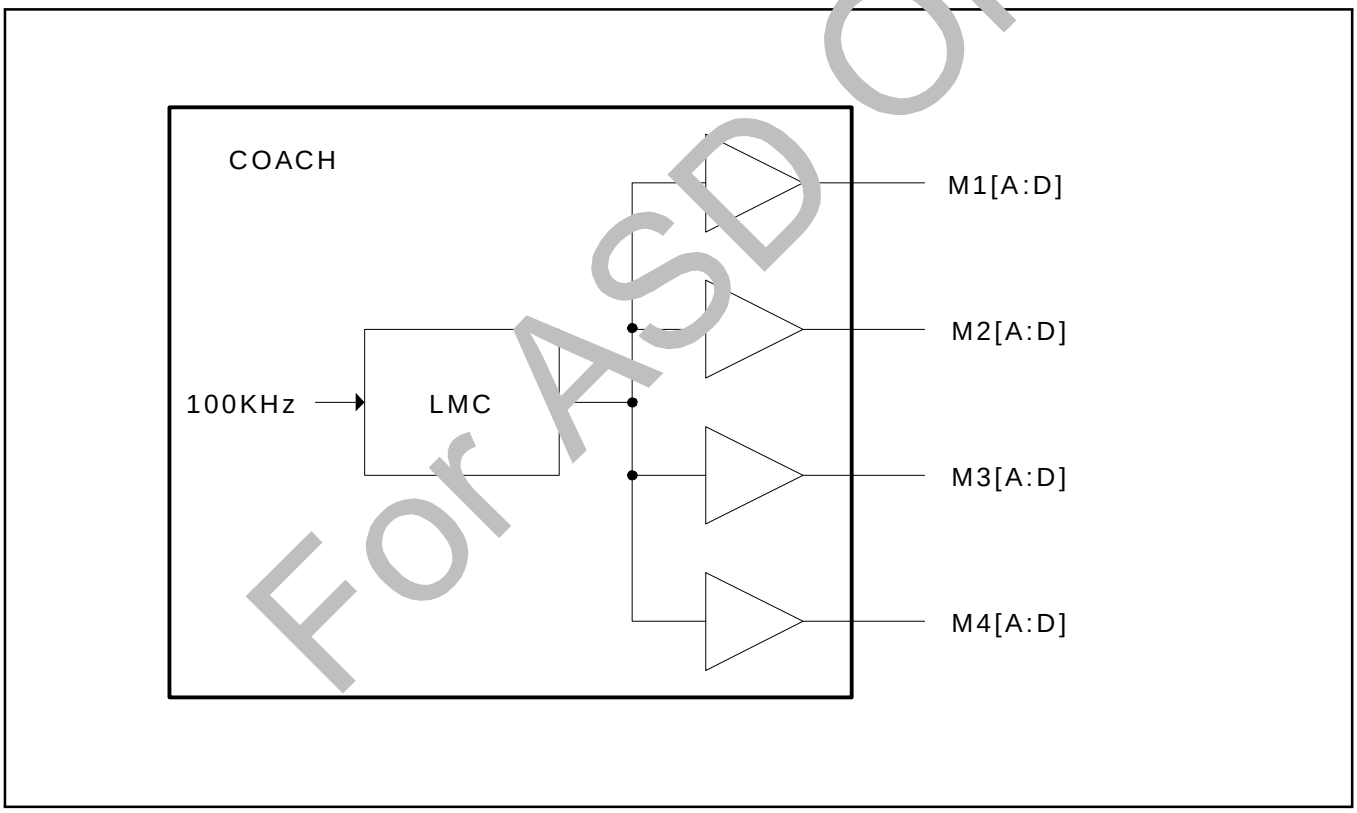

Figure 5-12: *LMC Port Outputs*

5.18.2 MOTOR CONTROL

The LMC digital outputs and programmable sequence make the interface ideal for driving stepper motors. Since these motors require currents larger than what the COACH digital outputs can provide, a current booster IC (usually a group of H-bridge networks) should be connected between the LMC outputs and the motors.

Typical zoom motors are DC type with an integral encoder. DC type motors have significant delays in their response, so the encoder provides a means to determine exact motor position at all times. A home position signal generated from an integral optocoupler provides a reference position and the number of pulses from the encoder determines how much the motor has turned. The XLGPIO1 pin was specifically designed with a counter for this purpose.

5.19 GPIO

Most COACH pins can be programmed as functional or General Purpose I/O (GPIO) as described in Chapter 4, 揾n Functions". The COACH also features dedicated GPIO pins, designated XLGPIO. There are four of these, XLGPIO [4], XLGPIO [2:0]. A counter is connected to XLGPIO1 to facilitate recording the number of pulses from a lens zoom motor encoder. It can operate up to and is synchronous to the COACH 108MHz clock. Almost all GPIO can be independently programmed to operate as input or output. A pin assigned to output direction can be set to "1" or "0" during operation. Many GPIO are capable of generating an interrupt, as shown in Chapter 4.

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5.20 GENERAL SERIAL INTERFACE (GSI)

The GSI can be used to implement up to two independent bidirectional serial communication channels. The six GSI pins are shared with PWM and Lens motor pins with the following mapping: GSI[5:0] = {PWM[7:6], M4[D:A]}. Thus each of these pins can be configured in one of 3 ways: as a GSIU pin, as a PWM or lens motor controller pin, or as a GPIO. The interface is supported by dedicated hardware consisting of shift registers, clock generators and associated control logic, to minimize software load.

Two independent serial protocols are supported simultaneously by two internal clock generator circuits connected to the GSI[5:4] I/O pins. The flexible clock circuits support multiple speeds up to 6.75MHz, clock stretching, clock polarity selection, and an external clock input option. The clock generators can generate clock frequencies that are 108MHz divided by a power of 2 from 2^4 to 2^{16}. Clock polarity is programmable in master mode (internal clock) and slave mode (external clock). The number of sequential clock cycles generated for each transmission is programmable up to a maximum of 63 cycles. Clock stretching by increasing the low period of the clock is supported in master and slave modes. The master can slow down the clock to accommodate slow slaves, and the slave device can hold the clock line low when performing other functions. When clock stretching is enabled in master mode the clock pin is either driven low or released (set to high impedance), rather than driven high. If clock stretching is used in slave mode, the bus master must drive the clock line low for at least one clock cycle. Only positive clock polarity is supported with clock stretching enabled.

Each of four bidirectional data I/O signals (GSI[3:0]) can be configured to sample on either one of the two clocks, each with programmable edge polarity in little-endian or big-endian sequence. The GSI can support several configurations such as: two independent channels with separate clocks, two independent channels sharing a clock, and a single channel configuration. The GSI port also supports interrupts for notification of external device requests on all the pins, as well as a number of internal events.

The GSI control hardware has power management with a sleep timer-counter and wake-on-event capabilities. The 12 bit counter can be used either as a sleep timer, in which case the GSI clock is stopped until a specified event occurs, or as a general purpose timer having no effect on the GSI clock. Events can be ANDed or ORed with each other and the result can be ANDed or ORed with a counter time out event.

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CHAPTER 6 AC/DC CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed under 撇bsolute Maximum Ratings?may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. All voltages are with respect to their corresponding grounds as mentioned in the list. Current out of a terminal is given as a negative value in all tables.

Table 6-1: Absolute Maximum Ratings

Parameter	Min	Max	Units
Operating Temperature	0	+70	癈
Storage Temperature	-65	+150	癈
VDDP to GND	-0.5	4.6	V
VDDCORE to GND	-0.5	3.6	V
VDDRAM to GND	-0.5	4.6	V
RAMVREF to GND	-0.5	4.6	V
VDDDAC to GNDDAC	-0.5	4.6	V
VDDAUD to GNDAUD	-0.5	4.6	V
VDDSPKR to GNDSPKR	-0.5	4.6	V
VDDUSB to GNDUSB	-0.5	4.6	V
VDDUSBPLL to GNDUSBPLL	-0.5	3.6	V
USBVBUS to GNDUSB	-0.5	6.6	V
VDDPLL to GNDPLL	-0.5	3.6	V
VDDPWR to GNDPWR	-0.5	4.6	V
VDDADC to GNDADC	-0.5	4.6	V
DC INPUT VOLTAGE	-0.5	VDDx + 0.3	V
DC INPUT CURRENT	-10	3	mA

Table 6-1: Absolute Maximum Ratings *(continued)*

Parameter	Min	Max	Units
DC OUTPUT CURRENT	-10	20 (total of 200)	mA
DC VOLTAGE into high Z OUTPUT - NON DDR signals	-0.5	VDDx + 0.3	V
DC VOLTAGE into high Z OUTPUT - DDR signals	-0.5	VDDRAM + 0.3	V

Table Notes:

1. VDDx is the actual supply voltage of a particular block associated with the specific input. For instance, the absolute maximum voltage on any ADC input pin is VDDADC + 0.3V, where VDDADC is the actual voltage on VDDADC.

6.2 RECOMMENDED OPERATING CONDITIONS

Table 6-2: Recommended Operating Conditions

Parameter	Min	Nom	Max	Units
VDDP[1]	3.135	3.300	3.465	V
VDDDAC, VDDAUD, VDDSPKR, VDDUSB, VDDADC	3.135	3.300	3.465	V
VDDCORE , VDDPLL[2], VDDUSBPLL[2]	1.71	1.80	1.89	V
VDDRAM	2.375	2.500	2.625	V
RAMVREF	0.49*VDDRAM	0.5*VDDRAM	0.51*VDDRAM	V
USBVBUS	4.40	5.00	5.25	V
VDDPWR[3]	1.9		3.6	V
GNDPWR, GNDDAC, GNDAUD, GNDSPKR, GNDUSB, GNDUSBPLL, GNDPLL, GNDADC, to GND	0	0	0	V

Table Notes:

1. Each voltage is referenced to its dedicated ground pin. For example, VDDDAC voltage is referenced to GNDDAC.
2. PLL circuits are extremely susceptible to power supply ripple. The maximum allowable power supply ripple is 1% for 1 Hz to 5 KHz; 1.5% for 5 KHz to 10 MHz; 3% for 10 MHz to 100 MHz; and 5% for 100 MHz or

greater.

3. VDDPWR minimum level is required to turn the COACH on, but VDDPWR can decrease to 1.5V during operation. Refer to Section 6.6, 揧WRC and RTC,?on page 6-5.

6.3 DIGITAL I/O ELECTRICAL CHARACTERISTICS

These are the DC characteristics of the digital I/Os that are powered by VDDP, that is, all digital I/Os with the exception of the DDR interface.

Table 6-3: Digital I/O Electrical Characteristics

VDDCORE=1.80V +/-5%, VDDP=3.3V +/-5%, T_A=+25癈

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input low voltage	VIL			0.8	V	
Input high voltage	VIH	2.0			V	
Low-level output voltage	VOL			0.4	V	IOUT=+10mA
High-level output voltage	VOH	2.4			V	IOUT=-10mA
Input hysteresis voltage	VHYS	0.15			V	
Input leakage current	ILK	-10		+10	uA	Internal PU and PD disconnected
Internal PU current	IOH			200	uA	VIN=0.8V
Internal PD current	IOL			200	uA	VIN=2.0V
Input capacitance	CIN		5		pF	

6.4 POWER CONSUMPTION

TBD

6.4.1 FUNCTIONAL UNIT POWER CONSUMPTION

TBD

6.5 CLOCK GENERATOR UNIT (CGU)

6.5.1 MAIN CLOCK OSCILLATOR

The internal main clock oscillator circuit operates at 12 MHz and is always enabled following a chip reset. It can be driven from either a crystal or an oscillator. A crystal is connected between VCLKI and VCLKO as shown in Figure 6-1, *Main Clock Oscillator with External Crystal* and should meet the requirements of Table 6-4 (*Recommended Main Crystal Parameters)*. The crystal must operate in fundamental mode. Capacitors C1 and C2 should be equal in value and chosen to satisfy the equation below, where CL is the load capacitance specified in Table 6-4. When an oscillator is used to drive the clock circuit, connect the oscillator output to VCLKI and leave VCLKO open circuit. The oscillator should meet the frequency specifications of Table 6-4 and interface requirements of COACH-9e.

$$CL = \frac{C_1 C_2}{C_1 + C_2}$$

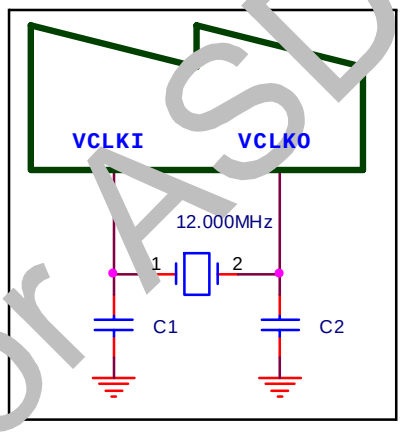

Figure 6-1: *Main Clock Oscillator with External Crystal*

Table 6-4: Recommended Main Crystal Parameters

PARAMETER/CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
Frequency of oscillation	f_0		12.000		MHz
Frequency tolerance	$\Delta f/f$	-30		+30	ppm
Series resistance	ESR			40	Ω
Load capacitance	C_L			16	pF
Shunt capacitance	C_o			7	pF

6.6 PWRC AND RTC

6.6.1 PWRC

Table 6-5: PWRC Characteristics

T_A=+25癈

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
VDDPWR Power Up Voltage	1.9		3.6	V	Start up voltage range. See note 1.
VDDPWR Operating Voltage	1.45		3.6	V	Operating voltage range. See note 1.
RESET# Voltage			VDDP	V	
RESET# Resistance	10			MΩ	
RESET# Hysteresis	150			mV	VDDPWR = 3.3V See note 2.
RESET# minimum pulse duration	15			us	
PDETECT Voltage			<VDDPWR	V	
PDETECT Resistance	10			MΩ	
PDETECT High Threshold	1.22		1.25	V	VDDPWR=1.5
	1.21		1.26		VDDPWR=3.0
	1.21		1.28		VDDPWR=3.6
PDETECT Low Threshold	1.18		1.21	V	VDDPWR=1.5
	1.18		1.21		VDDPWR=3.0
	1.19		1.21		VDDPWR=3.6

Table 6-5: PWRC Characteristics

T_A=+25癈

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
PDETECT Hysteresis	30		50	mV	VDDPWR=1.5
	30		50		VDDPWR=3.0
	30		60		VDDPWR=3.6
PWRON Voltage			VDDPWR	V	
PWRON Resistance	10			MΩ	
PWRON Hysteresis	150			mV	
PWRON to PWRENB delay	20			ns	
PWRENB Voltage			VDDPWR	V	

Table Notes:

1. This is the VDDPWR voltage range for which PWRON, PWRENB, PDETECT, RESET#, and the PWRC unit digital interfaces to the core maintain normal operation.
2. Hysteresis voltage varies with VDDPWR.

6.6.2 REAL TIME CLOCK (RTC)

The RTC oscillator circuit operates at 32.768 KHz. It can be driven from either a crystal or an oscillator. A crystal is connected between RTCXI and RTCXO as shown in Figure 6-2, *RTC Oscillator with External Crystal* and should meet the requirements of Table 6-6 (*Recommended RTC Crystal Parameters)*. The crystal must operate in fundamental mode. Capacitors C1 and C2 should be equal in value and chosen to satisfy the equation below, where CL is the load capacitance specified in Table 6-6. When an oscillator is used to drive the clock circuit, connect the oscillator output to RTCI and leave RTCO open circuit. The oscillator should meet the frequency specifications of Table 6-6 and interface requirements of COACH-9e.

$$CL = \frac{C_1 C_2}{C_1 + C_2}$$

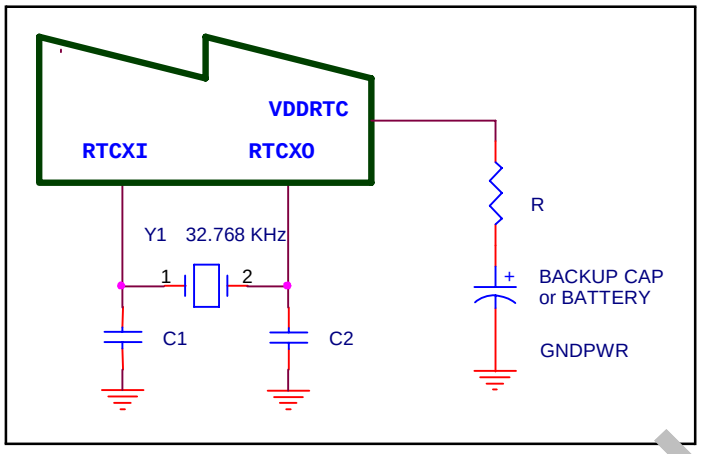

Figure 6-2: *RTC Oscillator with External Crystal*

Table 6-6: Recommended RTC Crystal Parameters

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS
Frequency of oscillation	f_0		32.768		KHz
Series resistance	ESR	30		60	KΩ
Load capacitance	CL		12.5		pF
Drive level	DL			1	µW

Table 6-7: RTC Characteristics

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
VDDRTC Voltage	1.5		3.6	V	
VDDRTC Current			2.0	µA	VDDPWR = VDDP= 0V (Battery disconnected)

6.7 DDR CONTROLLER

6.7.1 DDR CONTROLLER OUTPUT TIMING CHARACTERISTICS

The DDR-SDRAM memory controller is designed to meet the timing constraints of all JEDEC compliant DDR memory chips. Parameters that control specific DDR memory devices can be adjusted by the user through

configuration settings in the DDR initialization file. The remaining timing specifications required to generate a DDR write timing budget are defined in Table 6-8.

Table 6-8: DDR Controller Output Timing Characteristics

RAMCLK=108 MHz, VDDCORE=1.80V +/-5%, VDDP=3.3V +/-5%, T_A=+25癈

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RAMCLK to Address delay	tCA	1.2		7.5	ns	
RAMCLK to Control delay	tCC	1.2		7.5	ns	
Data and Mask to Strobe setup time	tDQS	0.7			ns	1
Data and Mask to Strobe hold time	tDQH	0.8			ns	2

Table Notes:

1. This is the minimum amount of time the data (RAMDATx) or mask signal (RAMUDM/RAMLDM) will be valid before the data strobe (RAMUDS/RAMLDS) transitions during a DDR write cycle.
2. This is the minimum amount of time the data (RAMDATx) or mask signal (RAMUDM/RAMLDM) will remain valid after the data strobe (RAMUDS/RAMLDS) transitions during a DDR write cycle.
3. Timing data relative to RAMCLK is referenced to the crossing point of RAMCLK and RAMCLK#.
4. Timing data relative to RAMLDQS or RAMUDQS is referenced to the 50% edge level.

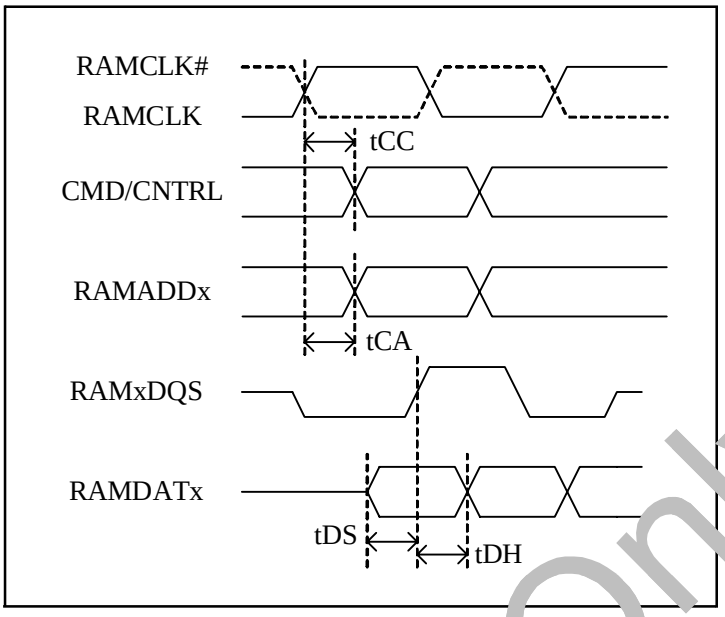

Figure 6-3: *DDR Timing Diagram*

6.8 USB CHARACTERISTICS

The USB interface is USB-IF certified for Full Speed and High Speed.

6.9 ASC

Table 6-9: ASC Characteristics

VDDCORE=1.80V +/-5%, VDDP, VDDAUD=3.3V +/-5%, T_A=+25癈, VCM, AREF load capacitance = 1礵

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Microphone Bias					
MICENB voltage		VDDAUD		V	
Microphone Preamp Input (MICP, MICN)					
Full-Scale Input Voltage at 0db gain		0.2		Vpp	Differential, Note1
High frequency filter response	100		200	KHz	-3dB
Input Resistance	10			KΩ	
Programmable Gain Amplifier (PGA)					
Gain range	-26		12	dB	
Gain step size		0.5		dB	

Table 6-9: ASC Characteristics *(continued)*

VDDCORE=1.80V +/-5%, VDDP, VDDAUD=3.3V +/-5%, T_A=+25癈, VCM, AREF load capacitance = 1礵

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Automatic Level Control (ALC)					
Programmable Gain	0		12	dB	
Programmable Gain step size		3		dB	
Ramp-up time	0.003		24.576	s	Note 2
Ramp-down time	0.003		24.576	s	Note 2
Hold time	0.0026		87.4906	s	Note 3
Noise gate threshold		-63		dBFS	
Output Path (DAC) : 0 dBFS input level, 0 dB gain, unless otherwise specified					
Speaker Output (SPKRP, SPKRN with 8Ω bridge tied load)					
Low voltage setting		2.00		Vpp	Differential, Note 4
Midrange voltage setting		2.25		Vpp	differential
High voltage setting		2.50		Vpp	differential
Total Harmonic Distortion (THD)		-73	-58	dB	-2 dBFS, 1 KHz
Signal to Noise Ratio (SNR)	64			dB	
Load Resistance		8		Ω	
Load Capacitance			20	pF	
Headphone Output (See Fig. 5-64 for load circuit, data is for both channels)					
Output Voltage		2.00		Vpp	
Total Harmonic Distortion (THD)		-68	-63	dB	-2 dBFS, 1 KHz
Signal to Noise Ratio (SNR)	64			dB	
Load Resistance		16		Ω	
Load Capacitance					Fig. 5-64
Line Output (R_L=10KΩ)					
Output Voltage		2.00		Vpp	
Total Harmonic Distortion (THD)		-78	-61	dB	-1 dBFS, 1 KHz
Signal to Noise Ratio (SNR)	79	80		dB	

Table 6-9: ASC Characteristics *(continued)*

VDDCORE=1.80V +/-5%, VDDP, VDDAUD=3.3V +/-5%, T_A=+25癈, VCM, AREF load capacitance = 1礵

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Load Resistance		10		KΩ	
Load Capacitance			20	pF	
Input Path (ADC) : 0dBFS input level, 0dB gain					
Total Harmonic Distortion (THD)		-71		dB	
Signal to Noise Ratio (SNR)	78.5	79		dB	
Digital Filter (fs=44.1KHz)					
Passband Ripple	-0.1		0.1	dB	
Lower passband			20	Hz	+/-0.1dB, Note 5
Upper passband	20			KHz	+/-0.1dB, Note 5
Passband linear phase deviation					
20Hz to 100Hz			5		degrees
10Hz to 1KHz			1		degrees
1KHz to 20KHz			0.1		degrees
Stopband			24.1	KHz	
Stopband attenuation	65			dB	

Table Notes:

1. Full-Scale input voltage is proportional to VDDAUD.
2. Ramp-up and Ramp-down times are defined as the time it takes the PGA to sweep 90% of its gain range.
3. Hold time is the time between detecting a signal as too quiet and the start of a gain increase.
4. Maximum output voltages for speaker, headphone, and line are proportional to VDDSPKR.
5. The passband and stopband frequencies scale with fs (sample rate).
6. THD, SNR and Output Power are verified with characterization data. All other parameters are guaranteed by design

6.10 TV MONITOR

Table 6-10: TV Monitor Characteristics

T_A=+25癈

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Differential Gain	DG			4	%	
Differential Phase	DP			4		
Luminance non-linearity	LNL			5	%	
Luminance noise	LN			-55	dB	
Chrominance AM noise	CAN			-55	dB	
Chrominance PM noise	CPN			-50	dB	

6.11 LCD CONTROLLER

The LCD controller is designed to meet the timing constraints of most direct digital interface panels. Parameters that control specific LCD devices can be adjusted by the user through software configuration settings. The remaining timing specifications required to generate a LCD timing budget are defined in Table 6-11.

Table 6-11: LCD Controller Output Timing Characteristics

VDDCORE=1.80V +/-5%, VDDP=3.3V +/-5%, T_A=+25癈

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock frequency	fCLK	3		27	MHz	
DVCLK duty cycle		47	50	53	%	
DVCLK to DVDAT/DVCNTL output delay	tDLY	-5	0	5	ns	1

Table Notes:

1. Timing is referenced to the user-specified active edge.

The figure below shows the most commonly used case, where data and control signals are synchronized to the falling edge of the clock; typically, the LCD panel samples the signals on the rising edge of the clock.

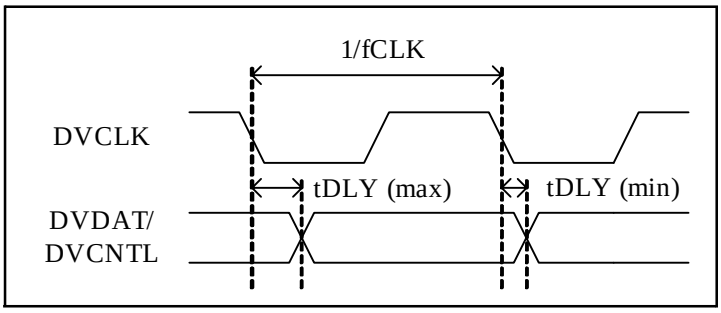

Figure 6-4: *LCD Controller Timing Diagram*

6.12 CCD TIMING

6.12.1 CCD TIMING CHARACTERISTICS

Table 6-12: CCD Timing Characteristics

VDDCORE=1.80V +/-5%, VDDP=3.3V +/-5%, T_A=+25癈

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CCLKOUT frequency	fCCLK	10		80	MHz	
CCLK Period	tCCD1	12.5		100	ns	
HIS rising edge delay from active clock edge	tCCD2			12	ns	Master mode
HIS falling edge delay from active clock edge	tCCD3			13	ns	Master mode
VIS rising edge delay from active clock edge	tCCD4			11	ns	Master mode
VIS falling edge delay from active clock edge	tCCD5			11	ns	Master mode
VIDx setup time on rising clock edge	tCCD6	5			ns	Master mode
VIDx setup time on falling clock edge	tCCD7	6			ns	Master mode
VIDx hold time on rising clock edge	tCCD8	5			ns	Master mode
VIDx hold time on falling clock edge	tCCD9	1			ns	Master mode
VIDx, HIS, VIS setup time on rising clock edge	tCCD10	2			ns	Slave mode
VIDx, HIS, VIS setup time on falling clock edge	tCCD11	5			ns	Slave mode
VIDx, HIS, VIS hold time on rising clock edge	tCCD12	5			ns	Slave mode

Table 6-12: CCD Timing Characteristics

VDDCORE=1.80V +/-5%, VDDP=3.3V +/-5%, T_A=+25癈

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
VIDx, HIS, VIS hold time on falling clock edge	tCCD13	1			ns	Slave mode

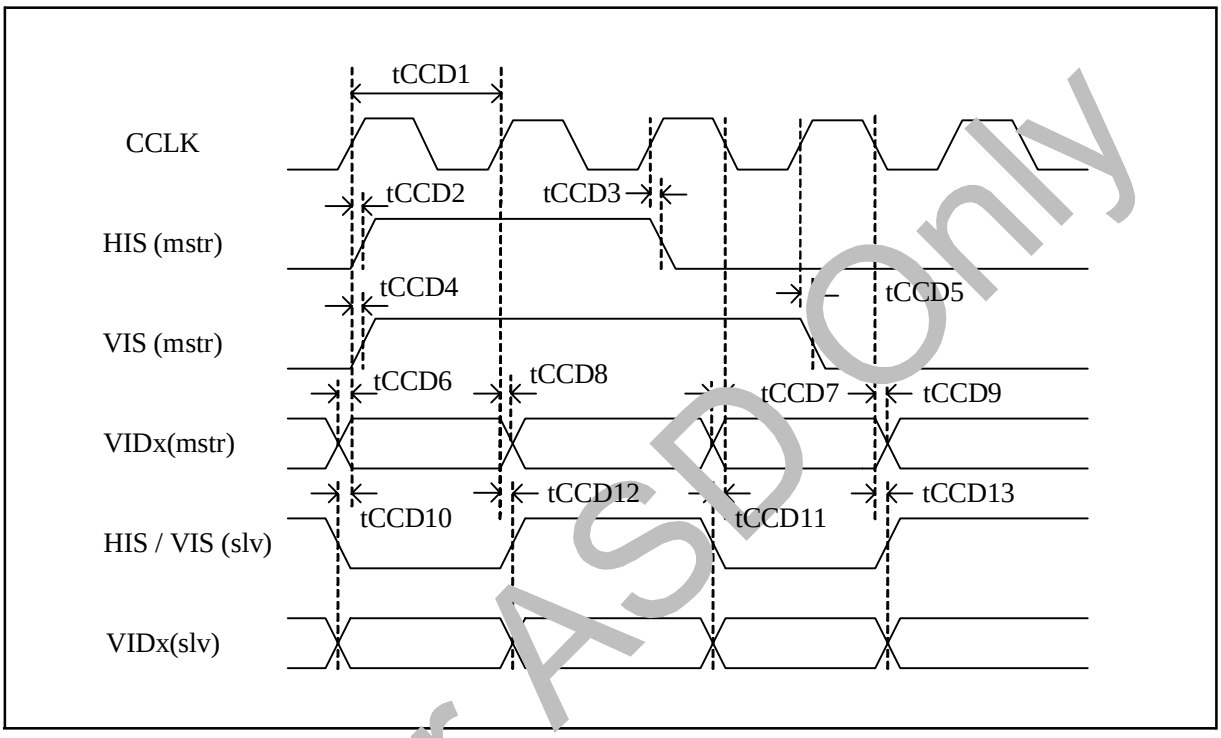

Figure 6-5: *CCD Timing Diagram*

6.13 GPIO TIMING

Table 6-13: GPIO Timing Characteristics

VDDCORE=1.80V +/-5%, VDDP=3.3V +/-5%, T_A=+25癈

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Rise Time	trGPIO			3.0	ns	
Fall Time	tfGPIO			3.0	ns	

6.14 SD TIMING CHARACTERISTICS

The frequency of the SD clock is programmable in the range 216 KHz ≤ f_{CLK} ≤ 21.6 MHz. The available frequencies in this range are expressed as 108/N MHz, where 5 ≤ N ≤ 500.

Table 6-14: SD Timing Characteristics

VDDCORE=1.80V +/-5%, VDDP=3.3V +/-5%, T_A=+25癈

SIGNAL	PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCL	Clock frequency in data transfer mode	fPP		21.6	21.6	MHz
	Clock frequency in identification mode	fOD		395		KHz
	Clock low time in data transfer mode	tWL	24	27		ns
	Clock high time in data transfer mode	tWH	16	19		ns
	Clock rise time	tTLH		2.5	5	ns
	Clock fall time	tTHL		2	5	ns
DATA/CMD	Input Setup time	tSU	5			ns
	Input Hold time	tH	5			ns
	Delay of DATA/CMD output from rising edge of COACH clock	tDLY	13.5	18.5	23.5	ns

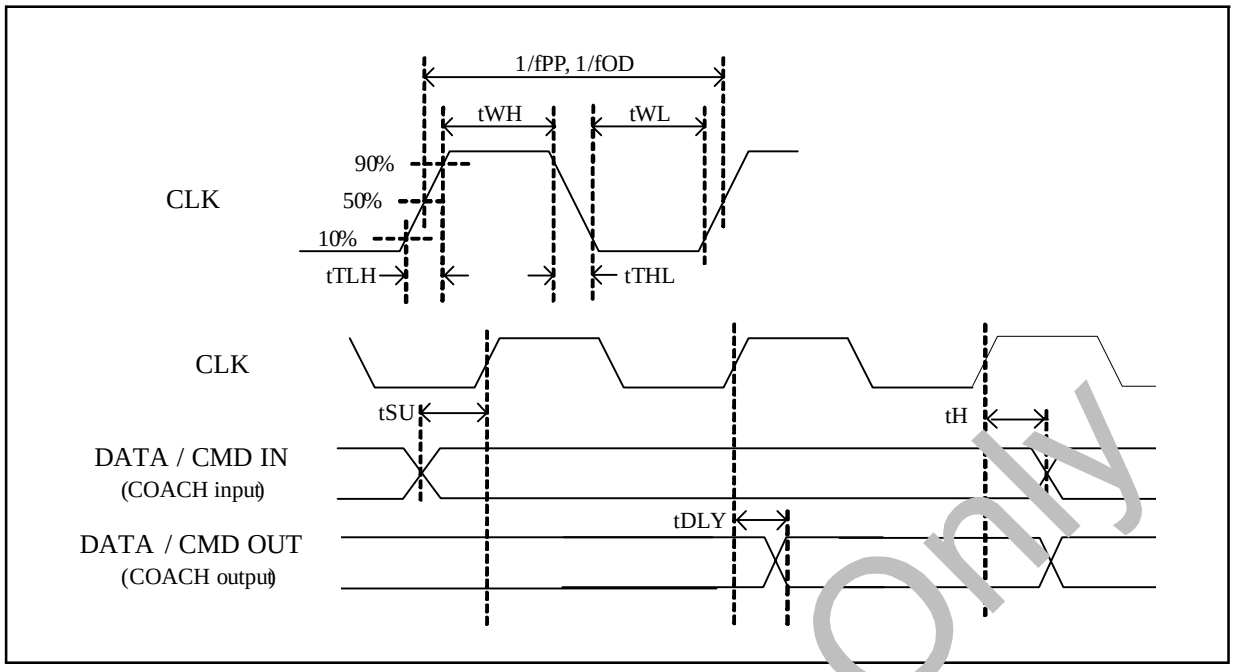

Figure 6-6: *SD Timing Diagram*

6.15 NAND FLASH TIMING CHARACTERISTICS

The timing data in this section pertains to reading of the NAND flash memory by the COACH hardware during Boot from NAND flash. Once the software has been booted, NAND flash accesses are controlled by COACHWare firmware and the timing can be modified to suit the system requirements.

Table 6-15 and <HotSpot>Figure 6-7 show the Command and Address Write. Table 6-16 and <HotSpot>Figure 6-8 show the Data Read.

Table 6-15: Command and Address Write

VDDCORE=1.80V +/-5%, VDDP=3.3V +/-5%, T_A=+25癈

TIME INTERVAL	DESCRIPTION	MIN	MAX	UNITS
1	Command Data to WE# falling edge	60		ns
2	CLE rising edge to WE# falling edge	40		ns
3	CE# falling edge to WE# falling edge	50		ns
4	WE# active width, command phase			
	"Fast" boot speed	50		ns
	"Slow" boot speed, or 2K page size	160		ns
5	WE# rising edge to ALE rising edge	60		ns

Table 6-15: Command and Address Write

VDDCORE=1.80V +/-5%, VDDP=3.3V +/-5%, T_A=+25癈

TIME INTERVAL	DESCRIPTION	MIN	MAX	UNITS
6	ALE rising edge to Data transition	60		ns
7	Data transition to WE# falling edge	5		ns
8	WE# rising edge to Data transition	60		ns
9	WE# recovery	70		ns
10	WE# rising edge to ALE falling edge	50		ns

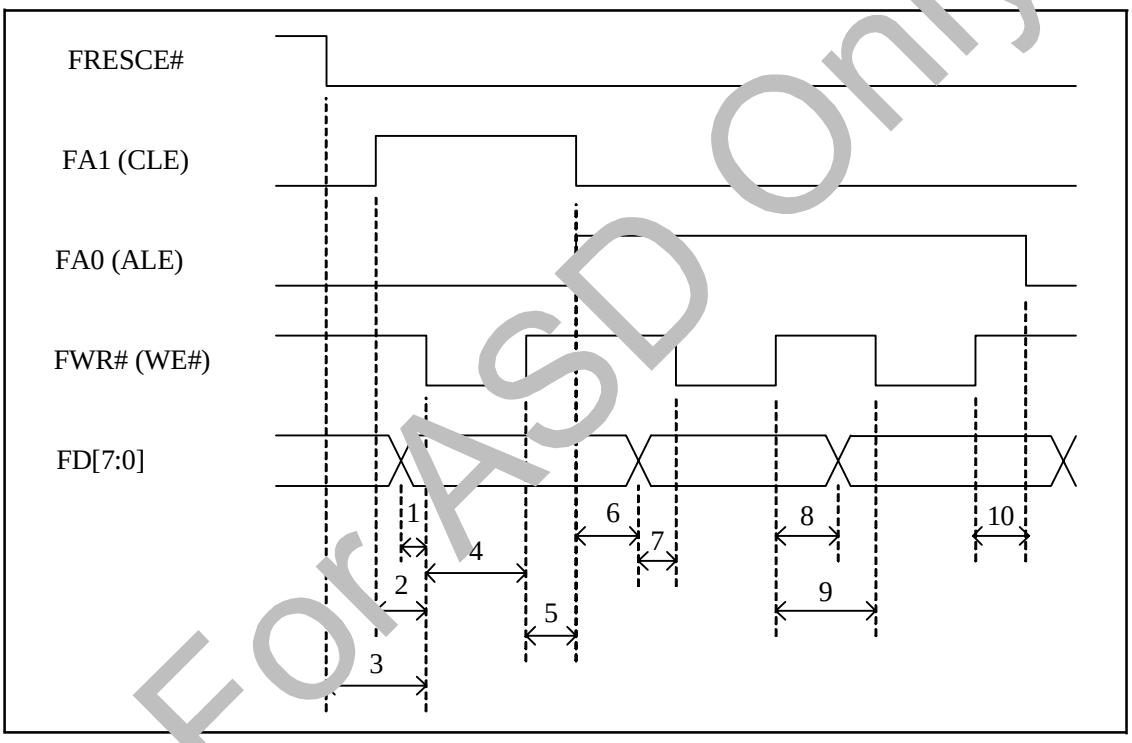

Figure 6-7: *Command and Address Write*

Table 6-16: Data Read

VDDCORE=1.80V +/-5%, VDDP=3.3V +/-5%, T_A=+25癈

TIME INTERVAL	DESCRIPTION	MIN	MAX	UNITS
11	RE# active width			
	"Fast" boot speed	50		ns

Table 6-16: Data Read

VDDCORE=1.80V +/-5%, VDDP=3.3V +/-5%, T_A=+25癈

TIME INTERVAL	DESCRIPTION	MIN	MAX	UNITS
	"Slow" boot speed, or 2K page size	125		ns
12	RE# recovery			
	"Fast" boot speed	15		ns
	"Slow" boot speed, or 2K page size	85		ns
13	Data input setup requirement	10		ns
14	Data input hold requirement	0		ns

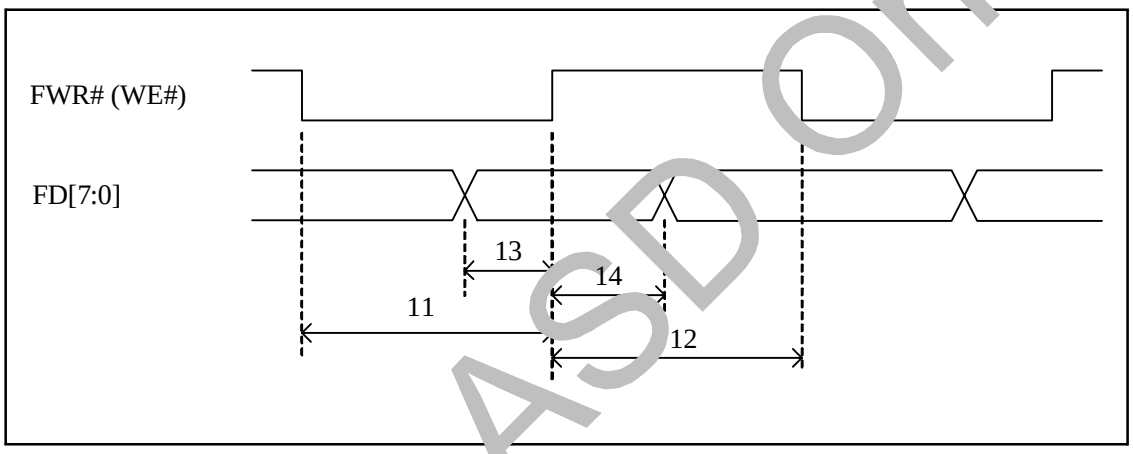

Figure 6-8: *Data Read*

6.16 Z^{2}C

Table 6-17 shows the Z^{2}C timing characteristics.

Table 6-17: Z^{2}C Timing Characteristics

VDDCORE=1.80V +/-5%, VDDP=3.3V +/-5%, T_A=+25癈

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock frequency in HW mode	fSCL	42.2		400	KHz	
SCL High Time			2/5		tSCL	1
SCL Low Time			3/5		tSCL	
Setup Time	tSU		1/5		tSCL	2

Table 6-17: Z^2C Timing Characteristics

VDDCORE=1.80V +/-5%, VDDP=3.3V +/-5%, T_A=+25癈

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Hold Time	tHD		1/5		tSCL	

Table Notes:

1. tSCL is one SCL clock cycle time.
2. Actual setup and hold times depend on pull up resistor value and the circuit capacitance.

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CHAPTER 7 PACKAGE SPECIFICATIONS

7.1 PACKAGE DIMENSIONS ? 293 BGA

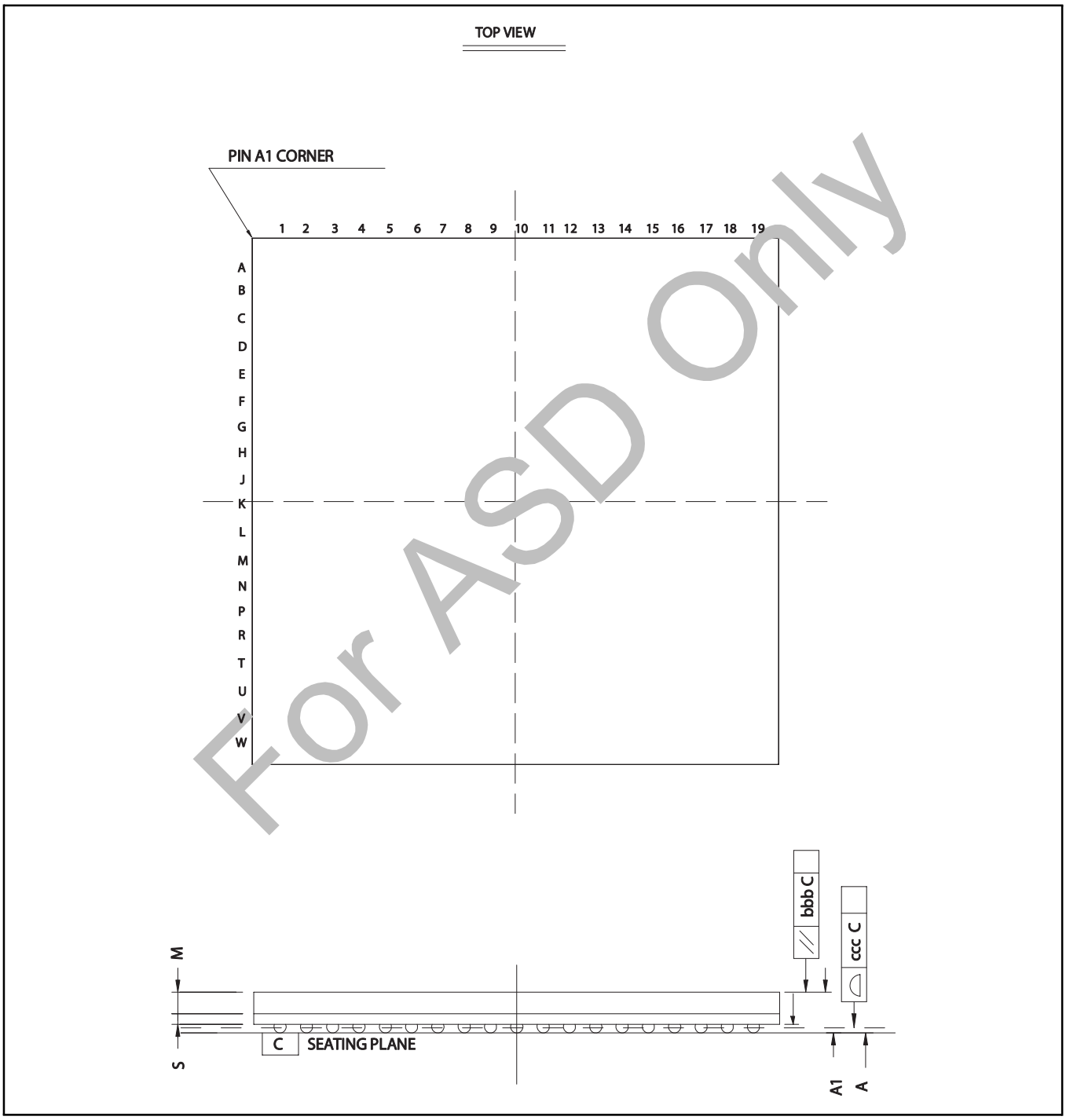

Figure 7-1: *Package Dimensions ? Top View*

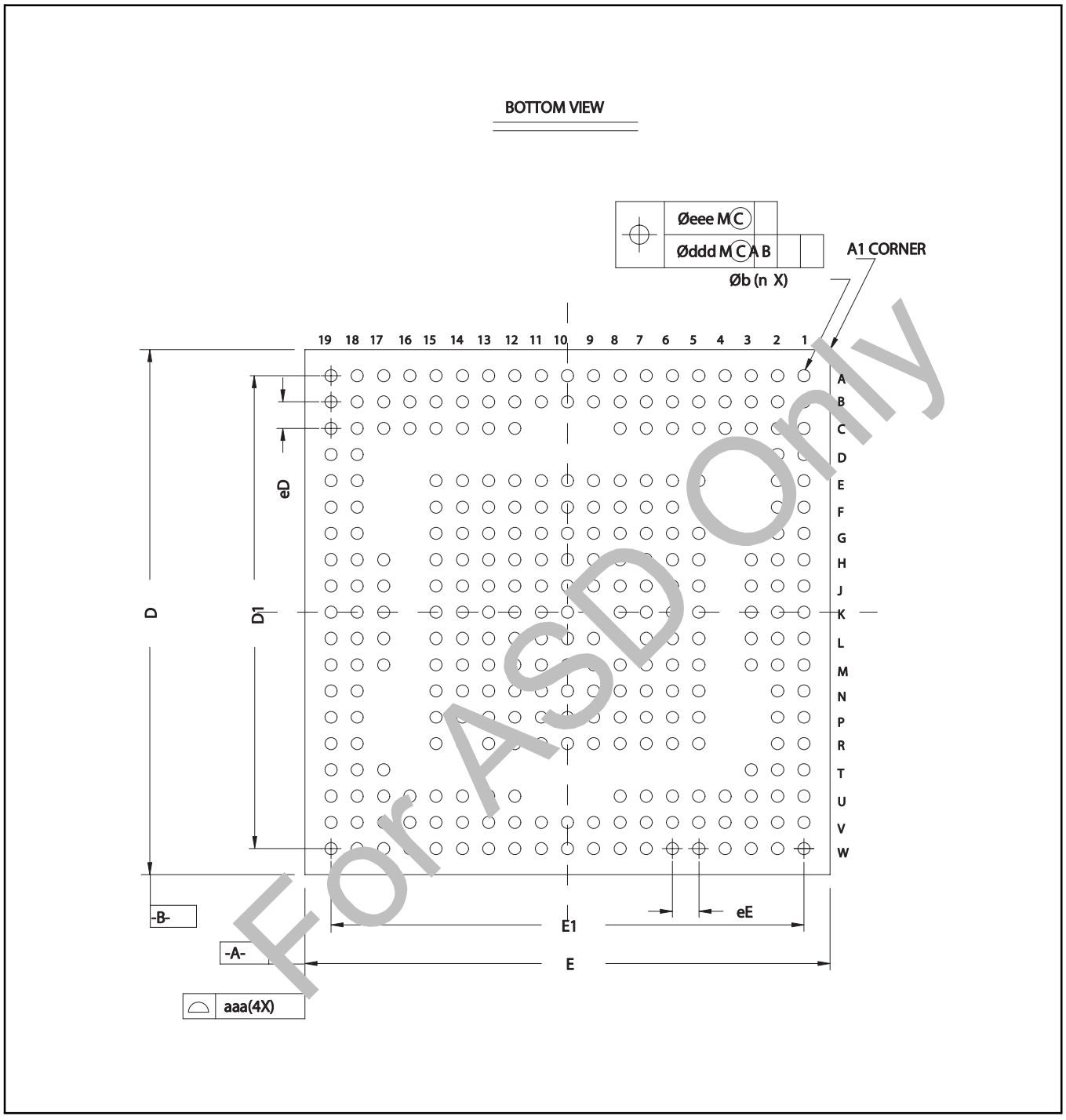

Figure 7-2: *Package Dimensions ? Bottom View*

Table 7-1: Package Dimensions

		Symbol	Common Dimensions
Package :			TFBGA
Body Size:	X	E	13.000
	Y	D	13.000
Ball Pitch :	X	eE	0.650
	Y	eD	0.650
Total Thickness :		A	1.200 MAX
Mold Thickness :		M	0.530 Ref.
Substrate Thickness :		S	0.260 Ref.
Ball Diameter :			0.300
Stand Off :		A1	0.160 ~ 0.260
Ball Width :		b	0.270 ~ 0.370
Package Edge Tolerance :		aaa	0.150
Mold Flatness :		bbb	0.200
Coplanarity:		ccc	0.080
Ball Offset (Package) :		ddd	0.150
Ball Offset (Ball) :		eee	0.080
Ball Count :		n	293
Edge Ball Center to Center :	X	E1	11.700
	Y	D1	11.700

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CHAPTER 8 REVISION HISTORY

8.1 REVISION HISTORY

Table 8-1: Revision History

Date	Section and Page Number	Change Description
12/07/2006	All Sections	Initial release
12/20/2006	various sections	corrected typos and changed page numbering to restart at 1 in every chapter.
02/20/2007	Section 4-9, 搭SB Port Interface (8 Pins),?on page 4-7	Changed USB RSET resistor to 6.19k
04/04/2007	Chapter 2, 揾unctional Overview,?on page 2-1	Changed CPU from 4kec to 4kem
04/04/2007	Figure 5.15.3, *Power Sequence*	Added power up sequence
04/04/2007	Figure 2.5, *Interface Features:*	Changed number of GPIO t0 over 100

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