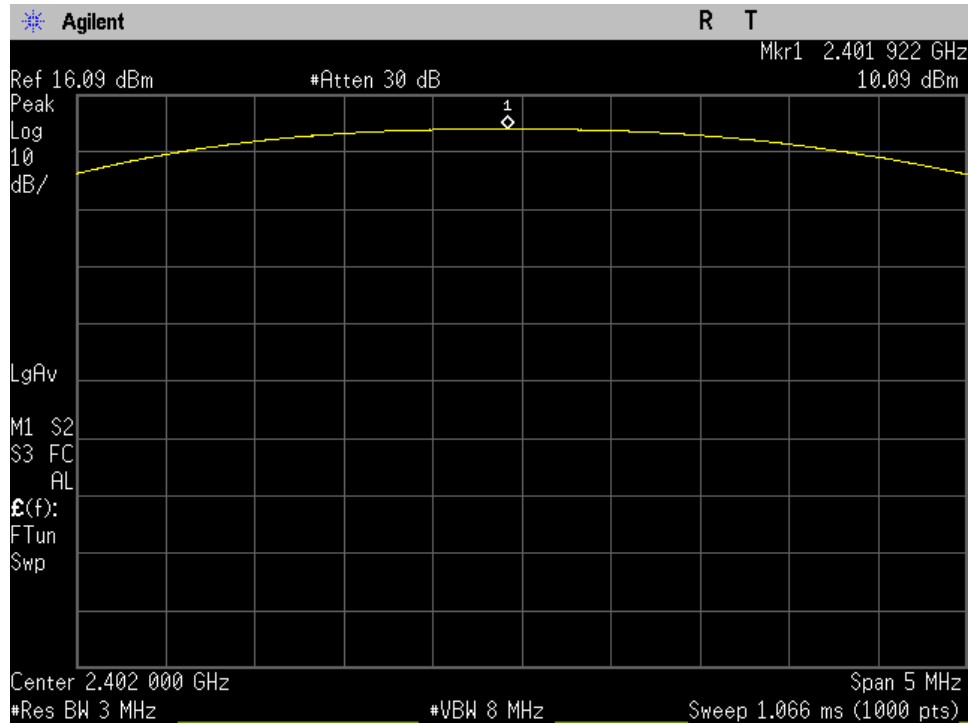


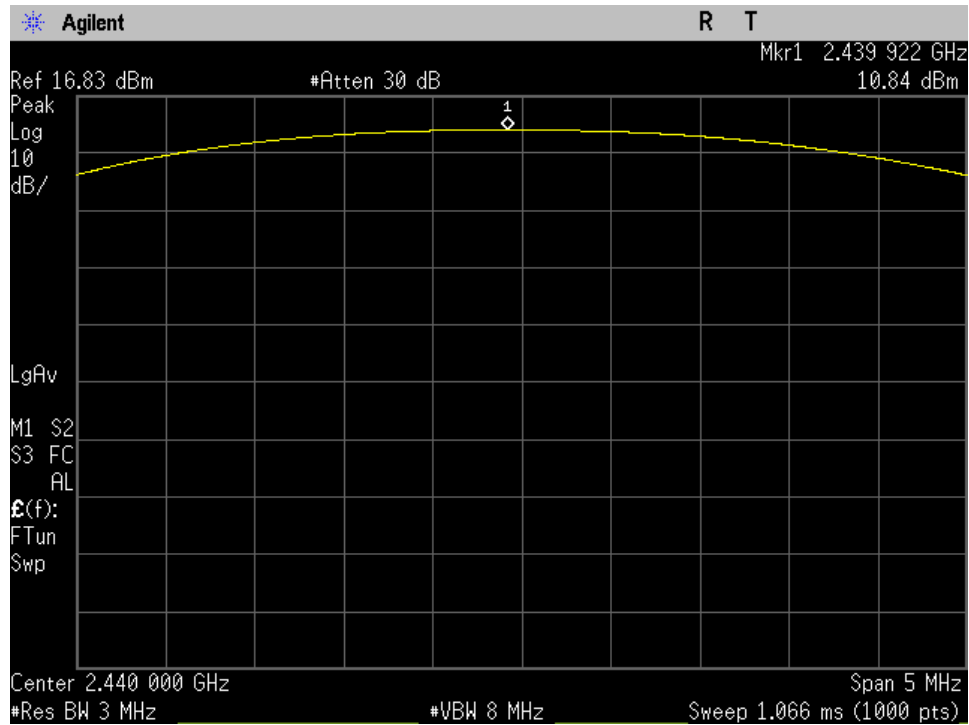
Annex B: Maximum Output Power

GFSK

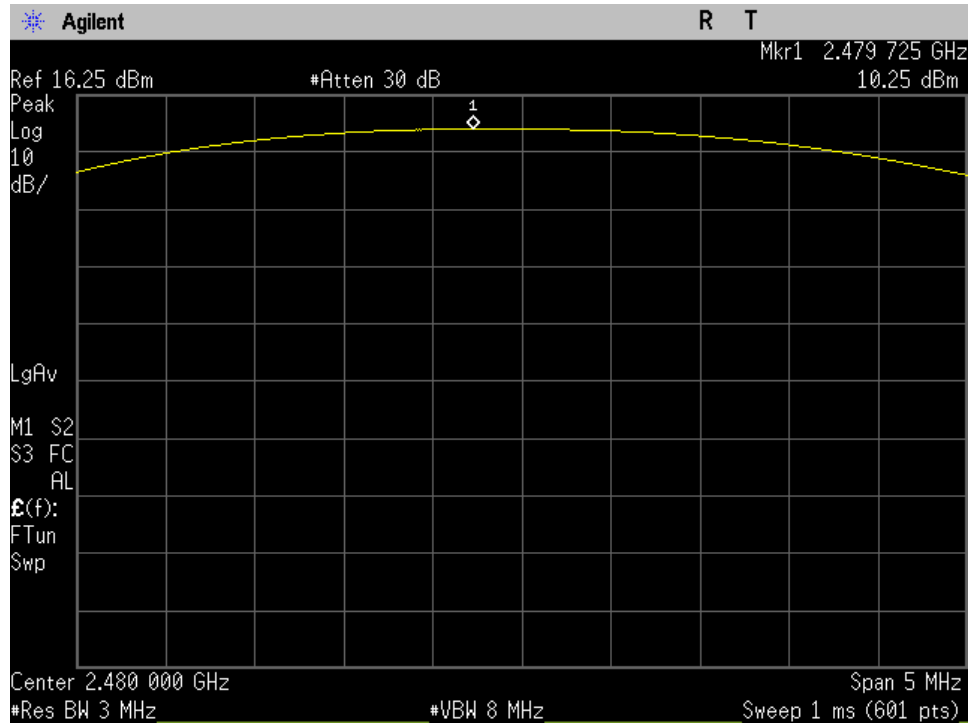
Low Ch_2402MHz_GFSK_Output Power_Port 1



Mid Ch_2440MHz_GFSK_Output Power_Port 1

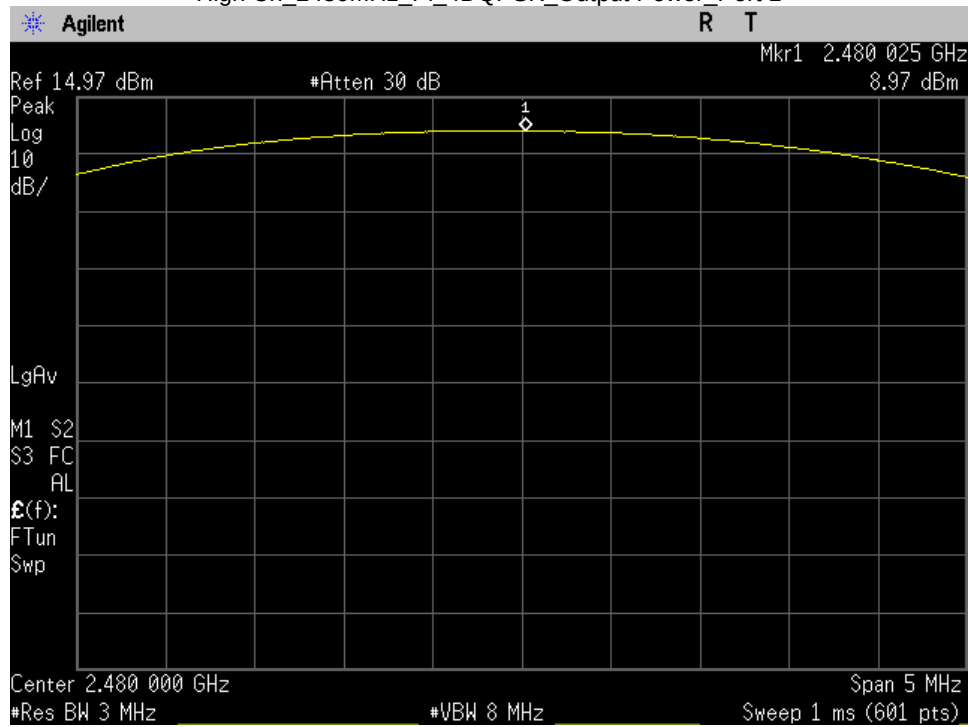


High Ch_2480MHz_GFSK_Output Power_Port 1

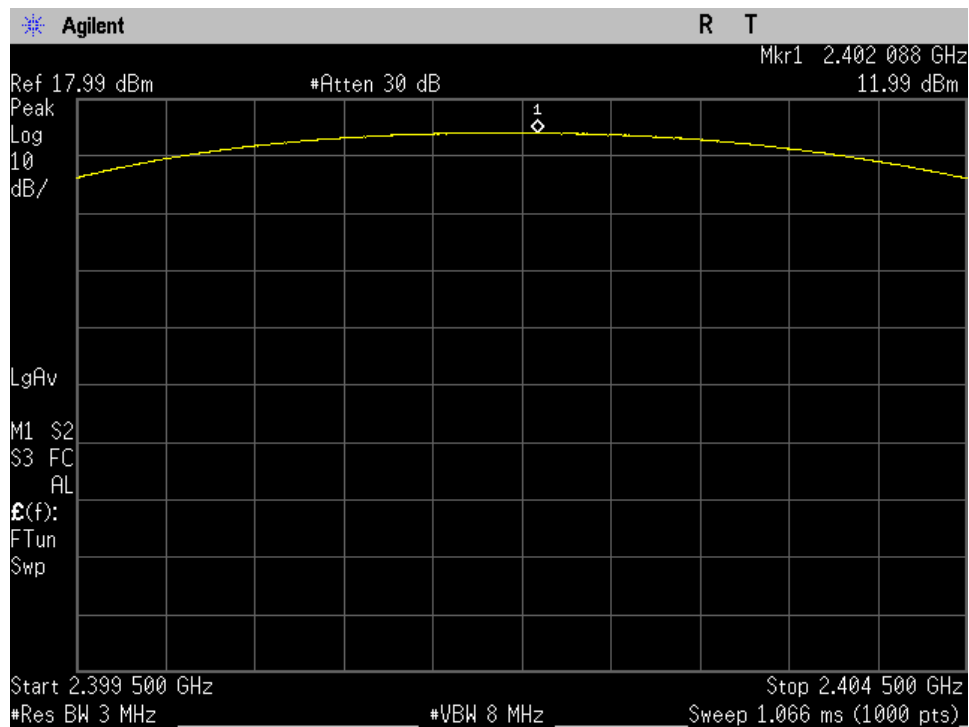


$\pi/4$ DPSK

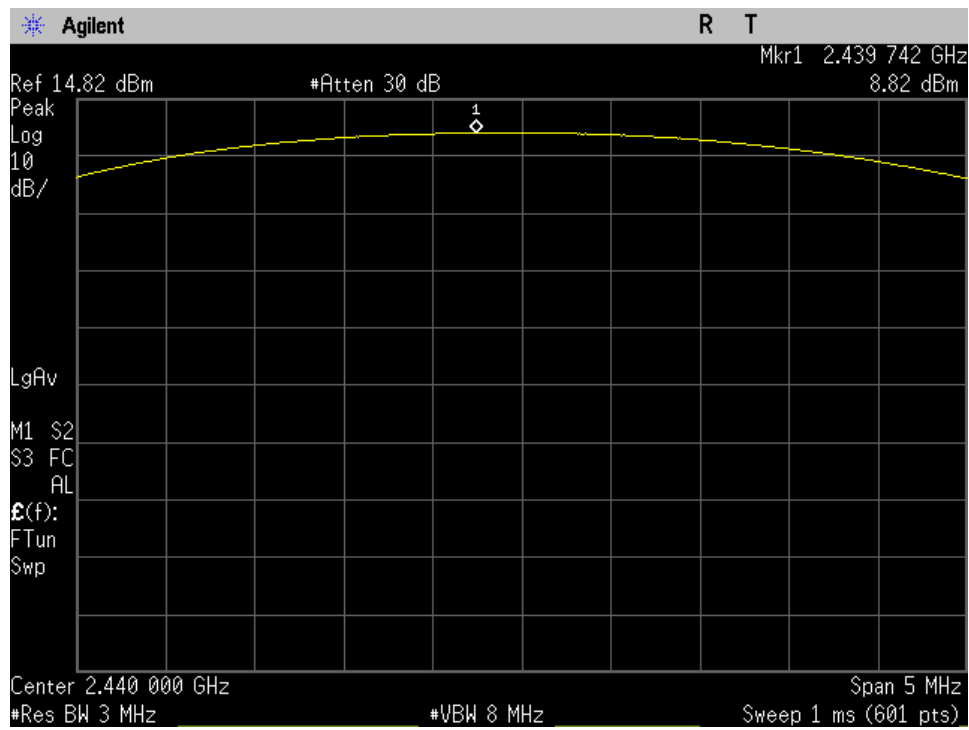
High Ch_2480MHz_Pi_4DQPSK_Output Power_Port 1



Low Ch_2402MHz_Pi_4DQPSK_Output Power_Port 1

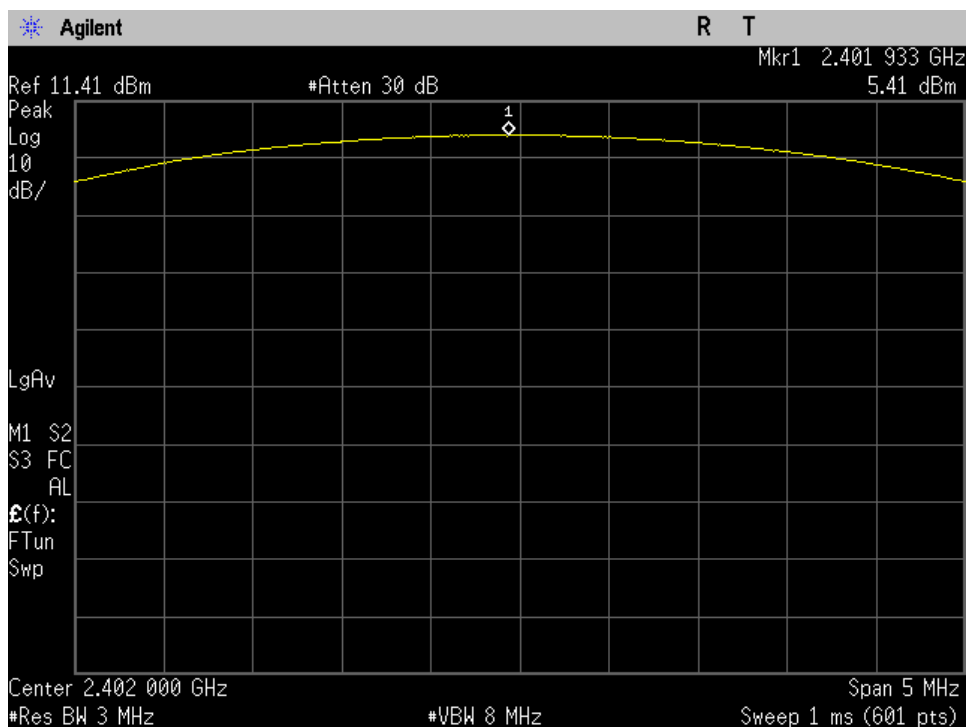


Mid Ch_2440MHz_Pi_4DQPSK_Output Power_Port 1

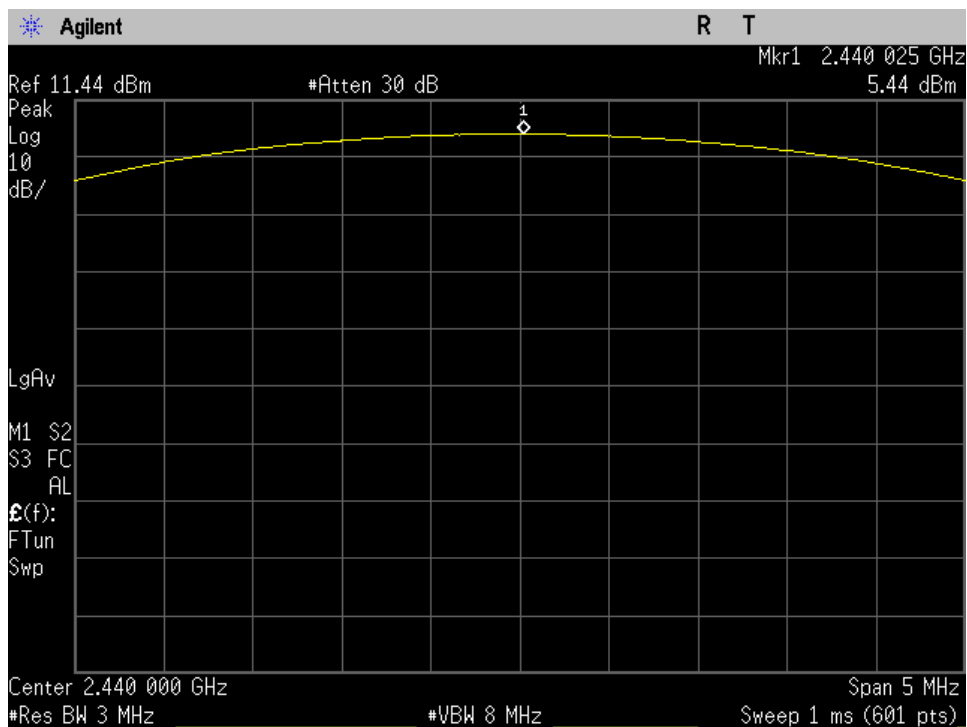


8DPSK

Low Ch_2402MHz_8DPSK_Output Power_Port 1



Mid Ch_2440MHz_8DPSK_Output Power_Port 1



High Ch_2480MHz_8DPSK_Output Power_Port 1

