Prepared (Subject resp)		No.		
ESAVMIK		TA8AKRD901060 / 287AB-AS901060		
Approved (Document resp)	Checked	Date	Rev	Reference
ESAVMIK		2015-12-04	B	

Exhibit 12 Technical Circuit Description - Confidential

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Approved (Document resp)	Checked	Date	Rev	Reference
ESAVMIK		2015-12-04	B	

Exhibit 12 – Technical Circuit Description FCC ID: TA8AKRD901060 and IC ID 287AB-AS901060

Contents

1 2.1033(c) Circuit Description

1.1 (2) FCC ID: TA8AKRD901060 and IC ID 287AB-AS901060

This WCDMA/LTE RBS 6402 Product is a synthesized Transmitter and Receiver designed for use in the 3GPP (Third Generation Partnership Project) LTE (Long Term Evolution) and WCDMA (Wideband Code Division Access).
.

This RBS 6402 operates in operating frequency bands 2, 25, 4 and 7 defined by 3GPP. The Transmitter part of this RBS 6402 operates in the frequency band of:

1930 to 1990 MHz for Band 2
1930 to 1995 MHz for Band 25
2110 to 2155 MHz for Band 4
2620 to 2690 MHz for Band 7

and the Receiver part of this RBS 6402 operates in the frequency band of:

1850 to 1910 MHz for Band 2
1850 to 1915 MHz for Band 25
1710 to 1755 MHz for Band 4
2500 to 2570 MHz for Band 7

For WCDMA, this RBS6402 Band 2 supports modulations of QPSK, 16QAM and 64QAM. It is able to transmit in dual carrier.

For LTE, this RBS 6402 supports modulations of QPSK, 16QAM and 64QAM. The Channel Bandwidth is configurable within 5.0 MHz, 10 MHz, 15 MHz and 20 MHz with possibility to activate 25, 50 and 100 Resource Blocks (RB). It is able to transmit dual carrier. This RBS supports 4x4 MIMO. (Multiple Input Multiple Output) for LTE.

This RBS 6402 is has two a dual-TX radio units where two RF chains are identical. Can be configured to two 2x2 MIMO per radio or CA inter-band CA, intra band CA with two radio cards and 4x4 MIMO with two radio cards

This RBS 6402 supports two Radio Modules of which both have two identical down-link and up-link signal paths.

This RBS 6402 has following functions:

- Transmitting and Receiving Processing (TRP).
- Downlink (Transmitter) and Uplink (Receiver) signal processing and RF filtering.
- 2-TX (Transmitter) with one Radio Module.
- 2-RX (Receiver) with one Radio Module.
- Possibility to use integrated wide Sector antenna or alternative external antenna(s).

- Low output power (max 250mW, min 20mW total configured power per branch). If two carriers per branch, total power is divided between carriers.

Integrated antenna:
Integrated omni antenna, consisting of two integrated antennas operating on the same frequency band e.g. in dual polarized antenna. In CA configuration, another radio module might have low band antenna and another radio module might have high band antenna.
Product no KRE 105 660/1: Minimum gain: Gain per antenna port
$-180deg \leq \theta \leq +180deg$ and $0deg \leq \phi \leq -45deg$ is > -6.0 dBi.
Maximum gain: Gain per antenna port, is 4 dBi.

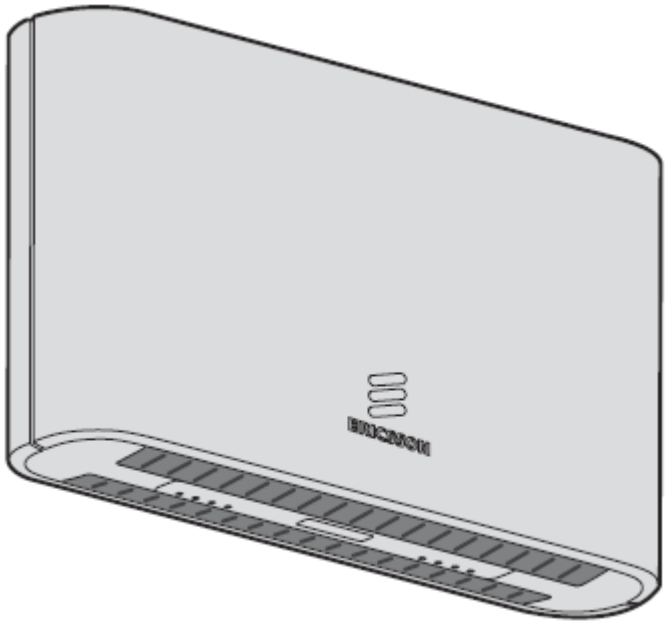

Figure 1 RBS 6402

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Table 1 RBS 6402 HW configuration

Function Designation	Product nr.	FCC ID:	IC:	IC MODEL NO:
KRD 901 060/1 = One radio module, include Band 2, Band 25, Band 4, Band 7	KRD 901 060/1	TA8AKRD901060	287AB-AS901060	AS9010601
KRD 901 060/2 = Two radio module, include Band 2, Band 25, Band 4, Band 7	KRD 901 060/2	TA8AKRD901060	287AB-AS901060	AS9010602
KRD 901 060/7 = One radio module, include Band 2, Band 25	KRD 901 060/7	TA8AKRD901060	287AB-AS901060	AS9010607
KRD 901 060/8 = One radio module, include Band 4	KRD 901 060/8	TA8AKRD901060	287AB-AS901060	AS9010608
KRD 901 060/9 = One radio module, include Band 7	KRD 901 060/9		287AB-AS901060	AS9010609

1.2 (4) Type of Emission

LTE:

QPSK: 4M48G7D 16QAM and 64QAM: 4M48W7D
Channel bandwidth BWChannel: 5 MHz
Transmission bandwidth configuration NRB (Number of Resource Blocks): 25
Transmission bandwidth configuration, DL(TX): 4.515MHz
Transmission bandwidth configuration, UL(RX): 4.500MHz

QPSK: 8M93G7D 16QAM and 64QAM: 8M93W7D
Channel bandwidth BWChannel: 10 MHz
Transmission bandwidth configuration NRB (Number of Resource Blocks): 50
Transmission bandwidth configuration, DL(TX): 9.015 MHz
Transmission bandwidth configuration, UL(RX): 9.000 MHz

QPSK: 13M4G7D 16QAM and 64QAM: 13M4W7D
Channel bandwidth BWChannel: 15 MHz
Transmission bandwidth configuration NRB (Number of Resource Blocks): 75
Transmission bandwidth configuration, DL(TX): 13.015 MHz
Transmission bandwidth configuration, UL(RX): 13.000 MHz

QPSK: 17M9G7D 16QAM and 64QAM: 17M9W7D
Channel bandwidth BWChannel: 20 MHz
Transmission bandwidth configuration NRB (Number of Resource Blocks): 100
Transmission bandwidth configuration, DL(TX): 18.015MHz
Transmission bandwidth configuration, UL(RX): 18.000MHz

WCDMA:
4M18F9W: Channel bandwidth BWChannel: 5.0 MHz

1.3 (5) Frequency Range

Downlink band frequency range (TX):

1930 to 1990 MHz for Band 2
1930 to 1995 MHz for Band 25
2110 to 2155 MHz for Band 4
2620 to 2690 MHz for Band 7

Uplink band frequency range (RX):

1850 to 1910 MHz for Band 2
1850 to 1915 MHz for Band 25
1710 to 1755 MHz for Band 4
2500 to 2570 MHz for Band 7

1.4 (6) Range of Operating Power

This dual-TX RBS 6402 (two RF chains are identical) is designed to supply a nominal power level of 24.0 dBm on each TX output connector and it supports also lower power level down to 13 dBm.
For WCDMA, power dynamic range ≥ 17.7 dB per carrier.

For LTE, the dynamic power range is the difference between the maximum and the minimum scheduled output power in the supported bandwidth when the output power is Pcell (in case no cell range reduction is required, Pcell = Pnom).

Table 2: Power dynamic ranges (LTE)

Supported BW (MHz)	Power dynamic range relative to Pcell as defined above (dB)
5	-13.50
10	-16.50
15	-18.30
20	-19.60

1.5 (7) Maximum Power Rating

The maximum nominal power rating one dual-TX (two RF chains are identical) is equal to 2x24 dBm / 2x250 mW with tolerance ±1dB.

1.6 (8) Final Amplifier Voltage and Current in Normal Operation

Table 3: Final Amplifier Voltage and Current in Normal Operation

	Max Average Power 2x250 mW output power Values for Power Amplifier
Voltage	5V
Current	2 x 425mA

1.7 (9, 10) Frequency Stabilizing Circuit Description

The base station has an internal temperature compensated oscillator to generate clocks for the air interface circuitry and an internal PPS pulse for synchronization.

Synchronization reference for the oscillator is provided over global navigation satellite system (GNSS), PTP protocol (IEEE-1588v2), (S)NTP or Synchronous Ethernet. Time of day is synchronized from GNSS, PTP or NTP.

PTP over IP, Synchronous Ethernet and NTP can be used for frequency synchronization. Precise time demanded, for example to assist CDMA handover or to support CoMP, requires GNSS or high quality PTP (PTP over Ethernet). Synchronous Ethernet clock recovery is dependent on an unbroken chain of Synchronous Ethernet capable devices between the timing server and client and requires upstream node to support synchronous Ethernet status messaging.

External GNSS Receiver Unit (GRU) is used and it supports only GPS (L1 band 1575.42 MHz).
Two Transmitters (TX) inside RBS 6402 each consists of Integrated Doherty Power amplifiers (PA).
One or two TX branches are filtered in DFE, PAR reduction and DPD is applied and then fed to a TXIC (transmitter integrated circuit) which is capable to handle one or two TX branches. In the TXIC signal or signals are digitally filtered, interpolated, digital to analog converted, analog filtered, direct up-converted into RF and amplified with variable gain. Up-converted RF-signal or RF-signals pass through filtering, gain block, another filtering, power amplifier, coupler, isolator and duplex filter. The TX is capable of delivering a 40MHz wide transmit band for LTE modulation. IBW is 40 MHz, meaning that carriers need not to be adjacent.

The receiver is a direct down-conversion dual receiver. It consists of two RF-paths with duplex filter, by-passable LNA, filters and a RXIC (receiver integrated circuit). The RXIC is dual-receiver circuit. In the RXIC signals are amplified with variable gain, filtered, direct down-converted, decimated and digitally filtered.

The receiver is a direct down-conversion dual receiver. It consists of two RF-paths with duplex filter, by-passable LNA, filters and a RXIC (receiver integrated circuit). The RXIC is dual-receiver circuit. In the RXIC signals are amplified with variable gain, filtered, direct down-converted, decimated and digitally filtered.

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Block diagrams of RBS 6402 are presented in Figure 2,Figure 3 and Figure 4.

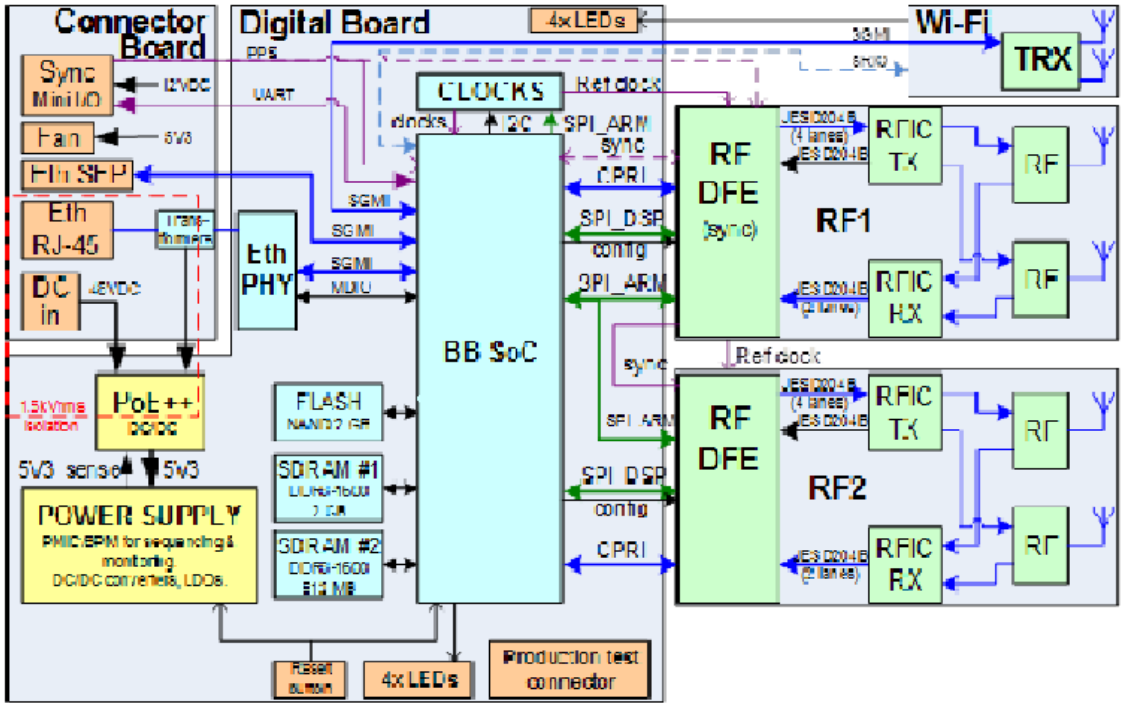

Figure 2 RBS 6402 Block diagram

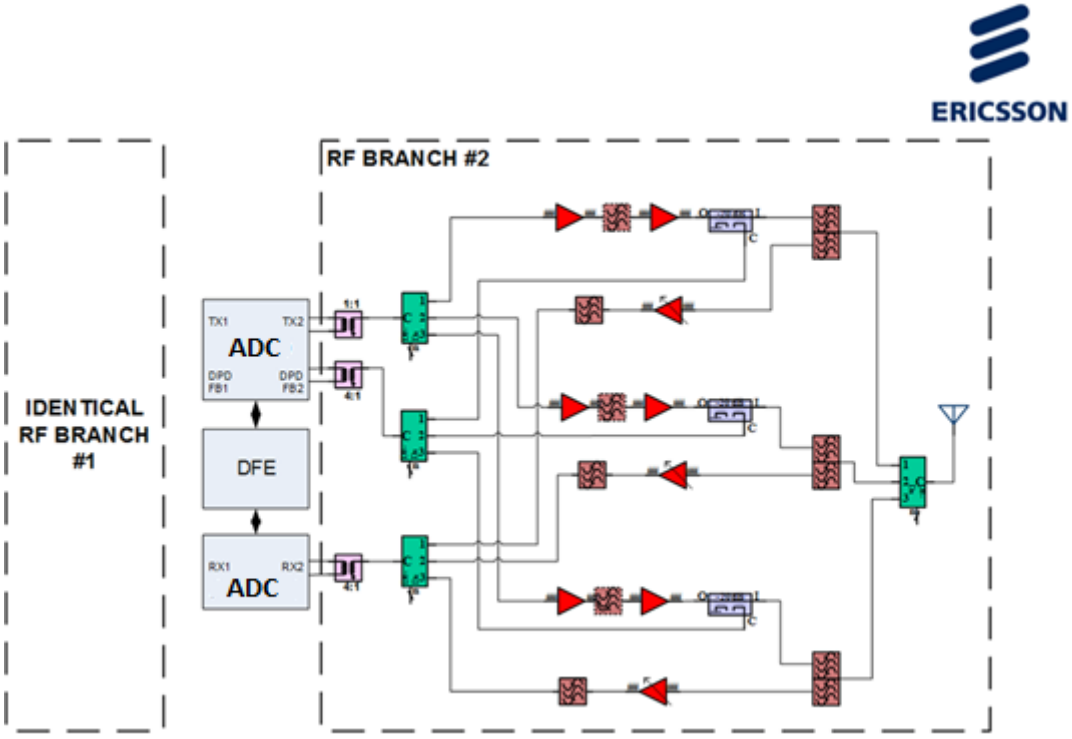

Figure 3 RF block diagram of the low-band RF-module

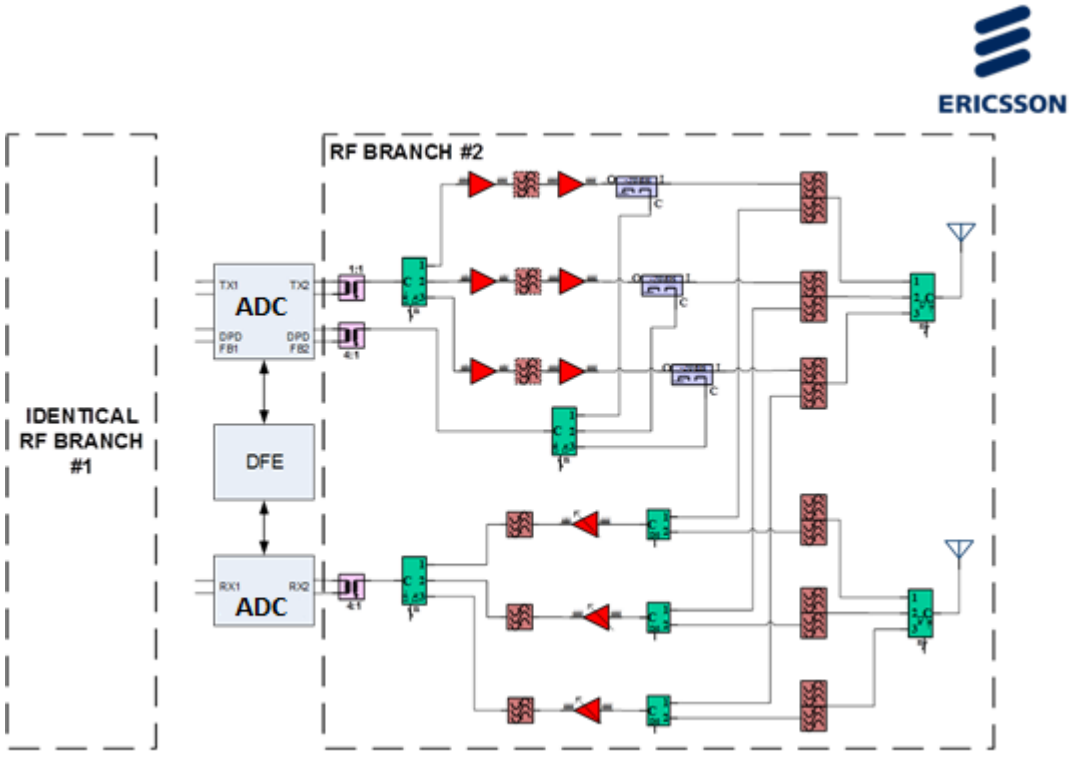

Figure 4 RF block diagram of the high-band RF-module

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(10) Spurious and Harmonic Suppression

Spurious and harmonic suppression is achieved by using several filters before PA and duplexer filter after PA.

1.8 (9, 10) Power Tune Up - Limiting Power

RBS 6402 controls its output power by measuring it after PA. Every unit is calibrated individually over frequency range to eliminate the effect of losses between PA and antenna connector. Unit is also calibrated over its temperature range.

1.9 (10) LTE MIMO Description

MIMO (Multiple-Input, Multiple-Output) antenna systems are used in modern wireless standards, in order to support enhanced data throughput even under conditions of interference, signal fading, and multipath.

General description of several different transmission techniques where multiple receive and transmit antennas are used.

4x4 MIMO is that four transmit antennas on the RBS and four receive antennas on the UE are employed. MIMO standardized in 3GPP Rel-8.

1.10 (10) LTE Downlink Transmission

1.10.1 Physical-layer processing

The downlink physical-layer processing of transport channels consists of the following steps:

- CRC insertion: 24 bit CRC is the baseline for PDSCH;
- Channel coding: Turbo coding based on QPP inner interleaving with trellis termination;
- Physical-layer hybrid-ARQ processing;
- Channel interleaving;
- Scrambling: transport-channel specific scrambling on DL-SCH, BCH, and PDH. Common MCH scrambling for all cells involved in a specific MBSFN transmission;
- Modulation: QPSK, 16QAM, and 64QAM;
- Layer mapping and pre-coding;
- Mapping to assigned resources and antenna ports.

1.10.2 Channel Coding

The error correcting coder selected for DL_SCH is Parallel Concatenated Convolutional Code (PCCC) with two 8-state constituent encodes and one turbo code internal interleaver (simply called “the Turbo code” in the following). The coding rate of the Turbo encoder is 1/3. This is the same Turbo code used as in R6 UMTS, with exception that the internal interleaver works differently.

1.10.3 OFDM baseband signal generation

The downlink transmission modulation scheme is based on conventional OFDM (Orthogonal Frequency Division Multiplexing) using a cyclic prefix. The OFDM sub-carrier spacing is Δf = 15 kHz. 12 consecutive sub-carriers during one slot corresponding to one downlink *resource block*. In the frequency domain, the number of resource blocks, N_{RB}, can range from N_{RB} -min=6 to NRB-man=50. In addition there is also a reduced sub-carrier spacing $\Delta flow$ = 7.5 kHz, only for MBMS dedicated cell.

Table 3 lists the value of $N_{CP,l}$ that shall be used. Note that different OFDM

symbols within a slot in some cases have different cyclic prefix lengths.

Table 3: OFDM parameters

Configuration		Cyclic prefix length $N_{CP,l}$
Normal cyclic prefix	Δf = 15 kHz	160 for l = 0 144 for l = 1,2,…6
Extended cyclic prefix	Δf = 15 kHz	512 for l = 0,1,…5
	Δf = 7.5 kHz	1024 for l = 0,1,2

1.10.4 Modulation and upconversion

Modulation and upconversion to the carrier frequency of the complex-valued OFDM baseband signal for each antenna port is shown in Figure 5.

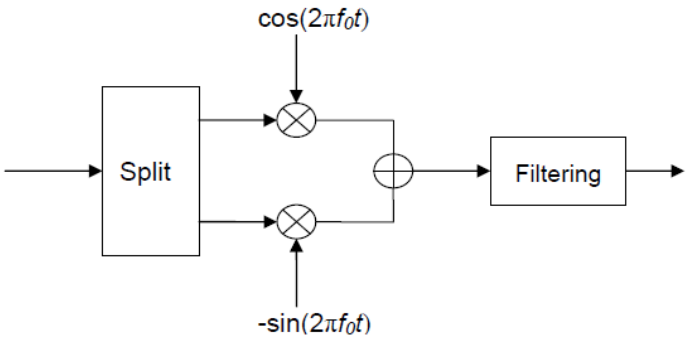


Figure 5: Downlink modulation

1.10.5 Modulation mapper

The modulation mapper takes binary digits, 0 or 1, as input and produces complex-valued modulation symbols, $x=I+jQ$, as output.

1.10.5.1 BPSK

In case of BPSK modulation, a single bit, $b(i)$, is mapped to a complex-valued modulation symbol $x=I+jQ$ according to Table 4.

Table 4: BPSK modulation mapping

$b(i)$	I	Q
0	1/ √2	1/ √2
1	-1/ √2	-1/ √2

1.10.5.2 QPSK

In case of QPSK modulation, pairs of bits, $b(i),b(i+1)$, are mapped to complex- valued modulation symbols $x=I+jQ$ according to Table 5.

Table 5: QPSK modulation mapping

$b(i),b(i+1)$	I	Q
00	1/ √2	1/ √2
01	1/ √2	-1/ √2
10	-1/ √2	1/ √2
11	-1/ √2	-1/ √2

1.10.5.3 16QAM

In case of 16QAM modulation, quadruplets of bits, $b(i),b(i+1),b(i+2),b(i+3)$, are mapped to complex-valued modulation symbols $x=I+jQ$ according to Table 6.

Table 6: 16QAM modulation mapping

$b(i),b(i+1),b(i+2),b(i+3)$	I	Q
0000	1/ √10	1/ √10
0001	1/ √10	3/ √10
0010	3/ √10	1/ √10
0011	3/ √10	3/ √10
0100	1/ √10	-1/ √10
0101	1/ √10	-3/ √10
0110	3/ √10	-1/ √10
0111	3/ √10	-3/ √10
1000	-1/ √10	1/ √10
1001	-1/ √10	3/ √10
1010	-3/ √10	1/ √10
1011	-3/ √10	3/ √10
1100	-1/ √10	3/ √10
1101	-1/ √10	-3/ √10
1110	-3/ √10	-1/ √10
1111	-3/ √10	-3/ √10

1.10.5.4 64QAM

In case of 64QAM modulation, hextuplets of bits, $b(i),b(i+1),b(i+2),b(i+3),b(i+4),b(i+5)$, are mapped to complex-valued modulation symbols $x=I+jQ$ according to Table 7.

Table 7: 64QAM modulation mapping

$b(i),b(i+1),b(i+2),b(i+3),b(i+4),b(i+5)$	I	Q	$b(i),b(i+1),b(i+2),b(i+3),b(i+4),b(i+5)$	I	Q
000000	3/ √42	3/ √42	100000	-3/ √42	3/ √42
000001	3/ √42	1/ √42	100001	-3/ √42	1/ √42
000010	1/ √42	3/ √42	100010	-1/ √42	3/ √42
000011	1/ √42	3/ √42	100011	-1/ √42	1/ √42
000100	3/ √42	5/ √42	100100	-3/ √42	5/ √42
000101	3/ √42	7/ √42	100101	-3/ √42	7/ √42
000110	1/ √42	5/ √42	100110	-1/ √42	5/ √42
000111	1/ √42	7/ √42	100111	-1/ √42	7/ √42
001000	5/ √42	3/ √42	101000	-5/ √42	3/ √42
001001	5/ √42	1/ √42	101001	-5/ √42	1/ √42
001010	7/ √42	3/ √42	101010	-7/ √42	3/ √42
001011	7/ √42	1/ √42	101011	-7/ √42	1/ √42
001100	5/ √42	5/ √42	101100	-5/ √42	5/ √42
001101	5/ √42	7/ √42	101101	-5/ √42	7/ √42
001110	7/ √42	5/ √42	101110	-7/ √42	5/ √42
001111	7/ √42	7/ √42	101111	-7/ √42	7/ √42
010000	3/ √42	-3/ √42	110000	-3/ √42	-3/ √42
010001	3/ √42	-1/ √42	110001	-3/ √42	-1/ √42
010010	1/ √42	-3/ √42	110010	-1/ √42	-3/ √42
010011	1/ √42	-1/ √42	110011	-1/ √42	-1/ √42
010100	3/ √42	-5/ √42	110100	-3/ √42	-5/ √42
010101	3/ √42	-7/ √42	110101	-3/ √42	-7/ √42
010110	1/ √42	-3/ √42	110110	-1/ √42	-5/ √42
010111	1/ √42	1/ √42	110111	-1/ √42	-7/ √42
011000	5/ √42	-3/ √42	111000	-5/ √42	-3/ √42
011001	5/ √42	-1/ √42	111001	-5/ √42	-1/ √42
011010	7/ √42	-3/ √42	111010	-7/ √42	-3/ √42
011011	7/ √42	-1/ √42	111011	-7/ √42	-1/ √42
011100	5/ √42	-5/ √42	111100	-5/ √42	-5/ √42
011101	5/ √42	-7/ √42	111101	-5/ √42	-7/ √42
011110	7/ √42	-5/ √42	111110	-7/ √42	-5/ √42
011111	7/ √42	-7/ √42	111111	-7/ √42	-7/ √42

1.10.6 Physical channels

A downlink physical channel corresponds to a set of resource elements carrying information originating from higher layers and is the interface defined between
36.212 and 36.211. The following downlink physical channels are defined:

- Physical Downlink Shared Channel, PDSCH
- Physical Broadcast Channel, PBCH
- Physical Multicast Channel, PMCH
- Physical Control Format Indicator Channel, PCFICH
- Physical Downlink Control Channel, PDCCH
- Physical Hybrid ARQ Indicator Channel, PHICH

1.10.7 Physical signals

A downlink signal corresponds to a set of resource elements used by the physical layer but does not carry information originating from higher layers. The following downlink physical signals are defined:

- Reference signal
- Synchronization signal

1.10.8 General structure for downlink physical channels

This section describes a general structure, applicable to more than one physical channel.

The baseband signal representing a downlink physical channel is defined in terms of the following steps:

- Scrambling of coded bits in each of the code words to be transmitted on a physical channel
- Modulation of scrambled bits to generate complex-valued modulation symbols
- Mapping of the complex-valued modulation symbols onto one or several transmission layers

- Precoding of the complex-valued modulation symbols on each layer for transmission on the antenna ports
- Mapping of complex-valued modulation symbols for each antenna port to resource elements
- Generation of complex-valued time-domain OFDM signal for each antenna port antenna port

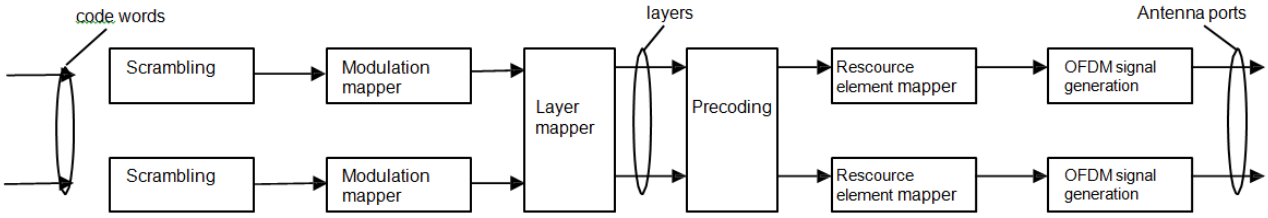


Figure 6: Overview of physical channel processing

1.10.8.1 IQ combining

The real valued chip sequence on the Q branch shall be complex multiplied with j and summed with the corresponding real valued chip sequence on the I branch, thus resulting in a single complex valued chip sequence.

1.10.8.2 Scrambling

The bits in the code word are scrambled with specific scrambling sequence prior to modulation.

1.10.8.3 Modulation

Standard QPSK, 16QAM or 64QAM modulation mapping, resulting in complex modulation symbols carrying 2, 4 or 6 coded bits respectively.

1.10.8.4 Layer mapping

The modulation symbols from one or two (scrambled) code words are mapped onto 1, 2, antenna ports. Thus, this step is related to MIMO or TX diversity operation. Basically, a layer corresponds to a spatial multiplexed channel.

1.10.8.5 Precoding

This step is also related to MIMO or TX diversity. Precoding is applied to allow the UE to separate the different antenna streams.

1.10.8.6 Resource Element Mapping

The precoded code words are mapped onto a number of 2-dimensiol time-frequency Resource Elements available for the transmission.

1.10.8.7 OFDM Signal Generation

OFDM symbols are created, as described in chapter 1.12.3, using the number of sub-carriers allocated for transmission. A cyclic prefix is appended to each OFDM symbol and the symbols (with CP) are then mapped onto 2 consecutive
radio frame slots constituting a subframe. The Resource Element Mapping stage and the OFDM Signal Generation stage takes place separately for each antenna port assigned for the transmission.

1.11 (10) WCDMA Downlink Transmission

1.11.1 Downlink Spreading

Figure 9 illustrates the spreading operation for all physical channel except SCH. The spreading operation includes a modulation mapper stage successively followed by a channelisation stage, an IQ combining stage and a scrambling stage. All the downlink physical channels are then combined as specified in sub subclause 1.11.1.5.

The non-spread downlink physical channels, except SCH, AICH, E-HICH, AP-AICH, CD/CA-ICH, E-HICH and E-RGCH consist of a sequence of 3-valued digits taking the values 0, 1 and "DTX". Note that "DTX" is only applicable to those downlink physical channels that support DTX transmission.

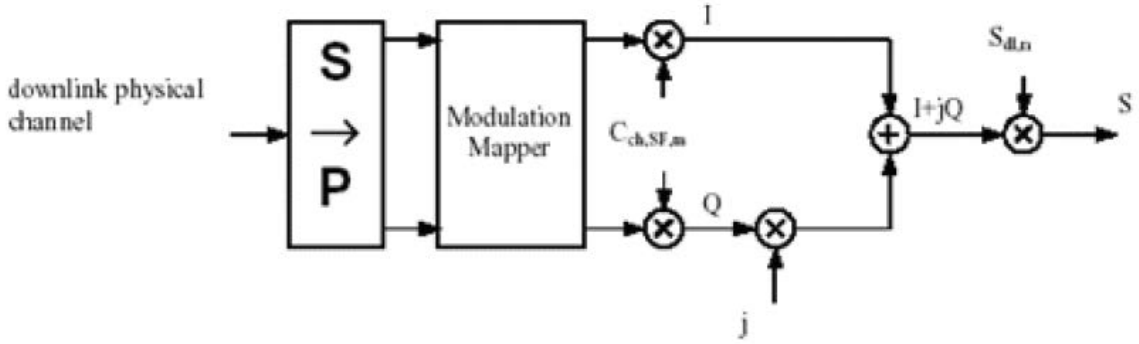


Figure 9: Spreading for all downlink physical channels except SCH

NOTE: Although subclause 1.11.1 has been reorganized in this release, the spreading operation as specified for the DL channels in the previous release remains unchanged.

1.11.1.1 Modulation mapper

Table 7 defines which of the IQ mapping specified in subclauses 1.11.1.1.1 and 1.11.1.1.2 may be used for the physical channel being processed.

Table 7: IQ mapping

Physical channel	IQ mapping
HS-PDSCH, S-CCPCH*	QPSK, 16QAM or 64QAM
All other channels (except the SCH)	QPSK

* For MBSFN FACH transmissions, QPSK and 16QAM can be used.

1.11.1.1.1 QPSK

For all channels, except AICH, AP-AICH, CD/CA-ICH, E-HICH and E-RGCH, the input digits shall be mapped to real-valued symbols as follows: the binary value "0" is mapped to the real value +1, the binary value "1" is mapped to the real value –1 and "DTX" is mapped to the real value 0.
For the indicator channels using signatures (AICH, AP-AICH, CD/CA-ICH), the real-valued input symbols depend on the exact combination of the indicators to be transmitted as specified in 3GPP TS 25.211, sub clauses 5.3.3.7, 5.3.3.8 and 5.3.3.9. For the E-HICH and the E-RGCH the input is a real valued symbol sequence as specified in 3GPP TS 25.211.

Each pair of two consecutive real-valued symbols is first converted from serial to parallel and mapped to an I and Q branch. The definition of the modulation mapper is such that even and odd numbered symbols are mapped to the I and Q branch respectively. For all QPSK channels except the indicator channels using signatures, symbol number zero is defined as the first symbol in each frame or sub-frame. For the indicator channels using signatures, symbol number zero is defined as the first symbol in each access slot.

1.11.1.1.2 16QAM

In case of 16QAM, a set of four consecutive binary symbols n_k, n_{k+1}, n_{k+2}, n_{k+3} (with k mod 4 = 0) is serial-to-parallel converted to two consecutive binary symbols ($i_1 = n_k$, $i_2 = n_{k+2}$) on the I branch and two consecutive binary symbols ($q_1 = n_{k+1}$, $q_2 = n_{k+3}$) on the Q branch and then mapped to 16QAM by the modulation mapper as defined in table 8.
The I and Q branches are then both spread to the chip rate by the same real-valued channelisation code $C_{ch,16,m}$. The channelisation code sequence shall be aligned in time with the symbol boundary. The sequences of real-valued chips on the I and Q branch are then treated as a single complex-valued sequence of chips. This sequence of chips from all multicodes is summed and then scrambled (complex chip-wise multiplication) by a complex-valued scrambling code $S_{dl,n}$.
The scrambling code is applied aligned with the scrambling code applied to the P-CCPCH.

Table 8: 16QAM modulation mapping

i1q1 i2q2	I branch	Q branch
0000	0.4472	0.4472
0001	0.4472	1.3416
0010	1.3416	0.4472
0011	1.3416	1.3416
0100	0.4472	-0.4472
0101	0.4472	-1.3416
0110	1.3416	-0.4472
0111	1.3416	-1.3416
1000	-0.4472	0.4472
1001	-0.4472	1.3416
1010	-1.3416	0.4472
1011	-1.3416	1.3416
1100	-0.4472	-0.4472
1101	-0.4472	-1.3416
1110	-1.3416	-0.4472
1111	-1.3416	-1.3416

In the case of 16-QAM on S-CCPCH, a sequence of four consecutive symbols n_k, n_{k+1}, n_{k+2}, n_{k+3} (with k mod 4 = 0) at the input to the modulation mapper may contain values from the set 0, 1, and 'DTX'. In the event that all 4 bits of the quadruple are DTX bits, the output from the modulation mapping on both the I and Q branches is equal to the real value 0.

For all other cases, all DTX bits in the quadruple are replaced with other non-DTX bits from the quadruple according to the following:

The quadruple consists of two bit pairs, $\{n_k,n_{k+2}\}$ on the I branch, and $\{n_{k+1},n_{k+3}\}$ on the Q branch. For any bit pair, if a non-DTX bit is available in the same pair, the DTX bit shall be replaced with the non-DTX bit value. If a non-DTX bit is not available in the same pair, the two DTX bits in that pair shall be replaced by the non-DTX bits in the other pair (using the same bit ordering when the other pair contains two non-DTX bits).

The bit positions and values of non-DTX bits in the quadruple are not affected.

1.11.1.1.3 64QAM

In case of 64QAM, a set of six consecutive binary symbols n_k, n_{k+1}, n_{k+2}, n_{k+3}, n_{k+4}, n_{k+5} (with k mod 6 = 0) is serial-to-parallel converted to three consecutive binary symbols ($i_1= n_k$, $i_2= n_{k+2}$, $i_2= n_{k+4}$) on the I branch and three consecutive binary symbols ($q_1=n_{k+1}$, $q_2= n_{k+3}$, $q_2= n_{k+5}$) on the Q branch and then mapped to 64QAM by the modulation mapper as defined in table 9.
The I and Q branches are then both spread to the chip rate by the same real-valued channelisation code $C_{ch,16,m}$. The channelisation code sequence shall be aligned in time with the symbol boundary. The sequences of real-valued chips on the I and Q branch are then treated as a single complex-valued sequence of chips. This sequence of chips from all multicodes is summed and then scrambled (complex chip-wise multiplication) by a

complex-valued scrambling code $S_{dl,n}$. The scrambling code is applied aligned with the scrambling code applied to the P-CCPCH.

Table 9: 64QAM modulation mapping

i1q1i2q2 i3q3	I branch	Q branch	i1q1i2q2 i3q3	I branch	Q branch
000000	0.6547	0.6547	100000	-0.6547	0.6547
000001	0.6547	0.2182	100001	-0.6547	0.2182
000010	0.2182	0.6547	100010	-0.2182	0.6547
000011	0.2182	0.2182	100011	-0.2182	0.2182
000100	0.6547	1.0911	100100	-0.6547	1.0911
000101	0.6547	1.5275	100101	-0.6547	1.5275
000110	0.2182	1.0911	100110	-0.2182	1.0911
000111	0.2182	1.5275	100111	-0.2182	1.5275
001000	1.0911	0.6547	101000	-1.0911	0.6547
001001	1.0911	0.2182	101001	-1.0911	0.2182
001010	1.5275	0.6547	101010	-1.5275	0.6547
001011	1.5275	0.2182	101011	-1.5275	0.2182
001100	1.0911	1.0911	101100	-1.0911	1.0911
001101	1.0911	1.5275	101101	-1.0911	1.5275
001110	1.5275	1.0911	101110	-1.5275	1.0911
001111	1.5275	1.5275	101111	-1.5275	1.5275
010000	0.6547	-0.6547	110000	-0.6547	-0.6547
010001	0.6547	-0.2182	110001	-0.6547	-0.2182
010010	0.2182	-0.6547	110010	-0.2182	-0.6547
010011	0.2182	-0.2182	110011	-0.2182	-0.2182
010100	0.6547	-1.0911	110100	-0.6547	-1.0911
010101	0.6547	-1.5275	110101	-0.6547	-1.5275
010110	0.2182	-1.0911	110110	-0.2182	-1.0911
010111	0.2182	-1.5275	110111	-0.2182	-1.5275
011000	1.0911	-0.6547	111000	-1.0911	-0.6547
011001	1.0911	-0.2182	111001	-1.0911	-0.2182
011010	1.5275	-0.6547	111010	-1.5275	-0.6547
011011	1.5275	-0.2182	111011	-1.5275	-0.2182
011100	1.0911	-1.0911	111100	-1.0911	-1.0911
011101	1.0911	-1.5275	111101	-1.0911	-1.5275
011110	1.5275	-1.0911	111110	-1.5275	-1.0911
011111	1.5275	-1.5275	111111	-1.5275	-1.5275

1.11.1.2 Channelisation

For all physical channels (except SCH) the I and Q branches shall be spread to the chip rate by the same real-valued channelisation code $C_{ch,SF,m}$, i.e. the output for each input symbol on the I and the Q branches shall be a sequence of SF chips corresponding to the channelisation code chip sequence multiplied by the real-valued symbol. The channelisation code sequence shall be aligned in time with the symbol boundary.

1.11.1.3 IQ combining

The real valued chip sequence on the Q branch shall be complex multiplied with j and summed with the corresponding real valued chip sequence on the I branch, thus resulting in a single complex valued chip sequence.

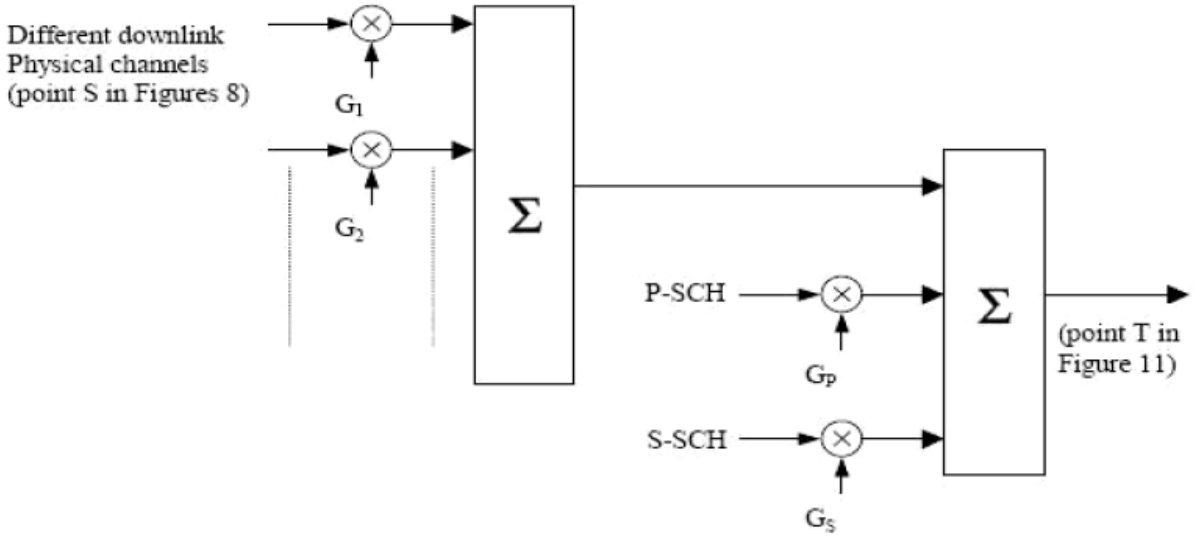
1.11.1.4 Scrambling

The sequence of complex valued chips shall be scrambled (complex chip-wise multiplication) by a complex-valued scrambling code $S_{dl,n}$. In case of P-CCPCH, the scrambling code shall be applied aligned with the P-CCPCH frame boundary, i.e. the first complex chip of the spread P-CCPCH frame is multiplied with chip number zero of the scrambling code. In case of other downlink channels, the scrambling code shall be applied aligned with the scrambling code applied to the P-CCPCH. In this case, the scrambling code is thus not necessarily applied aligned with the frame boundary of the physical channel to be scrambled.

1.11.1.5 Channel combining

Figure 10 illustrates how different downlink channels are combined. Each complex-valued spread channel, corresponding to point S in Figure 8, may be separately weighted by a weight factor G_i. The complex-valued P-SCH and SCH, as described in 3GPP TS 25.211, sub-clause 5.3.3.5, may be separately weighted by weight actors G_p and G_s. All downlink physical channels shall then be combined using complex addition.

Figure 10: Combining of downlink physical channels



1.11.2 Code generation and allocation

1.11.2.1 Channelisation codes

The channelisation codes of figure 8 are the same codes as used in the uplink, namely Orthogonal Variable Spreading Factor (OVSF) codes that preserve the orthogonality between downlink channels of different rates and spreading factors.

The channelisation code for the Primary CPICH is fixed to $C_{ch,256,0}$ and the channelisation code or the Primary CCPCH is fixed to $C_{ch,256,1}$.The channelisation codes for all other physical channels are assigned by UTRAN.

With the spreading factor 512 a specific restriction is applied. When the code word $C_{ch,512,n}$, with n=0,2,4….510, is used in soft handover, then the code word $C_{ch,512,n+1}$ is not allocated in the cells where timing adjustment is to be used. Respectively if $C_{ch,512,n}$, with n=1,3,5….511 is used, then the code word $C_{ch,512,n-1}$ is not allocated in the cells where timing adjustment is to be used. This restriction shall not apply in cases where timing adjustments in soft handover are not used with spreading factor 512.

When compressed mode is implemented by reducing the spreading factor by 2, the OVSF code used for compressed frames is:
- $C_{ch,SF/2,n/2\_}$ if ordinary scrambling code is used.
- $C_{ch,SF/2,n \bmod SF/2}$ if alternative scrambling code is used (see subclause 1.11.2.2);

where $C_{ch,SF,n}$ is the channelisation code used for non-compressed frames.

For F-DPCH, the spreading factor is always 256.

For HS-PDSCH, the spreading factor is always 16.

For HS-SCCH, the spreading factor is always 128.

Channelisation-code-set information over HS-SCCH is mapped in following manner: the OVSF codes shall be allocated in such a way that they are positioned in sequence in the code tree. That is, for P multicodes at offset O the following codes are allocated:

$C_{ch,16,O}$ … $C_{ch,16,O+P-1}$

The number of multicodes and the corresponding offset for HS-PDSCHs mapped from a given HS-DSCH is signaled by HS-SCCH.

For E-HICH and for E-RGCH, the spreading factor shall always be 128. In each cell, the E-RGCH and E-HICH assigned to a UE shall be configured with the same channelisation code.

For E-AGCH, the spreading factor shall always be 256.

1.11.2.2 Scrambling code

A total of 2_{18}-1 = 262,143 scrambling codes, numbered 0…262,142 can be generated. However not all the scrambling codes are used. The scrambling codes are divided into 512 sets each of a primary scrambling code and 15 secondary scrambling codes.
The primary scrambling codes consist of scrambling codes n=16*i where i=0…511. The i:th set of secondary scrambling codes consists of scrambling codes 16*i+k, where k=1…15.

There is a one-to-one mapping between each primary scrambling code and 15 secondary scrambling codes in a set such that i:th primary scrambling code corresponds to i:th set of secondary scrambling codes.

Hence, according to the above, scrambling codes k = 0, 1, …, 8191 are used. Each of these codes are associated with a left alternative scrambling code and a right alternative scrambling code, that may be used for compressed frames. The left alternative scrambling code corresponding to scrambling code k is scrambling code number k + 8192, while the right alternative scrambling code corresponding to scrambling code k is scrambling code number k + 16384. The alternative scrambling codes can be used for compressed frames. In this case, the left alternative scrambling code is used if n<SF/2 and the right alternative scrambling code is used if n□SF/2, where $C_{ch,SF,n}$ is the channelisation code used for noncompressed frames. The usage of alternative scrambling code for compressed frames is signaled by higher layers for each physical channel respectively.

In case F-DPCH is configured in the downlink, the same scrambling code and OVSF code shall be used in F-DPCH compressed frames and normal frames
.
The set of primary scrambling codes is further divided into 64 scrambling code groups, each consisting of 8 primary scrambling codes. The j:th scrambling code group consists of primary scrambling codes 16*8*j+16*k, where j=0..63 and k=0..7.

Each cell is allocated one and only one primary scrambling code. The primary CCPCH, primary CPICH, PICH, MICH, AICH, AP-AICH, CD/CA-ICH, CSICH and S-CCPCH carrying PCH shall always be transmitted using the primary scrambling code. The other downlink physical channels may be transmitted with either the primary scrambling code or a secondary scrambling code from the set associated with the primary scrambling code of the cell.

The mixture of primary scrambling code and no more than one secondary scrambling code for one CCTrCH is allowable. In compressed mode during compressed frames, these can be changed to the associated left or right scrambling codes as described above, i.e. in these frames, the total number of different scrambling codes may exceed two.

In the case of the CCTrCH of type DSCH, all the PDSCH channelisation codes that a single UE may receive shall be under a single scrambling code (either the primary or a secondary scrambling code). In the case of CCTrCH of type of HSDSCH then all the HS-PDSCH channelisation codes and HS-SCCH that a single UE may receive shall be under a single scrambling code (either the primary or a secondary scrambling code).
In each cell, the E-RGCH, E-HICH and E-AGCH assigned to a UE shall be configured with same scrambling code.

The scrambling code sequences are constructed by combining two real sequences into a complex sequence. Each of the two real sequences are constructed as the position wise modulo 2 sum of 38400 chip segments of two binary msequences generated by means of two generator polynomials of degree 18. The resulting sequences thus constitute segments of a set of Gold sequences. The scrambling codes are repeated for every 10 ms radio frame. Let x and y be the two sequences respectively. The x sequence is constructed using the primitive (over GF(2)) polynomial $1+X_7+X_{18}$. The y sequence is constructed using the polynomial $1+X_5+X_7+ X_{10}+X_{18}$.

The sequence depending on the chosen scrambling code number n is denoted z_n, in the sequel. Furthermore, let $x(i)$, $y(i)$ and $z_n(i)$ denote the i:th symbol of the sequence x, y, and z_n, respectively.

The m-sequences x and y are constructed as:

Initial conditions:

− x is constructed with x (0)=1, x(1)= x(2)=...= x (16)= x (17)=0.

− y(0)=y(1)= … =y(16)= y(17)=1.

Recursive definition of subsequent symbols:

− $x(i+18) = x(i+7) + x(i)$ modulo 2, $i=0,\ldots,2_{18}-20$.

− $y(i+18) = y(i+10)+y(i+7)+y(i+5)+y(i)$ modulo 2, $i=0,\ldots, 2_{18}-20$.

The n:th Gold code sequence z_n, $n=0,1,2,\ldots,2_{18}-2$, is then defined as:

− $z_n(i) = x((i+n)$ modulo $(2_{18} - 1)) + y(i)$ modulo 2, $i=0,\ldots, 2_{18}-2$.

These binary sequences are converted to real valued sequences Z_n by the following transformation:

$$Z_n(i) = \begin{cases} +1 & \text{if } z_n(i) = 0 \\ -1 & \text{if } z_n(i) = 0 \end{cases} \quad for \quad i = 0,1,\ldots,2^{18} - 2.$$

Finally, the n:th complex scrambling code sequence $S_{dl,n}$ is defined as:
− $S_{dl,n}(i) = Zn(i) + j\ Zn((i+131072)$ modulo $(2_{18}-1))$, i=0,1,…,38399.
Note that the pattern from phase 0 up to the phase of 38399 is repeated.

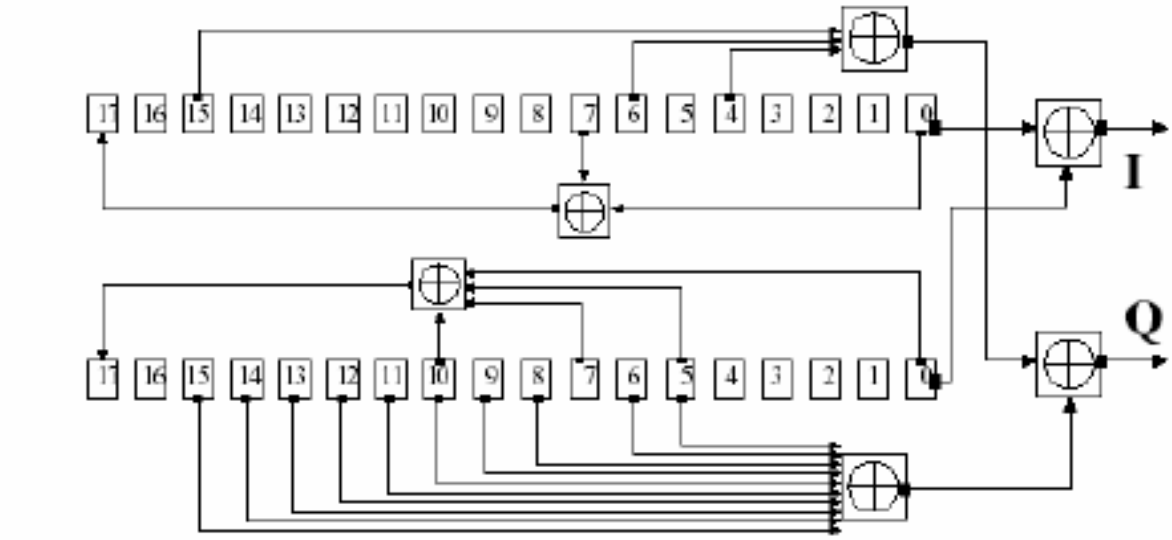


Figure 11: Configuration of downlink scrambling code generator

1.11.2.3 Synchronisation codes

1.11.2.3.1 Code generation

The primary synchronization code (PSC), C_{psc} is constructed as a so-called generalized hierarchical Golay sequence. The PSC is furthermore chosen to have good periodic auto correlation properties.

Define:

− a = <x_1, x_2, x_3, …, x_{16}> = <1, 1, 1, 1, 1, 1, -1, -1, 1, -1, 1, -1, 1, -1, -1, 1>

The PSC is generated by repeating the sequence a modulated by a Golay complementary sequence, and creating a complex-valued sequence with identical real and imaginary components. The PSC C_{psc} is defined as:

− C_{psc} = (1 + j) ☐ <a, a, a,-a, -a, a, -a, -a, a, a, a, -a, a, -a, a, a>;

where the leftmost chip in the sequence corresponds to the chip transmitted first in time.

The 16 secondary synchronization codes (SSCs), {$C_{ssc,1}$,…,$C_{ssc,16}$}, are complex-valued with identical real and imaginary components, and are constructed from position wise multiplication of a Hadamard sequence and a sequence z, defined as:

− z = <b, b, b, -b, b, b, -b, -b, b, -b, b, -b, -b, -b, -b, -b>, where

− b = <x_1, x_2, x_3, x_4, x_5, x_6, x_7, x_8, -x_9, -x_{10}, -x_{11}, -x_{12}, -x_{13}, -x_{14}, -x_{15}, -x_{16}> and x_1,

x_2, …, x_{15}, x_{16}, are same as in the definition of the sequence a above.

The Hadamard sequences are obtained as the rows in a matrix H_8 constructed recursively by:

$$H_0 = (1)$$
$$H_k = \begin{pmatrix} H_{k-1} & H_{k-1} \\ H_{k-1} & -H_{k-1} \end{pmatrix}, \quad k \geq 1$$

The rows are numbered from the top starting with row *0* (the all ones sequence).

Denote the *n*:th Hadamard sequence as a row of H_8 numbered from the top, n = 0, 1, 2, …, 255, in the sequel.

Furthermore, let $h_n(i)$ and $z(i)$ denote the *i*:th symbol of the sequence h_n and *z*, respectively where *i* = 0, 1, 2, …, 255 and *i* = 0 corresponds to the leftmost symbol.

The *k*:th SSC, $C_{ssc,k}$, *k* = 1, 2, 3, …, 16 is then defined as:

− $C_{ssc,k}$ = (1 + *j*) x <h_m(0) x *z*(0), h_m(1) x *z*(1), h_m(2) x *z*(2), …, h_m(255) x *z*(255)>;

where *m* = 16x(*k* – 1) and the leftmost chip in the sequence corresponds to the chip transmitted first in time.

1.11.2.3.2 Code allocation of SSC

The 64 secondary SCH sequences are constructed such that their cyclic-shifts are unique, i.e., a non-zero cyclic shift less than 15 of any of the 64 sequences is not equivalent to some cyclic shift of any other of the 64 sequences. Also, a non-zero cyclic shift less than 15 of any of the sequences is not equivalent to itself with any other cyclic shift less than 15. Table 10 describes the sequences of SSCs used to encode the 64 different scrambling code groups. The entries in table 4 denote what SSC to use in the different slots for the different scrambling code groups, e.g. the entry "7" means that SSC $C_{ssc,7}$ shall be used for the corresponding scrambling code group and slot.

Table 10: Allocation of SSCs for secondary SCH

Scrambling Code Group	slot number														
	#0	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14
Group 0	1	1	2	8	9	10	15	8	10	16	2	7	15	7	16
Group 1	1	1	5	16	7	3	14	16	3	10	5	12	14	12	10
Group 2	1	2	1	15	5	5	12	16	6	11	2	16	11	15	12
Group 3	1	2	3	1	8	6	5	2	5	8	4	4	6	3	7
Group 4	1	2	16	6	6	11	15	5	12	1	15	12	16	11	2
Group 5	1	3	4	7	4	1	5	5	3	6	2	8	7	6	8
Group 6	1	4	11	3	4	10	9	2	11	2	10	12	12	9	3
Group 7	1	5	6	6	14	9	10	2	13	9	2	5	14	1	13
Group 8	1	6	10	10	4	11	7	13	16	11	13	6	4	1	16
Group 9	1	6	13	2	14	2	6	5	5	13	10	9	1	14	10
Group 10	1	7	8	5	7	2	4	3	8	3	2	6	6	4	5
Group 11	1	7	10	9	16	7	9	15	1	8	16	8	15	2	2
Group 12	1	8	12	9	9	4	13	16	5	1	13	5	12	4	8
Group 13	1	8	14	10	14	1	15	15	8	5	11	4	10	5	4
Group 14	1	9	2	15	15	16	10	7	8	1	10	8	2	16	9
Group 15	1	9	15	6	16	2	13	14	10	11	7	4	5	12	3
Group 16	1	10	9	11	15	7	6	4	16	5	2	12	13	3	14
Group 17	1	11	14	4	13	2	9	10	12	16	8	5	3	15	6
Group 18	1	12	12	13	14	7	2	8	14	2	1	13	11	8	11
Group 19	1	12	15	5	4	14	3	16	7	8	6	2	10	11	13
Group 20	1	15	4	3	7	6	10	13	12	5	14	16	8	2	11
Group 21	1	16	3	12	11	9	13	5	8	2	14	7	4	10	15
Group 22	2	2	5	10	16	11	3	10	11	8	5	13	3	13	8
Group 23	2	2	12	3	15	5	8	3	5	14	12	9	8	9	14
Group 24	2	3	6	16	12	16	3	13	13	6	7	9	2	12	7
Group 25	2	3	8	2	9	15	14	3	14	9	5	5	15	8	12
Group 26	2	4	7	9	5	4	9	11	2	14	5	14	11	16	16
Group 27	2	4	13	12	12	7	15	10	5	2	15	5	13	7	4
Group 28	2	5	9	9	3	12	8	14	15	12	14	5	3	2	15
Group 29	2	5	11	7	2	11	9	4	16	7	16	9	14	14	4
Group 30	2	6	2	13	3	3	12	9	7	16	6	9	16	13	12
Group 31	2	6	9	7	7	16	13	3	12	2	13	12	9	16	6
Group 32	2	7	12	15	2	12	4	10	13	15	13	4	5	5	10
Group 33	2	7	14	16	5	9	2	9	16	11	11	5	7	4	14
Group 34	2	8	5	12	5	2	14	14	8	15	3	9	12	15	9
Group 35	2	9	13	4	2	13	8	11	6	4	6	8	15	15	11
Group 36	2	10	3	2	13	16	8	10	8	13	11	11	16	3	5
Group 37	2	11	15	3	11	6	14	10	15	10	6	7	7	14	3

Scrambling Code Group	slot number														
	#0	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14
Group 38	2	16	4	5	16	14	7	11	4	11	14	9	9	7	5
Group 39	3	3	4	6	11	12	13	6	12	14	4	5	13	5	14
Group 40	3	3	6	5	16	9	15	5	9	10	6	4	15	4	10
Group 41	3	4	5	14	4	6	12	13	5	13	6	11	11	12	14
Group 42	3	4	9	16	10	4	16	15	3	5	10	5	15	6	6
Group 43	3	4	16	10	5	10	4	9	9	16	15	6	3	5	15
Group 44	3	5	12	11	14	5	11	13	3	6	14	6	13	4	4
Group 45	3	6	4	10	6	5	9	15	4	15	5	16	16	9	10
Group 46	3	7	8	8	16	11	12	4	15	11	4	7	16	3	15
Group 47	3	7	16	11	4	15	3	15	11	12	12	4	7	8	16
Group 48	3	8	7	15	4	8	15	12	3	16	4	16	12	11	11
Group 49	3	8	15	4	16	4	8	7	7	15	12	11	3	16	12
Group 50	3	10	10	15	16	5	4	6	16	4	3	15	9	6	9
Group 51	3	13	11	5	4	12	4	11	6	6	5	3	14	13	12
Group 52	3	14	7	9	14	10	13	8	7	8	10	4	4	13	9
Group 53	5	5	8	14	16	13	6	14	13	7	8	15	6	15	7
Group 54	5	6	11	7	10	8	5	8	7	12	12	10	6	9	11
Group 55	5	6	13	8	13	5	7	7	6	16	14	15	8	16	15
Group 56	5	7	9	10	7	11	6	12	9	12	11	8	8	6	10
Group 57	5	9	6	8	10	9	8	12	5	11	10	11	12	7	7
Group 58	5	10	10	12	8	11	9	7	8	9	5	12	6	7	6
Group 59	5	10	12	6	5	12	8	9	7	6	7	8	11	11	9
Group 60	5	13	15	15	14	8	6	7	16	8	7	13	14	5	16
Group 61	9	10	13	10	11	15	15	9	16	12	14	13	16	14	11
Group 62	9	11	12	15	12	9	13	13	11	14	10	16	15	14	16
Group 63	9	12	10	15	13	14	9	14	15	11	11	13	12	16	10

1.11.3 Modulation

1.11.3.1 Modulating chip rate

The modulating chip rate is 3.84 Mcps.

1.11.3.2 Modulation

Modulation of the complex-valued chip sequence generated by the spreading process is shown in Figure 11 below.

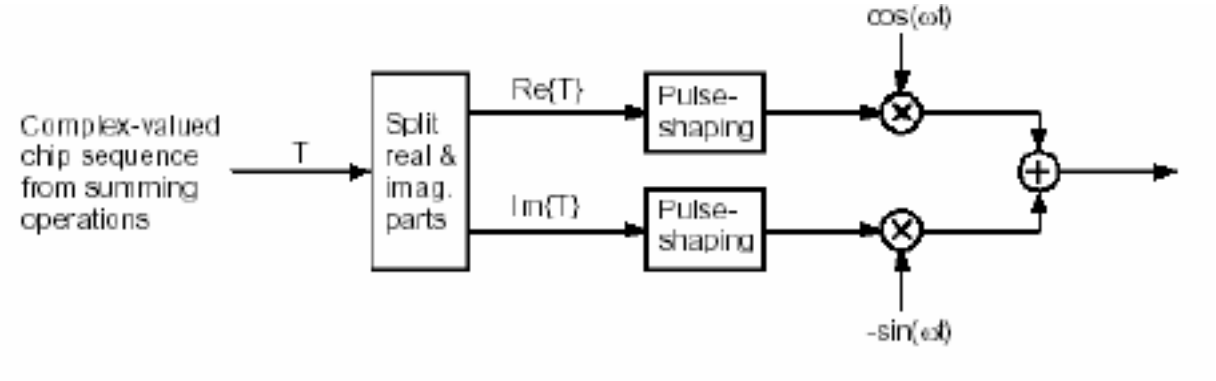


Figure 12: Downlink modulation

The pulse-shaping characteristics are described in 3GPP TS 25.104.

1.11.4 Different User Signaling Modes

From the Radio Base Station point of view doesn't it matter if the user/users have a video call, a data call, a normal speech call or a mix of all at the same time.
This is just a matter of base band signaling with maybe a difference in data volume in the used code packet/packets. This depends on the number of users in the system. For the Radio Equipment is this just seen as stream of data that shall be transmitted in QPSK, 16QAM or 64QAM Modulation depending of what the WCDMA system decides. The outdraw from the 3GPP standard for the three modulation forms above will explain this.