

SCHEMATIC

MODEL : DUALEYE-PCA20

DOC NO : EP06-06-004

PAGES : 10(include cover, history)

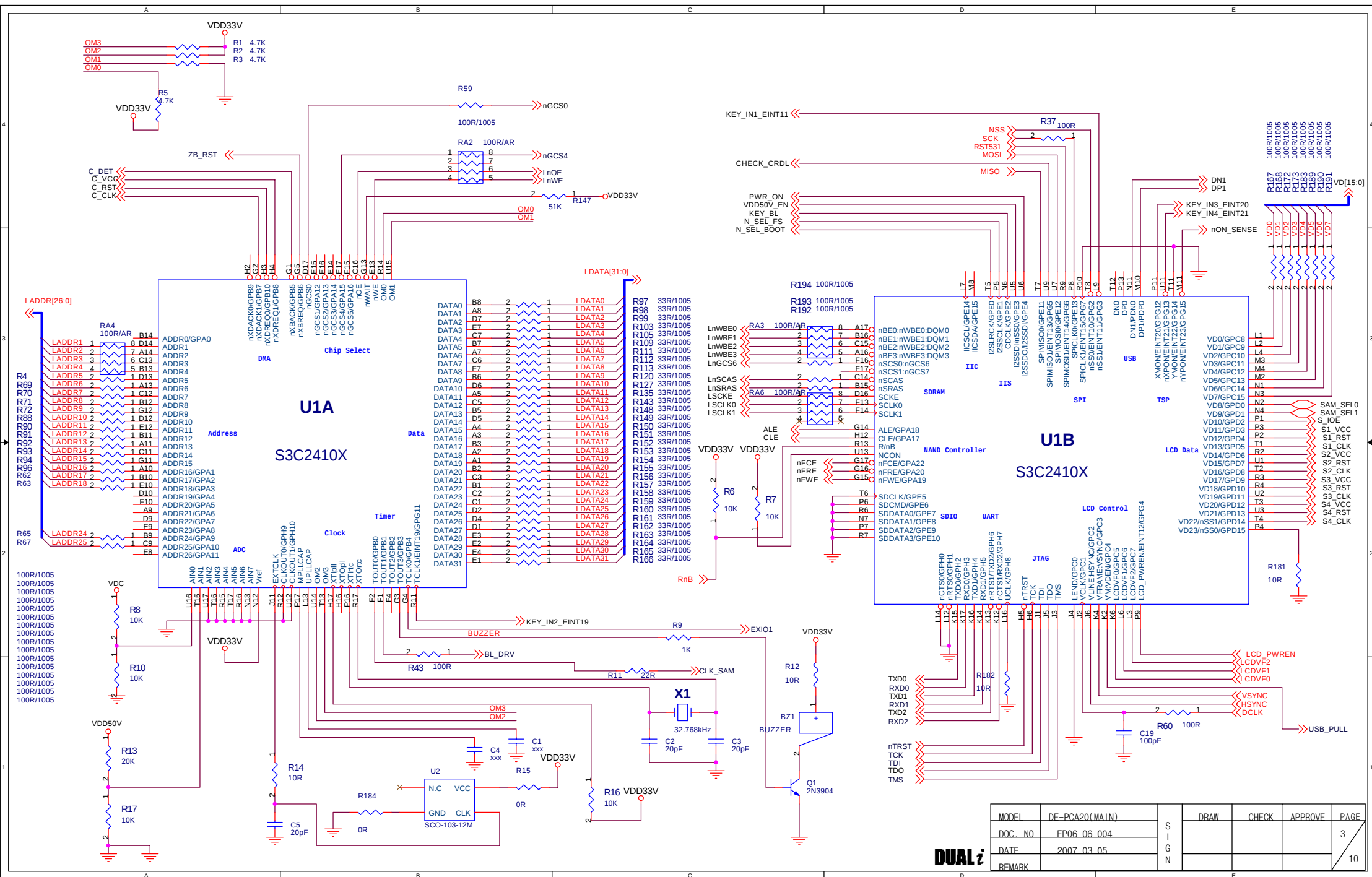
DATE : 2007.03.05

DRAW	CHECK	APPROVE

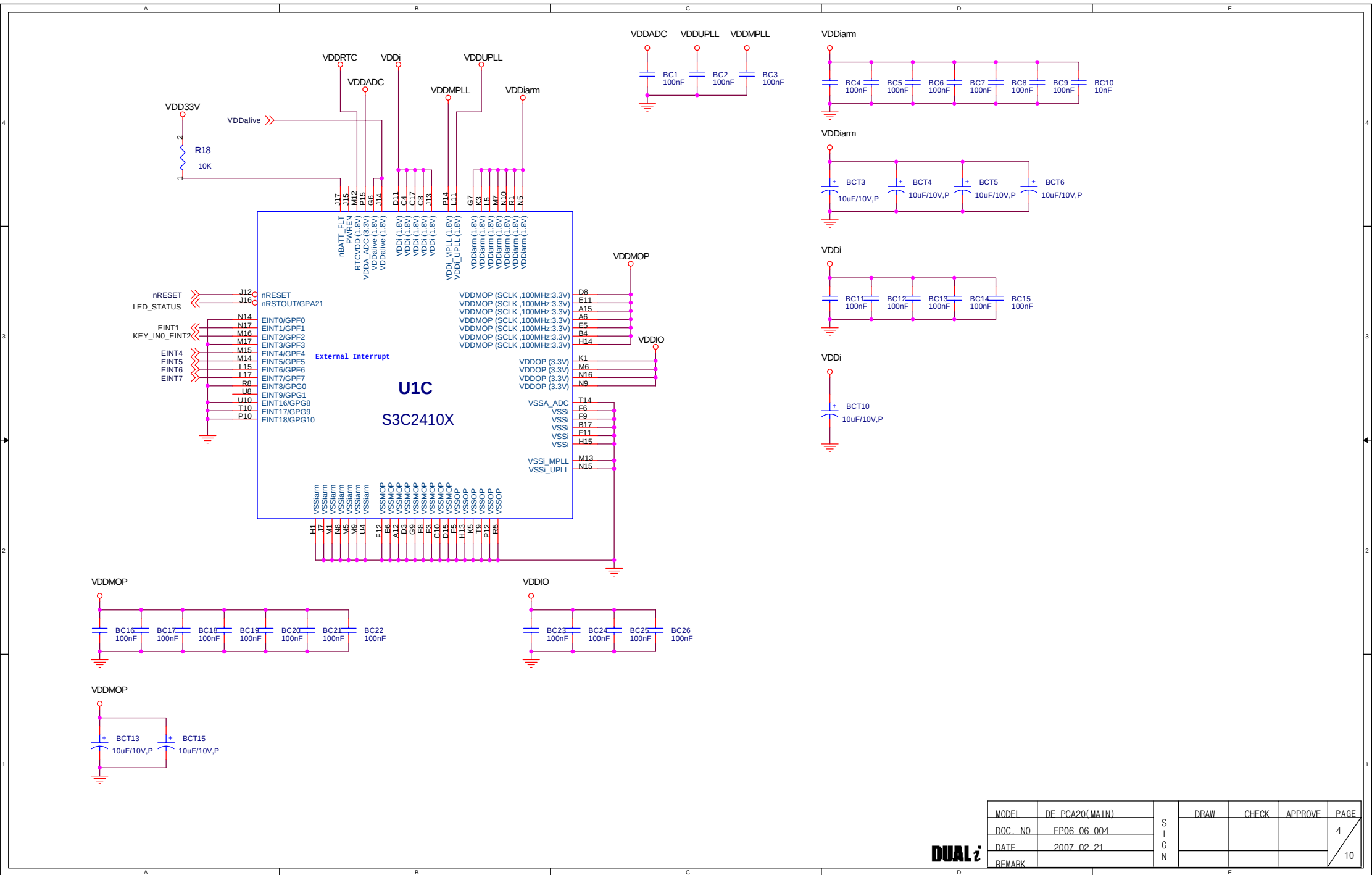
DUAL i INC.

HISTORY

NO	DATE	PAGES	DESCRIPTION
1	2006.09.20	ALL	FIRST DRAW
2	2006.11.13	ALL	Working Sample 후 수정
3	2006.12.14	ALL	P/P 용으 ?배포
4	2006.12.29	3,4,5,8,11	CPU 안쓰는 핀 GND 연결, Oscillator 주변 bead(저항) Test Point 저항처리, Nand CS 앞 ?저항추가, 안쓰는 LCD 콘넥터(J10) 제거 RF(J5)-접촉식 카드(J4) 콘넥터 합쳐서 DIP 콘넥터 하나로 변경(J5)
5	2007.02.05	3,5,6,8	3Page(U1 E15,E16,F10,F15,A9,D9,E8,E9 GND -> OPEN, R4,R37,R43추가) 5Page(U8C, U8D 韃뺏?GND 연결) 6Page(BD7, Q4추가, C6,C11,C19 추가) 8Page(U20 6번 ?GND 연결)
6	2007.02.21	3,5,6,7,10,11	3Page : RA1->R59 / insert R at DATA,ADDR,VDATA BUS / R60,C19 insert 5Page : Bead insert at SDRAM POWER / cap relocate 6Page : 3.3V, 5V, 2V inductor(L9,10,11) insert / cap relocate 7,10Page : Change cradle 232 comm to RS_TXD, RS_RXD / LAN delete 11Page : C72 insert
7	2007.03.05	3,7	DATA line 저항 100R-> 33R, 방사 대책 부품 교체(값 수정)
8			
9			
10			
11			
12			
13			

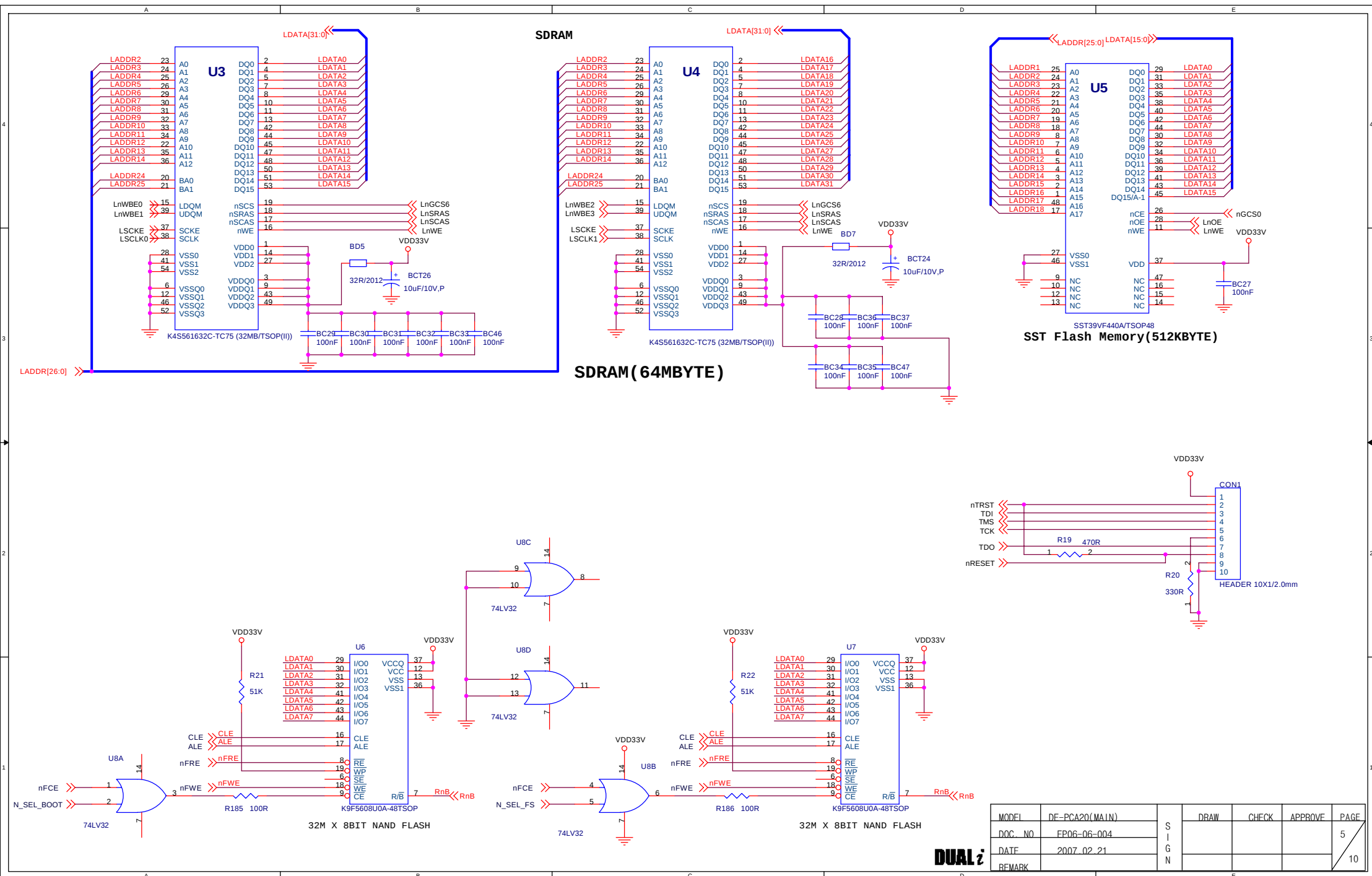


MODEL	DE-PCA20(MAIN)	SIGN	DRAW	CHECK	APPROVE	PAGE
DOC. NO	EP06-06-004					3
DATE	2007.03.05					10
REMARK						

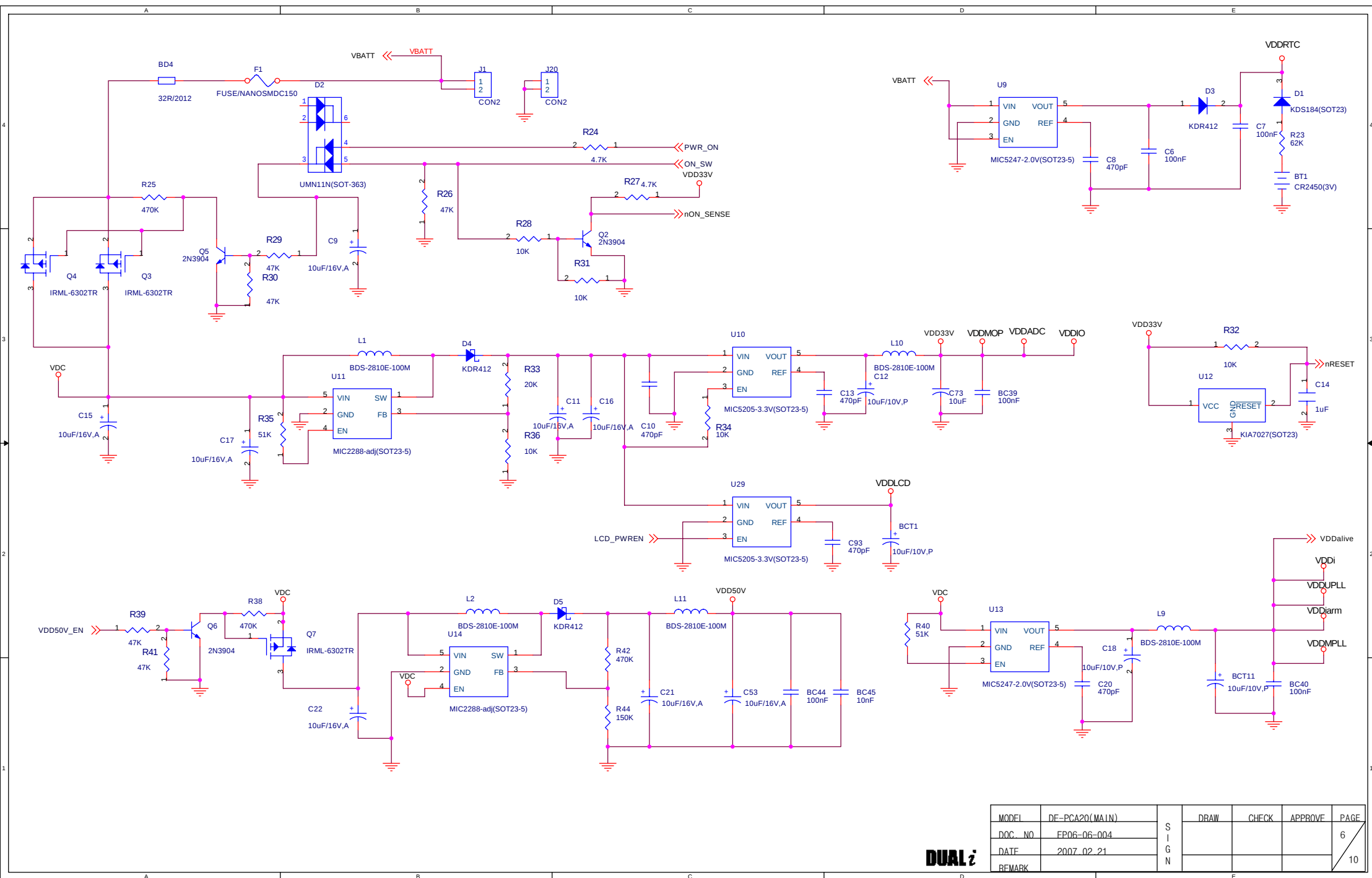


MODEL	DE-PCA20(MAIN)	S I G N	DRAW	CHECK	APPROVE	PAGE
DOC. NO	FP06-06-004					4
DATE	2007.02.21					10
REMARK						

DUALi



MODEL	DE-PCA20(MAIN)	S I G N	DRAW	CHECK	APPROVE	PAGE
DOC. NO	FP06-06-004					5
DATE	2007.02.21					10
REMARK						



MODEL	DF-PCA20(MAIN)	S I G N	DRAW	CHECK	APPROVE	PAGE
DOC_NO	FP06-06-004					6
DATE	2007.02.21					10
REMARK						

DUALi

