

# General Technical Description

**Model: T10**

**Date: 2012-08-14**

## 1. Scope

This document is shown and provided the more detail information about the platform we used. The basic description for the processor is also included.

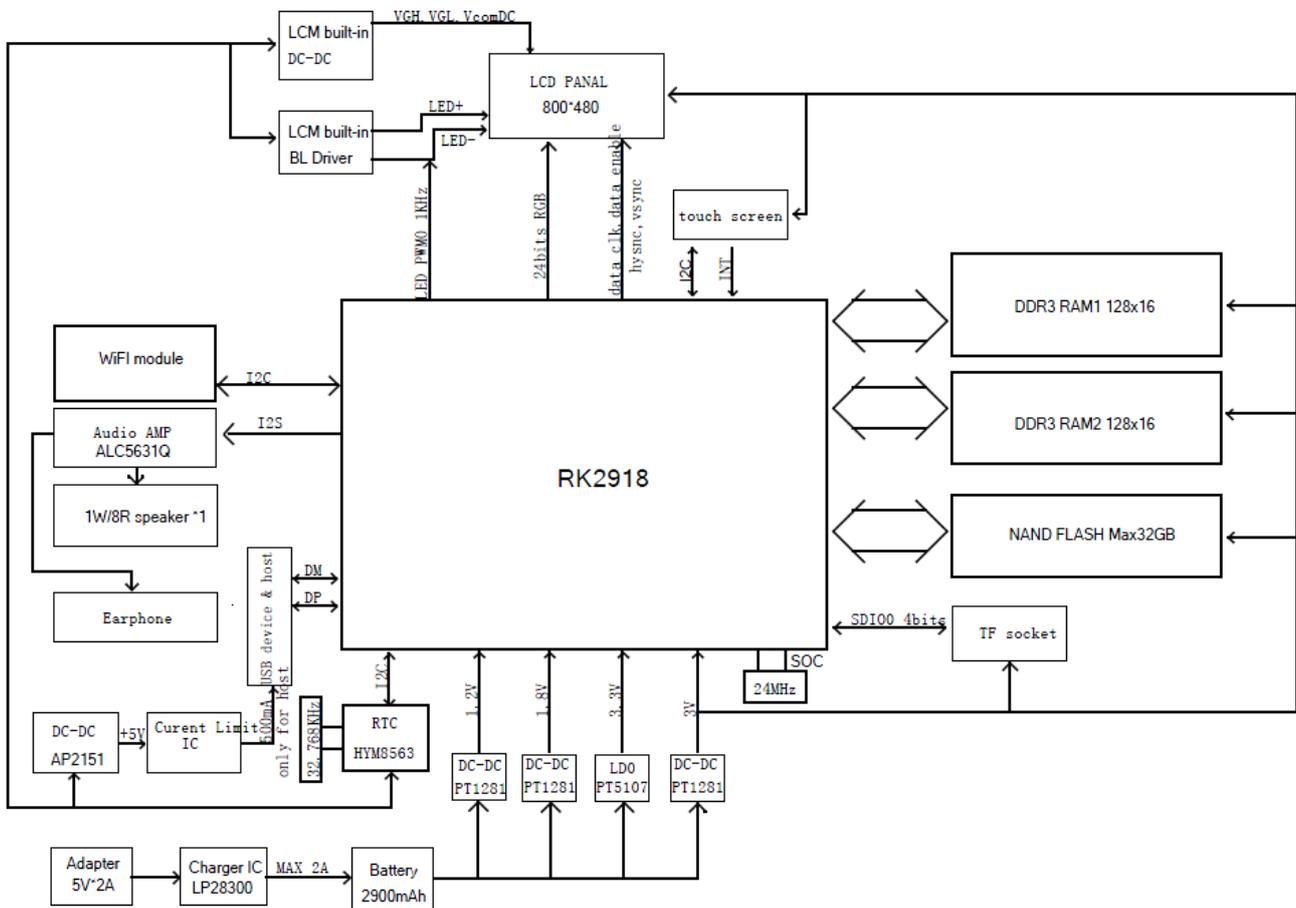
This product is a MID (Mobile Internet Devices) on Rockchip platform.

The Device has 7' multipoint Touch panel and 7'LCD, Touch points maximum five points. The maximum resolution is 800\*600.

This MID product can access to the Internet to enable high-speed network access experience via Fast Ethernet network by an embedded Wi-Fi module. It also has one USB 2.0 ports and one SD card port.

The main IC include the Processor (RK2918), DDRII (NT5CB256M8BN), FLASH (MT29F64G08CBA), Wi-Fi Module (RL-UM02BS-8188CUS-33), There is a DC jack on One Touch View for power supply through a 5V/2A adapter.

## 2. Detail Block Diagram



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### 3. Processor

RK2918 is a low power, high performance processor solution for mobile phones, personal mobile internet device and other digital multimedia applications.

RK2918 integrates an ARM Cortex-A8 with one NEON coprocessor. Many embedded powerful hardware accelerators provide optimized hardware performance for high-end application. RK2918 supports almost full-format video decoder by 1080p@30fps such as H264, H263, RMVB, MPEG2, MPEG4, VC1, AVS, VP8 etc. Also supports H.264 encoder by 1080P@30fps, high-quality JPEG encoder/decoder and special image preprocessor and postprocessor.

RK2918 has high-performance external memory interface (DDR3/DDR2/LPDDR) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications as follows:

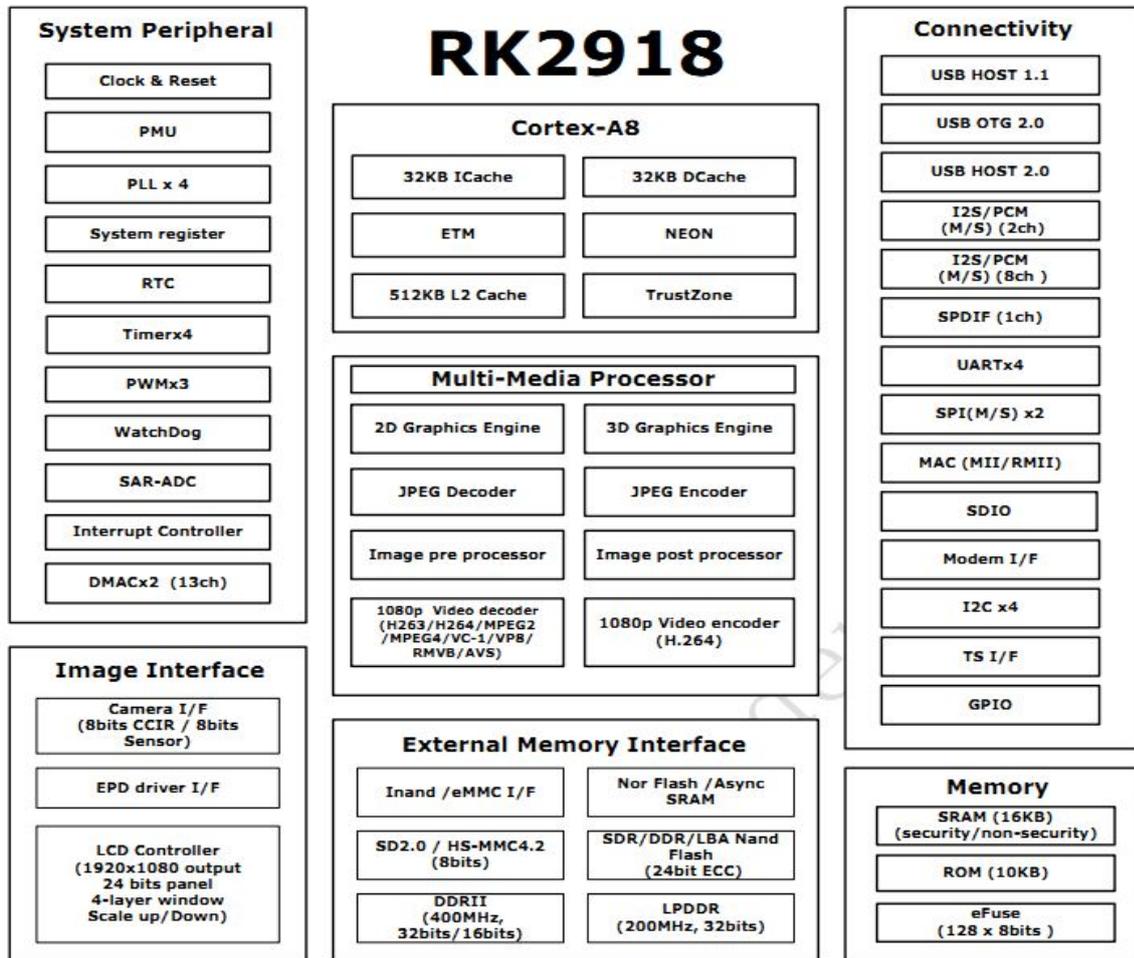
2 banks, 8bits/16bits Nor Flash/SRAM interface; 8 banks, 8bits/16bits Async NAND FLASH, LBA NANDN Flash, 8bits sync ONFI; NAND Flash, all embedded 24bits HW ECC; 2 ranks, 2GB Memory space, 16bits/32bits DDR3,DDR2-800,LPDDR-400; 8bits HS-MMC/SD, 4bits SDIO, 8bits eMMC interface; 24bits high-performance, 3-layers TFT LCD Controller with post-processor; 1920x1080 maximum display size; eBook display interface with 2048x2048 maximum resolution; 8bits sensor/CCIR656 interface and 10bits/12bits Raw data interface; 2ch I2S interface, 8ch I2S interface, PCM/SPDIF interface; USB OTG 2.0/USB Host2.0/ USB Host 1.0; RMI/MII interface; High-speed ADC interface, TS stream interface; 8bits/16bits async modem interface; 4x I2C, 4xUART with hardware flow-control , 2x SPI , 2x PWM

ARM Cortex-A8 processor is a high-performance, low-power, cached application processor that provides full virtual memory capabilities Full implementation of the ARM architecture v7-A instruction set superscalar processor featuring technology for enhanced code density and performance Embedded NEON technology for multimedia and signal processing by executing Advanced SIMD and VFP instruction sets Jazelle RCT Java-acceleration technology for efficient support of ahead-of-time and just-in-time compilation of Java and other byte code language Thumb-2 technology for greater performance, energy efficiency and code density TrustZone technology for secure transactions and DRM 13-stage main integer core pipeline and 10-stage NEON media core pipeline Dynamic branch prediction with branch target address cache, global history buffer and 8-entry return stack MMU and separate instruction and data TLBs of 32 entries each 64-bit high-speed AXI interface supporting multiple outstanding transactions Integrated 32KB L1 instruction cache , 32KB L1 data cache, 512KB L2 Cache with parity and ECC check ETM support for non-invasive debug, support JTAG and 8-wire trace interface ARMv7 debug with watchpoint and breakpoint registers and a 32-bit APB slave interface to a coresight debug system Four separate power domain to support Internal power switch on/off based on different application scene(Integer core/ETM&DBG/Neon/L2 Cache) Maximum frequency can be up to 650MHz@worst case and 1GHz@typical case

Shared internal memory and bus interface for video decoder and encoder

Video Decoder Real-time video decoder of MPEG-1, MPEG-2, MPEG-4,RMVB,H.263, H.264,AVS,VC-1, RV, VP8 , Sorenson Spark Error detection and concealment support for all video formats Output data structure after decoder is YCbCr 4:2:0 semi-planar to have more efficient bus usage, For H.264, YCbCr 4:0:0(monochrome) is also supported Minimum image size is 48x48 for all video formats

The RK2918 device architecture is illustrated in below Figure.



#### 4. Wi-Fi Support Modulation

MODE	Modulation
802.11b	DBPSK,DQPSK
802.11g	BPSK, QPSK,16-QAM,64-QAM
802.11n	BPSK, QPSK,16-QAM,64-QAM