

**VIA P4M266 SOCKET478 Micro-ATX M/B  
PFM-12V RA-2 Schematics**

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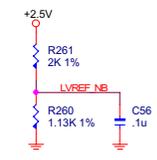
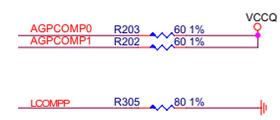
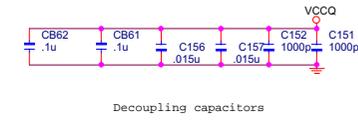
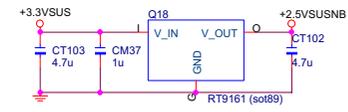
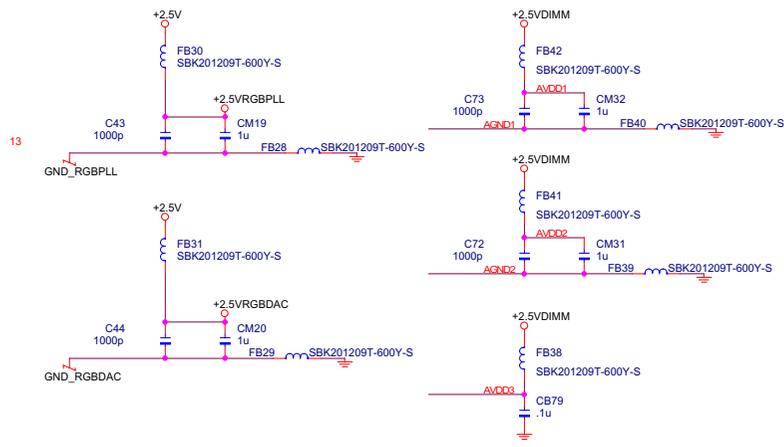
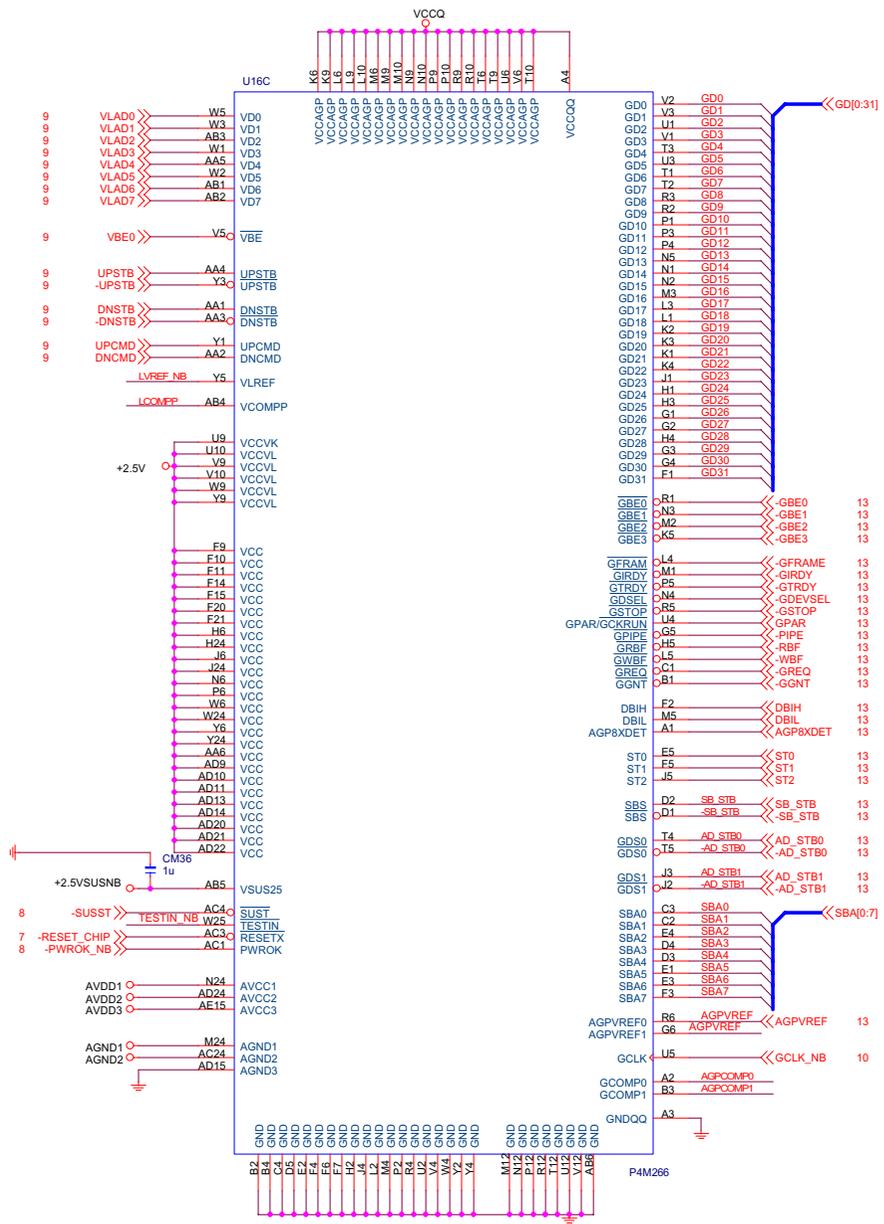
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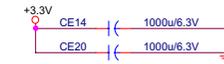
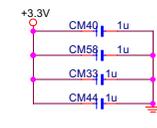
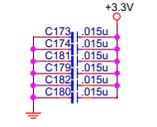
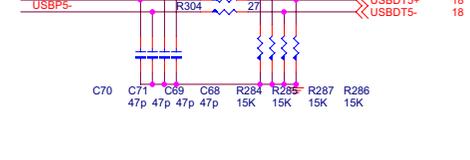
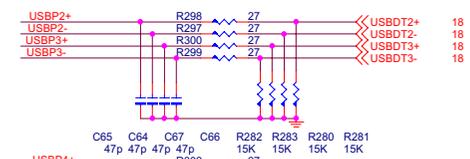
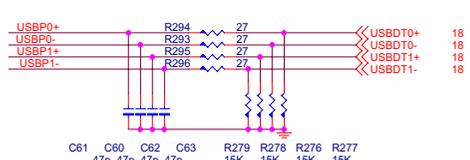
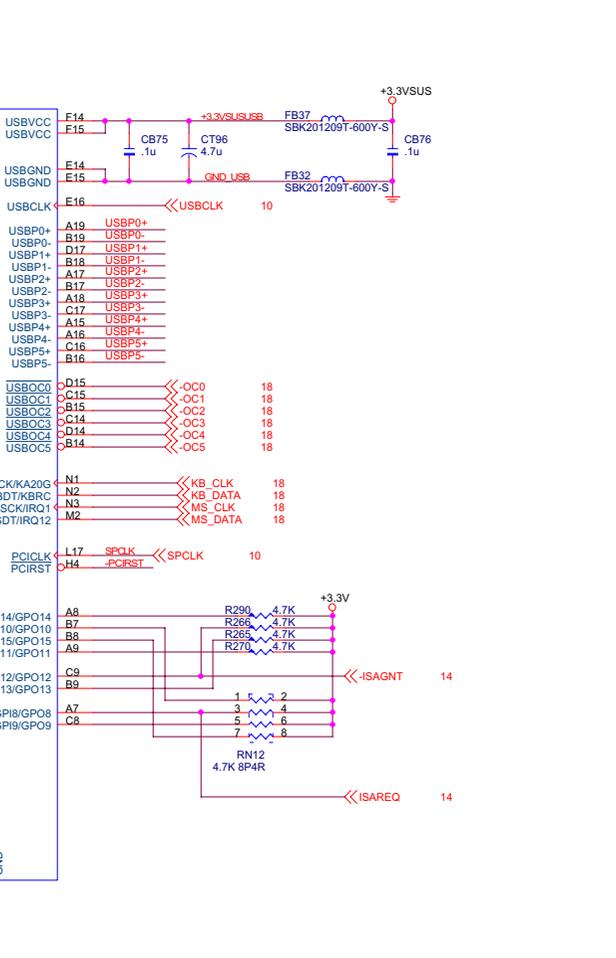
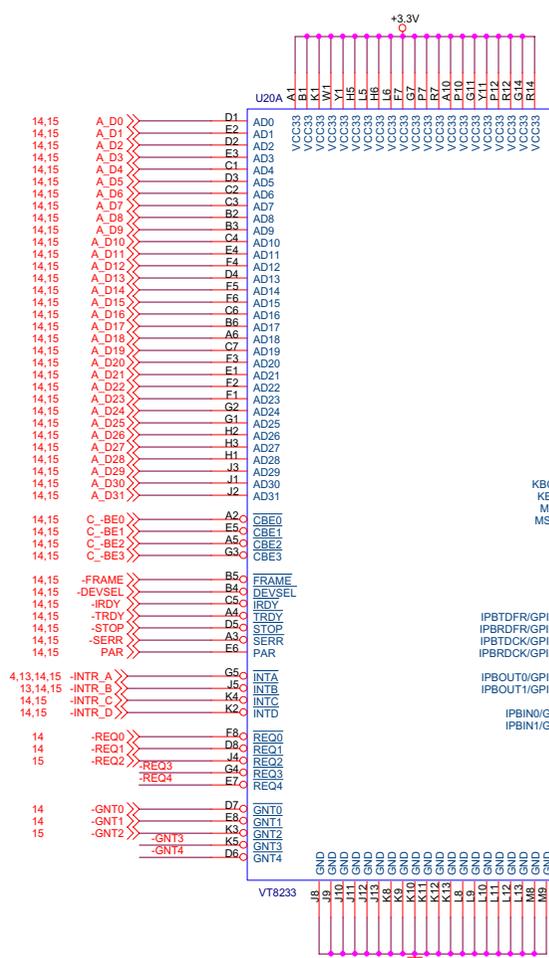




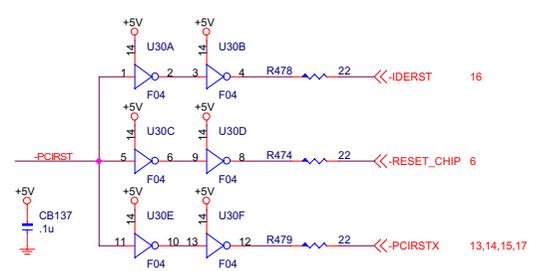
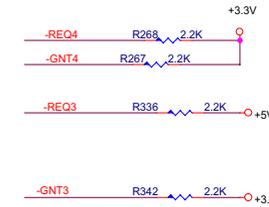




The voltage level of LVREF\_NB is 0.9V



SB Decoupling capacitors

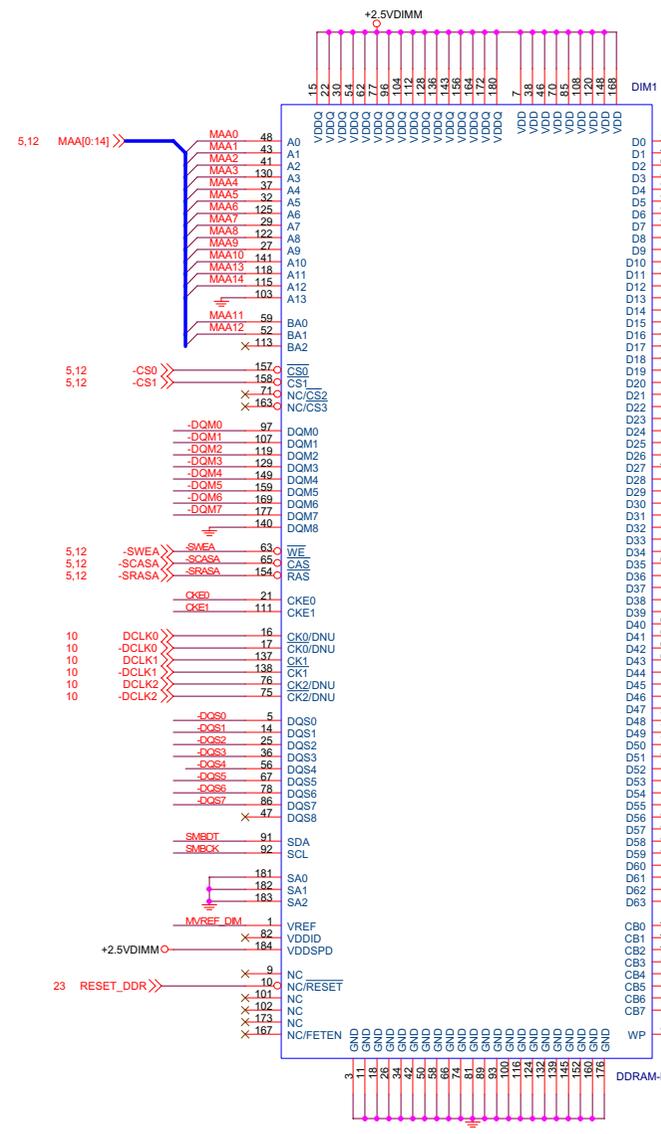


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SOUTH BRIDGE (PART1)		
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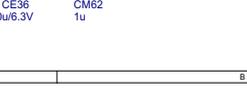
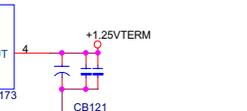
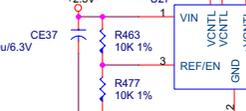
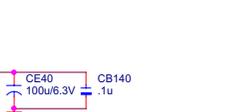
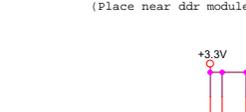
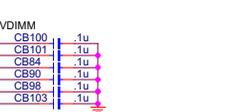
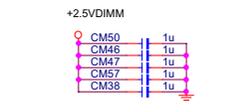
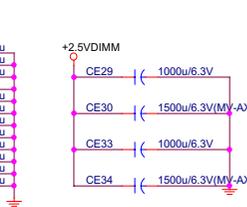
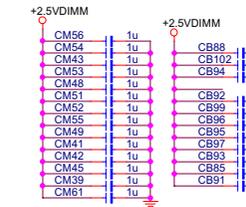
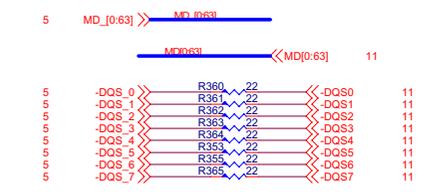
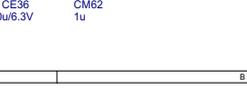
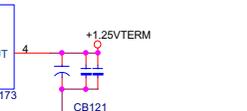
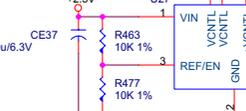
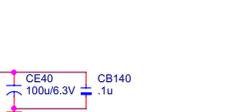
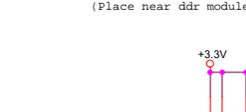
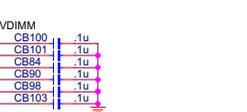
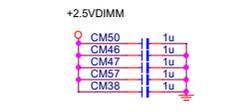
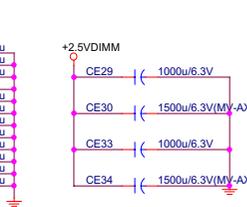
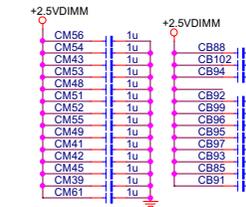
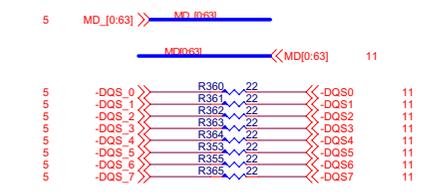
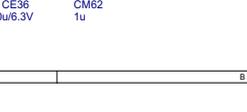
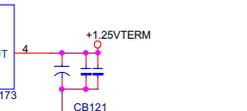
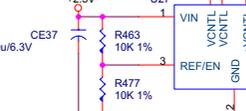
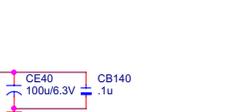
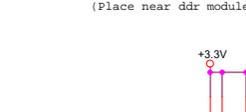
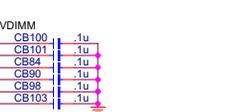
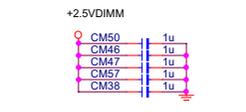
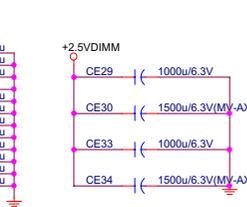
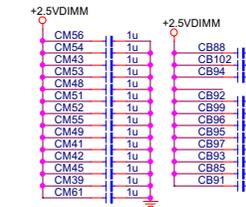
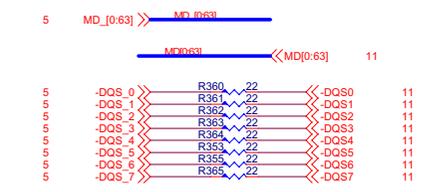
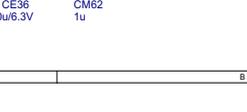
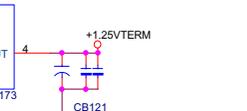
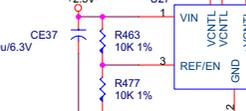
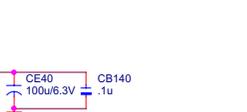
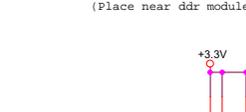
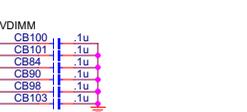
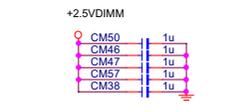
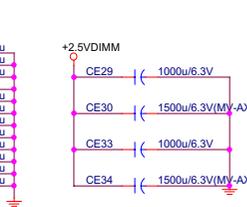
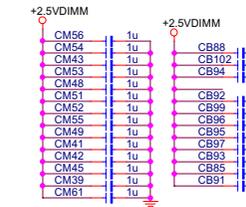
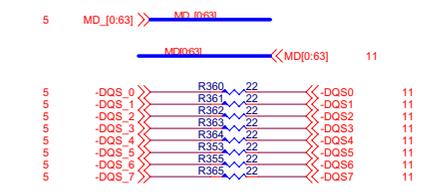
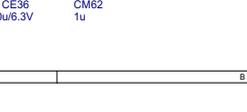
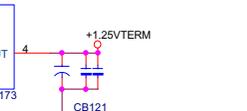
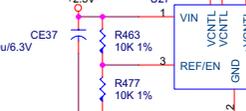
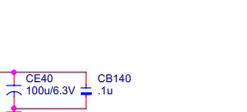
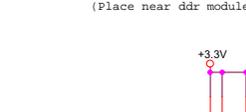
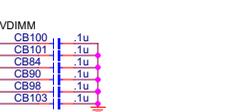
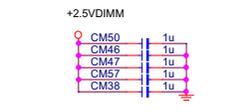
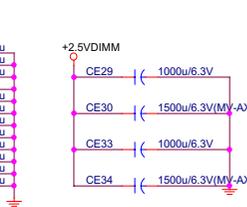
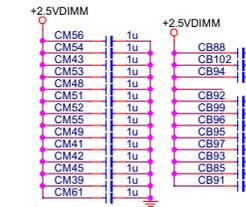
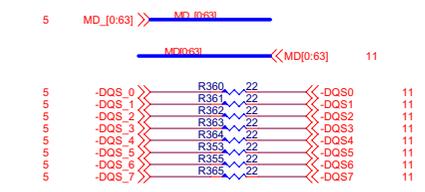
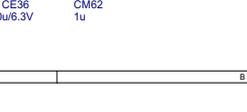
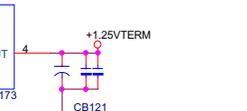
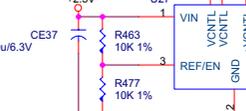
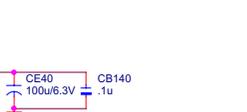
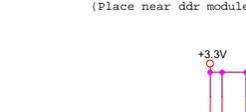
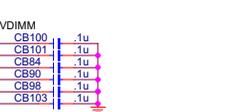
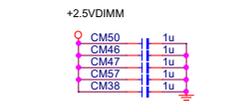
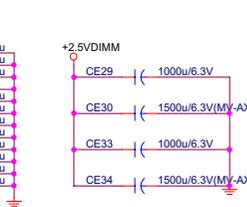
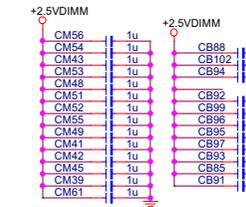
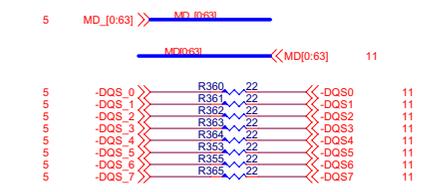
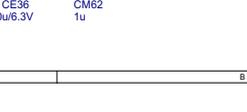
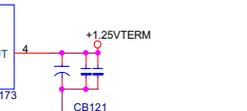
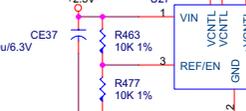
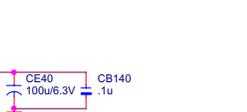
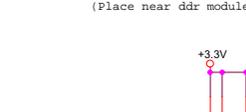
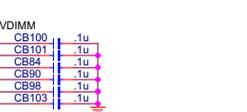
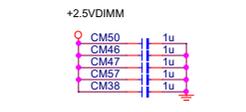
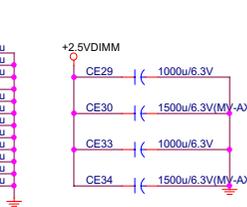
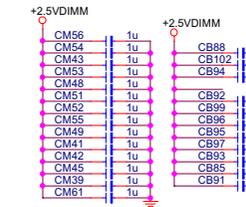
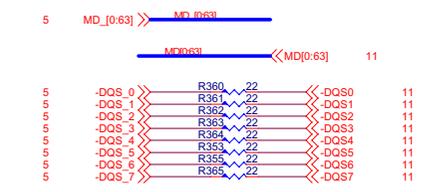
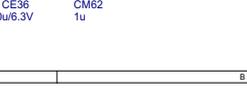
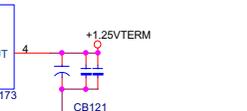
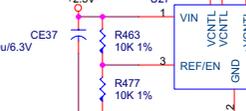
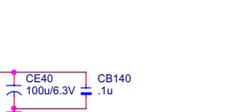
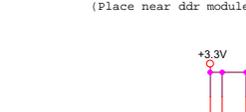
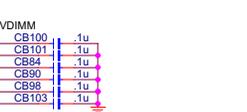
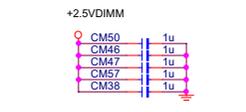
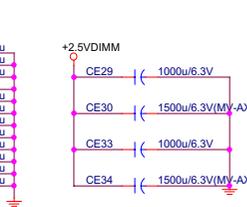
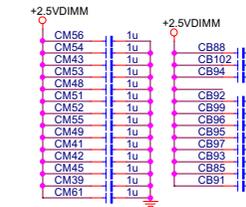
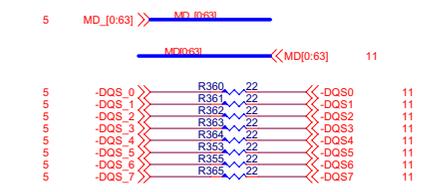
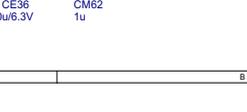
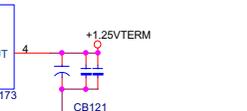
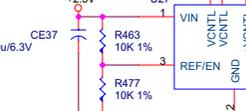
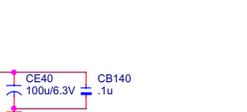
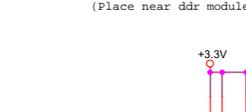
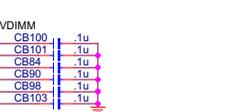
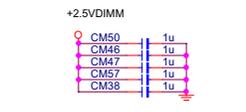
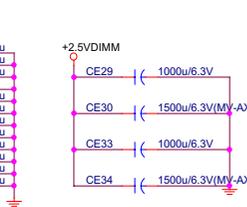
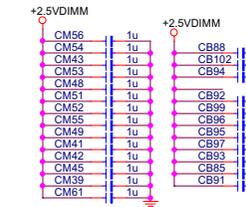
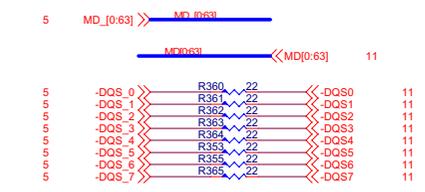
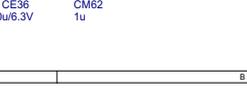
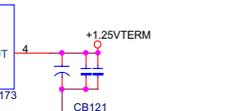
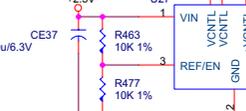
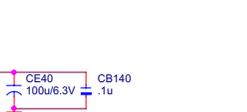
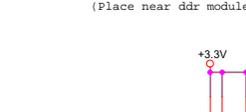
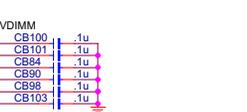
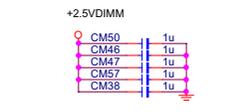
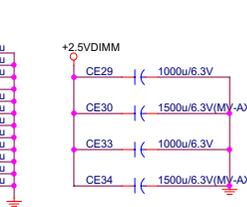
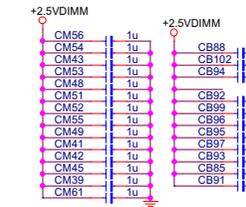
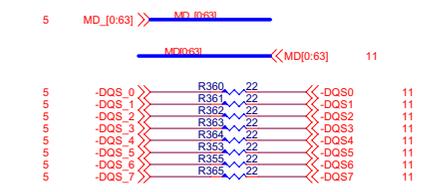
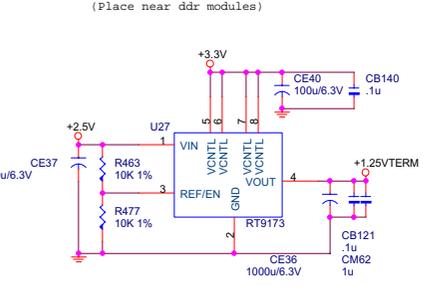
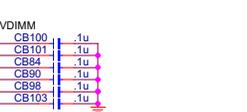
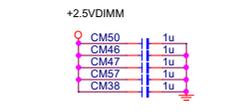
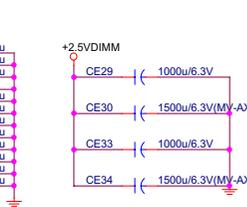
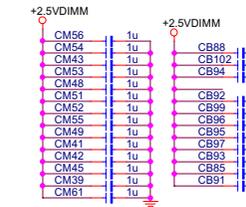
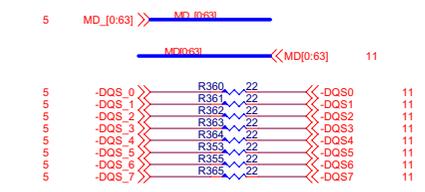
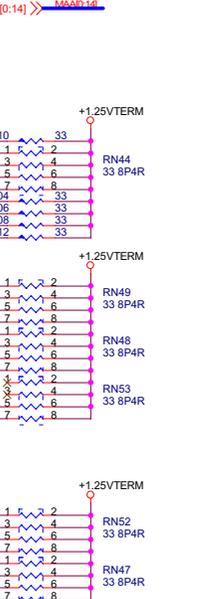
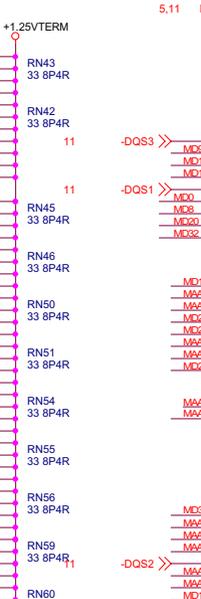
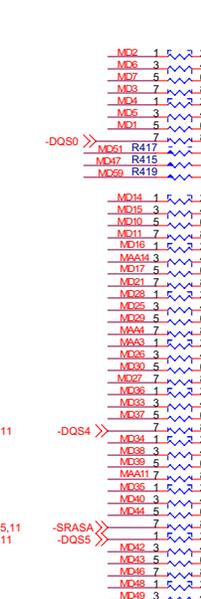
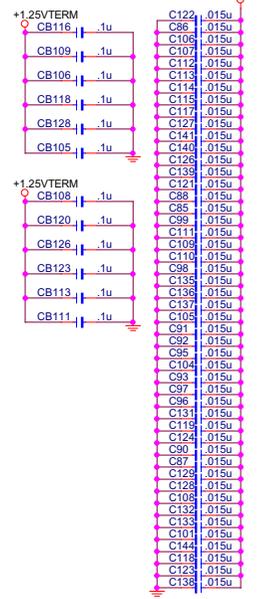
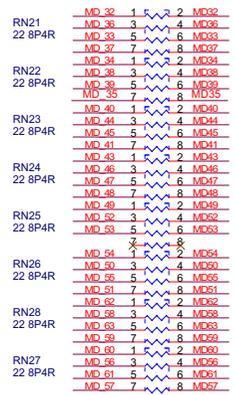
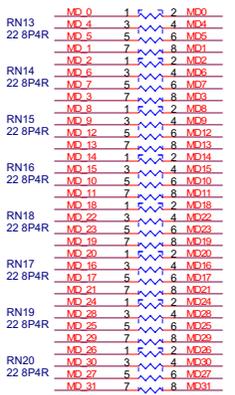




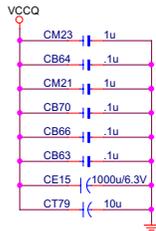
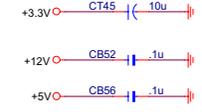
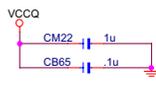
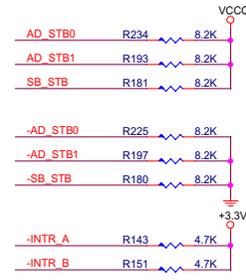
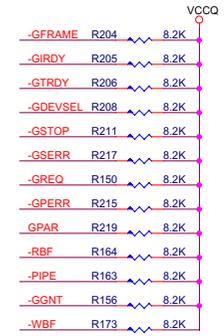
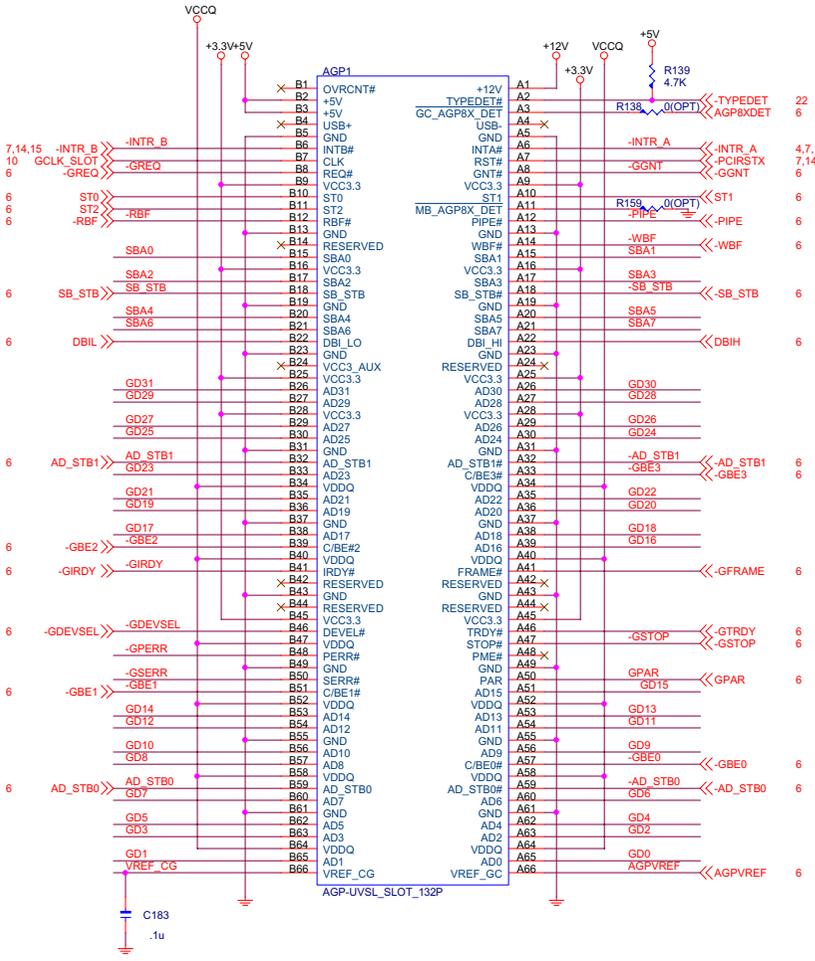




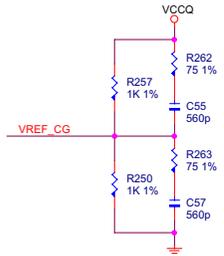
NOTE: Place these decoupling capacitors close to VTT\_MEM termination resistors. (one decoupling capacitor for each two R-packs)



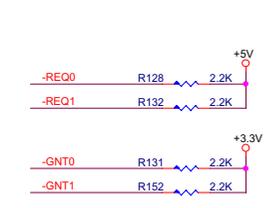
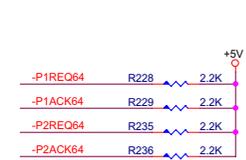
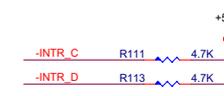
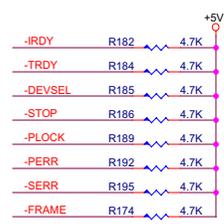
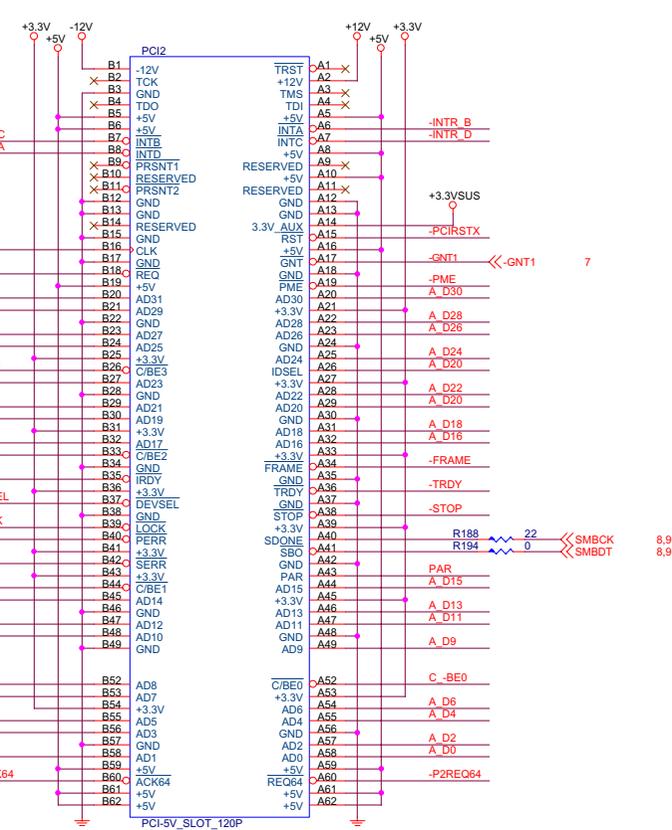
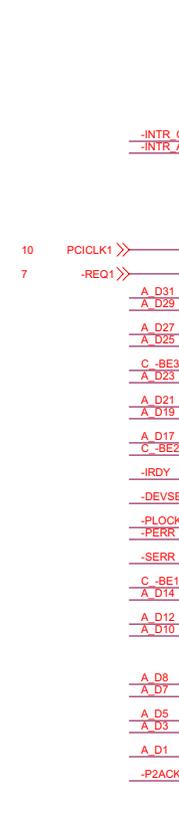
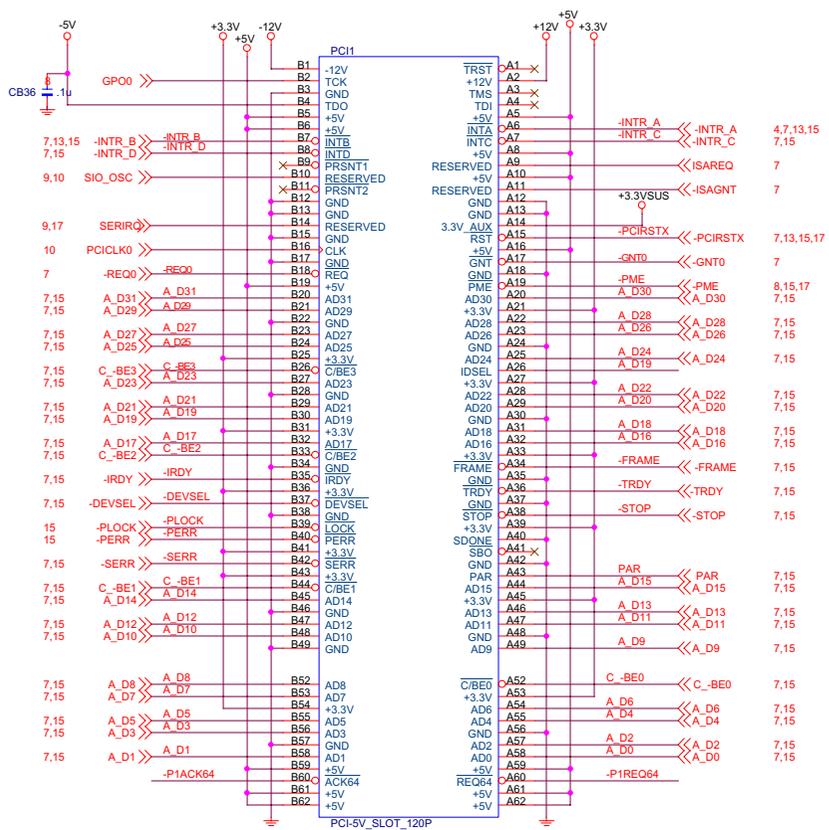
6 SBA[0:7] >> SBAN7  
 6 GD[0:31] >> GDN31



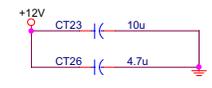
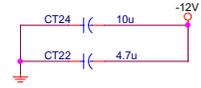
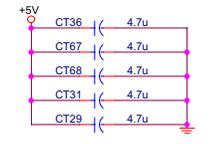
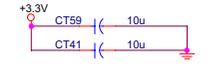
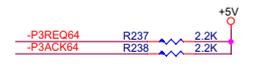
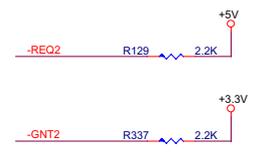
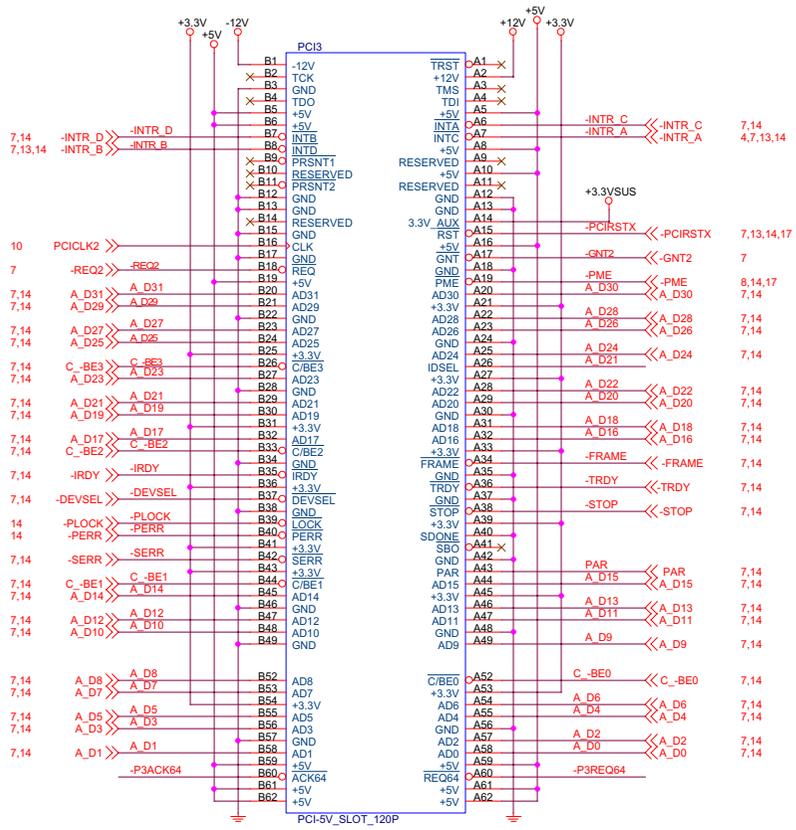
Decoupling capacitors  
 (Place near AGP slot)



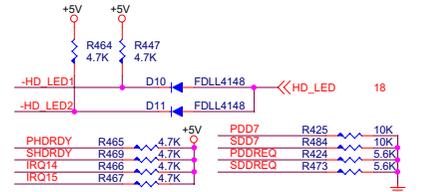
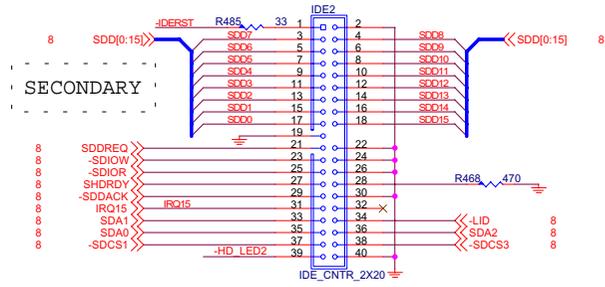
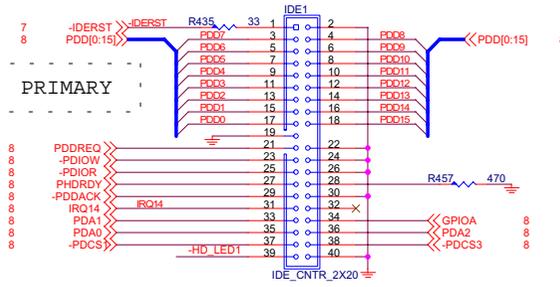
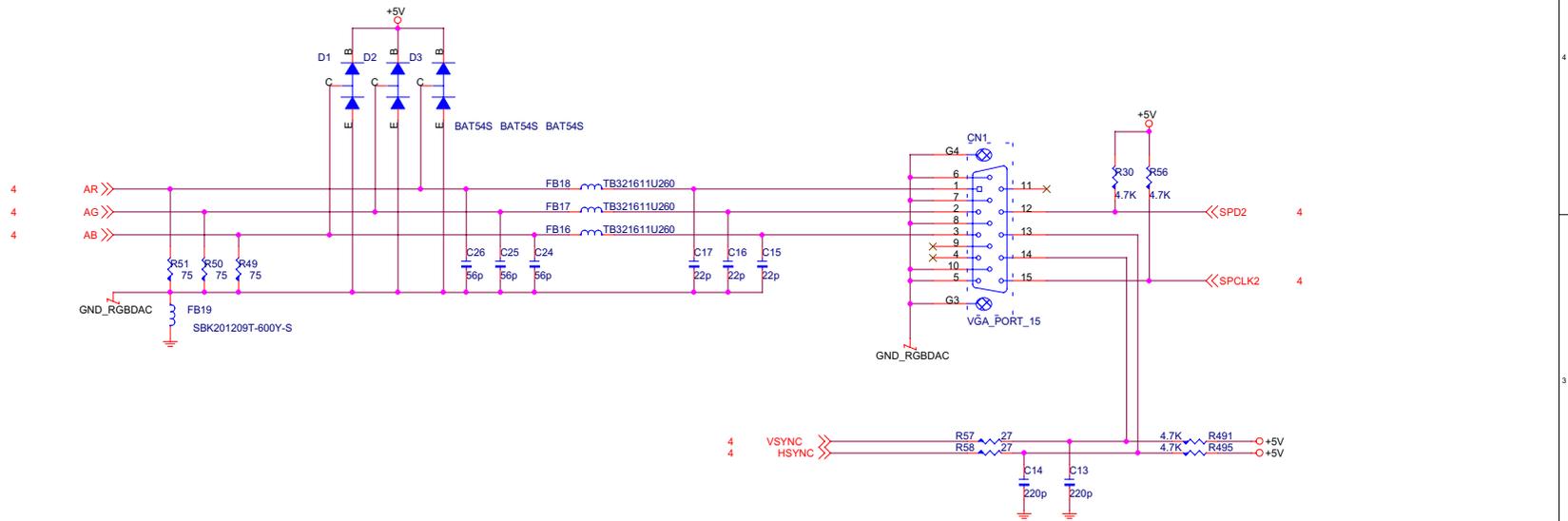
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Title PCI1 & PCI2 SLOTS		
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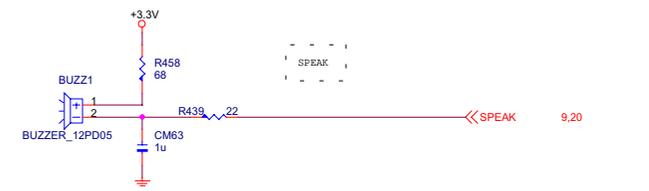
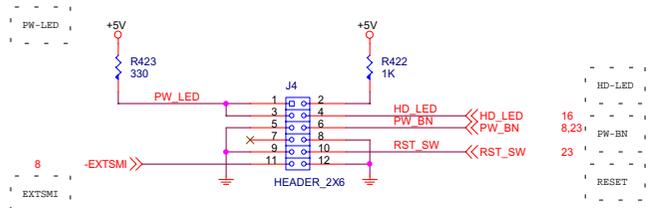
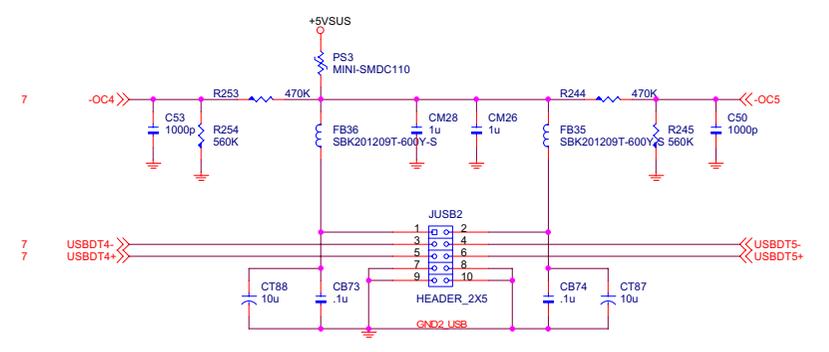
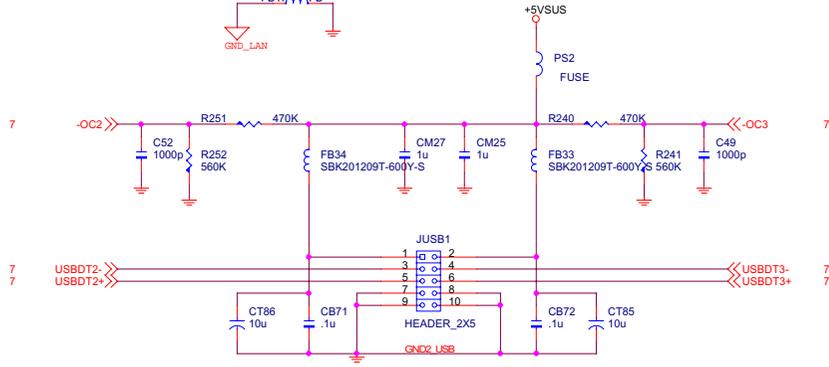
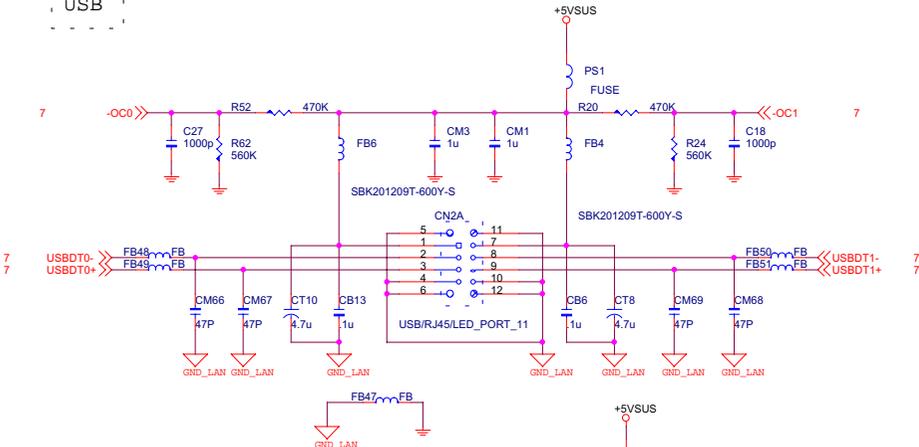
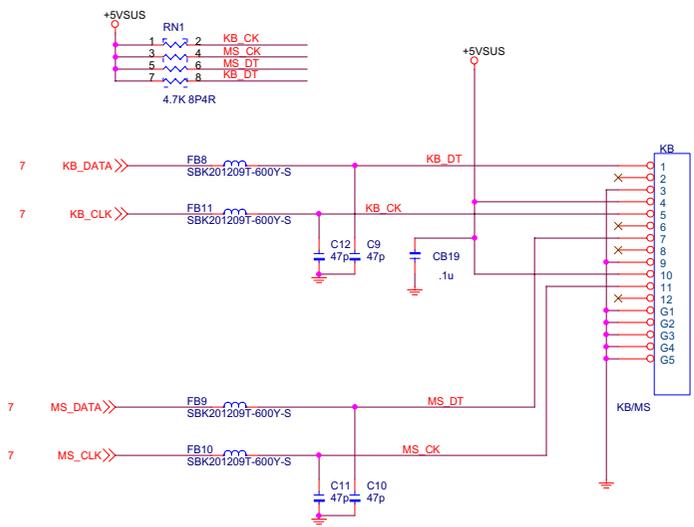
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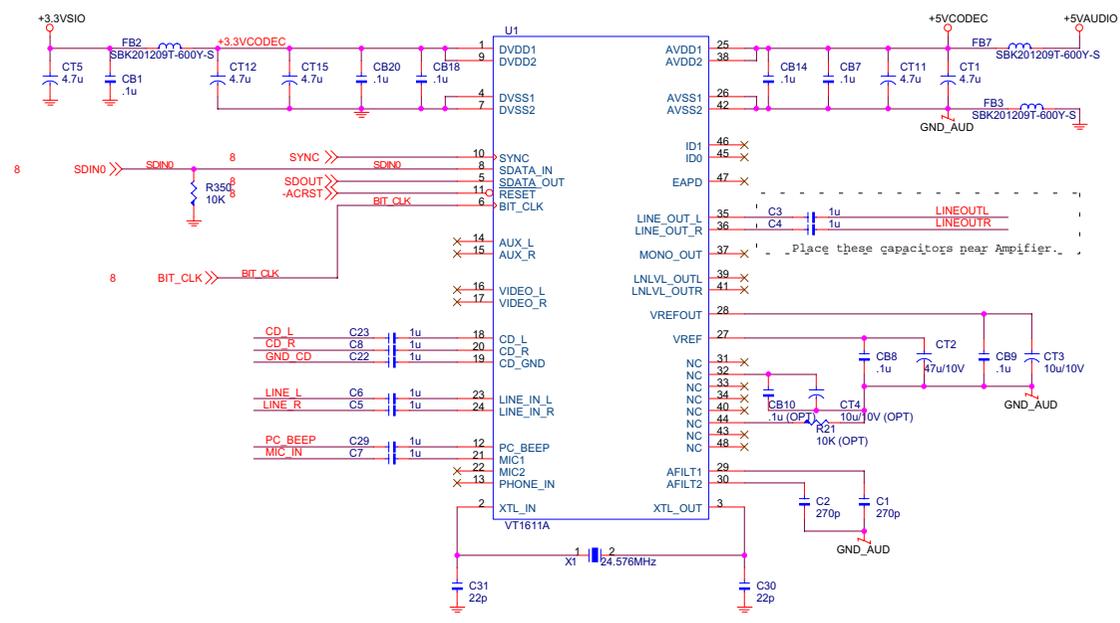
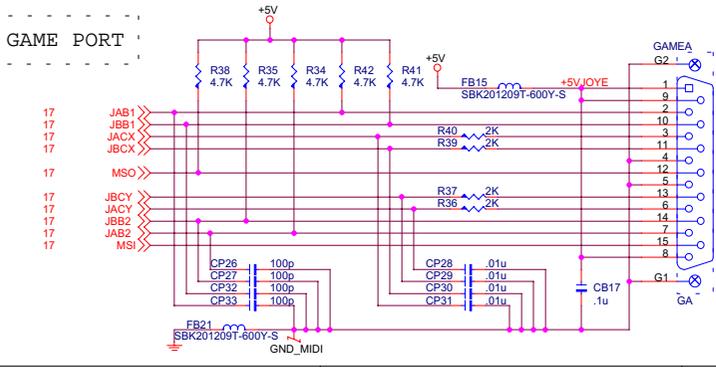
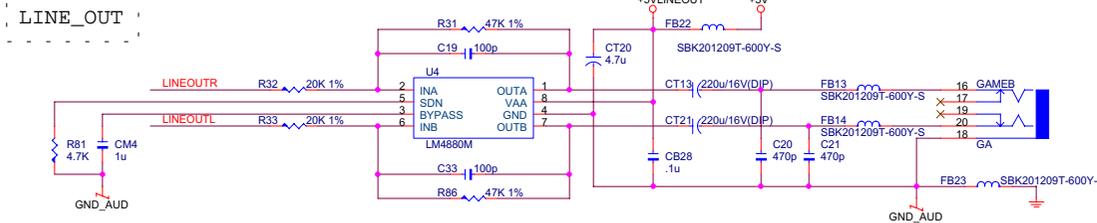
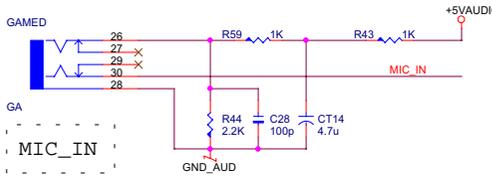
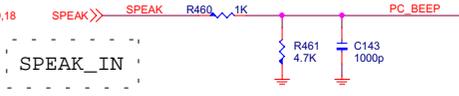
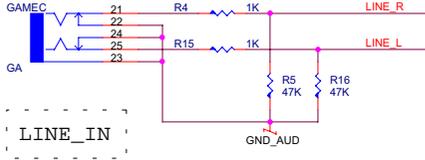
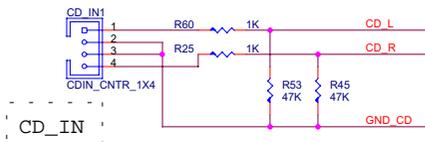


USB

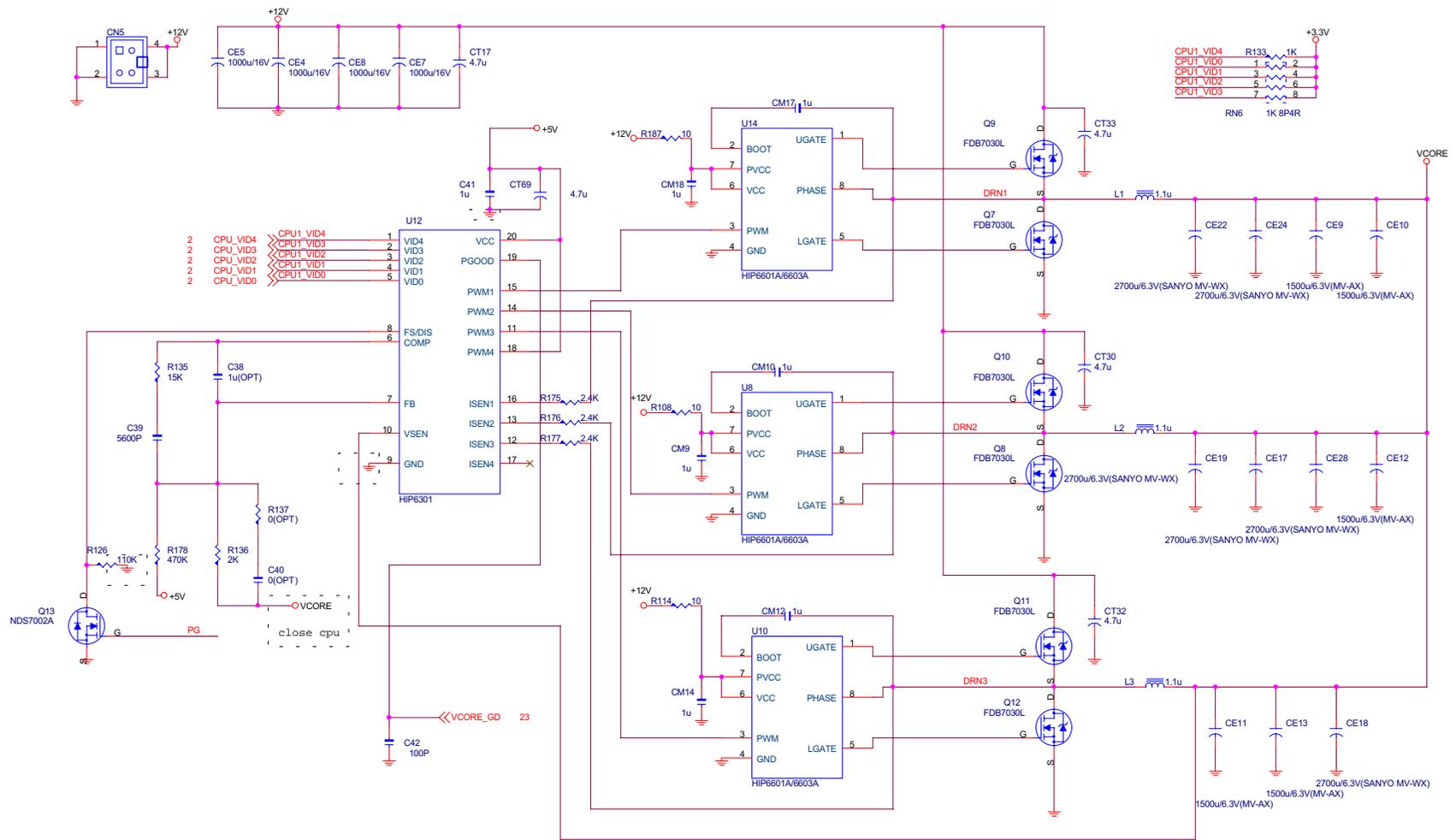


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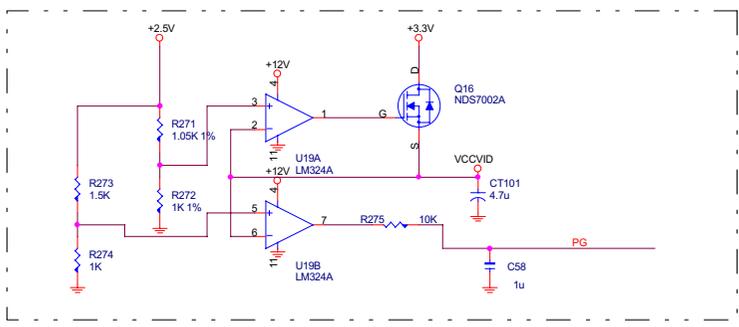


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- 2 CPU\_VID4 CPU1\_VID4
- 2 CPU\_VID3 CPU1\_VID3
- 2 CPU\_VID2 CPU1\_VID2
- 2 CPU\_VID1 CPU1\_VID1
- 2 CPU\_VID0 CPU1\_VID0

- CPU1\_VID4 R133 1K
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- CPU1\_VID2 5 6
- CPU1\_VID3 7 8
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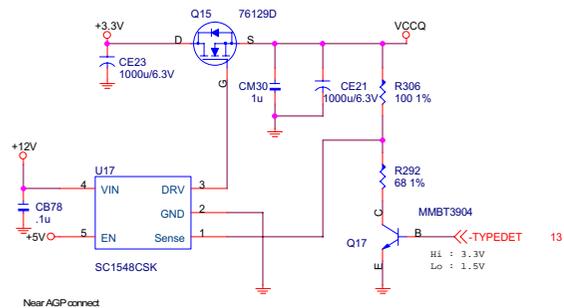
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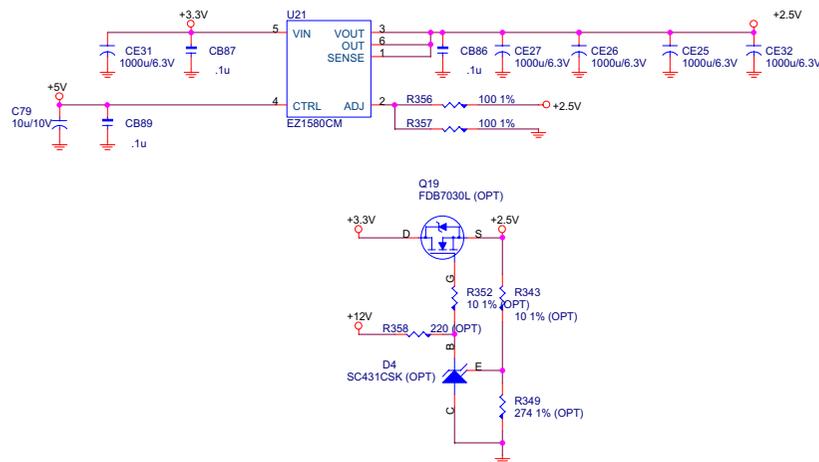
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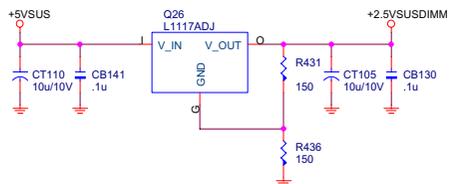
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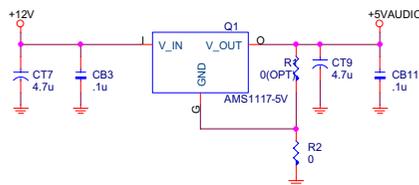
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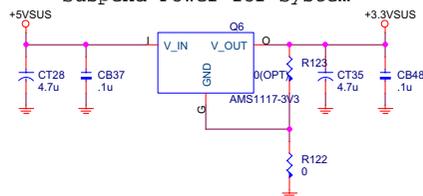
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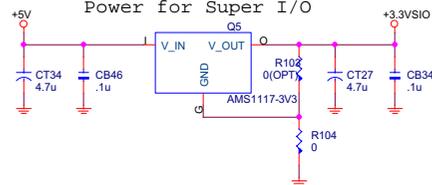
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Suspend Power for System



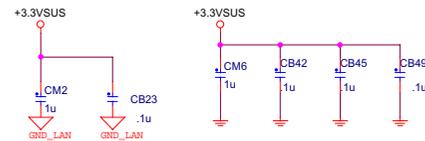
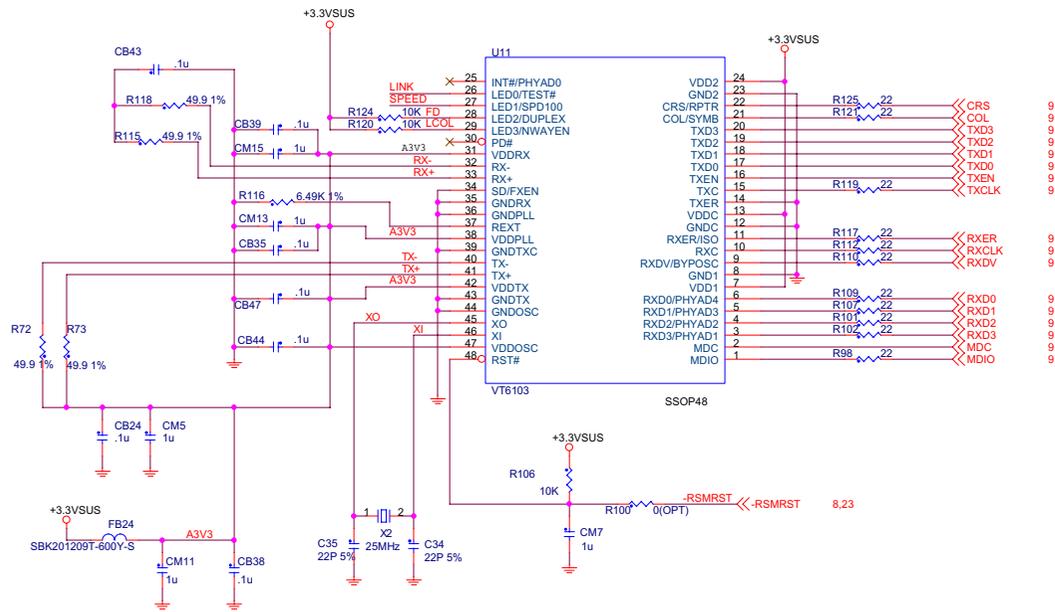
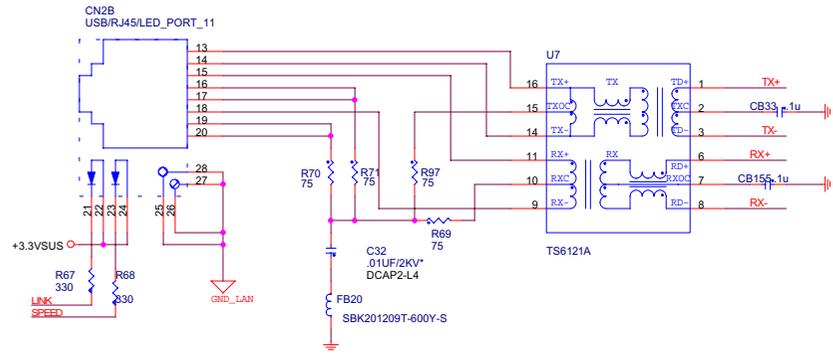
Power for Super I/O



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