BD23 Circuit Description:

CATEGORY	PART NUMBER	PART NAME	DESCRIPTION
Antenna	ANT002-2G450	Chip antenna (U2)	Chip antenna
Module	BTR200A	Bluetooth Module (U1)	2.4GHz Bluetooth Module
LED	KP-1608QBC-C	LED (D1)	LED BLUE
Switch		Switch (U6)	Tact Switch for On/Off
Battery	“AAA” 1.5V	Battery	Alkaline battery
IC	L6920DA	Converter IC (U7)	Step Up Converter
IC	XC6024B332MR	Regulator (U4)	Voltage Regulator 3.3V
IC	XCS921A18CMR	DC-DC Converter (U5)	DC-DC CONVERTER 1.8V
IC	USB6BX	Double transistor (U8)	DATA LINES PROTECTION
Socket	PQC-6GUDU-05S-X01	USB Socket (U3)	Mini USB B 5pin Socket
TRANSISTOR	MMBT3904LT1	Transistor (Q5)	NPN general purpose transistor

BLUETOOTH SPECIFICATION

1. FREQUENCY BANDS AND CHANNEL ARRANGEMENT

The Bluetooth system operates in the 2.4 GHz ISM band. This frequency band is 2400 - 2483.5 MHz.

Regulatory Range	**RF Channels**
2.400-2.4835 GHz	f=2402+k MHz, k=0,…,78

Table 1.1: Operating frequency bands

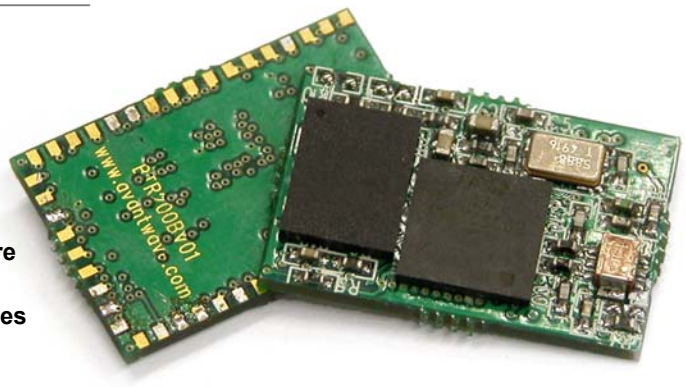
RF channels are spaced 1 MHz and are ordered in channel number k as shown in Table 1.1. In order to comply with out-of-band regulations in each country, a guard band is used at the lower and upper band edge.

Lower Guard Band	**Upper Guard Band**
2 MHz	3.5 MHz

Table 1.2: Guard Bands

Datasheet
BTR200

Key Features



- **A small and cost effective Bluetooth® System**
- **Bluetooth® specification v1.2/v2.0 compliant**
- **Class 2, up to 10-meter range**
- **Complete 2.4GHz Bluetooth® System including:**
  - Hardware: Radio, Baseband and Crystal & Memory
  - Standard Firmware: HCI or RFCOMM stack
- **Power management: low power 1.8V operation for Bluetooth® core**
- **Compact size: 20 mm x 13 mm x 2.2 mm**
- **Bluetooth® Profile Supported: HSP, HFP, A2DP and AVRCP profiles**
- **Built-in stereo codec**
- **External antenna**
- **On-board flash memory (8Mbits)**
- **Allow dual boots**
- **Audio streaming**
- **Optional echo cancellation software library**
- **Support multiple connections**
- **Surface mount module for embedded applications**
- **Several firmware options**
- **Rewritable flash memory for easy upgrade route**
- **Custom firmware production available**

Description

The **Bluetron™ BTR200 module** from AvantWave is a complete Bluetooth® solution for fast implementation, cutting your time-to-market. It is a short-range, compact and cost effective radio/baseband module that can be implemented in any kind of electronic devices, such as hands-free car kit, stereo headset and telephone gateway, etc.

In standard configuration the module includes a baseband processor with on board 8Mbit Flash memory, a radio front-end, antenna interface, supporting circuitry, together with some higher-level software protocols and applications such as L2CAP, SDP, SPP, GAP, HSP, HFP, A2DP and AVRCP are resided in the Flash.

The **Bluetron™ BTR200 module** is a power class 2 Bluetooth® devices, and is in compliance with version 1.2/2.0 of the Bluetooth® specification. It is supplied with Bluetooth® protocol stack firmware which runs on the internal microprocessor. **Bluetron™ BTR200 module** is built on CSR BC03 Multimedia External core with an 8Mbit Flash memory for firmware and application software storage.

Applications

- Stereo Bluetooth® headset
- Automotive car kit applications
- PDAs and other portable terminals
- MP3 headset

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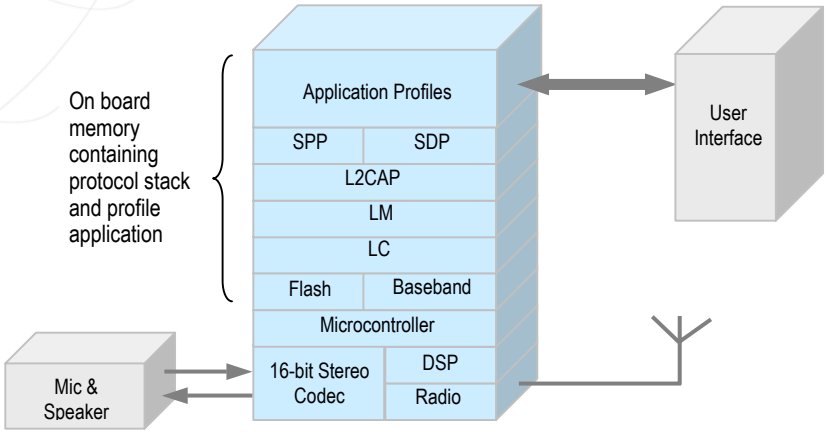
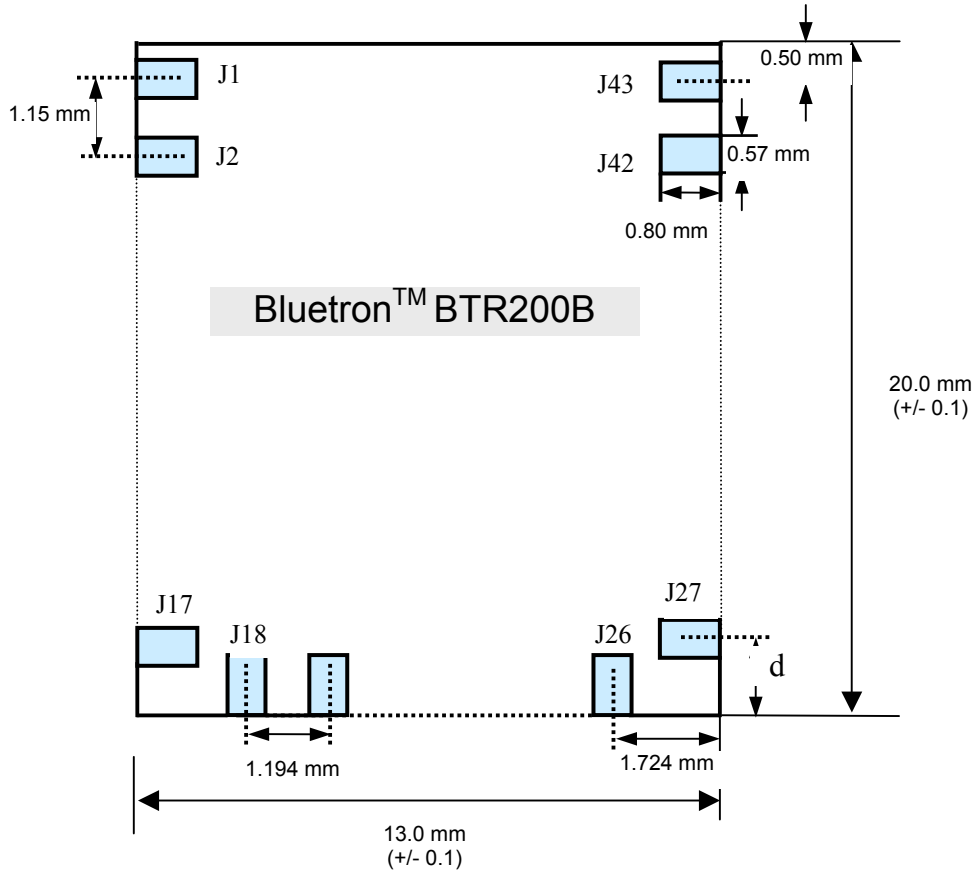
Software

The upper layers of the Bluetooth stack (above HCI) runs on-package. No external microcontroller is required.



Mechanical Specification

Top view



Side view

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Pin Assignment

Terminal	Name	Description
1	GND	Ground Connection
2	ANT	50 Ohm antenna port
3	AIO[1]	Programmable input/output line
4	AIO[0]	Programmable input/output line
5	AUDIO_OUT_P_LEFT	Analog speaker output positive (left side)
6	AUDIO_IN_N_LEFT	Analog microphone input negative (left side)
7	AUDIO_IN_P_LEFT	Analog microphone input positive (left side)
8	AUDIO_IN_N_RIGHT	Analog microphone input negative (right side)
9	AUDIO_IN_P_RIGHT	Analog microphone input positive (right side)
10	AUDIO_OUT_N_LEFT	Analog speaker output negative (left side)
11	AIO[3]	Programmable input/output line
12	SPI_CLK	Serial Peripheral Interface clock
13	+1.8V	Positive supply for analog, core (can be generated by internal linear voltage regulator)
14	GND	Ground connection
15	+3.3V	Positive supply for external flash and PIO and internal LDO regulator
16	USB_D+	USB data plus
17	PCM_CLK	PCM synchronous data clock
18	UART_RX	UART data input
19	SPI_CSB	Chip select for synchronous serial peripheral interface
20	UART_RTS	UART request to send active low
21	PIO[6]	Programmable input/output line
22	PIO[5]	Programmable input/output line
23	UART_CTS	UART clear to send active low
24	UART_TX	UART data output
25	PCM_IN	PCM Synchronous data input
26	PCM_OUT	PCM Synchronous data output

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27	RESET	Reset if high for >5ms
28	PCM_SYNC	PCM Synchronous data sync
29	USB_D-	USB data minus
30	PIO[1]	Programmable input/output line
31	SPI_MISO	Serial Peripheral Interface data output
32	SPI_MOSI	Serial Peripheral Interface data input
33	PIO[7]	Programmable input/output line
34	AUDIO_OUT_P_RIGHT	Audio Speaker Output Positive (right side)
35	AUDIO_OUT_N_RIGHT	Audio Speaker Output Negative (right side)
36	PIO[4]	Programmable input/output line
37	PIO[3]	Programmable input/output line
38	PIO[2]	Programmable input/output line
39	PIO[10]	Programmable input/output line
40	PIO[11]	Programmable input/output line
41	PIO[9]	Programmable input/output line
42	PIO[8]	Programmable input/output line
43	PIO[0]	Programmable input/output line

General Specifications

	Minimum	Typical	Maximum
Supply Voltage: +3.3V	3.0V	3.3V	3.6V
Regulated Output Voltage (load = 70 mA)	1.7V	1.78V	1.85V
Operating Temperature range	-40°C	-	85°C
Storage Temperature range	-40°C	-	150°C
Frequency Range	2.4 GHz	-	2.4835 GHz

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RF Specifications

Voltage Supplies = 1.8V
Temperature = 25°C
Frequency = 2.441GHz

Receiver	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity (DH1/3/5) at 0.1% BER	- 84	-82.5	- 81	-70	dBm
Maximum received signal	0	0.7	1.5	≥-20	dBm
C/I Co-channel		8	-	≤11	dB
C/I Adjacent channel (1MHz)	-	-4	-	≤0	dB
C/I Image rejection (carrier –3MHz)	-	-20	-	≤-9	dB
Transmitter	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Average Output Power	-2.0	0.8	4	+4 to –6	dBm
20dB bandwidth	-	800	-	≤ 1000	kHz
2nd ACP (+/-2MHz)	-	-40	-	≤ -20	dBc
3rd ACP (+/-3MHz)	-	-45	-	≤ -40	dBc

Codec Characteristics

Microphone Amplifier	Minimum	Typical	Maximum	Unit
Bandwidth	-	17	-	kHz
Input impedance	-	20	-	kΩ
Gain Resolution	-	3	-	dB
Distortion at 1KHz	-		-74	dB
Input full scale at maximum gain	-	4	-	mV rms
Input full scale at minimum gain	-	400	-	mV rms
Loudspeaker Driver				
Output power into 32Ω	-	30	-	mW pk
Output voltage ful scale swing	-	2.0	-	V pk-pk
Output current drive (at full scale swing)	10	20	40	mA
Output full scale current (at reduced swing)	-	75	-	mA
Distortion and noise (relative to full scale), THD	-	-75	-	dBc
Allowed load: resistive	16	-	O.C.	Ω
Allowed load: capacitive	-	-	500	pF

Note: For specified THD. Much greater current can be supplied by the loudspeaker driver with compromised THD.

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Power Consumption

Voltage Supplies = 1.8V
Temperature = 20°C
Frequency = 2.441GHz

	Average	Peak	Unit
SCO connection HV3 (30ms interval sniff mode)(slave)	21	-	mA
SCO connection HV3 (30ms interval sniff mode)(Master)	21	-	mA
SCO connection HV3 (no sniff mode)(slave)	28	-	mA
SCO connection HV1 (Slave)	42	-	mA
SCO Connection HV1 (Master)	42	-	mA
ACL data transfer 115.2kbps UART (Master)	5	-	mA
ACL data transfer 115.2kbps UART (slave)	22	-	mA
ACL data transfer 720kbps UART (Master or slave)	45	-	mA
ACL data transfer 720kbps USB (Master or slave)	45	-	mA
ACL connection, sniff mode 40ms interval, 38.4kbps UART	3.2	-	mA
ACL connection, sniff mode 1.28s interval, 38.4kbps UART	0.45	-	mA
Parked Slave, 1.28s beacon interval, 38.kpbs UART	0.55	-	mA
Standby Mode (Connected to host, no RF activity)	47	-	µA
Reset (RESET high or RESETB low)	15	-	µA

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Solder Profiles

In order to setup your application, it is required to have the soldering profile which based on various parameters.

Zone	Sensor	Description
Preheat Zone	1-2	This zone raises the temperature at a controlled rate
Equilibrium Zone	3	This zone brings the board to a uniform temperature and also activates the flux. The duration in this zone will need to be adjusted to optimize the out gassing of the flux
Reflow Zone	4	The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint.
Cooling Zone	5-6	The cooling rate should be fast, to keep the solder grains small which will give longer lasting joint.

Solder Re-Flow Profile for Devices with Lead-Free Solder Balls

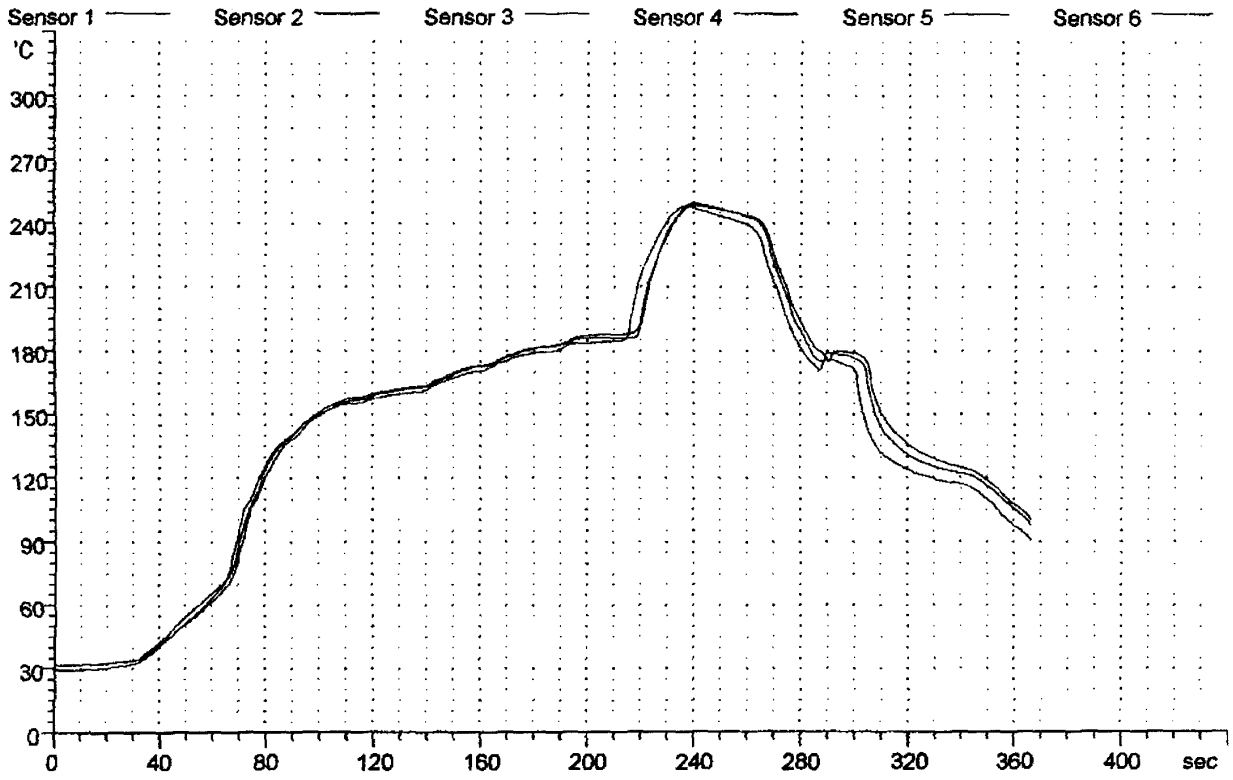

Figure 1.1: Typical Lead-Free Re-flow Solder Profile

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BlueCore™3-Multimedia External

Single Chip Bluetooth® v1.2 System

Production Information Data Sheet For

BC352239A

November 2004

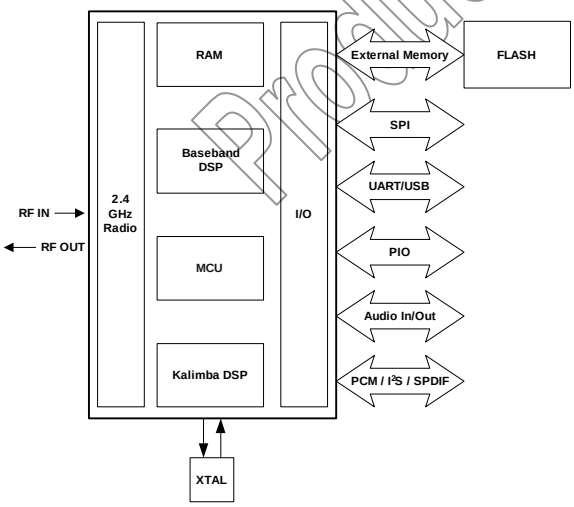
Device Features

- Fully Qualified Bluetooth system
- Bluetooth v1.2 Specification Compliant
- Kalimba DSP Open Platform Co-Processor
- Full Speed Bluetooth Operation with Full Piconet Support
- Scatternet Support
- Low Power 1.8V Operation
- 7 x 7mm 120-ball VFBGA Package
- Minimum External Components
- Integrated 1.8V regulator
- Dual UART Ports
- 16-bit Stereo Audio CODEC
- I^2S and SPDIF Interfaces
- RoHS Compliant

General Description

BlueCore3-Multimedia External is a single chip radio and baseband IC for Bluetooth 2.4GHz systems.

BC352239A interfaces to 8Mbit of external Flash memory. When used with the CSR Bluetooth software stack, it provides a fully compliant Bluetooth system to v1.2 of the specification for data and voice communications.



BlueCore3-Multimedia External System Architecture

Applications

- Stereo Headphones
- Automotive Hands-Free Kits
- Echo Cancellation
- High Performance Telephony Headsets
- Enhanced Audio Applications
- A/V Profile Support

BlueCore3-Multimedia External contains the Kalimba DSP, an open platform digital signal processor (DSP) co-processor supporting enhanced audio applications.

BlueCore3-Multimedia External has been designed to reduce the number of external components required, ensuring that production costs are minimised.

The device incorporates auto-calibration and built-in self-test (BIST) routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth v1.2 Specification.

1 Key Features

Radio

- Common TX/RX terminal simplifies external matching; eliminates external antenna switch
- BIST minimises production test time. No external trimming is required in production
- Full RF reference designs available
- Bluetooth v1.2 Specification compliant

Transmitter

- +6dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range >30dB
- Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch
- Class1 support using external power amplifier, with RF power controlled by an internal 8-bit DAC

Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesiser requires no external VCO, varactor diode, resonator or loop filter
- Compatible with crystals between 8 and 32MHz (in multiples of 250kHz) or an external clock
- Accepts 7.68, 14.44, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz TCXO frequencies for GSM and CDMA devices with sinusoidal or logic level signals

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shut down and wake up commands with an integrated low power oscillator for ultra-low power Park/Sniff/Hold mode
- 'Clock request' output to control an external clock
- On-chip linear regulator; 1.8V output from a 2.2-4.2V input
- Power-on-reset cell detects low supply voltage
- Arbitrary power supply sequencing permitted
- 8-bit ADC and DAC available to applications

Package Options

- 120-ball VFBGA, 7 x 7 x 1mm, 0.5mm pitch

Kalimba DSP

- DSP co-processor, 32MIPs, 24-bit fixed point DSP core
- Single cycle MAC; 24 x 24-bit multiply and 56-bit accumulator
- 32-bit instruction word, dual 24-bit data memory
- 4Kword program memory, 2 x 8Kword data memory
- Flexible interfaces to BlueCore3 subsystem

Baseband and Software

- External 8Mbit Flash for complete system solution
- Internal 32Kbyte RAM, allows full speed data transfer, mixed voice and data, and full piconet operation
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

Physical Interfaces

- Synchronous serial interface up to 4Mbaud for system debugging
- UART interface with programmable baud rate up to 1.5Mbaud with an optional bypass mode
- Full speed USB v1.1 interface supports OHCI and UHCI host interfaces
- Bi-directional serial programmable audio interface supporting PCM, I^2S and SPDIF formats
- Optional I^2C™ compatible interface

Stereo Audio CODEC

- 16-bit resolution, standard sample rates of 8kHz, 11.025kHz, 16kHz, 22.05kHz, 32kHz, 44.1kHz and 48kHz (DAC only)
- Dual ADC and DAC for stereo audio
- Integrated amplifiers for driving microphone and speakers with minimum external components
- Compatible with Kalimba DSP

Bluetooth Stack

CSR's Bluetooth Protocol Stack runs on the on-chip MCU in a variety of configurations:

- Standard HCI (UART or USB)
- Fully embedded RFCOMM
- Customised builds with embedded application code

5 Device Diagram

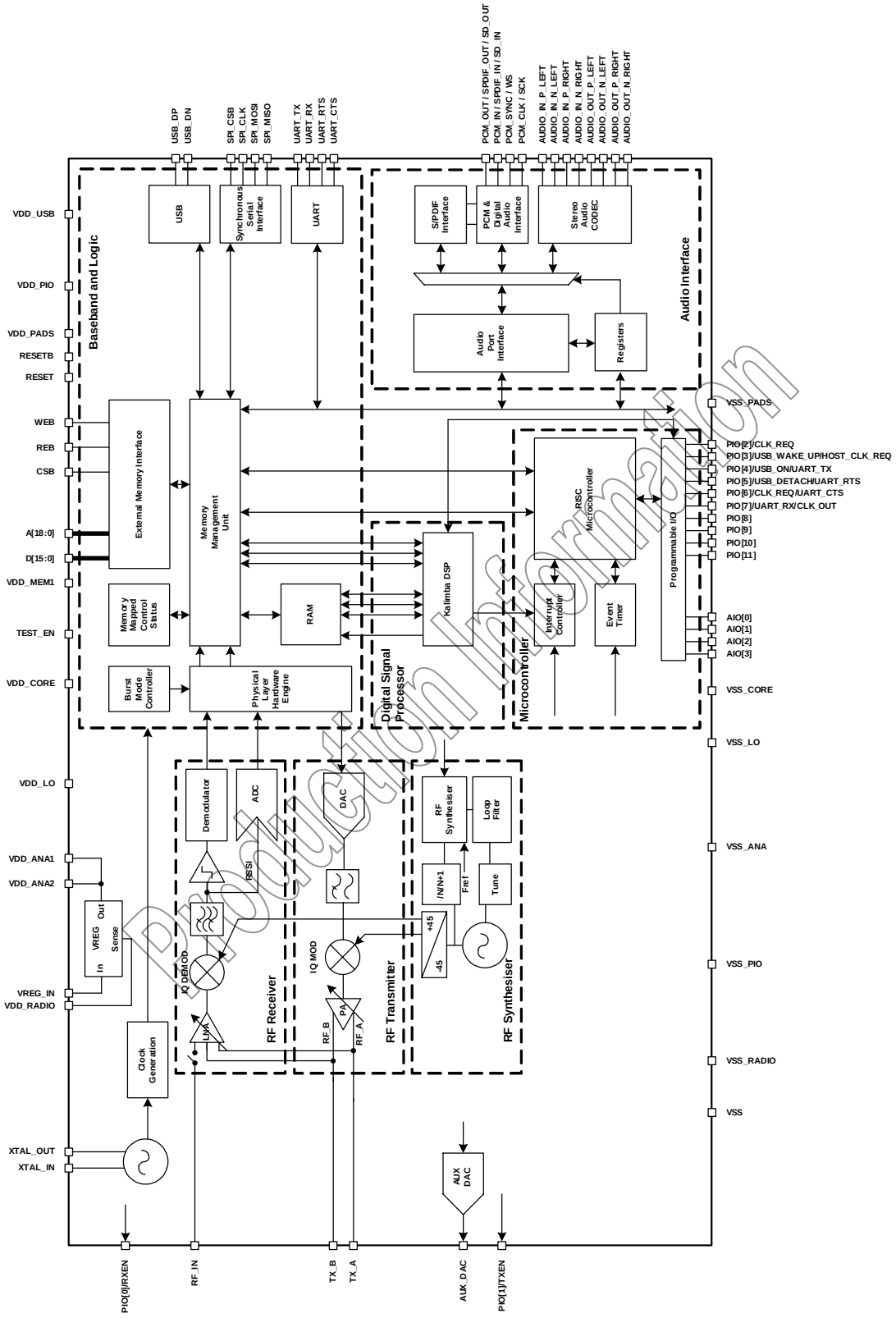


Figure 5.1: BlueCore3-Multimedia External Device Diagram

6 Description of Functional Blocks

6.1 RF Receiver

The receiver features a near-zero Intermediate Frequency (IF) architecture that allows the channel filters to be integrated on to the die. Sufficient out-of-band blocking specification at the Low Noise Amplifier (LNA) input allows the radio to be used in close proximity to Global System for Mobile Communications (GSM) and Wideband Code Division Multiple Access (W-CDMA) cellular phone transmitters without being desensitised. The use of a digital Frequency Shift Keying (FSK) discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore3-Multimedia External to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

6.1.1 Low Noise Amplifier

The Low Noise Amplifier (LNA) can be configured to operate in single-ended or differential mode. Single-ended mode is used for Class 1 Bluetooth operation; differential mode is used for Class 2 operation.

6.1.2 Analogue to Digital Converter

The Analogue to Digital Converter (ADC) is used to implement fast Automatic Gain Control (AGC). The ADC samples the Received Signal Strength Indicator (RSSI) voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

6.2 RF Transmitter

6.2.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

6.2.2 Power Amplifier

The internal Power Amplifier (PA) has a maximum output power of +6dBm allowing BlueCore3-Multimedia External to be used in Class 2 and Class 3 radios without an external RF PA. Support for transmit power control allows a simple implementation for Class 1 with an external RF PA.

6.2.3 Auxiliary DAC

An 8-bit voltage Auxiliary DAC is provided for power control of an external PA for Class 1 operation.

6.3 RF Synthesiser

The radio synthesiser is fully integrated onto the die with no requirement for an external Voltage Controlled Oscillator (VCO) screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v1.2 specification.

6.4 Clock Input and Generation

The reference clock for the system is generated from a TCXO or crystal input between 8 and 40MHz. All internal reference clocks are generated using a phase locked loop, which is locked to the external reference frequency.

6.5 Baseband and Logic

6.5.1 Memory Management Unit

The Memory Management Unit (MMU) provides a number of dynamically allocated ring buffers that hold the data which is in transit between the host, the air or Kalimba DSP. The dynamic allocation of memory ensures efficient use of the available Random Access Memory (RAM) and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

6.5.2 Burst Mode Controller

During radio transmission the Burst Mode Controller (BMC) constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During radio reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

6.5.3 Physical Layer Hardware Engine DSP

Dedicated logic is used to perform the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

The following voice data translations and operations are performed by the firmware:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/Continuously Variable Slope Delta (CVSD) (over the air)
- Voice interpolation for lost packets
- Rate mismatches

The hardware supports all optional and mandatory features of Bluetooth v1.2, including AFH and eSCO.

6.5.4 RAM

32Kbytes of on-chip RAM is provided to support the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

6.5.5 Kalimba DSP RAM

Further on-chip RAM is provided to support the Kalimba DSP as follows:

- 8K x 24-bit for data memory 1 (DM1)
- 8K x 24-bit for data memory 2 (DM2)
- 4K x 32-bit for program memory (PM)

6.5.6 External Memory Driver

The External Memory Driver interface can be used to connect to the external Flash memory and also to the optional external RAM for memory-intensive applications.

6.5.7 USB

This is a full speed Universal Serial Bus (USB) interface for communicating with other compatible digital devices. BlueCore3-Multimedia External acts as a USB peripheral, responding to requests from a Master host controller such as a PC.

6.5.8 Synchronous Serial Interface

This is a synchronous serial port interface (SPI) for interfacing with other digital devices. The SPI port can be used for system debugging. It can also be used for programming the Flash memory.

6.5.9 UART

This is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices.

6.6 Microcontroller

The microcontroller (MCU), interrupt controller and event timer run the Bluetooth software stack and control the radio and host interfaces. A 16-bit reduced instruction set computer (RISC) microcontroller is used for low power consumption and efficient use of memory.

6.6.1 Programmable I/O

BlueCore3-Multimedia External has a total of 16 (12 digital and 4 analogue) programmable I/O terminals. These are controlled by firmware running on the device.

6.7 Kalimba DSP

The Kalimba DSP is an open platform Kalimba DSP allowing signal processing functions to be performed on over-air data or CODEC data in order to enhance audio applications. Figure 6.1 shows how the Kalimba DSP interfaces to other functional blocks within BlueCore3-Multimedia External.

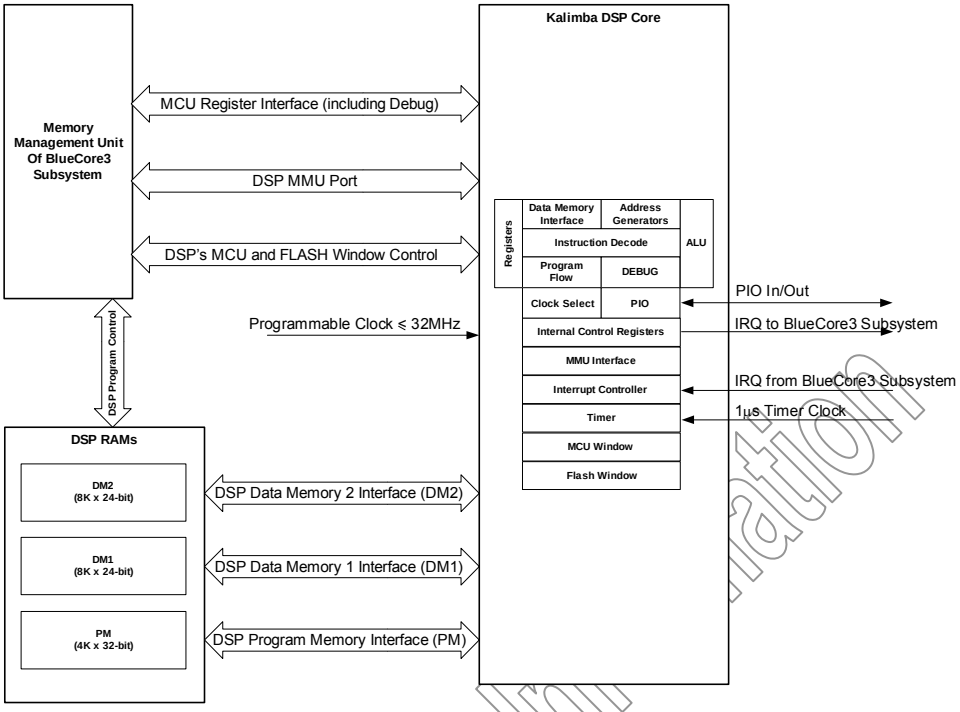


Figure 6.1: Kalimba DSP Interface to Internal Functions

The key features of the DSP include:

- 32MIPS performance, 24-bit fixed point DSP Core
- Single cycle MAC of 24 x 24-bit multiply and 56-bit accumulate
- 32-bit instruction word
- Separate program memory and dual data memory, allowing an ALU operation and up to two memory accesses in a single cycle
- Zero overhead looping and branching
- Zero overhead circular buffer indexing
- Single cycle barrel shifter with up to 56-bit input and 24-bit output
- Multiple cycle divide (performed in the background)
- Bit reversed addressing
- Orthogonal instruction set
- Low overhead interrupt

6.8 Audio Interface

The audio interface circuit consists of a stereo audio CODEC, dual audio inputs and outputs, and a PCM, I^{2}S or SPDIF configurable interface. Figure 6.2 outlines the functional blocks of the interface. The CODEC supports stereo playback and recording of audio signals at multiple sample rates with a resolution of 16-bit. The ADC and the DAC of the CODEC each contain two independent channels. Any ADC or DAC channel can be run at its own independent sample rate.

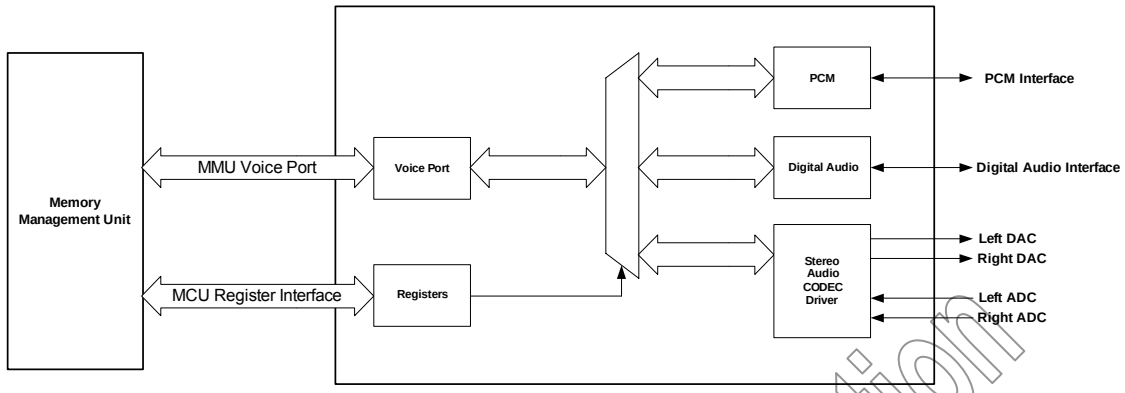


Figure 6.2: Audio Interface

The interface for the digital audio bus shares the same pins as the PCM CODEC Interface described in Section 8.8.9. This means that each of the audio busses are mutually exclusive in their usage. The pin out for the PCM interface with alternative pin descriptions can be seen in the device diagram shown in Figure 5.1 and Table 6.1 lists these alternative functions.

PCM Interface	SPDIF Interface	I^{2}S Interface
PCM_OUT	SPDIF_OUT	SD_OUT
PCM_IN	SPDIF_IN	SD_IN
PCM_SYNC		WS
PCM_CLK		SCK

Table 6.1: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

6.8.1 Audio Input and Output

The audio input circuitry consists of a dual audio input that can be configured to be either single ended or fully differential and programmed for either microphone or line input. It has a programmable gain stage for optimisation of different microphones.

The audio output circuitry consists of a dual differential class A-B output stage.

6.8.2 Digital Audio Interface

The digital audio interface supports various digital audio bus standard, which include I^{2}S, and the interfaces contained within the IEC 60958 specification such as SPDIF and AES3(1).

Note:

(1) Subject to firmware support; contact CSR for current status.