Exhibit 4.   Circuit Description -- Pursuant 47 CFR 2.1033(c)10

This section provides the description of circuits required by subpart 2.1033 of the Commission's rules.   The following are included:

4.1) Carrier Frequency Generation and Stabilization

4.2) Digital Modulation Technique

4.3) Modulation Limiting and Post Limiter Filter

4.4) Means for Output Power Limiting

4.5) Spurious and Harmonic Emissions Suppression

4.1. Carrier Frequency Generation and Stabilization

As shown in Figure 4-1 the synthesizer (U600) reference oscillator employs a crystal controlled Colpitts oscillator running at a frequency of 16.8MHz. The oscillator transistor and start-up circuit are located in the IC (U600) while the oscillator feedback capacitors, crystal, and tuning varactor are external. The crystal vendor characterizes the crystal over a specified temperature range and codes this information into a bar code which is printed on the crystal package. In production this crystal code is read via a 2-dimensional bar code reader and the parameters are saved in U801. Then voltage and frequency characteristics of the oscillator are measured and also stored in the Flash Memory of U801. The collected information is then used as input to a software algorithm in U801 that provides the necessary voltage adjustment for stabilization of the frequency at any given temperature.

This oscillator is temperature compensated as shown in Figure 4-1 to an accuracy of +/-5 PPM from -30 to 60 degrees C. The temperature compensation is implemented with the combination of the DSP software (U801) and the internal DAC (U600) at the power up of the radio only. This adjustment provides sufficient frequency correction to allow the radio to lock onto a base station channel. After a base station signal is detected, the compatible base station frequency serves as an accurate and stable reference for the transceiver's local reference oscillator by virtue of a transceiver AFC function inherent in the acquisition and lock process.
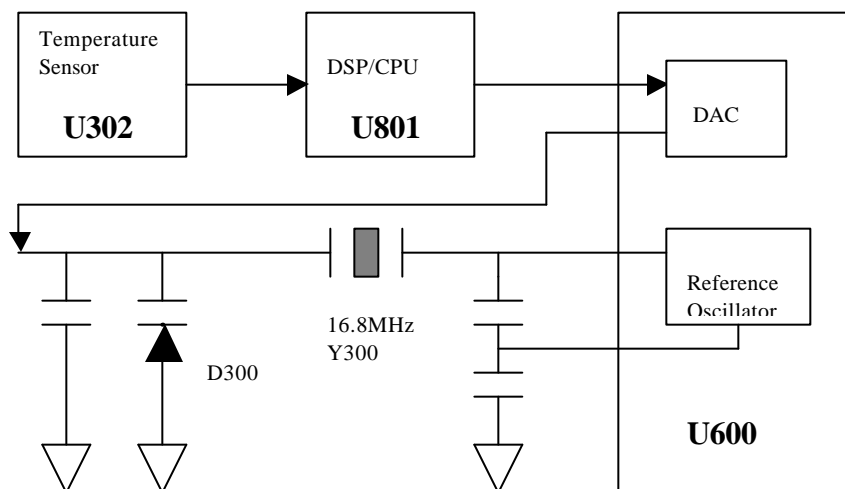
Figure 4-1: 16.8 MHz Reference Oscillator

The signal from the reference oscillator is used to control the stability of the main Voltage Controlled Oscillator (Q304 and Q308), which oscillates at a frequency between 960.65 – 979.65 and 1044.65 – 1056.65 MHz (see Figure 4-2). U600 also buffers the 16.8 MHz signal and provides a divided down 2.4 MHz to U506. The PLL inside the U506 uses the 2.4 MHz clock as the reference for the TX offset VCO (Q401). The frequency control for TX offset VCO is accomplished by a PLL that compares its frequency to the reference frequency thus locking the TX offset VCO to the reference oscillator.

The frequency of the TX offset VCO is 309.3 MHz which is divided by two in U506 and mixed with output of the main VCO to generate the transmit frequency. The transmitter frequency is programmed to a single frequency between 806 - 825 or 896 – 901 MHz. The mixer output is sent to a band pass filter (FL500 for 800MHz band and FL501 for 900MHz band), which rejects spurious signals.
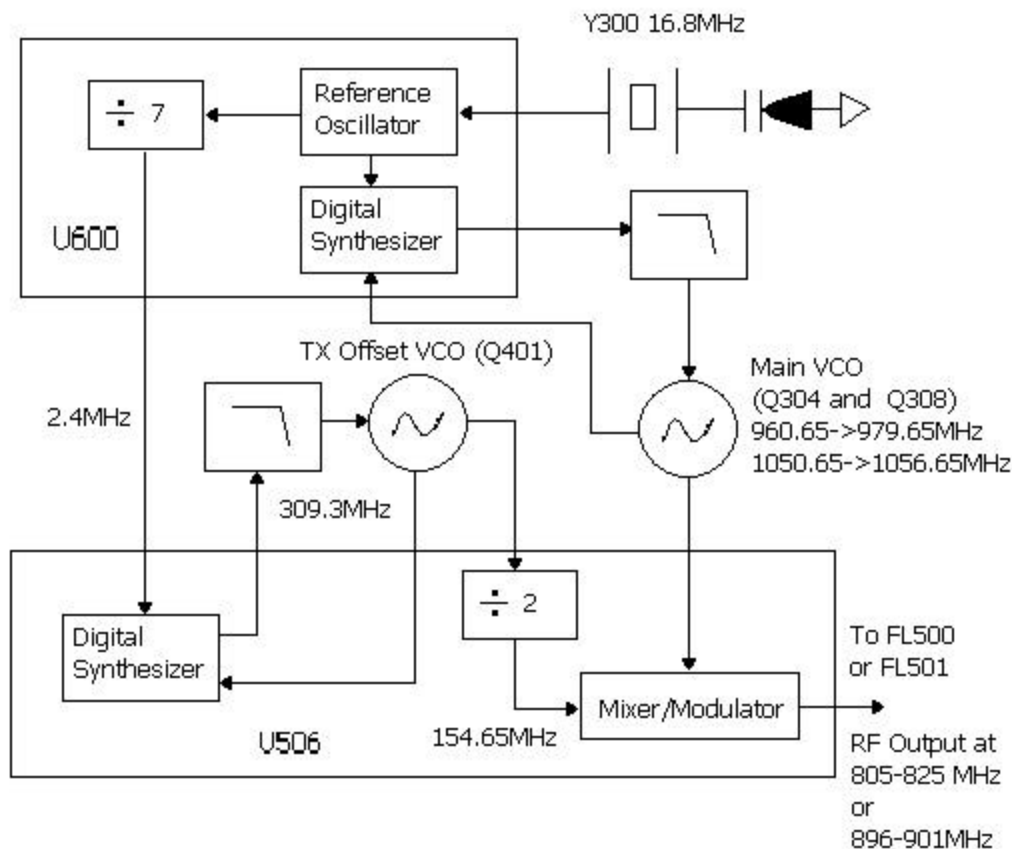
Figure 4-2: Transmitter Frequency Generation

4.2. Digital Modulation Techniques

The subject radio makes use of 3 different modulation techniques termed Quad-16QAM, Quad-64QAM, and Quad-QPSK. In voice mode, the radio will function in Quad-16QAM mode only. In data mode, the radio will use any one of the three different modulation techniques (Quad-16QAM, Quad-64QAM, and Quad-QPSK) in a given time division multiplexed slot. The transmitter is configured using TDMA time slotting so that up to 6 radio users can simultaneously share the 25 kHz channel. The following describes each of the modulation techniques:

The modulation technique termed Quad-QPSK is a linear digital modulation of a multi-channel variant of a 4-state Quadrature Phase Shift Keying. Data bits to be transmitted are split into four parallel lower rate streams, each of which is QPSK modulated to its own sub carrier frequency at a rate of 4k symbols per second. The four resulting sub channel signals are then combined in frequency division multiplex fashion to produce the composite Quad-QPSK signal. This spectrally efficient linear modulation can achieve transmission at 32K bits per second in a 25 kHz channel.

The modulation technique termed Quad-16QAM is a linear digital modulation of a multi-channel variant of a 16-state Quadrature Amplitude Modulation. Data bits to be transmitted are split into four parallel lower rate streams, each of which is 16QAM modulated to its own sub carrier frequency at a rate of 4k symbols per second. The four resulting sub channel signals are then combined in frequency division multiplex fashion to produce the composite Quad-16QAM signal. This spectrally efficient linear modulation can achieve transmission at 64K bits per second in a 25 kHz channel.

The modulation technique termed Quad-64QAM is a linear digital modulation of a multi-channel variant of a 64-state Quadrature Amplitude Modulation. Data bits to be transmitted are split into four parallel lower rate streams, each of which is 64QAM modulated to its own sub carrier frequency at a rate of 4k symbols per second. The four resulting sub channel signals are then combined in frequency division multiplex fashion to produce the composite Quad-64QAM signal. This spectrally efficient linear modulation can achieve transmission at 96K bits per second in a 25 kHz channel.

4.3. Modulation Limiting and Post Limiter Filter

The transmitted data or audio is processed using three software algorithms in a Digital signal Processor (U801) that automatically prevent modulation in excess of 100 percent. The software algorithms consist of a speech coder, a Quadruple-QPSK digital modulator, Quadruple-16QAM digital modulator, Quadruple-64QAM digital modulator, and a baseband filter. The baseband filter limits the bandwidth of the transmission message while the Cartesian feedback (U506) linearizes the output of the PA (U500) and thus minimizes adjacent channel spectral regrowth. The entire transmit signal generation process is shown in Figure 4-3.
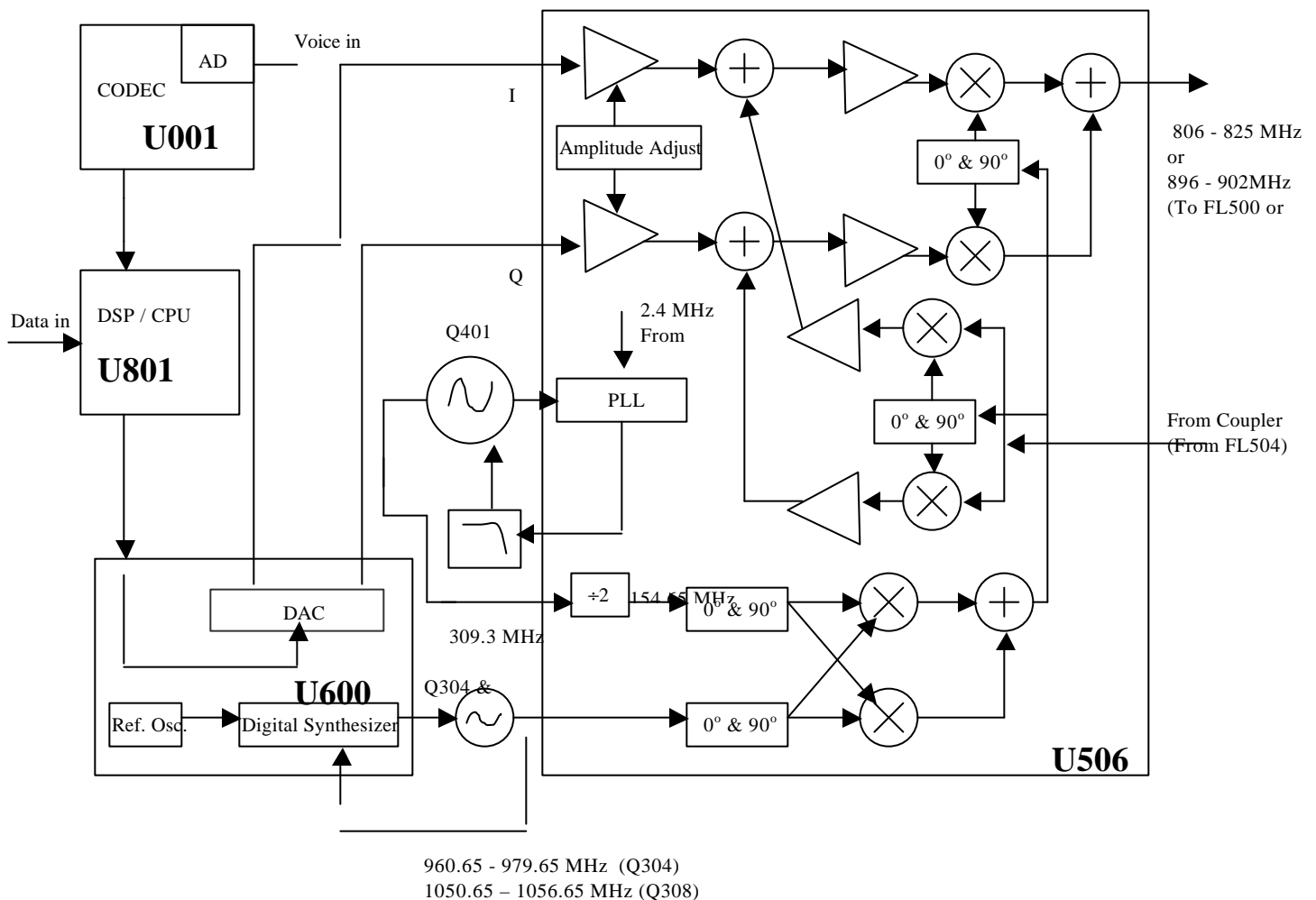

Figure 4-3: Transmitter Modulation System

4.4. Means for Output Power Limiting

The output power is set by varying the digitally programmable attenuators in the U506 which changes the level of RF power delivered to the power amplifier (U500), shown in Figure 4-4. The procedure to limit output power begins with a factory tuning procedure in which the attenuation is set to zero and the transmitter is configured to transmit in full power automatic level training mode. During automatic level training, U506 will set the lowest allowable baseband attenuation that results in a maximum power out of the radio without clipping the power amplifier. This power is typically higher than the targeted power setting. To lower the output power, the attenuation setting is iteratively increased until the output power is within the target window. The digital word that corresponds to that particular attenuator setting is stored into the Flash Memory (U801) as the minimum attenuator setting allowed.

During normal user operation, the transmitter periodically performs automatic level training. If automatic level training resulted in a power higher than the target power, the baseband attenuator would be set to the minimum attenuator setting stored in U801 to achieve the target power. If automatic level training resulted in a power lower than the target power, the baseband attenuator would not be decreased since doing so would clip the RF PA (U500) and potentially increase adjacent channel power.

In operation, output power is also attenuated from the maximum rated level in response to measured received signal strength. A high received signal strength indicates close proximity to a companion base station and thus the transmitter power required to maintain a quality link is lowered. To decrease the transmitter output power, the input level to the final RF Amplifying Module (U500) is reduced by increasing the attenuator settings in U506.
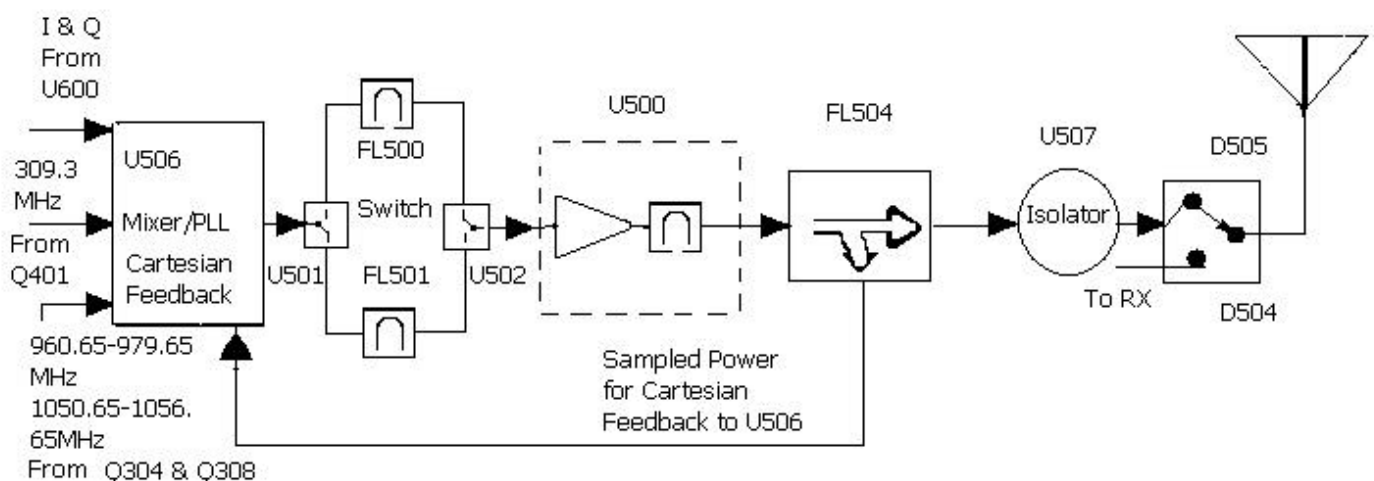
Figure 4-4: Transmitter Front Stage Line-Up

4.5. Spurious and Harmonic Emissions Suppression

Refer to Figure 4-4 on the previous page for the following description. In addition to the image rejection filter within U506, a SAW filter (which provides rejection at the image frequency) is placed before the Power Amplifier (U500) to insure that a clean transmitter frequency is delivered to the Power Amplifier input.   RF switches U501 and U502 are used to select the proper SAW filter depending on the band of operation (FL500 for 800MHz, FL501 for 900Mhz operation). The power amplifier output is isolated from mismatched loads in the antenna connector by an isolator. The isolator ensures that the power amplifier will see a stable load for any load variations applied to the antenna connector. A directional coupler is placed after the PA to serve as a coupling device back to the U506 for signal linearization through Cartesian feedback.

The bandpass SAW filter, PA and the isolator attenuate spurious and harmonic signals that are generated in the transmitter section. Proper shielding within the transceiver also attenuates radiated spurious emissions and harmonics.