AR4100 System in Package 802.11n– General Availability

Preliminary Data Sheet

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Revision history

Revision	Date	Description
Ver. 1.0	June 2011	Initial document release.
Ver. 2.0	July 2011	Initial document release for rel 1.3.
Ver. 3.0	August 2011	Updated for rel 1.4 with new pinout information.

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1 General Description

The AR4100 is a small form-factor, single stream, 802.11 b/g/n WiFi System-in-Package (SIP) solution. The AR4100 has been developed to support applications hosted by low-resource microcontrollers that send infrequent data packets over the network. Typically, these 802.11 applications place a higher priority on system cost, power consumption, ease of use, and fast wake-up times as compared to high throughput. The AR4100 integrates all WiFi functionality into a low-profile, 8.3 mm x 9.2 mm LGA package that can be easily mounted via low-cost PCB manufacturing flows. The device requires only a few external bypass capacitors and a connection to an antenna for a board-level design.

The AR4100 employs the world's lowest power consumption embedded architecture. It has been optimized for client applications in the home and enterprise that have lower data rates, and transmit or receive data on an infrequent basis. The AR4100 features standby current consumption as low as 5 µA. Additional optimizations, including a reduced host driver footprint, allow easy integration with low-cost microcontrollers.

The AR4100 also includes Qualcomm Atheros' industry leading high-efficiency, high-output EPA™ power amplifier with zero calibration and integrated LNAs. RF matching circuits, a reference crystal, and a T/R switch are also integrated, eliminating the need for an external RF components and thus enabling direct antenna connection. The end result is a device that is the best-in-class for ease of system design.

At the heart of the AR4100 is an ultra low-power radio architecture and proprietary power save technologies. An on-chip embedded CPU handles complete 802.11 b/g/n processing to minimize host processor loading.

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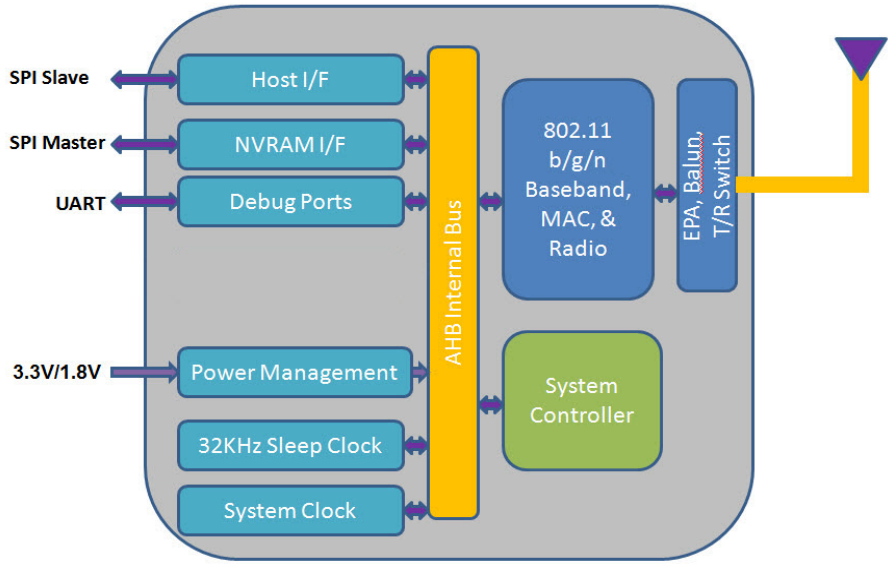
AR4100 Features

AR4100, ultra-low power, single stream (1x1) system-in-package IEEE 802.11n featuring:

- Low energy
  - Low power modes capable of 5 µA
  - Fast wakeup from host
- Low system resource requirements:
  - Small, simple host driver
  - Enable low resource MCU hosts
- Simple low-cost wireless system integration:
  - Simple design supporting 2- or 4- layer PCB support
  - Near zero RBOM
  - Integrated RF front end, RF shield, 32-KHz sleep clock, and system clock
  - Direct connect to a 50-Ω antenna
- Qualcomm Atheros world class leading 802.11n WiFi:
  - Best in class Rx sensitivity for superior throughput rate-over-range performance
  - Integrated high-power, high-efficiency linearized power amplifier
  - Low density parity check (LDPC) encoding for improved uplink robustness over range
  - WiFi protected setup (WPS)
- Standard interfaces:
  - SPI slave, SPI master, and UART

System Block Diagram



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2 Features Summary

2.1 Overview

The AR4100 is a single package combination IEEE 802.11 b/g/n. It supports 802.11 including full digital MAC and baseband engines that handle all 802.11b (CCK) and 11g/n (OFDM). An embedded low-power CPU core minimizes host loading to provide an easy-to-implement solution.

The AR4100 is architected for ultra-low power consumption, with near zero power consumption in power down modes with fast wakeup.

2.2 Integrated Radio Front End

The AR4100 consists of an integrated on-chip power amplifier that features the following:

- Atheros proprietary EPA™ linearization technology for WiFi
- Integrated crystal
- Integrated receive and transmit RF matching and switching to enable direct antenna connection with high performance, low power consumption, and near-zero RBOM for lowest solution cost

2.3 Power Requirements and Management

The AR4100 requires a 3.3 V and 1.8 V supplies to be provided from the system. The AR4100 power management engine utilizes advanced power save techniques such as: gating clocks to idle or inactive blocks, voltage scaling to specific blocks in certain states, fast start and settling circuits to reduce Tx and active duty cycles, CPU frequency scaling, and other techniques to optimize power consumption across all operation states.

For applications with a small transmit duty cycle, the AR4100 has the ability to quickly wake up and burst data out at a high rate and go back into standby mode, thus taking advantage of the 5 µA of power consumption in standby mode.

2.4 Manufacturing Calibration

The AR4100 utilizes internal self-calibration circuits to maintain optimal performance over temperature, time and process variation. The AR4100 does not require any customer manufacturing line calibration.

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2.5 Reference Frequency

The AR4100 incorporates a reference frequency crystal.

2.6 Internal Sleep Clock

The AR4100 incorporates an integrated on-chip sleep clock to regulate internal timing.

2.6.1 Standard Host Interface

The AR4100 supports a GSPI (Generic SPI) Slave Port when interfacing to a host MCU.

2.6.2 Other Interfaces

GSPI Master for interfacing to an external NVMEM for firmware load into the AR4100 upon power up.

2.7 802.11n

The AR4100 incorporates the latest generation of 802.11n technology from Qualcomm Atheros.

This includes hardware-based AES, AES-CCMP, and TKIP engines for faster data encryption, and supports industry leading security features including WiFi Protected Setup (WPS), along with standard WEP/WPA/WPA2 for personal environments.

2.8 Host Offloading (WiFi)

The AR4100 integrates a complete 802.11n MAC/BB/PHY processing to minimize host processor loading. The AR4100 offloads the complete 802.11 b/g/n baseband and MAC functions as standard feature, including:

- Link maintenance
- 802.11 frame transmission sequence to initiate the connection with an access point (AP)
- Background scanning, including transmission of probe request
- Signal quality detection and automated maintenance of current AP list
- Roaming to a new AP
- Rate adaptation, including automatic retry
- Encapsulation of 802.3 frames from the host to 802.11 frames
- Provides a full MAC interface that transacts 802.3 frames across the interface to the AR4100
- Encryption and decryption (hardware ciphers) for WEP/TKIP/AES-CCMP
- IEEE PowerSave; periodic wakeup when in sleep mode to check for buffered traffic
- Security negotiation
- WPS

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3 WiFi Functional Description

3.1 Overview

The AR4100 is a single chip 802.11 b/g/n device based on cutting edge technology, optimized for low power embedded applications.

3.2 Reset Control

The AR4100 CHIP_PWD_L pin can be used to completely reset the entire chip. After this signal has been de-asserted, the AR4100 waits for host communication through the GSPI. Once the host has initiated communication, the AR4100 turns on its crystal and later on its PLL. After all clocks are stable and running, the resets to all blocks are automatically de-asserted.

3.2.1 CPU Reset

CPU reset is different from the other resets mentioned above. There are three scenarios where the CPU reset can be asserted:

- The AR4100 CHIP_PWD_L pin is asserted or the host has not initiated communication.
- The polarity of a package pin is set to hold the CPU in reset until the host clears an internal AR4100 register.
- An internal AR4100 register is set by the host driver.

3.3 Reset Sequence

After a COLD_RESET event (e.g., host deasserts AR4100_CHIP_PWD_L) the AR4100 enters the HOST_OFF state. From that point the reset sequence is as shown:

1. The host writes the enable bit in the SPI_CONFIG register via the GSPI.
2. This bring the chip to a WAKEUP transient state from where it goes to an ON state (after the PLL clock has stabilized).
3. The ROM code executes the HOST_PROXY, which waits for the host to indicate whether to continue loading and executing firmware or whether to enter a boot message interface (BMI) state. The former is the normal mode; BMI is typically used to continue the host driving the AR4100 via BMI messages. BMI allows loading alternate firmware images into the RAM (e.g., to update the firmware in NVMEM, or run alternate firmware images for special tests).
4. If the host writes a special memory location (variable) to indicate that the firmware is to continue being loaded from host, then it does so and executes the loaded firmware. It eventually sends a WMIREADY event to the host
5. The host can now send further WMI commands.

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3.4 Hardware Power States

AR4100 hardware has five top level hardware power states. Table 3-1 describes the power states.

3.4.1 Sleep State Management

Sleep state minimizes power consumption while saving system states. In SLEEP state, all high speed clocks are gated off and the external reference clock source is powered off. The internal regulator supplies are also turned off during SLEEP. For the AR4100 to enter SLEEP state, the MAC, and CPU systems must not be active.

The system remains in sleep state until a WAKEUP event causes the system to enter WAKEUP state, wait for the reference clock source to stabilize, and then ungate all enabled clock trees. The CPU wakes up only when an interrupt arrives.

Table 3-1 Power Management States

State	Description
OFF	CHIP_PWD_L pin assertion immediately brings the chip to this state.
	Sleep clock is disabled.
	No state is preserved.
	Only host interface is active.
HOST_OFF	Most of the AR4100 is turned OFF. In this state the GSPI is enabled in a limited way such that only some of the registers are accessible. This state allows the host write to the SPI_CONFIG to move out of the HOST_OFF state.
SLEEP	Only the sleep clock is operating.
	The reference clock is disabled.
	Any wakeup events (MAC, host, LF-Timer) will force a transition from this state to the WAKEUP state.
	All internal states are maintained.
WAKEUP	A transient state between sleep/HOST_OFF and ON state.
ON	The high speed clock is operational and sent to each block enabled by the clock control register.
	Lower level clock gating is implemented at the block level, including the CPU, which can be gated OFF using the WAITI instruction while the system is ON. No CPU, host, and WLAN activities will transition to sleep states.

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Figure 3-1 depicts the state transition diagram.

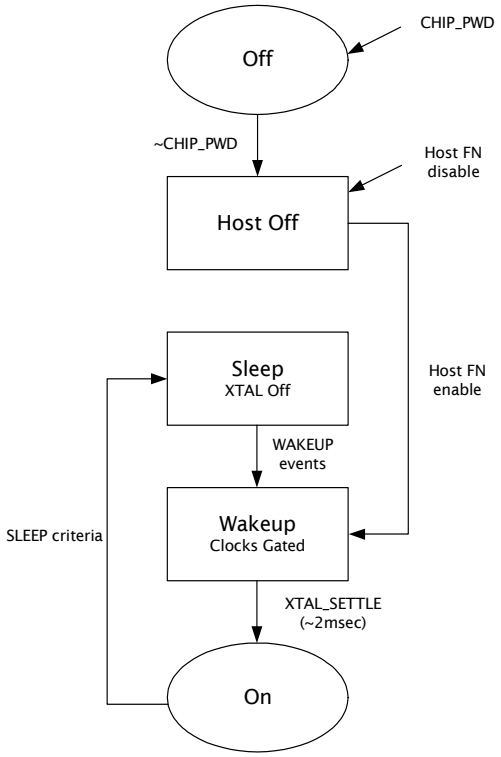

Figure 3-1 AR4100 Power States

3.5 System Clocking (RTC Block)

The AR4100 controls the clocks and power going to other internal modules.

The host interface clock represents another clock domain for the AR4100. This clock comes from the GSPI host and is completely independent from internal clocks. It drives the host interface logic as well as certain registers which can be accessed by the host in HOST_OFF and SLEEP states.

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4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 summarizes the absolute maximum ratings and Table 4-2 lists the recommended operating conditions for the AR4100. Absolute maximum ratings are those values beyond which damage to the device can occur.

Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

NOTE Maximum rating for signals follows the supply domain of the signals.

Table 4-1 Absolute Maximum Ratings

Symbol (Domain)	Parameter	Max Rating	Unit
AVDD18	Analog 1.8 V supply	–0.3 to 2.5	V
VDDIO	I/O supply	–0.3 to 4.0	V
HOST_POWER	Host interface I/O supply	–0.3 to 4.0	V
VDD33	Antenna and PA 3.3 V supply	–0.3 to 4.0	V
PAREG_BASE	External 3.3 V supply	–0.3 to 4.0	V
VBAT_42	External 3.3 V supply	–0.3 to 4.8	V
RF_{in}	Maximum RF input (reference to 50–Ω input)	+12 (including switch and balun loss)	dBm
T_{store}	Storage temperature	–45 to 135	°C
ESD	Electrostatic discharge tolerance	2000	V

4.2 Recommended Operating Conditions

Table 4-2 Recommended Operating Conditions

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
AVDD18	Analog 1.8 V supply	1.71	1.8	1.89	V
VDDIO	I/O supply	1.71	—	3.46	V
HOST_POWER	Host interface I/O supply	1.71	—	3.46	V
VDD33_PA	Antenna and PA 3.3 V supply	3.14	—	3.46	V
PAREG_BASE	External 3.3 V supply	3.14	3.3	3.46	V
VBAT_42	External 3.3 V supply	3.14	3.3	3.46	V
$T_{ambient}$	Ambient temperature	–30	—	85	°C

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4.3 DC Electrical Characteristics

Table 4-3 and Table 4-4 list the general DC electrical characteristics over recommended operating conditions (unless otherwise specified).

Table 4-3 General DC Electrical Characteristics (For 3.3 V I/O Operation)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage			0.7 x V_{dd}	—	—	V
V_{IL}	Low Level Input Voltage			—	—	0.3 x V_{dd}	V
I_{IL}	Input Leakage Current	Without Pull-up or Pull-down	0 V < V_{in} < V_{dd} 0 V < V_{out} < V_{dd}	0	—	–3	nA
		With Pull-up	0 V < V_{in} < V_{dd} 0 V < V_{out} < V_{dd}	16	—	48	µA
		With Pull-down	0 V < V_{in} < V_{dd} 0 V < V_{out} < V_{dd}	–14	—	–47	µA
V_{OH}	High Level Output Voltage		I_{oh} = –4 mA	0.9 x V_{dd}	—	—	V
			I_{oh} = –12 mA	0.9 x V_{dd}	—	—	V
V_{OL}	Low Level Output Voltage		I_{oh} = 4 mA	—	—	0.1 x V_{dd}	V
			I_{oh} = 12 mA	—	—	0.1 x V_{dd}	V

Table 4-4 General DC Electrical Characteristics (For 1.8 V I/O Operation)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage			0.7 x V_{dd}	—	—	V
V_{IL}	Low Level Input Voltage			—	—	0.3 x V_{dd}	V
I_{IL}	Input Leakage Current	Without Pull-up or Pull-down	0 V < V_{in} < V_{dd} 0 V < V_{out} < V_{dd}	0	—	–3	nA
		With Pull-up	0 V < V_{in} < V_{dd} 0 V < V_{out} < V_{dd}	3.5	—	13	µA
		With Pull-down	0 V < V_{in} < V_{dd} 0 V < V_{out} < V_{dd}	–6.2	—	–23	µA
V_{OH}	High Level Output Voltage		I_{oh} = –4 mA	0.9 x V_{dd}	—	—	V
			I_{oh} = –12 mA	0.9 x V_{dd}	—	—	V
V_{OL}	Low Level Output Voltage		I_{oh} = 4 mA	—	—	0.1 x V_{dd}	V
			I_{oh} = 12 mA	—	—	0.1 x V_{dd}	V

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Figure 4-1 and Figure 4-2 show the recommended power up/down and reset sequences for the AR4100 using external 3.3 V and 1.8 V supplies.

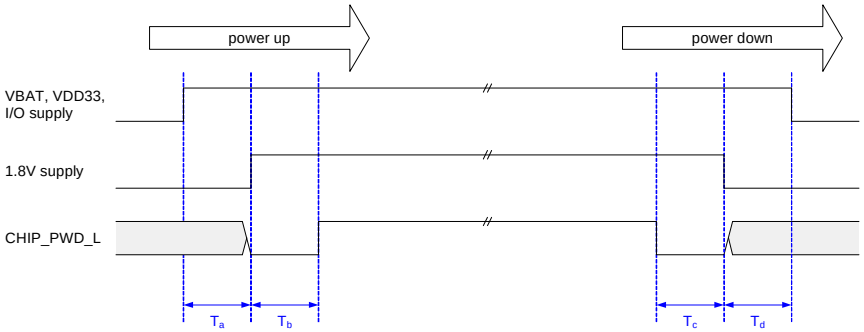

Figure 4-1 Power Up/Power Down Timing

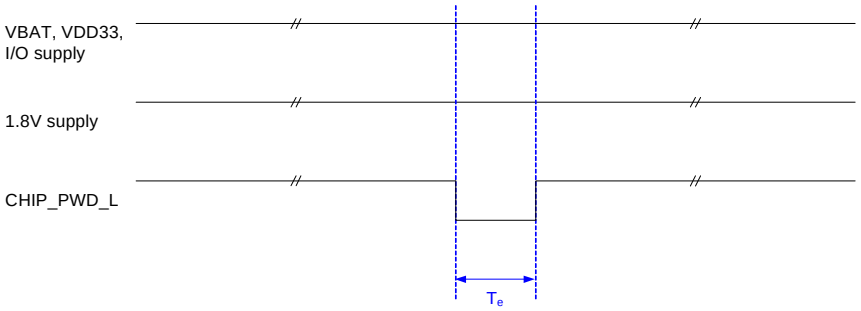

Figure 4-2 Reset and Power Cycle Timing

Where:
VBAT = VBATTERY_42
I/O = VDDIO, HOST_POWER

Table 4-5 Timing Diagram Definitions

Symbol	Description	Min (µsec)
T_a	Time between VBAT, VDD33, and I/O supplies valid and 1.8 V supply valid[1]	0
T_b	Time between 1.8 V supply valid and CHIP_PWD_L deassertion	5
T_c	Time between CHIP_PWD_L assertion and 1.8 V supply invalid	0
T_d	Time between 1.8 V supply invalid and VBAT, VDD33, and I/O supplies invalid	N/A[2]
T_e	Length of CHIP_PWDP_L pulse	5

1. Supply valid represents the voltage level has reached 90% level.
2. No strict requirements. This parameter can also be negative.

Table 4-6 summarizes the transmitter characteristics for AR4100.

Table 4-6 Frequency, Power Out and Reference Oscillator Frequency

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	—	2.412	—	2.484	GHz
Output power	—	—	—	19.0	dBm

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4.4 Typical Power Consumption Performance

Table 4-7 Typical Current Consumption – Low Power States (Individual Voltage Rails)

Mode	Typical Current Consumption [mA]	
	1.8 V[1]	**3.3 V[2]**
OFF	0.000	0.004
HOST_OFF	0.043	0.005
SLEEP	0.210	0.005

1. AVDD18, VDDIO
2. PAREG_BASE, VBAT_42, VDD33

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5 Pin Assignments and Descriptions

Table 5-1 shows the PCB footprint and pin assignments (bottom view of the chip) of the AR4100.

Table 5-2 and Table 5-3 show pin assignments and pin definitions.

The following nomenclature is used for signal names:

NC	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types:

IA	Analog input signal
I	Digital input signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
I/O	A digital bidirectional signal
OA	An analog output signal
O	A digital output signal
P	A power or ground signal

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Table 5-1 AR4100 Pin Assignment and Ball-Out

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	GND	AVDD18	AVDD18	VDDIO	NC	VDD33	VBAT_42	PAREG_ 33_OUT	PAREG _BASE	DVDD12	GND	NC	NC	NC	NC	NC	NC
B	AVDD12	NC	NC	NC	SW_REG_ OUT	VDD33	VBAT_42	PAREG_ 33_OUT	NC	NC	NC	NC	NC	NC	NC	NC	NC
C	HOST_ POWER	NC														NC	NC
D	SPI_MOSI	NC														NC	NC
E	SPI_CS	NC														NC	GND
F	NC	NC				E_ GND1	E_ GND2	E _GND3	E_ GND4	E_ GND5	E_ GND6					NC	NC
G	SPI_INT					E_ GND7	E_ GND8	E_ GND9	E_ GND10	E_ GND11	E_ GND12					NC	NC
H	SPI_MISO					E_ GND13	E_ GND14	E_ GND15	E_ GND16	E_ GND17	E_ GND18					NC	NC
J	SPI_CLK					E_ GND19	E_ GND20	E_ GND21	E_ GND22	E_ GND23	E_ GND24					NC	NC
K	GND					E_ GND25	E_ GND26	E_ GND27	E_ GND28	E_ GND29	E_ GND30					NC	NC
L	NC					E_ GND31	E_ GND32	E_ GND33	E_ GND34	E_ GND35	E_ GND36					NC	NC
M	NC	SPIM_ CS_N														NC	NC
N	NC	SPIM_ MISO														NC	NC
P	NC	SPIM_ CLK														NC	NC
R	NC	SPIM_ MOSI	NC	NC	NC	NC	HMODE1	NC	TDI	NC	NC	NC	NC	NC	NC	NC	GND
T	NC	NC	GND	WIFI_ RF	GND	DEBUG_ UART_ TX_D	HMODE0	TMS	TCK	DBG_ UART_ RXD	CHIP_ PWD_L	GND	NC	GND	NC	GND	NC

(Note: the 36 E_GND* pins are not aligned with the outer pins. See "Package Dimensions" on page 17.)

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Table 5-2 Pin Assignments and Descriptions

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
A1	GND	D2	NC	R2	SPIM_MOSI
A2	AVDD18	D16	NC	R3	NC
A3	AVDD18	D17	NC	R4	NC
A4	VDDIO	E1	SPI_CS	R5	NC
A5	NC	E2	NC	R6	NC
A6	VDD33	E16	NC	R7	HMODE1
A7	VBAT_42	E17	GND	R8	NC
A8	PAREG_33_OUT	F1	NC	R9	TDI
A9	PAREG_BASE	F2	NC	R10	NC
A10	DVDD12	F16	NC	R11	NC
A11	GND	F17	NC	R12	NC
A12	NC	G1	SPI_INT	R13	NC
A13	NC	G16	NC	R14	NC
A14	NC	G17	NC	R15	NC
A15	NC	H1	SPI_MISO	R16	NC
A16	NC	H16	NC	R17	GND
A17	NC	H17	NC	T1	NC
B1	AVDD12	J1	SPI_CLK	T2	NC
B2	NC	J16	NC	T3	GND
B3	NC	J17	NC	T4	WIFI_RF
B4	NC	K1	GND	T5	GND
B5	SW_REG_OUT	K16	NC	T6	DEBUG_UART_TXD
B6	VDD33	K17	NC	T7	HMODE0
B7	VBAT_42	L1	NC	T8	TMS
B8	PAREG_33_OUT	L16	NC	T9	TCK
B9	NC	L17	NC	T10	DEBUG_UART_RXD
B10	NC	M1	NC	T11	CHIP_PWD_L
B11	NC	M2	SPIM_CS_N	T12	GND
B12	NC	M16	NC	T13	NC
B13	NC	M17	NC	T14	GND
B14	NC	N1	NC	T15	NC
B15	NC	N2	SPIM_MISO	T16	GND
B16	NC	N16	NC	T17	NC
B17	NC	N17	NC	F6, F7, F8, F9, F10, F11, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L6, L7, L8, L9, L10, L11,	E-GND 1...36
C1	HOST_POWER	P1	NC		
C2	NC	P2	SPIM_CLK		
C16	NC	P16	NC		
C17	NC	P17	NC		
D1	SP_MOSI	R1	NC		

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Table 5-3 Signal-to-Pin Relationships and Descriptions

Signal Name	Pin	Type	Reset State	I/O Pad Supply Domain	Description
Digital Control					
HMODE0	T7	I	X	VDDIO	WiFi host mode select, floating input must be tied high or low; see design guide for configuration details
HMODE1	R7	I	X	VDDIO	WiFi host mode select, floating input must be tied high or low; see design guide for configuration details
CHIP_PWD_L	T11	I, PD	Low	HOST_POWER	WLAN power down (0=power down, 1=WLAN awake)
Host Interface (SPI Mode)					
SPI_CLK	J1	I	X	HOST_POWER	SPI clock must be driven
SPI_CS	E1	I/O	PU	HOST_POWER	SPI chip select
SPI_INT	G1	I/O	PU	HOST_POWER	SPI interrupt
SPI_MISO	H1	I/O	PU	HOST_POWER	SPI data output
SPI_MOSI	D1	I/O	PU	HOST_POWER	SPI data input
Master SPI Flash Interface					
SPIM_CLK	P2	I/O	X	VDDIO	Master SPI clock for SPI flash interface
SPIM_CS_N	M2	I/O	High	VDDIO	Master SPI chip select for SPI flash interface
SPIM_MISO	N2	I/O	High	VDDIO	Master SPI data input for SPI flash interface
SPIM_MOSI	R2	I/O	X	VDDIO	Master SPI data output for SPI flash interface
RF Port					
WIFI_RF	T4	A_I/O	N/A	N/A	RF antenna port
System Test					
DEBUG_ UART_RXD	T10	I/O	Low	VDDIO	Reconfigured after software download as debugging UART RXD
DEBUG_ UART_TXD	T6	O	High	VDDIO	Reconfigured after software download as debugging UART TXD
TCK	T9	I, PU	High	VDDIO	WiFi JTAG TCK Used with debugging only
TDI	R9	I, PU	High	VDDIO	WiFi JTAG TDI Used with debugging only
TMS	T8	I, PU	High	VDDIO	WiFi JTAG TMS Used with debugging only

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Signal Name	Pin	Description
Power Supply		
AVDD12	B1	Power supply bypass; WiFi analog 1.2 V supply from internal LDO, connect to external bypass capacitor
AVDD18	A2, A3	Power supply input; WiFi 1.8 V digital, RF, baseband, and synthesizer supplies
DVDD12	A10	Power supply bypass; WiFi digital 1.2 V supply from internal LDO, connect to external bypass capacitor
E_GND1...36	F6, F7, F8, F9, F10, F11, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L6, L7, L8, L9, L10, L11	Ground pads at center of package; All 36 must be connected to the ground plane with sufficient vias; follow design note recommendations (Note that these pins are not aligned to the outer pins. See "Package Dimensions" on page 17.)
GND	A1, A11, E17, K1, R17, T3, T5, T12, T14, T16	All ground pins must be grounded; follow design note recommendations
HOST_ POWER	C1	Power supply input; 1.8 V or 3.3 V Host IO () power supply input
PAREG_33_ OUT	A8, B8	Power supply bypass; internal regulator output, connect to external bypass capacitor
PAREG_BASE	A9	Power supply input, 3.3 V supply; see design guide for details
SW_REG_OUT	B5	Power supply bypass; internal regulator output, leave disconnected
VBAT_42	A7, B7	Power supply input; see design guide for details
VDD33	A6, B6	Power supply input; WiFi antenna and WiFi PA 3.3 V supplies
VDDIO	A4	Power supply input; WiFi digital I/O supply for XTAL oscillator
No Connect		
NC	A5, A12, A13, A14, A15, A16, A17, B2, B3, B4, B9, B10, B11, B12, B13, B14, B15, B16, B17, C2, C16, C17, D2, D16, D17, E2, E16, F1, F2, F16, F17, G16, G17, H16, H17, J16, J17, K16, K17, L1, L16, L17, M1, M16, M17, N1, N16, N17, P1, P16, P17, R1, R3, R4, R5, R6, R8, R10, R11, R12, R13, R14, R15, R16, T1, T2, T13, T15, T17	No connect

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6 Package Dimensions

Figure 6-1 and Figure 6-2 show the AR4100 package dimensions.

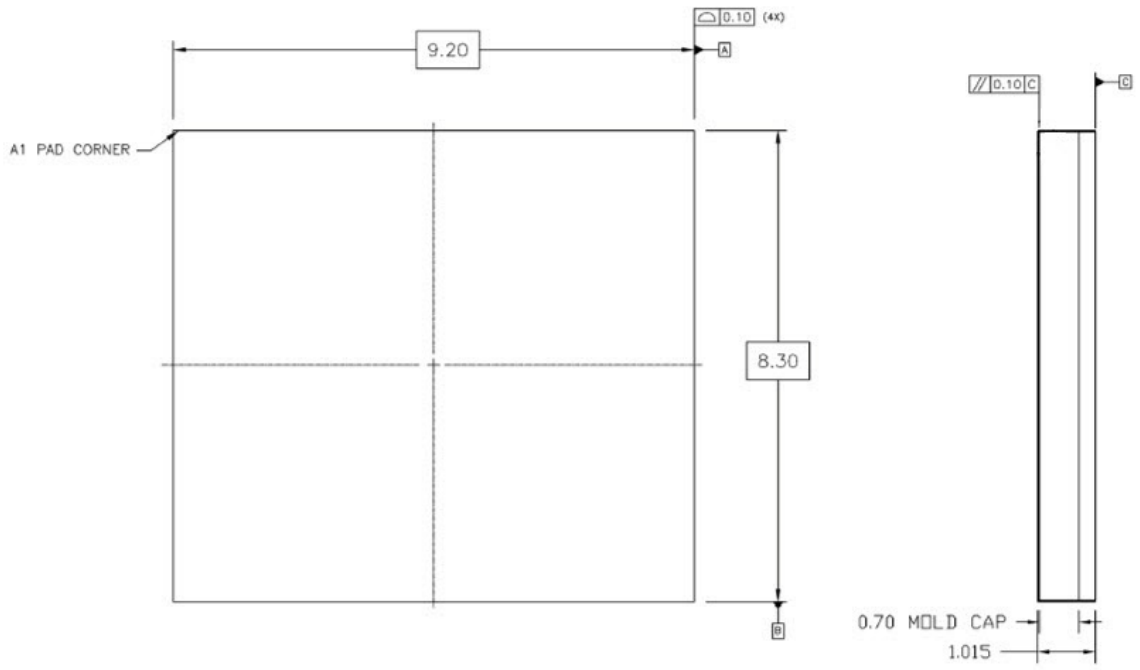

Figure 6-1 AR4100 Package Dimensions Top and Side Views

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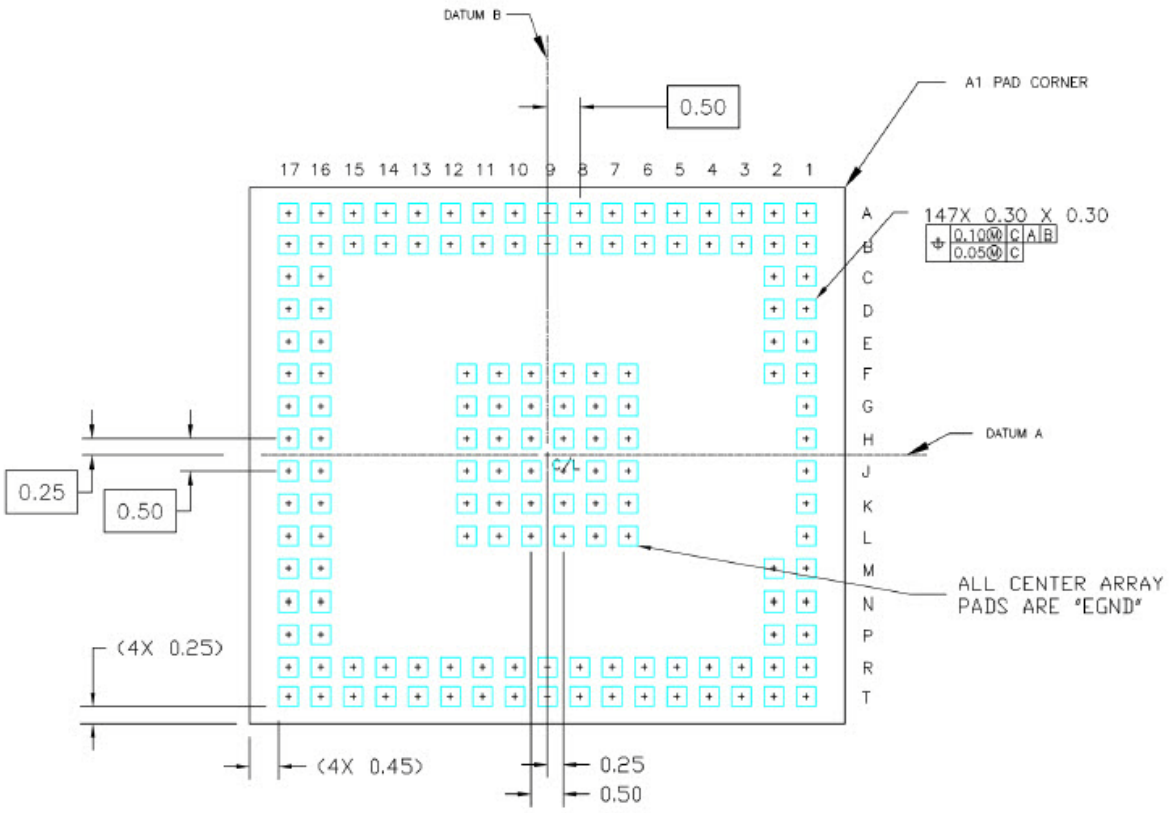

Figure 6-2 AR4100 Pin Assignments

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7 Assembly Guidelines

This section describes the assembly guidelines and solder material information.

Manufacturer Name	Kester
Solder Past Part Number	EM808-Sn96.5% Ag3.0% Cu0.5% SAC305 alloy with Type 3 powder, water soluble solder paste

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8 Design Guidelines

Refer to the *Internet of Things Wireless System Release (I-WSR) 1.4 System Specification* for detailed system requirements and specifications.

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9 Ordering Information

For more information on the AR4100 or other solutions from Qualcomm Atheros, contact your local representative:

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