ALPINE LXT821

Spread Spectrum Digital Cordless Telephone Transceiver

General Description

The ALPINE (LXT 821) is a single chip spread spectrum RF transceiver designed for use in 2.4 GHz Spread Spectrum Digital Cordless Telephone (SSDCT) applications. ALPINE is fully compliant with the FCC Part 15 2.4 GHz ISM band spectrum regulations.

Based on CMOS technology, ALPINE integrates a complete FM transceiver suitable for direct sequence spread spectrum applications. ALPINE includes a 2.4 GHz synthesizer, transmit power amplifier, receive low noise amplifier, antenna switch, channel select filtering, FSK demodulator, and a complete TDD burst-mode controller with forward error correction in a single integrated circuit.

ALPINE can be combined with an ADPCM CODEC and a micro-controller to create a complete SSDCT terminal. No other ICs are required.

The LXT 821 performs all multiplexing / de-multiplexing and spreading / de-spreading functions required to transmit a 32k b/s ADPCM voice signal and 4k b/s data channel over a 2.4 GHz radio link.

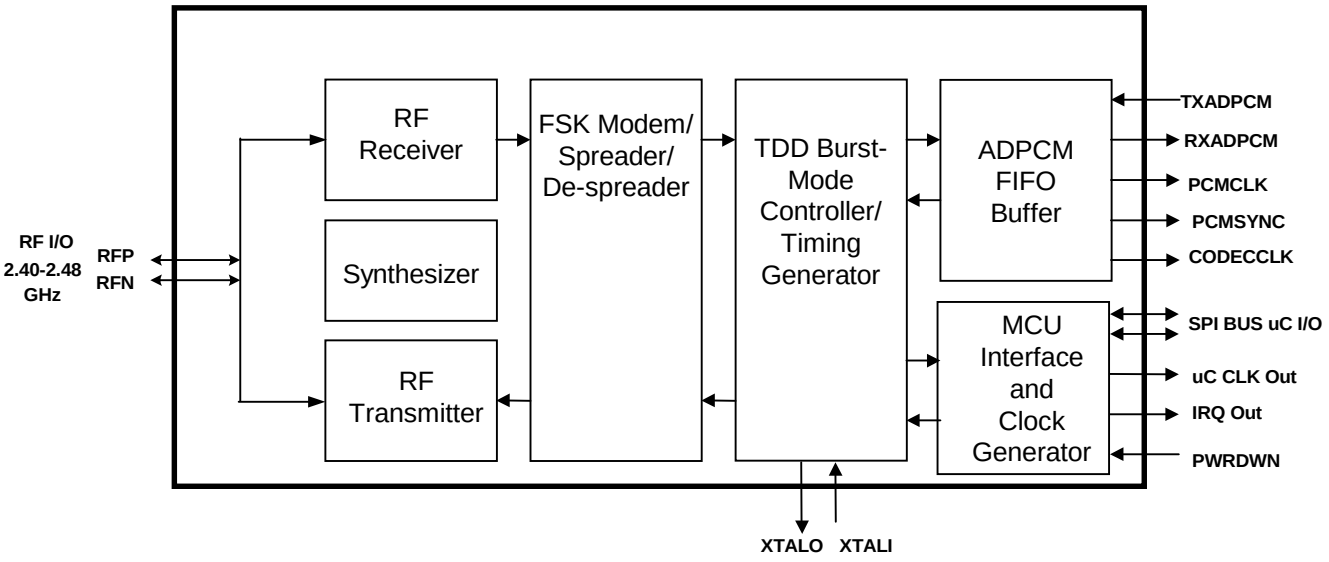
Applications

- Spread Spectrum Digital Cordless Telephones
- Wireless security and monitoring transceivers
- Wireless Spread Spectrum Data/Voice Transceivers

Features

- Single chip wireless transceiver: RF in, Data out
- 2.4 GHz ISM band compliant, 2.4015 to 2.4780 GHz
- Performs all RF transceiver functions on-chip:
  - RF Power Amplifier with 1 to 100 mW output
  - FSK Modulator
  - Synthesizer/Oscillator
  - LNA
  - All Channel Filtering
  - FSK Data Demodulator
  - TDD Burst Mode Controller
  - Receive Signal Strength Indicator (Receiver Gain)
- Very low external component count (<30 discretes)
- No external RF switches required due to TDD format
- 3.0 to 3.6 Volt operation
- Typical current consumption ~ 190 mA average current at maximum transmit power
- Allows for adaptive far end transmit power control
- 1.5 M Chip/s spread data rate
- 2.0 mS Time Division Duplex (TDD) frame rate for reduced side-tone delay
- 32k b/s voice and 4k b/s data channel provides high quality voice and high speed supervisory link between base and handset
- Industry standard SPI bus for control of all functions
- 0 to 70 C temperature range
- Package: 64 pin TQFP

ALPINE Block Diagram



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1. Revision History

Revision Number	Date	Originator	Revision description
1.0	11/18/99	C. Nilson	Initial Revision from LXT 820 Rev 1.4 and LXT 801 Rev 2.1
1.1	11/30/99	C. Nilson	Revised pin names and descriptions to correspond to LXT810
2.0	4/30/00	D. Jones	Update to B1 Revision, add sections on Pin Signal Muxing and Channel Coding
3.0	6/22/00	D. Jones E. Dukatz A. Dickinson	Major Revision of Register Descriptions, Pin Signal Descriptions, added Register Descriptions for new Auto-mute control via Window Path Metric.
3.1	6/25/00	D. Jones	Add description of IRQ timing in Slave search mode Update A1 to B1 changes list
3.2	6/28/00	L. Plouvier	Add full registers description, update definition, defaults and recommendations
4.0	9/21/00	E. Dukatz	Based on Rev 4.1 Design Specification
4.1	9/25/00	E. Dukatz	Corrected Crystal Specification and FRMCTRL register description
4.2	10/14/00	E. Dukatz	Revised Specifications
4.3	11/3/00	E. Dukatz	Changed lowest channel frequency and frequency deviation specification to provide margin on FCC spec.

ALPINE LXT821

Spread Spectrum Digital Cordless Telephone Transceiver

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5. Introduction

5.1 The ALPINE Spread Spectrum Digital Cordless Telephone RF Transceiver

ALPINE is a fully integrated spread-spectrum capable FSK RF Transceiver within a single integrated circuit, which has been optimized for 2.4 GHz spread spectrum digital cordless telephone applications.

A three-chip, single crystal SSDCT terminal can be implemented by combining ALPINE with an ADPCM CODEC, and a standard “off the shelf” micro-controller.

5.1.1

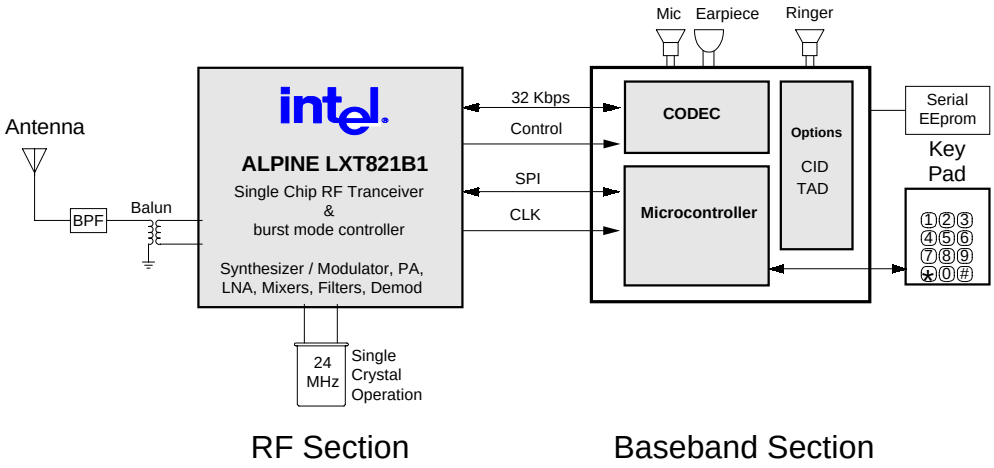


Figure 1: Low Cost RF / Baseband Configuration

5.2 Operation Overview

ALPINE provides all of the necessary active components for a complete 2.4 GHz ISM band FSK transceiver. The ALPINE burst-mode controller (BMC) block performs all spreading / de-spreading, framing / formatting, and time-division duplex (TDD) control required to implement a 2.4 GHz spread spectrum radio suitable for Spread Spectrum Digital Cordless Telephone applications (SSDCT). When combined with an external ADPCM voice codec and micro-controller (MCU), the LXT821 forms a complete SSDCT terminal (base or handset)

ALPINE performs virtually all RF link layer processing required for SSDCT use. Once initialized, the ALPINE is self-synchronizing, and MCU intervention is only required for monitoring RF link performance, RF channel selection and transmit output power setting.

A complete handset can be realized with three integrated circuits and fewer than 30 discrete components, such as, a ceramic 2.4 GHz band pass filter, balun, capacitors, inductors and resistors. No other active components are required.

5.2.1 Transmit Operation

In the transmit direction, the LXT821 combines a 32k b/s ADPCM data input with a 4k b/s data channel input, encapsulates the data in a TDD frame with a preamble and sync word and uses direct sequence spreading to create a binary TX chipping sequence for output to the RF transmitter block. TXCHIP is a digitally spread 1.5 Mchip/Sec signal that is then filtered and level shifted within ALPINE and directly modulates the 2.4 GHz synthesizer. The 2.4 GHz FSK modulated RF signal is then passed on to the internal power amplifier. The power amplifier is capable of transmitting at power levels of +20 dBm, +14 dBm, +8 dBm and +2 dBm.

The power amplifier is automatically disabled as long as the synthesizer is out of lock. This can be the case for a short duration of time (~ 2 mS) upon power up and during RF channel changes. The transmit power amplifier shares a common I/O port with the receive low noise amplifier. Due to the time division duplex operation, the transmitter and receiver are never on at the same time. Because of this, an external antenna switch is **NOT** required.

5.2.2 Receive Operation

For reception, the 2.4 GHz Spread FSK Receive Signal is first low noise amplified and then down converted into a baseband I and Q signal format. The baseband I and Q signals are then AGC amplified, offset cancelled, and filtered for channel selection purposes. The filtered I and Q baseband signals are then A/D converted and FSK demodulated. The BMC block accepts the resulting binary 1.5Mchip/s output, which is then de-spread and de-multiplexed into the 32k b/s ADPCM voice data and 4k b/s data channel signals.

The LXT821 provides radio link diagnostic information to the MCU for active link management capabilities (adaptive power control and channel hopping algorithms), including a Link Quality Alarm output (LQA). The LQA is available both in a register bit and at a dedicated pin making it suitable for antenna diversity applications.

5.2.3 Transceiver Control

The automatic gain control (AGC) section of the receiver supplies a Receive Signal Strength Indicator in the form of receiver gain to the MCU via the 4-wire serial peripheral interface (SPI) bus. The receiver gain data is valid for input levels from -96 dBm to -28 dBm. receiver gain changes in increments of 6dB.

The receiver gain information is useful for far end adaptive transmit power control. In addition, when the receiver gain data from ALPINE is combined with the Link Quality information, in-band interference can be determined. Channel selection can then be based on a combination of receive signal level and interference.

Channel selection is accomplished by programming the 2.4 GHz synthesizer within ALPINE via the 4 wire SPI Bus by the external micro-controller.

Finally, ALPINE can be powered down and will draw less than 100 uA of current. Power down is accomplished by writing to the appropriate SPI control register, or by driving the external PWRDNP pin.

5.2.4 Time Division Duplex

ALPINE uses the time division duplex (TDD) frame format shown in Figure 2.

The TDD frame is 2mS in length, and is composed of two symmetrical 960 uS TX and RX subframes. Each subframe contains 96 bits of 10uS duration, with 40 uS guard times between both TX and RX subframes.

Each subframe consists of the following four fields:

- A 12-bit Preamble field
- An 8-bit Sync Word
- An 8-bit Data Channel field
- A 64-bit Payload
- A 4-bit Post-amble

Both the 8-bit Sync Word and 8-bit Data Channel are programmable via the MCU interface. In addition, the 64-bit payload can be filled either with ADPCM voice data, or can be used by the host MCU as a fast data channel between base and handset. See the register descriptions that follow for details.

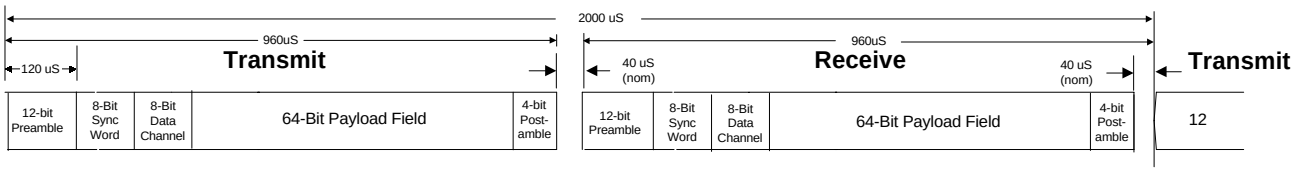


Figure 2: ALPINE TDD Frame Format

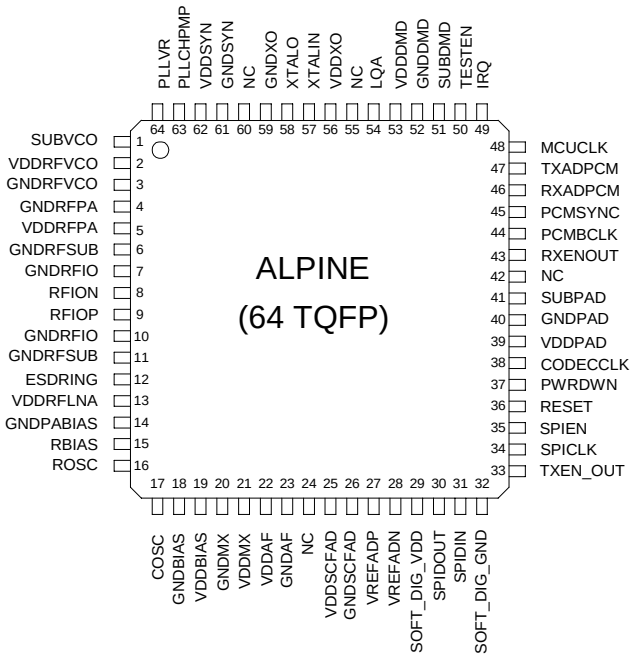
ALPINE LXT821

Spread Spectrum Digital Cordless Telephone Transceiver

6. Pin Assignments and Signal Descriptions

6.1 Package Description

ALPINE utilizes a 64 pin TQFP with package dimensions of 10 x 10 x 1.4 mm^3



6.2 RF Interface Pins

Table 1 : RF Interface Pin Descriptions

Pin #	Name	I/O	Description
8	RFION	I/O	**Balanced RF Input and Output Negative Side** Used in conjunction with RFIOP to create a balanced RF I/O port.
9	RFIOP	I/O	**Balanced RF Input and Output Positive Side** Used in conjunction with RFION to create a balanced RF I/O port.
33	TXEN_OUT	O	**Can be used by external circuitry.** When high this pin indicates that the transmitter is enabled. Normally Disconnected.
43	RXENOUT	O	**RXENOUT:** When high this pin indicates that the receiver is enabled.
54	LQA	O	**Link Quality Alarm:** The Link Quality Alarm indicates when the correlator error rate exceeds a programmed threshold. The threshold is programmed in register 0x11.
63	PLLCHPMPP	NA	**Phase Locked Loop Charge Pump:** The PLL loop filter components connect between PLLRC and PLLVR. Charge pump current drives the external loop filter on this pin.
64	PLLVR	NA	**Phase Locked Loop Varactor Reference Voltage:** A regulated varactor reference voltage is used to increase the VCO PSRR. The PLL loop filter components connect between PLLRC and PLLVR.

6.3 ADPCM Interface Pins

Table 2: ALPINE ADPCM Interface Pin Descriptions

Pin #	Name	I/O	Description
47	TXADPCM	I	**Transmit ADPCM Data: (TXADPCM)** TXADPCM receives the 32k b/s ADPCM data output signal of an external ADPCM CODEC IC.
46	RXADPCM	O	**Receive ADPCM Data: (RXADPCM)** RXADPCM drives the 32k b/s ADPCM data input line of an external ADPCM CODEC IC.
38	CODECCLK	O	**CODEC Master Clock: (CODECCLK)** The CODEC clock can be programmed to either 19.2 MHz or 24.0 MHz to drive the master clock input to an external ADPCM CODEC IC.
44	PCMBCLK	O	**PCM Bit Clock: (PCMBCLK)** PCM Clock operates at 32k b/s or 64k b/s and is used to clock both the transmit and receive PCM data to an external ADPCM CODEC IC
45	PCMSYNC	O	**PCM Synchronization Clock: (PCMSYNC)** PCMSYNC operates at 8 kHz and is used to synchronize the MSB of both transmit and receive ADPCM signals to an external ADPCM CODEC IC.

6.4 SPI bus Micro-controller Interface

Table 3: Micro-controller Interface Pin Descriptions

Pin #	Name	I/O	Description
30	SPIDOUT	O	**SPIDOUT: SPI Data Out** Data Output for byte-wise data transmitted serially to the MCU, MSB first. Data transitions are on the falling edge of SPICLKIN and the data is sampled by the MCU on the rising edge of SPICLKIN.
31	SPIDIN	I	**SPIDIN: SPI Data Input** Data input for byte-wise data transmitted serially from the MCU, MSB first. Data is sampled by the BMC on the rising edge of SPICLKIN.
34	SPICLK	I	**SPICLKIN: SPI Clock Input** Serial clock to synchronize the data movement both in and out of the BMC.
35	SPIEN	I	SPIEN**: SPI Bus Enable - Active Low** The SPIEN line is used to select ALPINE as a slave device for data transactions. It must be low prior to the beginning of a transaction and must stay low for the duration of the transaction.
48	MCUCLK	O	**MCUCLK: Micro-Controller Clock** The micro-controller clock frequency can be programmed to various operating frequencies, 100 kHz, 2 MHz, 4 MHz, 6 MHz, 12 MHz . In addition when the IC is powered down the MCUCLK is placed in a low speed mode (100 kHz or 200 kHz) to allow the external micro-controller to draw less power. When in the low power mode the frequency is determined by ROSC and COSC on pins 16 and 17 respectively.
49	IRQ	O	**IRQ: Interrupt Request:** The interrupt is generated on various edges of the transmit and receive frame as determined by register 0x14. When the interrupt is not selected the pin is used to monitor the state of the synthesizer unit cap controller for test purposes.

6.5 Miscellaneous Pin Descriptions

Table 4 : Miscellaneous Pin Description

Pin #	Name	I/O	Description
37	PWRDWN	I	**PWRDWN: Power Down: (Active Hi)** This can be driven from the CODEC or from an external micro-controller. **Errata**: The power down pin does not turn of the BMC section in the LXT821A1. In both the LXT821A1 and LXT821B1, it does not reset the receiver state machines.
36	RESET	I	**RESET: (Active Low)** Resets all registers to known states.
57	XTALIN	I	**Crystal Connection Input:** One terminal of a +/- 30 PPM AT Cut 24 MHz crystal is connected here. A 20 pF capacitor is also connected from this pin to ground for proper phasing. It is also possible to AC couple an external 24 MHz Clock of 0.2 to 2 Vp-p to this input.
58	XTALO	O	**Crystal Connection Output:** One terminal of a +/- 30 PPM AT Cut 24 MHz crystal is connected here. A 20 pF capacitor is also connected from this pin to ground for proper phasing. If an external 24 MHz signal is AC coupled to Pin 57 (XTALIN) then XTALO should be left unconnected.
16	ROSC	NA	**ROSC: Low Frequency Oscillator Resistor**, ROSC determines the frequency of the low speed oscillator that is output on the micro-controller clock during power down. **Note:** Rosc and Cosc must be installed for MCUCLK output to function.
17	COSC	NA	**COSC: Low Frequency Oscillator Capacitor** COSC determines the frequency of the low speed oscillator that is output on the micro-controller clock during power down.
15	RBIAS	NA	**Bias Resistor Connection:** External 10.0k ohm, 1% resistor is connected to ground.
27	VREFADP	NA	**VREF Bypass Connection:** External .1uF is connected to ground
28	VREFADN	NA	**VREF Bypass Connection:** External .1uF is connected to ground
50	TESTEN	I	Factory Scan Test Enable PIN: Normally grounded
24	NC	NA	Normally Disconnected
42	NC	NA	Factory Analog Test Pin: Normally Disconnected
55	NC	N/A	Factory Analog Test Pin: Normally Disconnected
60	NC	N/A	Factory Analog Test Pin: Normally Disconnected

6.6 Power Supply Pins

Table 5: Power Supply Pin Descriptions

Pin #	Name	I/O	Description
1	SUBVCO	NA	**VCO Substrate Connection:** Connect to Ground
2	VDDRFVCO	NA	**RF VCO Frequency Synthesizer Supply:** Connect to VDD. Bypass with .1uF and 3.9 pF capacitor
3	GNDRFVCO	NA	**RF VCO Frequency Synthesizer Ground:** Connect to Ground
4	GNDRFPA	NA	**Power AMP Driver Ground:** Connect to Ground
5	VDDRFPA	NA	**Power AMP Driver Supply:** Connect to VDD. Bypass with .1uF and 3.9 pF capacitor
6	GNDRFSUB	NA	**RF Substrate Connection:** Connect to Ground
7	GNDRFIO	NA	**RF I/O Ground:** Connect to Ground
10	GNDRFIO	NA	**RF I/O Ground:** Connect to Ground
11	GNDRFSUB	NA	**RF Substrate Connection:** Connect to Ground
12	ESDRING	NA	**ESD Ring Connection:** Connect to Ground
13	VDDRFLNA	NA	**RF Low Noise Amplifier Supply:** Connect to VDD. Bypass with .1uF and 3.9 pF capacitor
14	GNDPABIAS	NA	**PA BIAS Ground:** Connect to Ground
18	GNDBIAS	NA	**Bias Generator Ground:** Connect to Ground
19	VDDBIAS	NA	**Bias Generator Supply:** Connect to VDD. Bypass pin 19, 22, 25, 29, and 32 with single .1uF capacitor.
20	GNDMX	NA	**Mixer Ground:** Connect to Ground
21	VDDMX	NA	**Mixer Supply:** Connect to VDD. Bypass with .1uF and 3.9 pF capacitor
22	VDDAF	NA	**Anti-Alias Filter Supply:** Connect to VDD. Bypass pin 19, 22, 25, 29, and 32 with single .1uF capacitor.
23	GNDAF	NA	**Anti-Alias Filter Ground:** Connect to Ground
25	VDDSCFAD	NA	**Switched Capacitor Circuit Supply:** Connect to VDD. Bypass pins 19, 22, 25, and 29 with single .1uF capacitor.
26	GNDSCFAD	NA	**Switched Capacitor Circuit Ground:** Connect to Ground
29	SOFT_DIG_VDD	NA	**Timing generator, A/D and SCF digital Supply:** Connect to VDD. Bypass pins 19, 22, 25, and 29 with single .1uF capacitor.
32	SOFT_DIG_GND	NA	**Timing generator, A/D and SCF digital GND.**
39	VDDPAD	NA	**Digital PAD Driver Supply:** Connect to VDD. Bypass with single .1uF capacitor.
40	GNDPAD	NA	**Digital PAD Driver Ground:** Connect to Ground
41	SUBPAD	NA	**Digital PAD Substrate Connection:** Connect to Ground
51	SUBDMD	NA	**Digital Core Substrate Connection**: Connect to Ground
52	GNDDMD	NA	**Digital Core Ground**: Connect to Ground
53	VDDDMD	NA	**Digital Core Supply**: Connect to VDD. Bypass pins 53 and 56 with single .1uF capacitor.
56	VDDXO	NA	**Crystal Oscillator Supply:** Connect to VDD. Bypass pins 53 and 56 with single .1uF capacitor.
59	GNDXO	NA	**Crystal Oscillator Ground:** Connect to Ground
61	GNDSYN	NA	**Synthesizer Divider Ground:** Connect to Ground
62	VDDSYN	NA	**Synthesizer Divider Supply:** Connect to VDD. Bypass with .1uF and 3.9 pF capacitor

7. Interfaces and Functions

7.1 RF Interface Description

The RF interface consists of one Bi-directional Balanced RF port and requires two pins.

During the **Transmit Mode** the RFIOP and RFION terminals serve as the balanced Transmit Power Amplifier output terminals.

During the **Receive Mode** the RFIOP and RFION terminals serve as the balanced Low Noise Amplifier input terminals.

During either the **Ready Mode or the Power Down Mode** both RFIOP and RFION revert to a high impedance state.

7.1.1 Balanced RF Input and Output

Negative side RFION, Pin 8
Positive side RFIOP, Pin 9
ALPINE connects to an antenna through a network of balanced matching components, a balun, a 50 Ohm ISM band pass filter and a single ended 50 Ohm to antenna impedance matching network

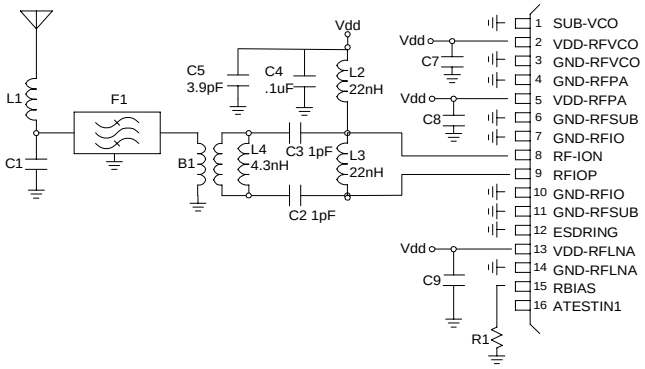


Figure 3: RF Input and Output

Inductors L2 and L3 are RF chokes that provide DC bias current to the RFION and RFIOP balanced RF I/O port. Capacitors C4 and C5 provide a RF ground at the Vdd terminal to L2 and L3. Vdd, L2, C4, and C5 can be connected on either side of L3. This unsymmetrical bias arrangement minimizes the power supply trace length to pins 8 and 9. This is done to eliminate potential instability at the RF I/O pins 8 and 9. The .1uF capacitor provides low frequency bypass and the 3.9 pF capacitor provides bypass at 2.4 GHz.

Components C2, C3 and L4 convert the complex impedance looking into RFION and RFIOP into 50 Ohms when monitored differentially across L4.

A balanced to unbalanced transformer (Balun) is used to convert the 50 Ohm differential signal to a 50 Ohm single ended signal. A 50 Ohm ISM band two pole ceramic resonator filter is used to help reject out of band signals. Matching components L1 and C1 convert the antenna impedance to 50 Ohm. Components L1 and C1 depend strongly on the type of antenna used and the size and shape of the printed circuit board ground plane.

Notes:

It is possible to use etched printed circuit board inductors and Balun for lower cost.

Other implementations, such as, fully differential antenna, filter and impedance circuits are possible.

When combined with external active components such as low noise amplifies, power amplifiers and PIN diode RF switches, it is possible to decrease the system noise figure and increase the available system output power; however, this is not recommended for low cost systems. If an external power amplifier is used, care must be taken during IC power up; the default condition places the IC into an active transmit mode at maximum output power. Refer to figure 18 for more details.

7.1.2 Synthesizer Phase Lock Loop

Table 6 Synthesizer Specifications

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Power Down To Synthesizer Lock Time	T_{PDRDY}	---	---	2	mS	Utilizing Synthesizer Test Circuit
Channel Change Time	T_{CH}	---	---	1	mS	Utilizing Synthesizer Test Circuit
Phase Locked Loop Closed Loop Band Width	BW_{PLL}	2.5	5	10	kHz	Utilizing Synthesizer Test Circuit
For Temperature = 25 ^{O}C, V_{DD} = 3.6 Volts,						

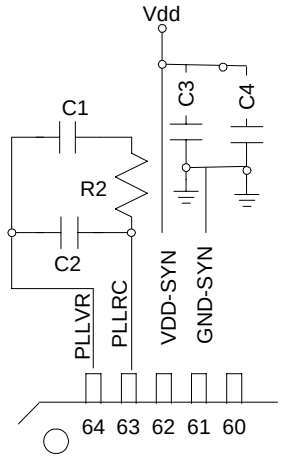


Figure 4: Synthesizer Test Circuit

Synthesizer Test Circuit Component Values:
C1 = 0.2 uF, R2 = 2 k ohm, C2 = 0.01uF, C3 = 0.1uF, C4 = 3.9 pF

The synthesizer phase lock loop bandwidth (PLL BW) can be changed by using either a high charge pump current or a low charge pump current. The high and low charge currents can be independently adjusted to 0 uA, 100 uA, 200 uA, 300 uA, 400 uA, 500 uA, 600 uA, or 800 uA by accessing registers 5B and 5C respectively.

Default operation will configure the PLL to use a low charge pump current of 100 uA. There is an option that will automatically enable the high charge pump current during transitions on the transmit enable and receive enable signals. This will increase PLL BW during supply current spikes thereby attenuating transmit spurs. This feature is normally disabled. The duration of high charge pump current operation is controlled by register 53.

Register 57 controls which charge pump current value is used and can enable the automatic charge pump switch.

When the channel frequency is changed the charge pump current should be set to 800 uA for 250 uS. If this is not done, the PLL can become unstable and lose lock during a channel change. The recommend channel change procedure is:

- Program register 57 = 0D hex: enable 800 uA high charge pump current
- Change channels by writing to registers 40, 41, and 42.
- Wait 250 uS
- Program register 57 = 04: enable 100 uA low charge pump current

This channel changing procedure will result in a maximum PLL settling time of 3 mS. PLL lock time will be 1mS or less.

The low charge pump current default value is 100 uA and the high charge pump current default value is 800 uA; therefore, registers 5B and 5C should never be reprogrammed.

Note:
The transmit power amplifier will automatically shut down if the PLL goes out of lock. This is done to eliminate unwanted radiation outside of the ISM band. This situation can arise due to a low supply voltage, a transition from the power down state to the ready state, or a channel change.

7.1.3 Crystal Clock

Table 7: Crystal Oscillator Specifications

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Externally applied XTALIN Voltage, AC coupled	V_{XI}	0.3	1	2.0	V_{PP}	AC coupled
Externally applied XTALIN Duty Cycle	D_{Cycle}	45/55	50/50	55/45	%	AC Coupled
XTALIN Pin capacitance	C_{XI}	---	1.7	2	pF	
XTALO Pin capacitance	C_{X0}	---	1.7	2	pF	
XTAL Oscillator Frequency Accuracy	F_{XO}	-30	0	+30	ppm	Total frequency variation due to both temperature and frequency accuracy. See test circuit below. Frequency measured at CODECCLK or MCUCLK pins.
XTAL Oscillator Duty Cycle	$D_{CycleXO}$	45/55	50/50	55/45	%	See test circuit below. Duty Cycle measured at CODECCLK pin.
Oscillator Turn On Time After Supply Power Up: After Power Down Disable:			 2.0 0.5	 5.0 1.0	mS	See test circuit below. **Note:** Turn On Time dependent on crystal specifications.
Crystal Signals Include; XTALIN and XTALO Crystal Oscillator Measurements are at 25 ^{O}C and V_{DD} = 3.3 Volts						

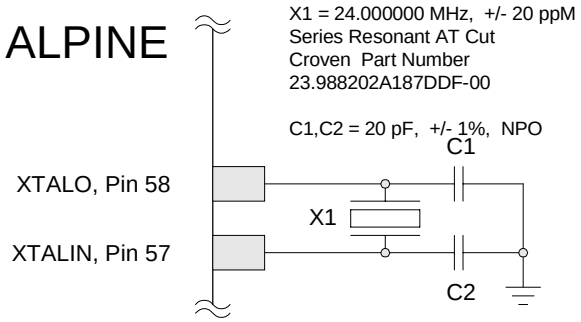


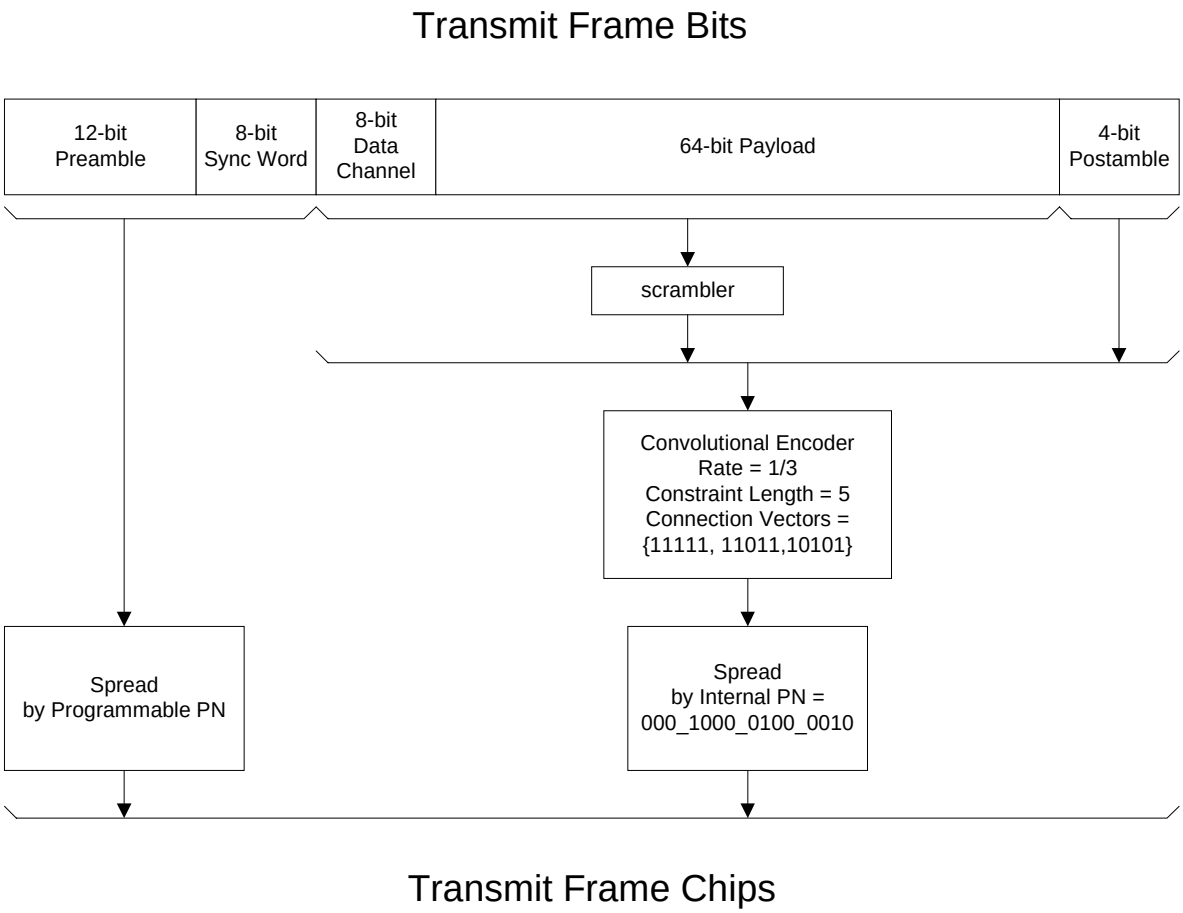
Figure 5: Crystal Oscillator test Circuit

7.2 Channel Coding and Direct Sequence Spreading

The various segments of the transmitted frame undergo different coding treatment and are spread by different PN sequences.

- The Preamble and Sync Word are spread with the user programmable PN code in PNREG1 and PNREG2 (addresses 0x00 and 0x01).
- The Data Channel and Voice / Fast Data Channel (FDC) Payload are scrambled, run through a rate 1/3 convolutional encoder, and spread with a preset, non-programmable, PN code.
- The Post-amble is treated the same as the Data Channel and Payload except that it is not scrambled; the four post-amble bits are always equal to zero.

Figure 6, Channel Coding and Spreading



7.2.1 Spreading

Each bit is spread by a 15-bit PN code. The spreading is exactly in phase with the start of the bit; start of Most-Significant-Chip coincides with start of bit. The user programmable PN is contained in registers 0x00 and 0x01.

7.2.2 Scrambler

Data scrambling is done with an LFSR:

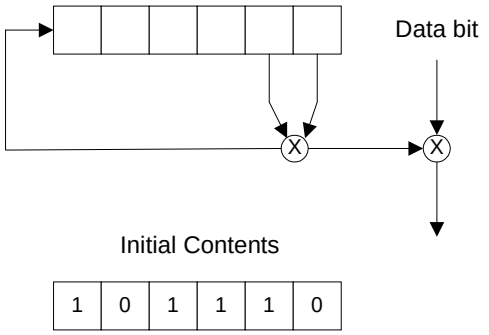


Figure 7, Data Scrambler LFSR

7.2.3 Convolutional Encoder

Figure 8 illustrates the Alpine convolutional encoder in so-called connection representation. In this representation, the encoder action is imagined to take place in two stages: First a bit is shifted into the shift register from the left, the rightmost bit being shifted out. Second, the rotary switch rotates, touching each of the three contacts in turn. The constraint length is 5, meaning that the shift register is 5 message bits wide. The code rate is 1/3 meaning that one message bit results in three code symbols. The three code symbols occupy one bit period.

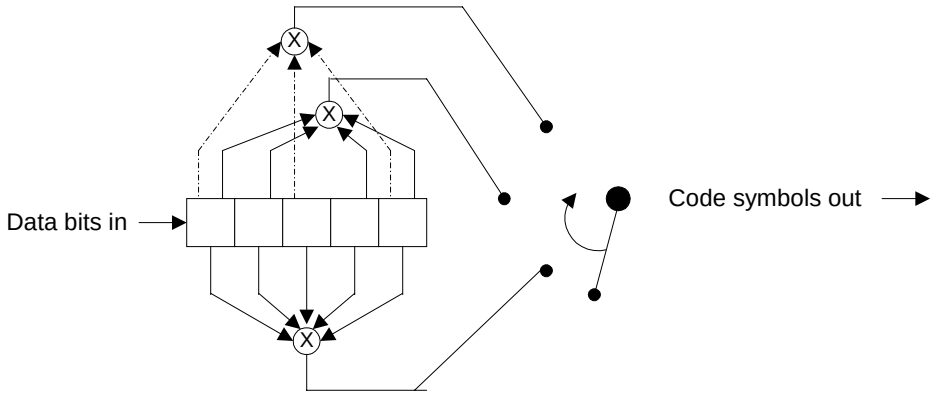


Figure 8, Alpine Convolutional Encoder

The connection vectors are the shift register taps. The vectors used in the Alpine encoder are well known optimal performing vectors for constraint length five and rate 1/3. Optimal means that the encoder is non-catastrophic and has maximal Hamming distance between code word sequences. (A catastrophic encoder has the property that certain finite sequences of erroneous code symbols will cause the decoder to decode an infinite sequence of bit errors.)

7.3 ADPCM CODEC Interface

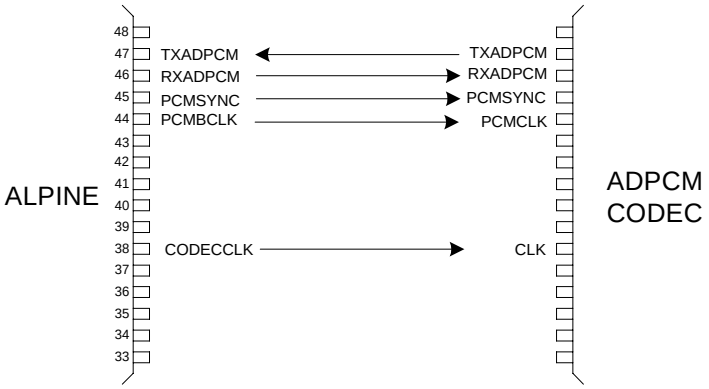


Figure 9 ALPINE / CODEC Interface Connections

The interface to the ADPCM Codec consists of five signal lines:

- TXADPCM – 32 k b/s voice data coming from the Codec to be transmitted over the RF link
- RXADPCM – 32 k b/s voice data received over the RF link to be output to the Codec
- PCMBCLK - A 32 kHz or 64 kHz bit clock
- PCMSYNC - An 8 kHz PCM Sync signal
- CODECCLK - A 19.2 MHz or 24.0 MHz clock used to drive the master clock input to the Codec. Can be deactivated if necessary.

7.3.1 ADCPM timing

The ADPCM Codec interface can be set to operate in one of two timing modes. These two modes are implemented to ensure compliance with different ADPCM Codec interface requirements

7.3.1.1 Mode 0

Mode 0 provides a continuous, non-gapped 32k b/s interface, which allows for simplified link BER testing

Operation in ADPCM Mode 0 (Register 0F **CLKCTRL[4]** = 0) is shown below

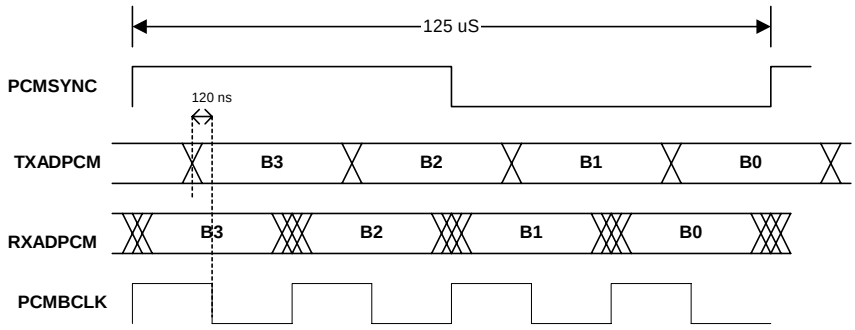


Figure 10: ADPCM Interface Timing Diagram Mode 0

Errata: In the LXT821A1 and LXT821B1, if the IC is operated in slave mode, the TXADCPM is sampled on the rising edge. The other TXADCPM and RXADPCM signals are sampled on the falling edge, whether Alpine is operated as either a slave or master mode.

7.3.1.2 Mode 1

Mode 1 is compliant with the OKI 7570L series ADPCM codec as well as codecs manufactured by AKM and others. Operation in ADPCM Mode 1 (Register 0F **CLKCTRL[4]** = 1) is shown below

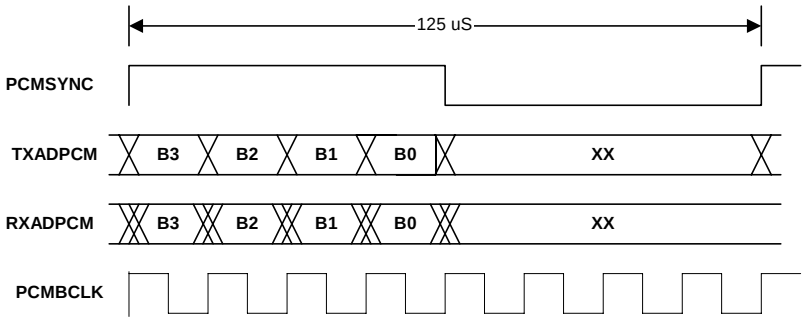


Figure 11: ADPCM Interface Timing Diagram Mode 1

7.4 Micro-Controller Interface Description

The Micro-Controller (MCU) interface provides external control and monitoring of all internal functions. The MCU interface is compatible with the industry standard Motorola Serial Peripheral Interface (SPI) bus. The SPI bus is organized in a master/slave manner*, with the host MCU usually being the master. ALPINE must be used as a SPI slave device.

*- **Note:** no relationship to TDD Master/Slave protocol operation

7.4.1 SPI Bus Description

The SPI bus used in ALPINE consists of the following four signals:

7.4.1.1 Micro-Controller Master CLK Output (MCUCLK)

Clock for input to the MCU. This clock can be programmed to a frequency of either 100kHz, 2, 4, 6, or 12 MHz using CLKCTRL[2:0].

This clock is switched to a low-frequency (100 kHz) standby oscillator when PWRDN[5] is asserted. The operating frequency of the low-speed clock is set by the capacitor and resistor connected to the COSC and ROSC pins. It is possible to increase this clock frequency to 200 kHz.

Note: The higher speed MCU clocks are divided down from the 24 MHz crystal clock. In addition, the circuit that switches between the high-speed and low-speed clocks is designed to be glitch-free, eliminating the possibility of generating fractional clock cycles during a switch-over. This circuit requires that both clocks be active during the switchover. The external components at the ROSC and COSC are required for the MCU clock output to operate, regardless of selected operating frequency.

7.4.1.2 SPI Data In (SPIDIN)

Data input for byte-wise data transmitted serially from the MCU, MSB first.

7.4.1.3 SPI Data Out (SPIDOUT)

Data Output for byte-wise data transmitted serially to the MCU, MSB first. Data transitions are on the falling edge of SPI CLK and the data is sampled by the MCU on the rising edge of SPICLK. **Note:** SPIDOUT is only made active when SPIEN is low and the SPI register being read from is within Alpine's 00h to 7Fh address space. Otherwise, SPIDOUT is placed in the high-impedance state.

7.4.1.4 SPI Clock In (SPICLK)

Serial clock to synchronize the data movement both in and out of Alpine. See timing diagrams in both **Figure 12** and **Figure 13** below.

7.4.1.5 SPI Enable (SPIEN)

The SPI EN line is used to select ALPINE as a slave device for data transactions. It must be low prior to the beginning of a transaction and must stay low for the duration of the transaction.

7.4.2 SPI Protocol Description

The SPI bus is a byte-wise serial transmission link between the system MCU and peripheral devices. To translate the byte-wise serial nature of the SPI bus to Alpine's register-mapped I/O, it uses the following protocol to communicate via the SPI bus. A typical ALPINE SPI bus transaction consists of two SPI bus operations, first the MCU transmits the address byte of the register to be written to/read from, after which the MCU or ALPINE outputs the data byte, depending on whether a read or write operation was indicated (see below).

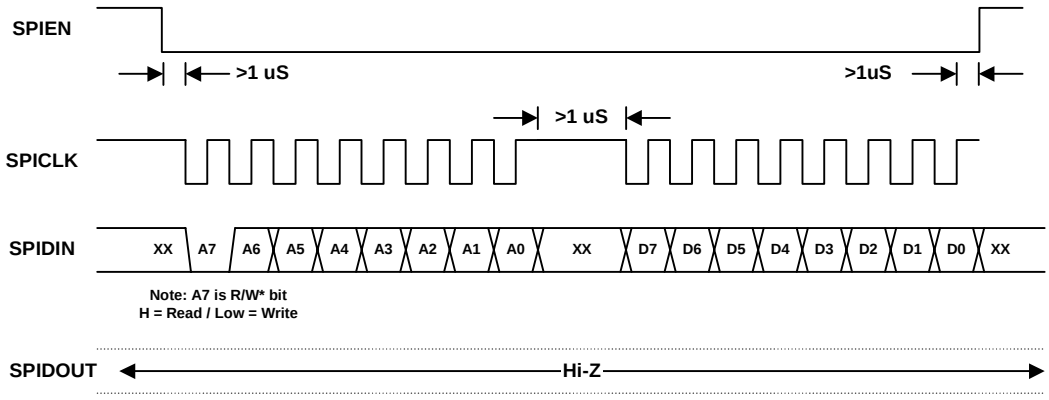
A SPI read or write is initiated by asserting SPIEN (active low), whose falling edge resets the internal SPI controller state machine, readying it for the first (address) byte. The MSB of the address byte (**A[7]**) indicates whether a read or write transaction is to be performed. **A[7]** is high for read operations and low for write operations. The remaining address bits (**A[6:0]**) address the individual registers in the ALPINE register map.

Note: Alpine's register map is divided into 3 sections. The analog section of the IC uses a Intel proprietary "Quiet Bus Technology" based on a Three Wire Interface (TWI) for minimum interference and area purposes. These 4-bit registers are accessed externally via the SPI interface, and are mapped to the low order nibble of addresses from 40h to 7Fh. The Burst Mode Controller section uses standard 8-bit SPI registers, which are mapped to addresses from 00h to 2Fh. The remainder of Alpine's 8-bit registers are mapped to addresses from 30h to 3Fh. Registers 40h and higher are not accessible during power down operation as they require a functioning 24.0 MHz clock.

7.4.3 SPI Write Operation

For a Write operation, the MCU first asserts SPIEN, and then outputs the address byte of the register to be accessed, with the MSB of the address byte (A7) set low. After all 8 address bits are transmitted the MCU outputs the data byte to be written into the addressed register, MSB first. Finally the MCU de-asserts the SPIEN line to high.

Figure 12: SPI Bus Write Operation Timing Diagram

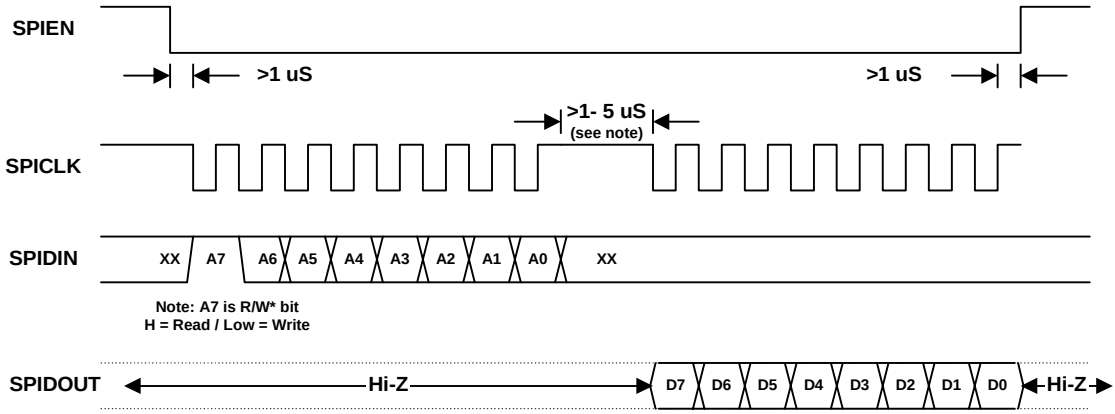


7.4.4 SPI Read Operation

For a Read operation, the MCU first asserts SPIEN, and then outputs the address byte of the register to be accessed, with the MSB of the address byte (A7) set high.

After all 8 address bits are transmitted the MCU issues a SPI Read command, which produces 8 cycles of SPICLK. The BMC responds by outputting the data byte read from the addressed register on SPIDOUT, MSB first, with transitions on the falling edges of SPI CLK. Finally the MCU de-asserts the SPIEN line to high.

Figure 13: SPI Bus Read Operation Timing Diagram



For more information on SPI bus operation, refer to the Motorola 68HC705 technical manual

7.4.5 Fast Data Channel

The Fast Data Channel (FDC) allows the system MCU to write/read from the 64-bit payload field of the TDD frame. This gives the MCU a much faster communications channel between handset and base when there is no need to send ADPCM voice data (i.e. when on-hook).

The Fast Data Channel mode uses the FDCCTRL, TXFDCBUF, and RXFDCBUF registers to provide a 32k b/s end-to-end high-speed data link.

To enable the Fast Data Channel, the system MCU must set the TX FDC Enable and RX FDC Enable bits (FDCCTRL[4] and FDCCTRL[0]).

7.4.5.1 TX Fast Data Channel Operation

The TX FDC buffer is a double-buffered 64-bit register that is copied into the TX payload field when **FDCCTRL[4]**=1. To write to the TX FDC Buffer, the MCU writes to the 64-bit TXFDC buffer (TXFDCBUF) with a 9-byte SPI bus operation as follows.

The MCU first outputs the TXFDCBUF address (09h), clearing the read / write bit. The MCU then writes eight bytes in succession which contain the 64 bits to be transmitted over the RF link. When ALPINE has received the eighth byte, it sets the TXFDC status flag (FDCCTRL[7]), and waits for the next TX frame to insert the contents of the TX FDC buffer into the outgoing TX payload field.

Once the payload has been output, the TX FDC status flag is cleared.

Note: If the write operation is aborted before all nine bytes have been received over the SPI bus (by disabling SPIEN), the contents of the TX FDC buffer will not be updated, and will contain the contents of the last successfully completed write operation.

In addition, as long as **FDCCTRL[4]** is set, the outgoing TX payload field will continue to transmit the contents of the TX FDC buffer regardless of whether the buffer has been updated since the last outgoing TX frame.

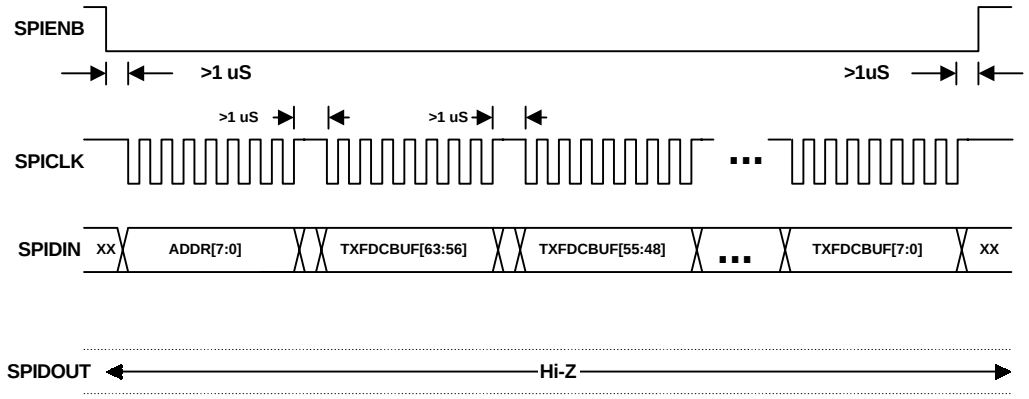


Figure 14: TX Fast Data Channel Write Operation Timing Diagram

7.4.5.2 RX Fast Data Channel Read

The RX FDC buffer is a double-buffered 64-bit register that is loaded with the RX payload field when **FDCCTRL[0]**=1. When RX FDC operation has been enabled (**FDCCTRL[0]** = 1), ALPINE waits for the next incoming RX frame, and then loads the contents of the incoming 64-bit payload field into the RX FDC buffer and sets the RX FDC status flag (**FDCCTRL[3]**).

To read the contents of the RX FDC Buffer, the MCU reads from the 64-bit RX FDC buffer (RXFDCBUF) with a 9-byte SPI bus operation as follows.

The MCU first outputs the RXFDCBUF address (0Ah), setting the read / write bit. The MCU then reads eight bytes in succession which contain the 64 bits received in the last incoming RX frame. When ALPINE has received the eighth byte, it clears the RXFDC status flag (**FDCCTRL[3]**), and waits for the next incoming RX frame.

The contents of the RX FDC buffer will be written over by each successive received frame, regardless of whether the MCU reads the contents of the RX FDC buffer.

Note: If the read operation is aborted before all nine bytes have been received over the SPI bus (by disabling SPIEN), the RXFDC status flag will not be cleared.

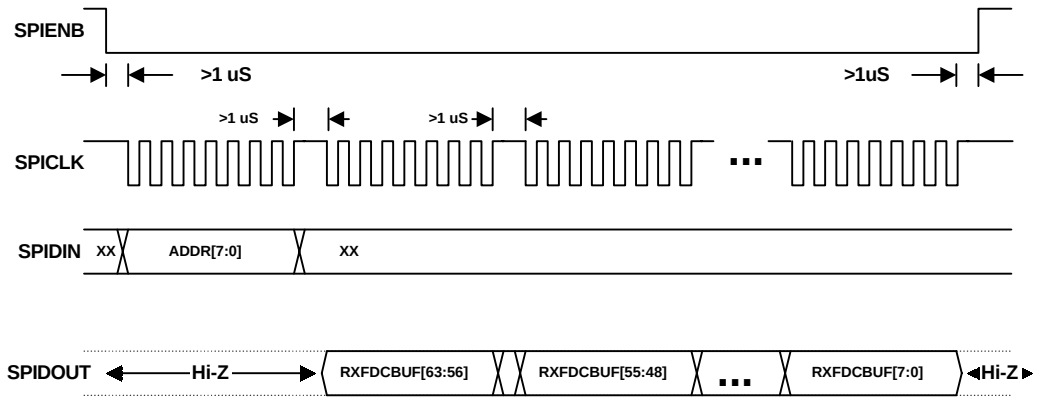


Figure 15: RX/TX Fast Data Channel Read Operation Timing Diagram

7.4.6 MCU Interrupt output (IRQ)

ALPINE provides an interrupt output, IRQ, to synchronize the MCU to the TDD burst timing. The IRQ output can be programmed to present up to two interrupts per TDD frame. Each interrupt consists of a 10 uS negative-going pulse. The number and timing of each interrupt is programmed in the **IRQFRMT** register.

The TX and RX slots each have their own interrupt, which can be independently enabled or disabled. When enabled, each TX/RX slot interrupt can be programmed to occur at either the beginning or end of their respective payload fields. The timing of these locations is shown below.

The IRQFRMT register controls the operation of the IRQ output. **IRQFRMT[1:0]** enables and sets the location of the RX interrupt, while **IRQFRMT[3:2]** enables and sets the location of the TX interrupt.

The IRQ TX/RX flag, **IRQFRMT[7]**, indicates whether the last interrupt generated was a TX interrupt or an RX interrupt. The flag is set upon generation of a TX interrupt, and cleared upon generation of an RX interrupt. If RX interrupts are disabled, the flag stays set, and if TX interrupts are disabled, the flag stays cleared.

Master/Slave behavior of the interrupts are as follows:

In Master mode, both the TX and RX interrupts are generated off of the free-running master clock. The TX slot interrupt occurs 330 uS after the rising edge of TXEN if **IRQFRMT[3:2]** = 01, or occurs 970 uS after the rising edge of TXEN if **IRQFRMT[3:2]** = 10. Note that TX interrupts are generated regardless of the state of the TX disable/abort bits **TXFRMT[4:3]**.

The RX interrupt is generated 1340 uS after the rising edge of TXEN if **IRQFRMT[1:0]** = 01, or occurs 1980 uS after the rising edge of TXEN if **IRQFRMT[1:0]** = 10. Note that the RX interrupt timing is not synchronized to the incoming RX slot, and the reference to its timing relationship to the incoming RX slot is approximate only. Also, RX interrupts are generated regardless of the sync state of the master, so that RX interrupts will be generated even if there is no incoming RX signal. Lastly, RX interrupts are generated regardless of the state of the RX disable bit **RXFRMT[4]**.

When in Slave mode and Frame Sync has not been obtained there is not a true TDD frame defined. Internally, though, the unit does generate the Frame timing signals as illustrated below in **IRQ Interrupt Timing**. The interrupt enable modes are then based on this internal timing structure. Thus if interrupts are enabled with respect to the TX Payload, either start or end, there will be an interrupt generated at the proper time according to the internal Frame timing signals. When Frame Sync is obtained, the frame and interrupt timing will be changed to correspond to the TDD frame timing then put into effect.

Note: The default value of IRQFRMT[7..0] = 00 hex disables all interrupt signals. This may be a critical consideration during power up.

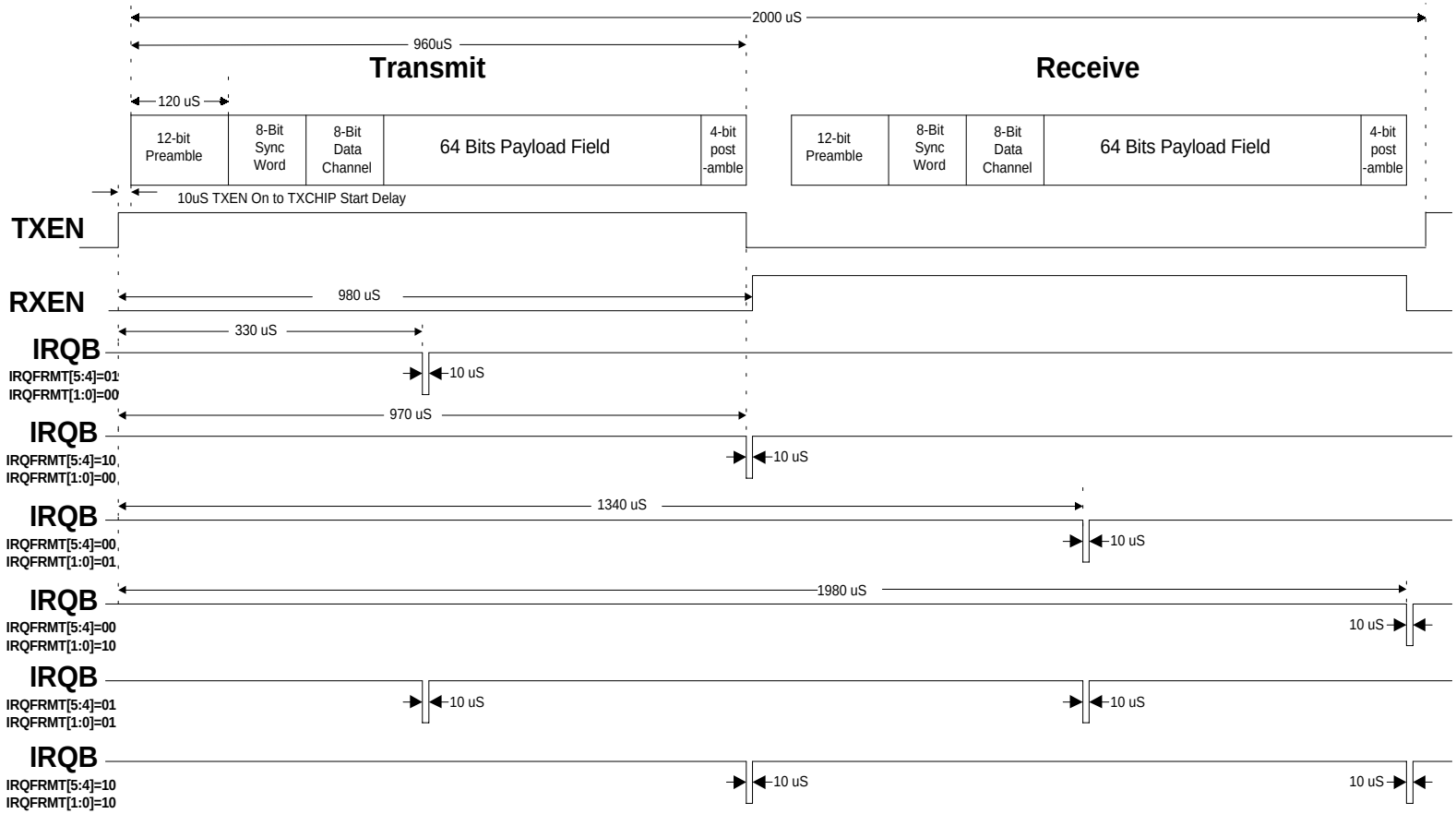


Figure 16- IRQ Interrupt Timing

7.4.7 RESET

ALPINE has an internal reset mechanism that is initiated two different ways:

- A supply voltage generated reset (power up reset). If the supply voltage crosses 2.4 volts and is increasing with time, a reset will be initiated. A reset will not be initiated if the supply voltage crosses 2.4 volts and is decreasing with time.
- An external reset pin (36). A low to high transition will initiate a reset.

Both mechanisms are logically OR'ed internally; each mechanism will generate a high-to-low transition on an internal reset signal. The internal reset will remain low for 100 uS and then return to a high state. This low to high transition will start the reset process. This will reset all internal state machines in Alpine (SPI, TDD Timing Generator) as well as restore all programmable registers to their default values. The reset sequence will be complete 1.3 to 1.4 mS after initiation.

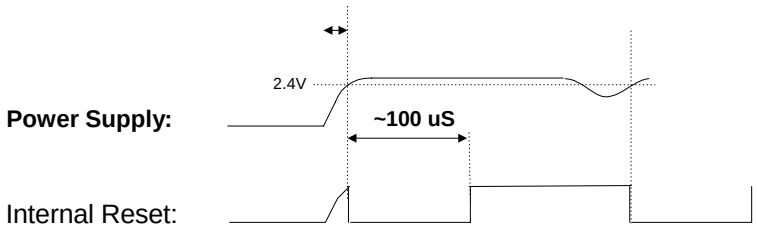


Figure 17: Power Up Reset Timing Vs Power Supply Voltage

A reset will configure Alpine into the following operating mode:

- Master Mode
- Channel Frequency = 2.4405 GHz
- Output Power = 20 dBm
- All IRQ signals disabled
- ADPCM Mode = 0
- MCU clock frequency = 2.0 MHz
- MCU low speed oscillator enabled but not active
- Codec clock disabled

This means that during under normal power up, Alpine will start transmitting power if no register commands are sent.

To prevent transmission after power up, the transmitter should be disabled during the time intervals indicated in figure 18:

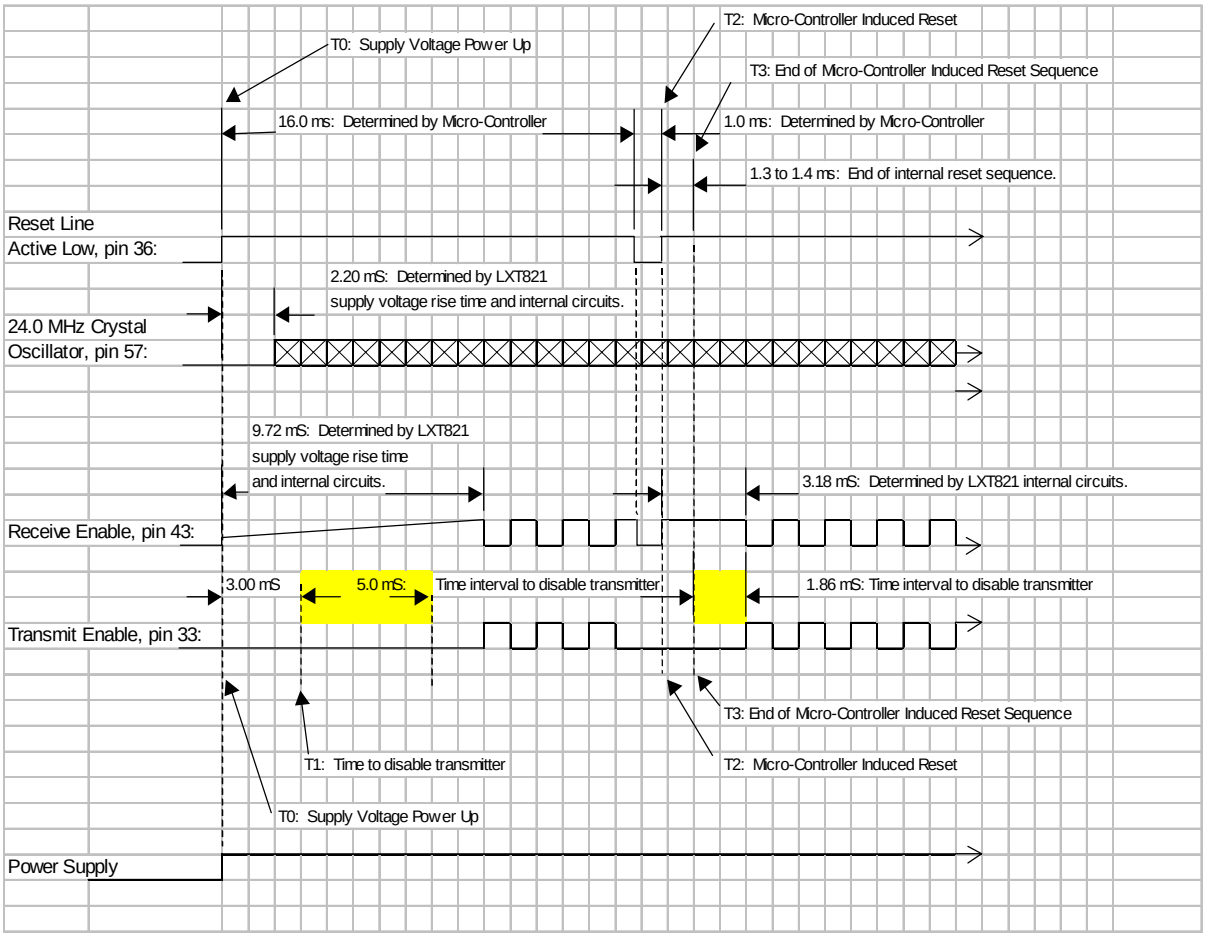


Figure 18: Reset Timing

In order to access registers with an address of 40 hex or greater, the 24.0 MHz oscillator must be active. This oscillator will be fully operational 2.0 to 5.0 mS after initiation of a power up reset.

7.4.8 Power Down (PWRDN)

There are three power-down signals in ALPINE:

- A BMC power-down, which is used to place the BMC portion of ALPINE in a dormant, low-power state
- An RF sub-circuit power-down mode, used to turn off all analog and digital RF circuitry
- An LFOSC enable signal to switch on the low-frequency MCU standby oscillator

7.4.8.1 BMC Power Down

Setting the BMC PWRDN bit, **PWRDN[6]**, places all internal ALPINE BMC circuitry into a low-power state,.
Note: In order to be immune to a slow decay of clock amplitude (resulting from the crystal clock being powered down), a switchover must be made to the LFOSC before **PWRDN[6]** is set.
When in the BMC PWRDN state, ALPINE I/Os assume the following conditions:

- Digital Outputs generally retain last set values.
- The SPI MCU Interface remains operational

7.4.8.2 RF Power Down

Setting the RF PWRDN bits, **PCNTEN[3:0]=1001**(hex address 33), places all internal ALPINE RF circuitry into a low-power state.

Note: when powering down via SPI register commands, the BMC section should be turned off before the radio section. In addition, the radio section should be turned on for at least 1.0 mS before the BMC section is turned on. This guarantees that a glitch free 24.0 MHz clock is available to the BMC section.

7.4.8.3 External Power Down Pin

Tying pin 37 to the power supply will place entire IC into power down mode.

Errata: The external power down pin (37) only turns off the radio section in the LXT821A1. In both the LXT821A1 and LXT821B1, the external power down pin does not reset the receiver state machine. To assure reliable operation, the BMC should be disabled by PWRDN[6] before enabling the external power down. In addition, the external power down should be disabled for at least 1mS before the BMC is enabled by PWRDN[6].

7.4.9 Low-speed MCU Clock

The following two register bits control the low-frequency MCU standby oscillator (LFOSC):

- The LFOSC enable bit **PWRDN[5] = 1** enables the low-speed MCU standby oscillator.
- The MCUCLK select bits **CLKCTRL[2:0]** = 100 selects the LFOSC output to drive the MCUCLK output.

The switchover circuit in the MCU clock selector requires both clock sources to be enabled prior to a switch from one clock source to another, to ensure a glitch-free switchover. Therefore, it is recommended that a switchover be controlled by the MCU in the following manner:

Note: Upon power-up, the LFOSC is enabled but inactive. The MCUCLK upon power up is 2.0 MHz.

To switch over to the high-speed MCUCLK:

- Enable the ALPINE Transceiver, 24 MHz oscillator, and BMC sections by setting **PCNTEN[0] = 0** and then **PWRDN[6] = 0** .
- Switch to the HF MCUCLK by setting **CLKCTRL[2:0]** = 000 (2MHz), 001 (4 MHz), 010 (6 MHz), or 011 (12 MHz).
- Disable the LFOSC by setting **PWRDN[5] = 0**.

To switch over to the low-speed MCU clock:

- Enable the LFOSC by setting **PWRDN[5] = 1**.
- Switch to the LF MCUCLK by setting **CLKCTRL[2:0]** = 100

- Disable the ALPINE BMC and Transceiver sections by setting **PWRDN[6] = 1** and **PCNTEN [3:0] = 1001**.

The low speed oscillator requires the external components COSC and ROSC indicated in Table 8.

Standby Oscillator Frequency	COSC value	ROSC value
100 kHz	68 pF, 1%	470 kOhm, 1%
200 kHz	68 pF, 1%	220 kOhm, 1%

Table 8 - Standby Oscillator Component Values

Note: if these components are not installed, the high speed MCU Clock will not operate.

Typical powerdown current is around 120 uA when the low speed oscillator is enabled; however, the power down current can be reduced to around 55 uA if the low speed oscillator is disabled. The low speed oscillator can be disabled by not installing the external components listed in Table 8 or by setting ALPCTRL[7] = 1, hex address 05. If these two options are implemented, a second MCU clock source is required.

7.5 Spread Spectrum Processor/Burst-mode Controller Description

The Spread Spectrum Processor / Time Division Duplex (TDD) Burst-mode Controller (BMC) does the spreading and de-spreading of the TX and RX data, and controls the TDD operation of the spread spectrum digital cordless telephone (SSDCT) system. This includes the spread spectrum generator, the receive correlator / de-spreader and timing recovery, framer / de-framer, and FIFO for buffering incoming ADPCM voice data.

The BMC block consists of the following sections:

- Transmit Framer and Direct Sequence Spread Spectrum generator.
- Timing generator and TDD controller.
- Receive side correlator /de-spreader with bit clock recovery loop.
- Receive side framer and data de-multiplexer.
- Link Quality Monitor to provide for status monitoring of the RF link, including Link Quality Alarm.
- 32k b/s ADPCM interface with TX/RX FIFO buffers
- TX and RX Fast Data Buffers which allow the system MCU to write/read data to/from the 32k b/s voice payload field .

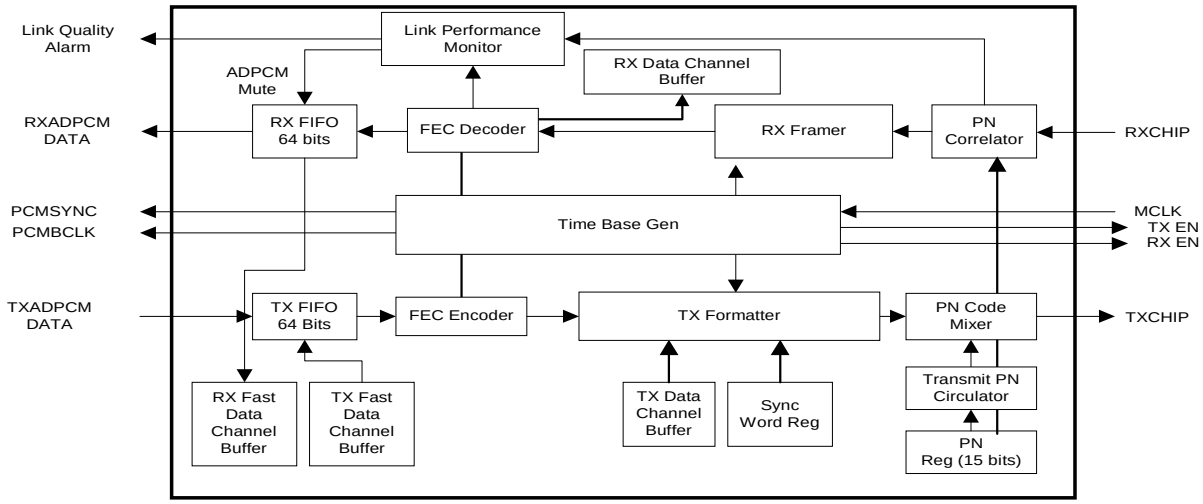


Figure 19 - Functional Block diagram of the Spread Spectrum Burst Mode Controller

7.5.1 BMC TDD Frame Format – normal mode

The BMC uses the TDD frame format shown in Figure 20 when set to normal mode (TXFRMT[6] and RXFRMT[6] set to 0)

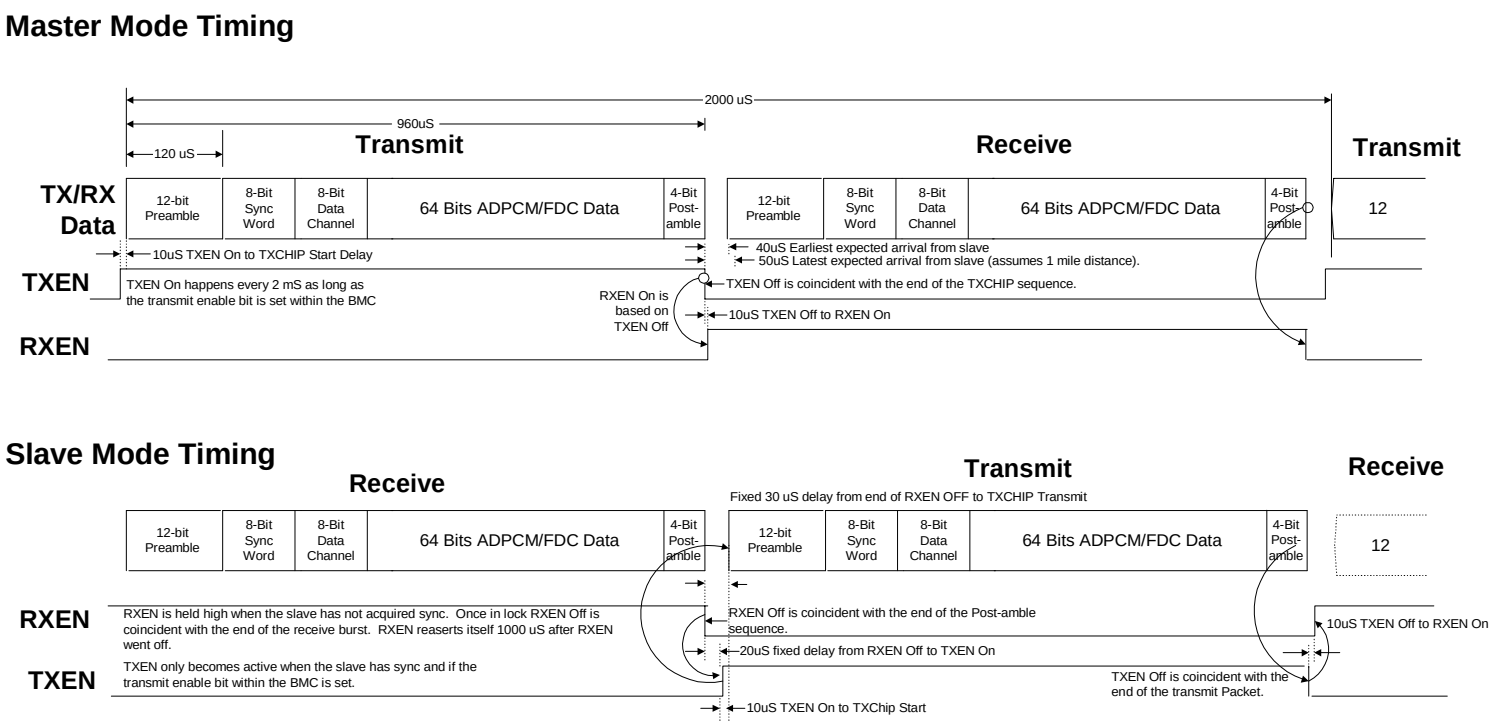


Figure 20 TDD Frame Format of BMC (normal mode)

7.5.2 BMC TDD Frame Format – short packet mode

The BMC uses the TDD frame format shown in Figure 21 when set to short packet mode (TXFRMT[6] and RXFRMT[6] set to 1). This feature allows the chip to save power in standby mode.

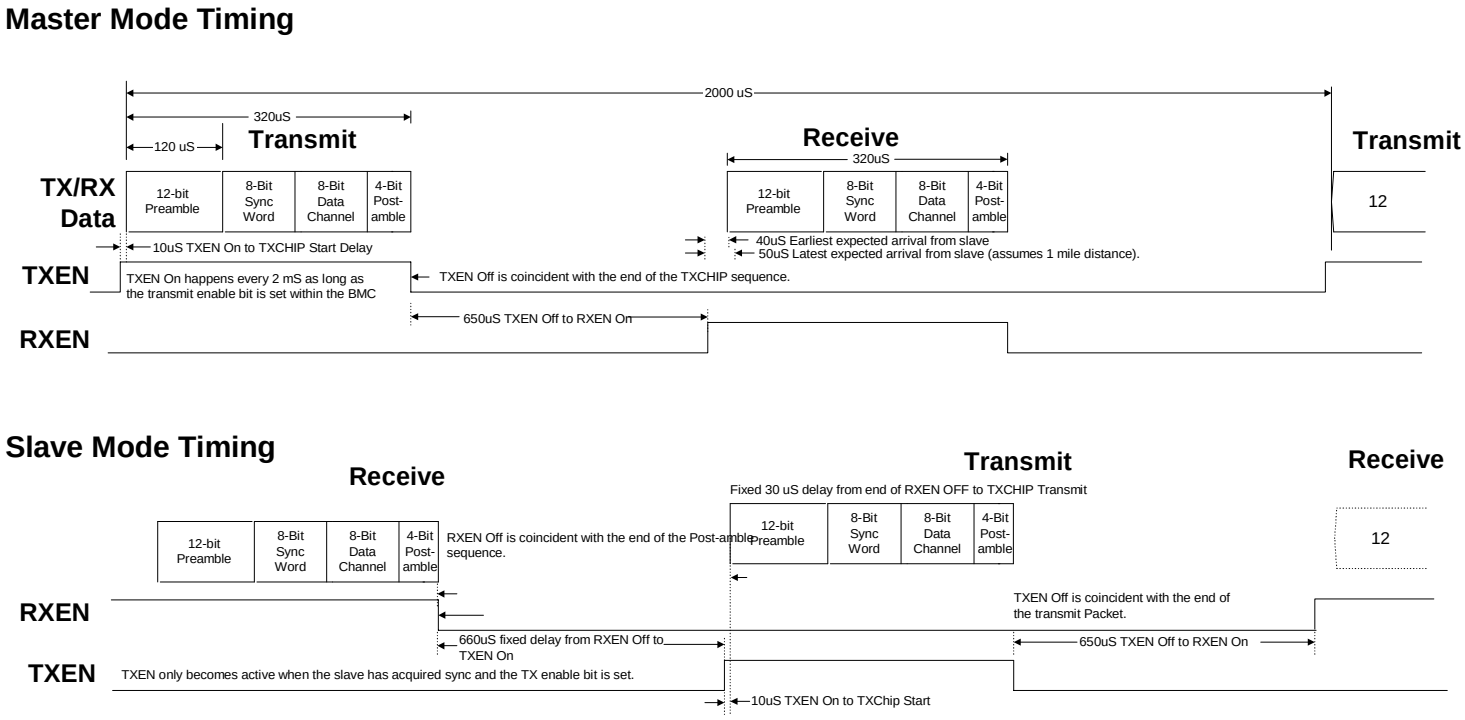


Figure 21 TDD Frame Format of BMC (short packet mode)

7.5.3 Master/Slave TDD Timing

Master / Slave programming of the BMC is set by **TXFRMT[7]**. When **TXFRMT[7]** = 1, the BMC is programmed for Master timing. When **TXFRMT[7]** = 0, the BMC operates in Slave mode.

The Master/Slave protocol of the BMC is as follows: In Master mode, the BMC transmits TX slots every 2 mS, switching to receive to listen for incoming RX slots between outgoing TX slots.. The Master will transmit TX slots regardless of whether incoming RX slots are received, and the timing of the TX slot in independent of the arrival time of RX slots.

In Slave mode, the BMC stays in receive mode until it has acquired sync, at which point it begins transmitting TX slots back to the Master with a single TX frame, and returns to receive mode. A Slave will continue to respond with TX frames until frame sync is lost.

7.5.3.1 Master Timing Mode

In Master timing mode, all TX timing is derived from the free-running 24 MHz crystal clock. The TX frame is set up as follows:

1. Assuming that TX is enabled (**TXFRMT[4,3]** = 00), the transmit enable line TXEN is asserted at the beginning of a TDD frame.
2. The 96-bit TX slot is output at TXCHIP starting 10 uS after TXEN is asserted.
3. TXEN then goes low after 96 bits have been transmitted, coincident with the end of the last bit cell (970uS after the rising edge of TXEN). TXEN stays low for the remaining 1030 uS of the current frame.
4. If the RX enable bit **RXFRMT[4]** = 0, RXEN is asserted 10 uS after TXEN goes low. It remains high while the RX framer is searching for frame sync. If RX frame sync is found, RXEN remains high until the end of the last received bit cell of the 96-bit RX frame. If sync is not acquired, RXEN returns to low 300 uS after the rising edge. **Errata**: In the LXT821A1 and LXT821B1, RXEN does not shorten to 300us if the master unit does not acquire sync.
5. If TX is still enabled, the sequence is restarted by asserting TXEN again 2000uS after the previous rising edge.

Note: The BMC limits the window during which an incoming RX sync word will be recognized. The Master will sync to incoming RX slots that range from arriving 45 uS prior to RXEN being asserted (effectively cutting out the first bits of the preamble), up to RX slots that that arrive 104 uS after RXEN is asserted.

As shown in Figure 21, the BMC can be configured to transmit short 320 uS packets consisting of the preamble, sync word, data channel, and post-amble. This allows single-byte messages to be transmitted and received using a minimum amount of battery power.

Setting TXFRMT[6] to 1 enables the TX short packet mode, and setting RXFRMT[6] to 1 sets the RX short packet mode. This mode has the same basic timing as the normal mode, except that TXEN and RXEN are turned off at the end of the shortened packet.

Errata: In the LXT821A1 and LXT821B1, the short packet mode does not have good sync acquisition performance. Analysis has revealed that this is related to AGC performance. A recommended counter measure is to insert 2 to 5 full duration payload frames when radio is first turned on and then disable the payload.

7.5.3.2 Slave Timing Mode

When in Slave mode (**TXFRMT[7]** = 0), it is the receive timing that sets the TX/RX cadence. The RX correlator recovers the incoming bit clock, and the RX framer detects the beginning of the TX frame as follows:

1. Assuming RX enable bit **RXFRMT[4]** = 0, BMC Slave enables the receiver by asserting RXEN. **Note:** RXEN will remain high until sync is acquired or the RX enable bit has been cleared. Unlike in Master mode, there is no time-out for the Slave RXEN.

2. Once the receiver acquires Frame Sync, RXEN remains enabled until the end of postamble . RXEN then goes low and remains low for 1000 uS.
3. Assuming that TX is enabled (**TXFRMT[4,3]** = 00), the Slave asserts TXEN 20uS after the falling edge of RXEN in the normal packet mode (660 uS in short packet mode).
4. 10uS after TXEN is asserted, the 96-bit TX frame is output at TXCHIP.
5. TXEN is disabled at the end of the post-amble.
6. If the RX enable bit is still set, a rising edge 1000uS after the previous falling edge of RXEN (equal to 10uS after the end of the TX frame in normal mode) restarts the Slave receive process.

7.5.3.3 Slave Receiver Toggle Feature

When Alpine operates in slave mode with no sync acquisition, the receiver enable signal is cleared every 3mS for a duration of 200 uS. This is to assure the internal DC offset circuits are continuously updated during long periods of non-sync operation. The DC offset circuits are re-converged every time the receive enable signal is asserted with a positive edge. This feature is enabled by setting **RXFRMT[7] =** 1 (default setting = 0). The timing of this is synchronous to the IRQ signal. If this feature is disabled, the receiver will have very poor sync acquisition performance.

Errata: This feature can degrade sync acquisition performance if the frame sync threshold is set to greater than 2. This is due to the long time the receiver is disabled. The 200 uS disable period guarantees the one out of three consecutive sync words will be declared bad regardless of signal quality.

7.5.4 TX Framer

The BMC TDD frame is based on symmetrical 96-bit transmit and receive frames, each composed of five fields:

1. A 12-bit Preamble field of alternating 1010…
2. An 8-bit Sync Word field read from **SYNCWD [7:0]** (MSB first)
3. An 8-bit Data Channel field whose contents are set by **TXDREG[7:0]** (MSB first).
4. A 64-bit Payload whose contents are selected by the value of **FDCCTRL[4]**. When **FDCCTRL[4]** = 0, the 64 bits are filled from the TX ADPCM FIFO buffer. When **FDCCTRL[4]** = 1, the 64 bits are from the 8-byte TX Fast Data Channel buffer.
5. A 4-bit all-zeroes Post-Amble which provides a binary convolutional code (BCC) trellis decoder with a known end state.

The TX Framer combines the ADPCM or Fast Data Channel payload bits and Data Channel bits with the Preamble and Sync word to create a TX frame for transmission over the RF link.

7.5.5 The BMC Receiver

The BMC Receiver consists of four blocks:

1. The PN Correlator, which recovers bit timing from the incoming RX chip sequence and, in conjunction with the sync word correlator, detects the Sync Word.
2. A BCC Trellis Decoder and demultiplexer, which performs error detection and correction of the data channel and payload fields, and demultiplexes the Data channel and ADPCM payload fields.
3. A link quality monitor, which measures the Trellis decoder output quality and reports it to the micro-processor interface.
4. A RX ADPCM FIFO, which de-gaps the outgoing ADPCM payload into a smooth 32k b/s data stream.

7.5.5.1 PN Correlator

The PN Correlator looks at the incoming RXCHIP sequence for matches with the stored PN sequence in **PNREG1** and **PNREG2.** When a correlation spike exceeding the threshold set by **CORCTRL[5:3]** is found, the bit timing loop sets a window for subsequent expected correlator spikes. Once a number of these spikes has been detected, the PN Correlator begins looking for the Sync Word set by **SYNCWD[7:0]**. (**Note:** the Sync Word correlator actually looks for a 9-bit Sync Word created by appending the last bit of the preamble (a zero) to the beginning of the 8-bit contents of **SYNCWD**). After successfully detecting the proper number of consecutive Sync Words (as set by **FRMRCTRL[2:0]**), the PN Correlator declares frame sync.

The sync algorithm has four states, which are reported in **RXSTAT[1:0]**:

Search state (00):	No PN code match has been found (no correlator spike above threshold), continue looking for a single PN code match
Pre-sync state (01):	A PN match has been detected, looking for consecutive PN code matches at 10 uS intervals
Frame Search state (10):	Three consecutive PN matches have been detected at 10 uS intervals, begin looking for first sync word and subsequent sync words at 2000 uS intervals (if **FRMRCTRL[2:0]** set from 1-7)
Sync state (11):	The number of consecutive Sync Words detected meets the frame sync threshold set by **FRMRCTRL[2:0]**. The BMC will remain in sync until the number of consecutive bad Sync Words equals or exceeds the loss-of-frame threshold set by **FRMRCTRL[7:3]**.

7.5.5.2 BCC Decoder and RX Framer

After acquiring sync, the BCC decoder performs error detection of the data, providing forward error correction (FEC) and a path metric which is used as a link quality monitor. The first 8 Data Channel data are stored in **RXDREG[7:0]**, while the remaining 64 payload bits are output to the RX ADPCM FIFO (if **FDCCTRL[0]** = 0) or the 8-byte RX Fast Data Channel buffer (if **FDCCTRL[1]** = 1).

The voice data bits are fed to the RX FIFO. The FIFO output is clocked at a constant 32k b/s or 64k b/s rate and supplied to the Receive ADPCM CODEC.

If the RX Fast Data Channel is enabled, the FIFO output is also clocked into the RX Fast Data Channel buffer, which can be accessed by the SPI bus as per section 7.4.5.2

7.5.5.3 Link Quality Monitor

The link performance monitor is based upon the accumulation of Hamming distances from the most likely path through the BCC. This is a measure of the number of chip errors the decoder thinks it has detected / corrected in each frame. For low noise conditions, this measure is a good indicator of the amount of noise on the channel, during high noise conditions it is a less accurate measure, since it will base its measurement on differences between entirely wrong branches through the trellis.

The path metric is stored in **LQMON[7:0]**, and is compared against the threshold set in **LQITHSLD[7:0]**. If the value of LQMON exceeds the value of LQITHSLD, the link quality alarm (LQA) bit **RXSTAT[2]** is set, and the LQA pin goes high.

Note: The LQA bit does not detect every single bit error the exact instant the error occurs. This is due the BMC's FEC capability. Adjusting LQITHSLD to the recommended threshold will assure that a high majority of true bit errors will coincide with an active LQA and that very few valid bits will coincide with an active LQA.

8. ALPINE Register Map

TWI decimal Address	SPI hex Address	Satellite Register Functional Description	Register Type	Default Value (hex)	Recommended Value (hex)	Name
NA	00	PN Code Word Register 1	R/W	B8		PNREG1
NA	01	PN code Word Register 2	R/W	5B		PNREG2
NA	02	Preamble Word 1	R	AA		PREAMBLE[7:0]
NA	03	Preamble word 2	R	AA		PREAMBLE[15:8]
NA	04	Sync Word 1	R/W	B4	F6	SYNCWD
NA	05	ALPINE control	R/W	60		ALPCTRL
NA	06	TX data channel register	R/W	44		TXDREG
NA	07	RX data channel register	R	NA		RXDREG
NA	08	FDC Control/ Status	R/W	00		FDCCTRL
NA	09	TX FDC Buffer	R/W	00		TXFDCBUF
NA	0A	RX FDC Buffer	R	00		RXFDCBUF
NA	0B	TX frame format control	R/W	80		TXFRMT
NA	0C	RX Frame Format control	R/W	00	80	RXFRMT
NA	0D	RX correlator Control Register	R/W	A0		CORCTRL
NA	0E	RX Frame Lock Control Register	R/W	39	38	FRMRCTRL
NA	0F	Clock Generator control Register	R/W	00	18	CLKCTRL
NA	10	Auto-mute control register	R/W	14	9F	AMUTE
NA	11	Link Quality Flag Threshold Register	R/W	33	12	LQITHSLD
NA	12	Link Quality Monitor	R	NA		LQMON
NA	13	Receiver Status	R	NA		RXSTAT
NA	14	Interrupt Timing Control	R/W	00	02	IRQFRMT
NA	15	Reserved	NA	NA		NA
NA	16	Power Down Control	R/W	38		PWRDN
NA	17	Reserved	NA	NA		NA
NA	18	RX Frame Sync	R/W	10		RXFRMSYNC
NA	19	RX Frame Search	R/W	1E		RXFRMSRCH
NA	1A	Path Metric Window Size	R/W	0A	10	MTRCWNDW
NA	1B to 2C	Unused	R/W	NA		NA
NA	2D	Clock Drivers strength	R/W	00	00	DRVSTR
NA	2E	Reserved	R/W	NA		NA
NA	2F	Chip Version	R	B1		ALPREV
NA	30	Receive Gain Indicator	R	NA		RSSIEN
NA	31	Reserved: Fuse blow and Test	R/W	00		ADTESTEN
NA	32	Reserved: RX AGC and offset timing	R/W	53	93	RXTIMEN
NA	33	Manual Power Control	R/W	78	40	PCNTEN
NA	34	Reserved: AGC High & Outside window threshold	R/W	FA		HI_OUTEN
NA	35	Reserved: AGC High & Inside window threshold	R/W	A0		HI_INEN
NA	36	Reserved: AGC Low & Outside window threshold	R/W	3C		LOW_INEN
NA	37	Reserved: AGC Low & Inside window threshold	R/W	14		LOW_OUTEN
NA	38	Reserved: Manual Gain setting	R/W	20		GAINEN
NA	39	Reserved: Manual offset control	R/W	00		OFFSETEN
NA	3A	Unused	R/W	NA		KEN
NA	3B	Reserved: TWI sync mode	R/W	00		TWISYNCEN
TWEN0	40	Synthesizer A count LSB's	R/W	04		SYNTHAEN
TWEN1	41	Synthesizer M count LSB's	R/W	0E		SYNTHBEN
TWEN2	42	Synthesizer M, A count MSB's	R/W	04		SYNTHMAEN
TWEN3	43	Transmit Power Setting	R/W	0F		RMPEN
TWEN4	44	Reserved: Transmit Power Center 2dBm	R/W	04	02	TXP00EN
TWEN5	45	Reserved: Transmit Power Center 8dBm	R/W	04	08	TXP01EN
TWEN6	46	Reserved: Transmit Power Center 14dBm	R/W	07	0C	TXP10EN
TWEN7	47	Reserved: Transmit Power Center 20dBm	R/W	05		TXP11EN
TWEN8	48	Reserved: TX Up-Conversion Mixer Tuning	R/W	0F		IQTUN5EN
TWEN9	49	Reserved: PA Driver Bias Adjust 2 dBm	R/W	03	01	TXPD00EN
TWEN10	4A	PA Driver Bias Adjust 8 dBm	R/W	05	04	TXPD01EN
TWEN11	4B	Reserved: PA Driver Bias Adjust 14 dBm	R/W	08	07	TXPD10EN
TWEN12	4C	Reserved: PA Driver Bias Adjust 20 dBm	R/W	0F	0C	TXPD11EN

TWI decimal Address	SPI hex Address	Satellite Register Functional Description	Register Type	Default Value (hex)	Recommended Value (hex)	Name
TWEN13	4D	Reserved: MSB Vrbias, 1st stage LNA bias	R/W	09		LNA0EN
TWEN14	4E	Reserved: LSB VrBias, 2nd stage LNA bias	R/W	08		LNA1EN
TWEN15	4F	Reserved: LNA Gain Trim	R/W	0C		LNA2EN
TWEN16	50	Reserved: Synthesizer Bias Control 1	R/W	03		SYNTH1EN
TWEN17	51	Reserved: Synthesizer Bias Control 2	R/W	08		SYNTH2EN
TWEN18	52	Reserved: Synthesizer Bias Control 3	R/W	08		SYNTH3EN
TWEN19	53	PLL High Bandwidth Duration	R/W	00		PLLSWEN
TWEN20	54	Reserved: VCO Buffer Tuning Reference divider	R/W	0D		SYNTHIEN
TWEN21	55	Reserved: Manual Unit Capacitor Value, LSB	R/W	08		MNACEN
TWEN22	56	Reserved: Manual Unit Cap Activate and MSB	R/W	02		MNBCEN
TWEN23	57	Manual Control of PLL Loop BW's	R/W	06	04	MNBWEN
TWEN24	58	Reserved: Read Unit Cap controller value LSB	R	AA		RDCAEN
TWEN25	59	Reserved: Read Unit Cap controller value MSB	R	AA		RDCBEN
TWEN26	5A	Reserved: VCO Regulator voltage and Buffer Current tr	R/W	06		BUFFIEN
TWEN27	5B	High BW Charge Pump Current set	R/W	07		CHGPMPHIEN
TWEN28	5C	Low BW Charge Pump Current set	R/W	01		CHGPMPLOEN
TWEN29	5D	Reserved: VCO Regulator voltage and Current trim	R/W	02		VCOIEN
TWEN30	5E	Reserved: Mixer and AA filter Test Select	R/W	00		MXAT0EN
TWEN31	5F	Reserved: Mixer and AA filter Test Select	R/W	00		MXAT1EN
TWEN32	60	Reserved: Divider, upconversion mixer & RX LO buffer	R/W	0B		IQCUR1EN
TWEN33	61	Reserved: Final PA Driver Tuning	R/W	0F		IQTUN1EN
TWEN34	62	Reserved: A/D Op amp and Comp Bias Select	R/W	0F		ADC0EN
TWEN35	63	Reserved: ADC Test mode mux control	R/W	00		ADC1EN
TWEN36	64	Reserved: ADC Test Mode Stage Select	R/W	00		ADC2EN
TWEN37	65	Reserved: First PA Driver Tuning	R/W	0F		PA1TUNBEN
TWEN38	66	Reserved: RXLO Buffer Tuning	R/W	0F		IRXLOTUNBEN
TWEN39	67	Reserved: RX Up-Conversion Mixer Tuning	R/W	0F		UPRXTUNBEN
TWEN40	68	Reserved: Fused, Transmit DAC Set	R/W	0F Fuse	00	TXDACEN
TWEN41	69	Reserved: Fused, Transmit RC Tau Set	R/W	0F Fuse	08	TXRCEN
TWEN42	6A	Reserved: Hard Wired Fuses Select test modes.	R/W	01 Fuse	01	TXMISCEN
TWEN43	6B	Reserved: Fused, Band Gap Voltage Set	R/W	0F Fuse		VBGEN
TWEN44	6C	Reserved: Bit 0 Fused only, Others are hardwired "Fuse	R/W	08 Fuse	00	BSTSTEN
TWEN[45..47]	6D to 6F	Unused	R/W	NA		UNUSED
TWEN48	70	Reserved: RXLO Buffer & Up-conversion Mixer Current	R/W	07		IQCUR2EN
TWEN[49..63]	71 to 7F	Unused	NA	NA		UNUSED

Table 9: Alpine Register Map

9. Alpine Register Description

9.1 PN Code Word 1 – Address 00 hex

Register Name: PNREG1
Address: 00
Default: 1011 1000 Hex: B8
Access: Read/Write

PNREG1 programs the 8 LSB's of the 15-bit PN code word used by the PN mixer

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PN[7]	PN[6]	PN[5]	PN[4]	PN[3]	PN[2]	PN[1]	PN[0]

9.2 PN Code Word 2 – Address 01 hex

Register Name: PNREG2
Address: 01
Default: 0101 1011 Hex: 5B
Access: Read/Write

PNREG2 programs the 7 MSB's of the 15-bit PN code word used by the PN mixer

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	PN[14]	PN[13]	PN[12]	PN[11]	PN[10]	PN[9]	PN[8]

Bit 7 Reserved
Bits 6-0 Most significant byte (7-bits) of PN code word.

Note: PN code defined by PNREG1 and PNREG1 is only used in the preamble and sync word portion of the TDD frame.

9.3 Preamble – Low and High – Address 02 and 03 hex

Register Name:	PREAMBLE[7:0]	PREAMBLE[15:8]
Address:	02	03
Default:	1010 1010 Hex: AA	1010 1010 Hex: AA
Access:	Read only	Read only

The two PREAMBLE registers contain the value of the preamble field transmitted with each frame. The value of these registers is controlled by ALPCTRL[3].

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PREAMBLE[7:0]							

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PREAMBLE[15:8]							

9.4 Sync Word – Address 04 hex, Recommended: F6

Register Name: SYNCWD
Address: 04
Default: 1011 0100 Hex: B4 Recommended: F6
Access: Read/Write

SYNCWD programs the contents of the 8 bit Sync field of the TX Frame

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYNCWD[7:0]							

9.5 Alpine Control – Address 05 hex

Register Name: ALPCTRL
Address: 05
Default: 0110 0000 Hex: 60
Access: Read/Write

Controls low speed oscillator (LFOSC), BMC mode (normal or bypassed), link quality alarm (LQA) / transmit chip output (TX CHIP), external receive chip input, and preamble value (either AAAA or FFFF).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LFOSC TRISTATE	BMCEN	ENLQA	EN_EXT_ RXCHIP	PREAMBLE MODE	Reserved	Reserved	Reserved

Bit 7 LFOSC_TRISTATE
1: Tri-state all external LFOSC-related pins.
0: Do not tri-state all external LFOSC-related pins.

Bit 6 BMCEN
1: Enable Alpine's BMC (Burst Mode Controller).
0: Bypass the BMC. In this mode, Alpine's RF section is connected directly to external pins; the BMC is disabled.

Bit 5 ENLQA: Controls output signal at pin 54.
1: Enables the LQA (Link Quality Alarm) output. Disables Transmit CHIP output
0: Enables Transmit CHIP output. Disables the LQA output.

Bit 4: EN_EXT_RXCHIP
1: Use an external RX chip. In this test mode, the BMC processes chips from an external input -- the normal RF to BMC input path is disabled, and an external RX chip signal is routed into the BMC.
0: Functional mode – use the RX chips from Alpine's RF section.

Bit 3: PREAMBLE_MODE. Sets the value of the PREAMBLE register (addresses 02 and 03).
1: PREAMBLE = FFFF
0: PREAMBLE = AAAA

Bits 0-2: Reserved

9.6 TX Data Channel – Address 06 hex

Register Name: TXDREG
Address: 06
Default: 0100 0100 Hex: 44
Access: Read/Write

The contents of the next 8Bit Data Channel field to be transmitted.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TXDREG[7:0]							

9.7 RX Data Channel – Address 07 hex

Register Name: RXDREG
Address: 07
Access: Read only

The contents of the 8 bit Data Channel field of the last incoming RX Frame.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RXDREG[7:0]							

9.8 Fast Data Channel Control/Status – Address 08 hex

Register Name: FDCCTRL
Address: 08
Default: 0000 0000 Hex:00
Access: Read/Write

FDCCTRL Enables/disables the Fast Data Channel mode. It also contains the buffer full/empty flags used for flow control.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX Fast Data Channel Status Flag (Read Only)	Reserved		TX Fast Data Channel Enable	RX Fast Data Channel Status Flag (Read Only)	Reserved		RX Fast Data Channel Enable

Bit 7 TX Fast Data Channel Buffer status flag. Reads back the status of the TX FD Channel buffer.
- 0: TX Fast Data Channel Buffer empty - content transmitted in an outgoing TX frame
- 1: TX Fast Data Channel Buffer full - content has not yet been transmitted.

Bits 6:5 Reserved

Bit 4 TX Fast Data Channel Enable
- 0: Disables Fast Data Channel - TX FIFO is loaded with TX ADPCM voice data (default)
- 1: Enables FDC - TX FIFO is loaded with contents of TX Fast Data Channel buffer.

Bit 3 RX Fast Data Channel Buffer status flag. Reads back the status of the RX FDC Buffer
- 0: RX Fast Data Channel Buffer empty - content unchanged since last buffer read operation.
- 1: RX Fast Data Channel Buffer full - contents have been updated since last read operation

Bits 2:1 Reserved

Bit 0 RX Fast Data Channel Enable
- 0: Disables Fast Data Channel - RX FIFO contents are output to RX ADPCM voice data (default)
- 1: Enables Fast Data Channel - RX FIFO contents are loaded into the RX Fast Data Channel buffer.

9.9 TX Fast Data Channel Buffer – Address 09 hex

Register Name: TXFDCBUF
Address: 09
Default: 00
Access: Read/Write

TXFDCBUF programs contents of the 64 bit payload field of the next outgoing TX Frame when the FDCCTRL[4] = 1

Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
TXFDBUF[63:0]							

The TXFDCBUF is organized as eight byte-wide registers accessed sequentially under a common address.
SPI access is done by first writing the TXFDCBUF address byte (with read/write bit cleared) and then outputting eight bytes in succession.

Note: Contents of TXFDBUF will not be loaded into the transmit payload until a SPI transaction to the TXFDCBUF register (either Read or Write) is completed.

9.10 RX Fast Data Channel Buffer – Address A hex

Register Name: RXFDCBUF
Address: 0A
Access: Read Only

RXFDCBUF contains the contents of the 64 bit payload field of the last incoming RX Frame when the FDCCTRL[0] = 1

Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
RXFDBUF[63:0]							

The RXFDCBUF is organized as eight byte-wide registers accessed sequentially under a common address.
SPI access is done by first writing the RXFDCBUF address byte (with read bit set), and then reading eight bytes in succession.

9.11 TX Frame Format Control – Address 0B hex

Register Name: TXFRMT
Address: 0B
Default: 1000 0000 Hex: 80
Access: Read/Write

TXFRMT controls the BMC transmit formatter.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Master/ Slave Mode	TX Payload Disable	Reserved	TX Abort	TX Disable	Reserved	Reserved	Reserved

Bit 7 Sets the BMC for Master or Slave timing mode.
0: Slave Mode
1: Master Mode (default)

Bit 6 Enables/Disables Transmitter operation during the ADPCM Payload field of the TX Burst
0: TX Enabled during Payload field (default)
1: TX Disabled during Payload field

Bit 5 Reserved

Bit 4 Transmit Abort
0: Default (transmission not aborted)
1: Immediately stop transmission of the current TX Frame, regardless of Bit 3

Bit 3 Transmit Disable
0: Enable transmission (default)
1: Disable transmission at the end of the current TX Frame

Bit 2:0 Reserved

9.12 RX Frame Format Control – Address 0C hex, Recommended: 80

Register Name: RXFRMT
Address: 0C
Default: 0000 0000 Hex: 00 Recommended: 80 (enables RXEN toggle in slave mode)
Access: Read/Write

RXFRMT controls the RX Framer .

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RXEN Toggle enable	RX ADPCM Payload Disable	Reserved	RX Enable	RX ADPCM Mute	Reserved	Reserved	Reserved

Bit 7 0: Disables RXEN toggle in SLAVE mode
1: Enables RXEN toggle in SLAVE mode
Bit 6 Enables/Disables Receiver operation during the ADPCM Payload field of the TX Burst
0: RX Enabled during Payload field (default)
1: RX Disabled during Payload field
Bit 5 Reserved
Bit 4 Receiver Disable
0: Enables RF Receiver (default)
1: Disables RF Receiver at the end of the current RX Frame
Bit 3 RX ADPCM Mute
0: Enables output of RX ADPCM FIFO (default)
1: Disables output of RX ADPCM FIFO. Send all-zeroes to ADPCM Codec
Bit 2:0 Reserved

9.13 RX Correlator Control – Address 0D hex

Register Name: CORCTRL
Address: 0D
Default: 1010 0000 Hex: A0
Access: Read/Write

CORCTRL sets the operating parameters of the BMC RX correlator/bit timing recovery block.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		Correlator Threshold			Reserved		

Bit 7-6 Reserved

Bit 5-3 Sets the three least significant bits of the correlator threshold (default = 100B). Only effects correlator used in detecting both the preamble and sync word.
Bit 2-0 Reserved

9.14 RX Framer Control – Address 0E hex, Recommended: 38

Register Name: FRMRCTRL
Address: 0E
Default: 0011 1001 Hex: 39 Recommended: 38 (changes sync declaration threshold to 1 valid sync word)
Access: Read/Write

FRMRCTRL sets the operating parameters of the BMC RX framer block.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Loss-of-Frame Threshold					Framer Sync Threshold		

Bit 7-3 Sets loss of sync threshold, defined as the number of consecutive invalid sync words received before "Loss of Frame" is declared. " The sync word threshold is set by the RXFRMSYCN register, hex address 18 when the IC is in sync.
00011: Default = 4 frames
00000: 2 frames (minimum)

Note: FRMCTRL uses both the sync word correlator and the link quality monitor to determine the quality of a received sync word. If a sync word is declared bad and the link quality monitor is greater than 20, the loss of frame counter is incremented by two. If a sync word is declared bad but the link quality monitor is 20 or less, the loss of frame counter is incremented by one. Table 10 indicates loss of sync threshold for a link quality monitor value of greater than 20.

FRMCTRL [7..3]	Number of consecutive invalid frame words required for declaring loss of sync (search) Link Quality Monitor > 20	FRMCTRL [7..3]	Number of consecutive invalid frame words required for declaring loss of sync (search) Link Quality Monitor > 20
00000	1: NOT RECOMMENDED	10000	9
00001	2	10001	10
00010	2	10010	10
00011	3	10011	11
00100	3	10100	11
00101	4	10101	12
00110	4	10110	12
00111	5	10111	13
01000	5	11000	13
01001	6	11001	14
01010	6	11010	14
01011	7	11011	15
01100	7	11100	15
01101	8	11101	16
01110	8	11110	16
01111	9	11111	16

Table 10: Loss of Sync Threshold, Link Quality Monitor > 20

Bit 2-0 Sets sync declaration threshold, defined as the number of valid sync words received before declaring sync. The sync word threshold is controlled by the RXFRMSRCH register, hex address 19 when the IC is not in sync.
001: Default = 2 frames
000: = 1 frame

FRMCTRL [2..0]	Number of Valid Sync Words Required for Declaring Sync
000	1
001	2
010	3
011	4
100	5
101	6
110	7
111	7

Table 11: Sync Declaration Threshold

Errata: Setting FRMCTR[7..0] to 0000 is not recommended. This configuration can induce sync failure in master mode operation. Failure is not evident in slave mode operation.

9.15 Clock Generator Control – Address 0F hex, Recommended: 18

Register Name: CLKCTRL
Address: 0F
Default: 0000 0000 Hex: 00 Recommended: 18
Access: Read/Write

Controls both the codec clock and micro-controller (MCU) clock outputs. In addition, it controls the ADPCM operating mode. Mode 0: a continuous 32 kB/s data stream using a 32 kHz clock. Mode 1: a burst mode 32 kB/s data stream using a 64kHz clock.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Codec clock select		Reserved	ADPCM Mode	Reserved	MCU clock select		

Bits 7-6 Codec clock output select
- 00: Off
- 01: Off
- 10: 24MHz
- 11: 19.2MHz gapped clock

Bit 5: Reserved

Bit 4: ADPCM mode
- 0: Mode 0 using a 32 kHz clock
- 1: Mode 1 using a 64 kHz clock

Bit 3: Reserved

Bits 2-0: MCU clock output select
- 000: 2MHz
- 001: 4MHz
- 010: 6MHz
- 011: 12MHz
- 100: Low-frequency oscillator (LFOSC)
- 101: Reserved
- 110: Reserved
- 111: Off

Note: MCU clock requires LFOSC's external resistor and capacitor to be installed. MCU clock will not operate at any frequency without these components.

9.16 Auto-mute Control – Address 10 hex Recommended: 9F

Register Name: AMUTE
Address: 10
Default: 0001 0100 Hex: 14 Recommended: 9F (changes the mute threshold from 14 to 1F)
Access: Read/Write

AMUTE sets the operating parameters of the Auto-mute function. Auto-Mute is activated using a path metric that includes only the contributions from the most recent **n** information bits decoded. The **n** is programmable via register 0x1A
When Auto-mute is enabled, the RX ADPCM FIFO output data will be muted (set to all-zeroes) when the Auto-mute detect criteria are met.

The Auto-mute Threshold is applied to the 7 MSBs of the window path metric.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AMUTE Enable	Auto-mute Threshold						

Bit 7 Automute Enable
0: Disable Auto-mute function (default)
1: Enable Auto-mute function (default)

Bit 6:0 Sets the threshold for path metric value needed to trigger the auto-mute circuit (default = 0x14). The outgoing ADPCM data is unmuted once a whole frame has gone by that doesn't trigger an auto-mute event.

9.17 Link Quality Alarm Threshold – Address 11 hex, Recommended: 12

Register Name: LQITHSLD
Address: 11
Default: 0011 0011 Hex: 33 Recommended: 12 (changes the LQA threshold from 33 to 12)
Access: Read/Write

LQICTRL sets the operating parameters of the Link Quality Alarm (LQA). A Link Quality Alarm is generated when the path metric exceeds the threshold set by LQITHSLD[6..0].

The Link Quality Alarm is indicated in the RXSTAT register 13[2]. In addition, it will be output to pin 54 if the ALPCTRL register 05[5] = 1.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	LQA Threshold						

Bit 7 Reserved
Bits 6-0 LQA alarm threshold

9.18 Link Quality Monitor Control – Address 12 hex

Register Name: LQMON
Address: 12
Access: Read Only

LQMON measures the growth of the path metric accumulators during the current received frame. This value is cleared at the beginning of every received frame and is latched at the end of the frame, so that it can still be read during the following transmit frame.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Path Metric Accumulator Value						

Bit 7 Reserved. Reads back zero.
Bits 6-0 Contains the path metric accumulator value of the last RX slot.

9.19 Receiver Status – Address 13 hex

Register Name: RXSTAT
Address: 13
Access: Read only

RXSTAT contains the RX Framer status indicators.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				AMUTE Status	Link Quality Alarm	RX Framer Sync State	

Bits 7-4: Reserved.
Bit 3: Auto-mute Status: **Note:** This bit is updated once per frame at the end of the RX slot
0: Auto-mute is not active or not enabled (**AMUTE[7]**=0)
1: Auto-mute is enabled (**AMUTE[7]**=0) and is currently active.
Bit 2 Link Quality Interrupt Alarm: **Note:** This bit is updated once per frame at the end of the RX slot.
0: The Link Quality Alarm Threshold set by **LQITHSLD[7:0]** hasn't been triggered
1: The Link Quality Alarm Threshold set by **LQITHSLD[7:0]** has been triggered
Bit 1:0 RX Framer Sync state indicator: **Note:** These bits are updated in real-time:
00: Search mode - no preamble PN code detected
01: pre-sync mode - a single preamble PN code detected
10: Sync Word search - Three preamble PN codes detected, looking for sync word(s)
11: Sync - the RX Framer is in Frame Sync

9.20 Interrupt Timing Control – Address 14 hex Recommended: 02

Register Name: IRQFRMT
Address: 14
Default: 0000 0000 Hex: 00 Recommended: 02
Access: Read/Write

The Interrupt timing control register allows the timing of the IRQ interrupt signal to be moved relative to the TDD frame. Alpine can be programmed to output zero, one, or two IRQB output pulses per TDD frame. This is true regardless of if the IC has sync or not.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQB TX/RX Flag (Read Only)	Reserved			TX Interrupt timing select		RX Interrupt timing select	

Bit 7 Reads back the source of the current interrupt
- 0: Last interrupt was an RX interrupt
- 1: Last interrupt was a TX interrupt

Bits 6-4 Reserved. Reads return zeroes, subject to change in future silicon revisions.

Bits3:2 TX IRQB Timing select
- 00: Disable TX interrupt (default)
- 01: IRQB falling edge coincident with start of TX Payload field
- 10: IRQB falling edge coincident with end of TX Payload field
- 11: Reserved

Bits1:0 RX IRQB Timing select
- 00: Disable RX interrupt (default)
- 01: IRQB falling edge coincident with start of RX Payload field
- 10: IRQB falling edge coincident with end of RX Payload field
- 11: Reserved

Note: the power up default value of the IRQFRMT register disables all IRQ timing.

9.21 Power Down Control – Address 16 hex

Register Name: PWRDN
Address: 16
Default: 0011 1000 Hex: 38
Access: Read/Write

PWRDN provides independent standby/power down control for Alpine's BMC. It also enables the low-frequency oscillator (LFOSC).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	BMC Power Down	MCU LFOSC Enable	Reserved	Reserved	Reserved	Reserved	Reserved

Bit 7 Reserved
Bit 6 Enables/Disables BMC power down mode
0: BMC enabled (default)
1: BMC placed in Power Down (standby) mode
Bit 5 Enable/Disables low frequency MCU standby oscillator. **Note:** This bit does not switch MCUCLK output to LFOSC. The selection of the MCUCLK is done by **CLKCTRL[2:0]**
0: LFOSC disabled
1: LFOSC enabled (default)
Bits 4-0 Reserved

9.22 RX Frame Sync – Address 18 hex

Register Name: RXFRMSYNC
Address: 18
Default: 0001 0000 Hex: 10
Access: Read/Write

Sets the threshold for detecting a valid sync word when in the frame sync state.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RXFRMSYNC [7:0]							

9.23 RX Frame Search – Address 19 hex

Register Name: RXFRMSRCH
Address: 19
Default: 0001 1110 Hex: 1E
Access: Read/Write

Sets the threshold for detecting a valid sync word when in the frame search state.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RXFRMSRCH [7:0]							

9.24 Path Metric Window Size – Address 1A hex, Recommended: 10

Register Name: MTRCWNDW
Address: 1A
Default: 0000 1010 Hex: 0A Recommended: 10 (increases the path metric window)
Access: Read/Write

Sets the size of the path metric window that is used to control the Auto-mute. The window will include only the contributions from the most recent **n** information bits decoded, where **n** is specified by the contents of this register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MTRCWNDW [7:0]							

Bits4:0 Path Metric Window Size select
Range is from 1 through 20 decimal.

9.25 Drive Strength Control – Address 2D hex,

Register Name: DRVSTR
Address: 2D
Default: 0000 0000 Hex: 00
Access: Read/Write

Sets the drive strength of the micro-controller clock output.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved						DRVSTR[1:0]	

Bits 7-2: Reserved
Bits 1-0: Drive strength for MCUCLK_SYNCLCCLKP (pin 48)
00: 4 mA
01: 16 mA
10: 12 mA
11: 24 mA

9.26 Chip Version – Address 2F hex

Register Name: ALPREV
Address: 2F
Default: 1011 0001 Hex: B1
Access: Read Only

Alpine version number.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ALPREV[7:0]							

9.27 Receive Gain Indicator – Address 30hex - Read Only

Register Name: RSSIEN
Address: 30
Default: NA Hex: NA
Access: Read Only

The Receive Gain Indicator can be used to monitor a channel to determine if a carrier is present or if the far end transmit power should be increased for better near end reception.

The Receive Gain Indication Register Set allows an external micro-controller to monitor the receiver signal strength from a low of -98 dBm to a high of -28 dBm in steps of 6 dB with +/- 4 dB accuracy.

The Receive Gain Indicator is accessed via one read only register.

Table 12: Receive Gain Indicator Bit Definitions

Bit	Mode	Description	Default
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Gain LNA	N/A
Bit 4	R	Gain Control E	N/A
Bit 3	R	Gain Control D	N/A
Bit 2	R	Gain Control C	N/A
Bit 1	R	Gain Control B	N/A
Bit 0	R	Gain Control A (MSB)	N/A

Table 13: Receive Gain Given Register State

Received Signal Level, (dBm) +/- 4 dB	Receiver Gain Bits LNA,E,D,C,B,A	Receiver Gain (Addr 30) Value (hex)
-28	1,0,0,0,0,0	20
-34	1,0,0,0,1,0	22
-40	1,1,0,0,0,0	30
-46	1,1,0,0,1,0	32
-52	1,1,1,0,0,0	38
-58	1,1,1,0,1,0	3A
-64	1,1,1,1,0,0	3C
-48	0,0,0,0,0,0	00
-54	0,0,0,0,1,0	02
-60	0,1,0,0,0,0	10
-66	0,1,0,0,1,0	12
-72	0,1,1,0,0,0	18
-78	0,1,1,0,1,0	1A
-84	0,1,1,1,0,0	1C
-90	0,1,1,1,1,0	1D
-96	0,1,1,1,1,1	1F

Note: RXEN High to Low Transition Latches the Receive Gain result at the end of every receive burst.

9.28 Manual Power Control, TXCHIP, and Clock Drive Strength – Address 33 hex –Def: 78, Recommended: 40

SPI Add. 33 Hex	SPI Address Name PCNTEN	SPI Address Gross Functionality Transmit Data Invert, MCLK strength adjust and Manual control of TXEN, RXEN and Power Down
Bit	Bit Name, Default	Bit Function
7	No Connect	No Function
6	INVTXCHIP	0 = non invert of incoming TXChip, 1 = invert. (default)
5	MCLKSTR1	These signals control the drive strength of the codec clock output at pin 38 MCLKSTR<1:0> 00 Minimum drive strength 01 10 11 Maximum drive strength (default) Adjust while monitoring PIN 38 for adequate waveform.
4	MCLKSTR0	See above Cell
3	PDNMAN	Manual Power Down Command
2	TXMAN	Manual Transmit Enable Control
1	RXMAN	Manual Receive Enable Control
0	PCMAN	0 = Normal Operation, When = 1 Selects manual control of RXEN, TXEN, PWRDWN as opposed to BMC control.

Automatic Power Control: BMC Enabled: X = Don't Care			PCTEN[3..0]Register Bits: X = Don't Care				Alpine Operating Mode
RXEN:	TXEN:	Power Down: Pin 37 or PWRDN [6]	RXMAN	TXMAN	PDNMAN	PCMAN	
X	X	0	0	0	0	1	**Transmitter and Receiver Off:** Crystal Oscillator and Synthesizer active
X	X	0	1	0	0	1	**Receiver On:** Crystal Oscillator and Synthesizer active
X	X	0	0	1	0	1	**Transmitter On:** Crystal Oscillator and Synthesizer active
X	X	0	1	1	0	1	**Burn In Mode:** Transmitter, Receiver, Crystal Oscillator, and Synthesizer active
X	X	0	0	0	1	1	**Power Down.** All radio section bias currents turned off. Internal registers remain unchanged
0	0	0	X	X	X	0	**Transmitter and Receiver Off:** Crystal Oscillator and Synthesizer active
1	0	0	X	X	X	0	**Receiver On:** Crystal Oscillator and Synthesizer active
0	1	0	X	X	X	0	**Transmitter On:** Crystal Oscillator and Synthesizer active
X	X	1	X	X	X	0	**Power Down.** All Bias currents turned off to BMC and radio section. Internal registers remain unchanged

Table 14: Power Control Functionality

9.29 Channel Select Registers – Address 40 to 42 hex – Defaults: 04, 0E and 04 (Channel @ 2.4405 GHz)

Channel selection is done by writing to the Channel Select Register Set via the SPI bus. The Channel select registers program one of the available channels within the 2.4 GHz ISM band. The Channels start at 2.400 GHz and continue to 2.480 GHz in steps of 1.5 MHz.

Register Name	Address	Default
"A" Counter Set	**40 hex**	**04 hex**
"M" Counter Set	**41 hex**	**0E hex**
"A / M" Counter Set	**42 hex**	**04 hex**

Table 15: Channel Select register Set

Note:

All three registers must be written to in the order listed above to implement an RF channel change. The channel selection register set is doubled buffered. When the last address, 42Hex is written, internal circuitry within the synthesizer section parallel loads the twelve bits from the three registers into the synthesizer divider registers.

9.29.1 Synthesizer Programming

9.29.2 Channel Select Register Set Bit definitions.

Each register contains 4 bits as follows. Note that all four registers use only the least-significant four bits. The four MSB's are ignored.

Bit	Mode	Description	Default
Bit 3	R/W	ACNTD	0
Bit 2	R/W	ACNTC	1
Bit 1	R/W	ACNTB	0
Bit 0	R/W	ACNTA	0

Table 16 Address 40h, LSB's of the A count setting, bit definitions.

Bit	Mode	Description	Default
Bit 3	R/W	MCNTD	1
Bit 2	R/W	MCNTC	1
Bit 1	R/W	MCNTB	1
Bit 0	R/W	MCNTA	0

Table 17 Address 41h, LSB's of the M count setting, bit definitions.

Bit	Mode	Description	Default
Bit 3	R/W	ACNTE	0
Bit 2	R/W	MCNTG	1
Bit 1	R/W	MCNTF	0
Bit 0	R/W	MCNTE	0

Table 18 Address 42h, MSB'S of both A and M count settings, bit definitions.

To select a particular channel load the three registers as indicated below.

ACNT E,D,C,B,A	A decimal number 0 to 32	Default 4
MCNT G,F,E,D,C,B,A	A decimal number 77 or 78	Default 78

MCNT<= 32+ACNT

The VCO Center frequency is given by:

f_{VCO} = 3,000,000 { 16(128-MCNT) + (31-ACNT) /2 }

Default Frequency = 2440.5 MHz

Channel Number	Channel Frequency (MHz)	M Count Decimal	A Count Decimal	Channel Number	Channel Frequency (MHz)	M Count Decimal	A Count Decimal
1	2400.00	78	31	28	2440.50	78	4
2	2401.50	78	30	29	2442.00	78	3
3	2403.00	78	29	30	2443.50	78	2
4	2404.50	78	28	31	2445.00	78	1
5	2406.00	78	27	32	2446.50	78	0
6	2407.50	78	26	33	2448.00	77	31
7	2409.00	78	25	34	2449.50	77	30
8	2410.50	78	24	35	2451.00	77	29
9	2412.00	78	23	36	2452.50	77	28
10	2413.50	78	22	37	2454.00	77	27
11	2415.00	78	21	38	2455.50	77	26
12	2416.50	78	20	39	2457.00	77	25
13	2418.00	78	19	40	2458.50	77	24
14	2419.50	78	18	41	2460.00	77	23
15	2421.00	78	17	42	2461.50	77	22
16	2422.50	78	16	43	2463.00	77	21
17	2424.00	78	15	44	2464.50	77	20
18	2425.50	78	14	45	2466.00	77	19
19	2427.00	78	13	46	2467.50	77	18
20	2428.50	78	12	47	2469.00	77	17
21	2430.00	78	11	48	2470.50	77	16
22	2431.50	78	10	49	2472.00	77	15
23	2433.00	78	9	50	2473.50	77	14
24	2434.50	78	8	51	2475.00	77	13
25	2436.00	78	7	52	2476.50	77	12
26	2437.50	78	6	53	2478.00	77	11
27	2439.00	78	5	54	2479.50	77	10

Table 19: Valid A and M Count Values

For Example, to select a channel of 2440.50 MHz,

M Count = 78, M Count bit G is the most significant bit so; M_{CG}=1, M_{CF}=0, M_{CE}=0, M_{CD}=1, M_{CC}=1, M_{CB}=1, M_{CA}=0.

A Count = 4, A Count bit E is the most significant bit so; A_{CE}=0, A_{CD}=0, A_{CC}=1, A_{CB}=0, A_{CA}=0.

Load Address 40_{hex} with 04_{hex}, Load Address 41_{hex} with $0E_{hex}$, Load Address 42_{hex} with 04_{hex}

9.30 Transmit Power Adjust – Address 43hex – Default: 0F (1.5 MHz PA ramp on and 20 dBm)

The Transmit Power Adjust Register allows an external micro-controller to set the transmit output power to one of 4 output power settings.

ALPINE is capable of transmitting at power levels of +2 dBm, +8 dBm, +14 dBm, and +20 dBm.

Note: Bits 2 and 3 of the Transmit Power Adjust Register should be set to 00 when adjusting the TX power level.

Table 20 Transmit Power Set Bit Definitions

SPI Address	**43 hex**
Register Description	**RMPEN, User Transmit Power Set**
Default On Reset (3,2,1,0)	**Binary 1 1 1 1, Hex , 0F**
Satellite Bit D or SPI Bit 3	TXDIV, 0 = 3MHz PA Ramp Clock, 1 = 1.5 MHz PA Ramp Clock
Satellite Bit C or SPI Bit 2	RMPDWN, 0 = No PA ramp down, 1 = PA ramp down
Satellite Bit B or SPI Bit 1	PAGB, Settings: PAGB PAGA 1 1 = 20 dBm output power 1 0 = 14 dBm output power 0 1 = 8 dBm output power 0 0 = 2 dBm output power
Satellite Bit A or SPI Bit 0	PAGA, See above cell

Note:
The transmit power setting is transferred to the transmit power amplifier after the beginning of a receive burst.. This done so that the transmit power can not be altered in the middle of a transmit burst. The receiver must toggle on and off before the new power will be observed at the RF port (i.e. receive mode must be enabled in order to affect changes in output power settings)

9.31 PLLSWEN TWI Register - Address 53 hex – Default: 00

SPI Address	**53 hex**
Register Description	**PLLSWEN, High PLL Charge Pump Current Duration Select.**
Default On Reset (3,2,1,0)	**Binary 0000 , hex 00**
Satellite Bit D or SPI Bit 3	PLLSW<3>
Satellite Bit C or SPI Bit 2	PLLSW<2>
Satellite Bit B or SPI Bit 1	PLLSW<1>
Satellite Bit A or SPI Bit 0	PLLSW<0>

Note: SPI Address 57 hex Bit 2 = 1 disables hi charge pump current
SPI Address 57 hex Bit 2 = 0 enables hi charge pump current for the duration listed below.

Bits 3 2 1 0	Charge Pump Current Set to Hi Band Width For the Following Duration After TXEN or RXEN
0000	10.66 uS
0001	21.33 uS
0010	32.00 uS
0011	42.66 uS
0100	53.33 uS
0101	64.00 uS
0110	74.66 uS
0111	85.33 uS
1000	96.00 uS
1001	106.66 uS
1010	117.33 uS
1011	128.00 uS
1100	138.66 uS
1101	149.33 uS
1110	160.00 uS
1111	170.66 uS

Table 21: PLL Switch Time Duration

9.32 MNBWEN TWI Register - Address 57 hex – Default: 06 Recommended: 04

SPI Address	**57 hex**
Register Description	**MNBWEN, Manual Control of PLL Charge Pump Current**
Default On Reset (3,2,1,0)	**Binary 0110, Hex 06 Rec: 0100, Hex 04**
Satellite Bit D or SPI Bit 3	MANBW, When high selects MNHIBW as control to select high charge pump cur
Satellite Bit C or SPI Bit 2	DISSW, When low enables hi charge pump current during idle state + X us determined by PLLSWEN control bits at SPI Address 53 hex.
Satellite Bit B or SPI Bit 1	WIDE, selects wide varactor voltage window within the unit cap controller.
Satellite Bit A or SPI Bit 0	MNHIBW, 0 = low charge pump current, 1 = high charge pump current

9.33 CHPMPHIEN TWI Register - Address 5B hex – Default: 07

SPI Address	5B hex
Register Description	CHGPMPHIEN, Selects Hi bandwidth PLL Charge Pump current
Default On Reset (3,2,1,0)	Binary 0111, Hex 07
Satellite Bit D or SPI Bit 3	No Connect
Satellite Bit C or SPI Bit 2	hi400u MSB high charge pump current High band Width Charge Pump Current Ihichpmp = 100uAx(4xHI400U + 2xHI200U + HI100U+ HI400UxHI200UxHI100U)
Satellite Bit B or SPI Bit 1	hi200u
Satellite Bit A or SPI Bit 0	hi100u LSB high charge pump current

9.34 CHPMPLOEN TWI Register - Address 5C hex – Default: 01

SPI Address	5C hex
Register Description	CHGPMPLOEN, Selects Low bandwidth PLL Charge Pump current
Default On Reset (3,2,1,0)	Binary 0001, Hex 01
Satellite Bit D or SPI Bit 3	No Connect
Satellite Bit C or SPI Bit 2	lo400u MSB low charge pump current Ilochpmp = 100uAx(4xLO400U + 2xLO200U + LO100U+ LO400UxLO200UxLO100U)
Satellite Bit B or SPI Bit 1	lo200u
Satellite Bit A or SPI Bit 0	lo100u LSB low charge pump current

10. Alpine A1 vs. B1 Differences

The following Alpine features are not implemented in the A1 silicon:

- MCU clock with programmable drive strength
- CODEC clock with programmable drive strength
- Low frequency oscillator
- Fast data channel
- New Auto-mute control
- Various additions to Pin Signal Muxing
- Manufacturing scan test
- Manufacturing burn-in test
- Manufacturing IDDQ test

Accordingly, control registers which affect the features listed above are not implemented in the A1 silicon. They are:

- ALPCTRL Register: hex address 05[7]
- FDCCTRL Register: hex address 08[7..0]
- TXFDCBUF Register: hex address 09[63..0]
- RXFDCBUF Register: hex address 0A[63..0]
- CLKCTRL Register: hex address 0F[7..6] and 0F[2..0]
- PWRDN Register: hex address 16[5]
- MTRCWNDW Register: hex address 1A[7..0]
- DRVSTR Register: hex address 2D[7..0]

11. RF System Specifications:

All specifications are at 3.0 to 3.6 Vdc supply voltage and 25 C unless otherwise noted. Specifications are referenced to single ended port of external balun.

#	Parameter	Notes	Sym.	Min.	Typ.	Max.	Units
1.	RF Frequency Range	2400 MHz ISM Band	Fc	2403.0		2479.5	MHz
2.	Crystal Frequency	Includes temp, aging and tolerance.	Fr	-30	24.0 MHz	+30	ppm
3.	Chip rate	1.5 M Chips/Second	Rc		1.5		Mc/s
4.	Sensitivity	Measured at a Bit Error Rate of 1.0 e-3	Sens	-100	-102		dBm
5.	Input Third order Intercept	CW interferers at 10 and 20 MHz from Channel Frequency	IIP3	-25	-23		dBm
6.	Receiver Gain Range	6 dB Steps with hysteresis	Rgain	36		104	dB
7.	Channel Spacing	52 Channels	ChSp		1.5		MHz
8.	Adjacent channel selectivity at various offset frequencies from desired channel.	Desired signal at -97 dBm Achieves Bit Error rate < 1.0 e-3. Adjacent Channel Interferer = CW mode 1.5 MHz ⇨ 3.0 MHz equal to or greater than 4.5 MHz	Sel	 19 42 44	 23 49 53		 dB dB dB
9.	Co-Channel interference performance	Desired signal at -97 dBm Achieves Bit Error rate < 1.0 e-3. Interferer = FM signal , not C/W	CoInt	-4	0		dB
10.	Frequency Deviation	Peak Deviation	Fdev	400	525	650	kHz
11.	Occupied RF bandwidth	Measured at 3 dB down points	BW		1.7	2.0	MHz
12.	RF Output Power, Low power Mid low power Mid high power High power	In 4 steps, 1.5 mW 6.3 mW 25 mW 100 mW	Pout	-2 4 10 17	0 6 13 19		dBm dBm dBm dBm
13.	Adjacent channel transmit power 1.5 MHz from center 3 MHz from center 4.5 MHz from center	Measured with 100 kHz Resolution Bandwidth (RBW)	Padj		 -21 -40 -48	 -18 -36 -40	 dBc dBc dBc
14.	Emissions due to transmit transients 1.5 MHz from center 3 MHz from center 4.5 MHz from center	Measured with 100 kHz RBW	TransTX		 -16 -24 -34		 dBc dBc dBc
15.	TX Harmonic Output levels	All Measured in a 1 MHz RBW 2nd 3rd 4th 5th 6th 7th 8th +	HarmTX		 -33 -38 -50 -50 -50 -50 -50		 dBc dBc dBc dBc dBc dBc dBc
16.	Out-of band spurious emissions	All Measured in 1 MHz resolution bandwidth and at the output of the balun 0 - 216 MHz 216 - 960 MHz above 960 MHz	SpurTX		 -55 -55 -50		 dBc dBc dBc
17.	Supply Voltage	+/- 10 % Tolerance, Functional @ 2.7 V	Vdd	3.0	3.3	3.6	Vdc
18.	Current Consumption Time Division Duplex Mode (TDD): Transmitter on 50%, Receiver on 50%.	Receive Mode TDD Mode: Transmit Power = 2 mW TDD Mode: Transmit Power = 8 mW TDD Mode: Transmit Power = 25 mW TDD Mode: Transmit Power = 100 mW	IRX ITDD2 ITDD8 ITDD14 ITDD20		135 105 115 135 185	150 125 135 155 215	mA mA mA mA mA

		Power Down: low speed oscillator disabled low speed oscillator enabled	IPDL IPDH		55 125		uA uA
19.	Turn on-time, Power down to Rx / TX	Time To PLL Locked	Ton		1.5	5	ms
20.	Temperature Range	Commercial Range	Temp	0		70	C

Table 22 ALPINE RF System Specification Sheet

12. Electrical Specifications

12.1 Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC Supply Voltage	V_{DD}	-0.3	4.5	Volts
Ambient Operating Temperature	T_A	-10	75	^{O}C
Storage temperature	T_{STG}	-65	150	^{O}C

CAUTION, Operation at or beyond these maximum ratings may result in permanent damage to the device. Normal operation is not guaranteed at these extreme conditions.

12.2 Recommended Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
DC Supply Voltage	V_{DD}	3.0	3.3	3.6	Volts
DC Operational Supply Voltage ALPINE is Functional with Reduced	$V_{DD2.7}$		2.7		Volts
Ambient Operating Temperature	T_A	0	25	70	^{O}C

12.3 Digital I/O Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Low Voltage	V_{IL}	---	---	0.8	Volts	
Input High Voltage	V_{IH}	2.0	---	---	Volts	
Output Low Voltage	V_{OL}	---	---	0.4	Volts	I_{OL} = 1.6 mA
Output High Voltage	V_{OH}	2.4	---	---	Volts	I_{OH} = -1.0 mA
Output Rise Time	T_{OR}	---	---	6	nS	C_{LOAD} = 10pF
Output Fall Time	T_{OF}	---	---	5	nS	C_{LOAD} = 10pF
Digital Input Signals Include; SPIDIN, SPICLK, SPIEN, RESET, PWRDWN, and TXADPCM Digital Output Signals Include: SPIDOUT, TXEN_OUT, CODECCLK, RXEN_OUT, PCMBCLK, PCMSYNC, RXADPCM, MCUCLK, IRQ, and LQA						

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Alpine LXT821B1:

Questions and Answers

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1. Question: What are some general operating characteristics of both the Fast Data Channel (FDC) and Auto Mute functions?

Answer:

It is recommended to program the transmit FDC buffer to a desired value before enabling the same buffer. Otherwise, there is no way to control the contents of the first transmit frames containing FDC information. This information will be a random fixed value until the transmit FDC buffer is programmed.

Once the contents of the transmit FDC buffer is programmed to a given 64 bit data field, that same 64 bit field will be repeated indefinitely on succeesive transmit frames until the transmit FDC buffer is re-programmed to a different value.

The contents of the receive FDC buffer is also sent out on the RXADPCM pin in real time. In other words, the receive data will come out of the RXADPCM pin regardless of if the receive FDC buffer is enabled or not.

One subtlety to remember is that the RXADPCM data will become random if the radio loses sync. This is true regardless of if the receive FDC buffer is enabled.

The RXADPCM pin can be forced to output all zero's by programming RXFRMT[3] = 1. This is true regardless of if the receive fast data channel buffer is enabled or not. The RXADPCM pin will be forced to all zero's even if the radio loses sync. Programming RXFRMT[3] = 1 will **not** force the receive FDC buffer to 00 00 00 00 00 00 00 00.

Despite having the RXADPCM mute feature, it is highly recommended that any codec used with Alpine have it's own mute function. The main problem is that the PCMBCLK and PCMSYNC signals will always have timing jitter during the instant of sync acquisition. This timing jitter at sync acquisition can generate audible noise in some ADPCM codecs. The jitter is caused by a radio's RXADPCM data becoming synchronous with the other radio's TXADPCM data time base.

2. Question: What is the typical channel change time for Alpine?

Answer:

Refer to the table below. Channel change time is indicated in term of PLL settling time.

PLL settling time study vs. loop components and CP current				
Number of channels hopped	51	27	8	1
from ch # to ch # in Hex	1 to 34	19 to 34	2C to 34	33 to 34
from ch # to ch # in Decimal	1 to 52	25 to 52	44 to 52	51 to 52
	Time (ms)	Time (ms)	Time (ms)	Time (ms)
PLL Filter values = 10K-.022uF				
Charge Pump current = 100uA	1.5	1.25	0.75	0.5
PLL Filter values = 2K-.22uF//.01uF				
Charge Pump current = 100uA	6	5	2.5	1.25
Charge Pump current = 200uA	3.75	2.75	2	0.75
Charge Pump current = 800uA	2	1.5	1	0.5
CP = 800uA for 250us then cont at 100uA	3	2.5	2.5	1.25
CP = 800uA for 1000us then cont at 100uA	3	2.5	2.5	1.25
CP = 800uA for 250us then cont at 200uA	2.75	2.25	2	1
CP = 800uA for 1000us then cont at 200uA	2.5	2	1.75	1.25

Table 1: Alpine Channel Change Time

CP = Charge Pump Current.

3. Question: What PN codes can be used in Alpine?

Answer:

Refer to the table below:

PNREG2 Register Address 01	PNREG1 Register Address 00
5B (default)	**B8 (default)**
19	51
46	22
4A	3A
52	91
53	71
6D	16

Table 2: Alpine PN Codes

The PN code programmed by registers PNREG1 and PNREG2 is only used in the preamble and sync word frame fields. This programmable PN code is not used in the data channel, payload, or post-amble fields.

If the default RXFRMSYNC and RXFRMSRCH sync word correlator thresholds are used, all 7 of PN codes listed above provide adequate BER performance (sensitivity) and sync acquisition time. Increasing the sync word correlator thresholds to increase orthogonality between different PN codes is not recommended.

For example, increasing RXFRMSYNC to 15 will degrade sensitivity about 1 dB.

Increasing RXFRMSRCH to 22 will increase sync acquisition time, particularly at RF input power levels close to sensitivity. This change will not increase sync acquisition time at RF input power of -100.5 dBm or higher.

For best performance, RXFRMSYNC should be 10 hex and RXFRMSRCH should be 1E hex.

If the default PN code of 5BB8 is used, the 6 remaining PN codes cannot be used. The default PN code does not have enough orthogonality with the remaining PN codes. The 6 remaining PN codes can be used in the same system and have good orthogonality with respect to each other.

Any PN code not specifically listed in the table above should not be used. The only qualified PN codes suitable for Alpine are listed above. Other suitable PN codes do exist; however, they have not yet been fully qualified.

To review additional test results, review the excel file titled "alpine_lxt821b1_PNcode_performance.xls".

4. Question: How does the power down feature work in Alpine?

Answer:

?? Power Down Pin (pin 37, active high):

Activating this pin turns off both the radio section and BMC section of Alpine simultaneously. It will turn off the main clock to the BMC asynchronously. No state machines in the BMC section are reset.

?? Register 16[6] (active high):

Setting this bit turns off the BMC asynchronously; this means the BMC is not turned off synchronous to the TDD frame cadence. The BMC sync state machine is reset to SEARCH mode, regardless of it's state before power down. The FRMCTRL counters are reset. The receive frame pointers are reset. These pointers are used to determine when the receiver frame is supposed be received. The transmit frame pointers are not reset. These pointers are used to determine when the transmit frame is supposed to be transmitted. The radio section will remain powered up and the 24.0 MHz crystal oscillator will remain on.

?? Register 33[3] and 33[0] (active high):

Setting bits 3 and 0 will place radio section in power down mode and will disable the main clock to the BMC. The BMC section will remain active but will have no master clock from the radio section.

The transmit, receive, and crystal oscillator section will be disabled.

Registers 00 through 33 will still be accessible via the SPI bus when register bits 33[3] and 33[0] are set.

When placing Alpine into power down mode, it is recommended that register bit 16[6] be set before activating pin 37 or setting register bits 33[3] and 33[0]. This will assure that the BMC section has a stable main clock before it is turned off.

In addition, when taking Alpine out of power down mode, it is recommended 33[3] and 33[0] are cleared or pin 37 deactivated before enabling the BMC. This will assure that the BMC has a stable clock before it is activated.

Both the external power down pin or register bits 33[3] and 33[0] can be used to turn off the radio section; however, to reliably place Alpine into and out of power down, the register bit 16[6] must also be used in the manner described above.

If the BMC does not have a stable clock during power down or power up, it's internal state can become unpredictable and the IC can be rendered non-operational. The only way to recover the IC in this state is to initiate a reset.

5. Question: What is the RF port return loss in Alpine?

Answer:

When Alpine is in receive mode, the return loss varies from 12 to 14 dB, depending on channel frequency. The return loss increases to around 15 to 17 dB when Alpine is in maximum power (“20 dBm) transmit mode. For more details, refer to the excel file titled “alpine_lxt821b1_i_o_impedance.xls”.

6. Question: Is it possible for an Alpine radio in slave mode to acquire sync with another slave?

Answer:

Yes; however, this can only happen if a master / slave pair has already acquired sync with each other. In other words, the first slave must be synced in order for it to be transmitting.

Assuming that both slave units have the same sync word, PN code, and channel frequency, there is no systematic method of preventing the a slave from acquiring sync with another slave. The 2nd slave unit can acquire sync with the either a slave or master unit. Which unit it acquires sync with is dependent on the received signal strength of both. For example, if the master signal strength is greater the slave signal strength, the 2nd slave unit will acquire sync with that master and so on.

One suggested counter measure is to always identify a transmitter as either a slave or master. If a slave detects that it has acquired sync with another slave, it should never enable it's transmitter. In addition, any slave that is out of sync should have it's transmitter disabled by programming TXFRMT[4] = 1. Once a slave has acquired sync with a master then TXFRMT[4] can be re-programmed to 0. Setting TXFRMT[4] = 1 will not prevent a slave from acquiring sync. This countermeasure will prevent any slave from interfering with an existing master / slave pair already in sync.

This situation means that if two slave units are too close together and one slave acquires sync with a master, the remaining slave cannot acquire a valid sync on the same channel frequency currently occupied by the original master / slave pair.

7. Question: Is it possible to reduce Alpine's transmit power below the "2dBm" setting?

Answer:

Yes, it is possible to reduce the transmit power to around –22 dBm by using the following register settings:

1. Register 43 = 0C hex: sets output power to "2dBm" setting
2. Register 44 = 00 hex: reduces power amplifier bias current to minimum setting
3. Register 49 = 00 hex: reduces power amplifier driver bias current to minimum setting

This mode maintains full radio functionality; however, it has not been fully tested or qualified for all operating conditions.

8. Question: How much is sensitivity effected by 24.0 MHz Crystal oscillator offset?

Answer:

Refer to the figure below:

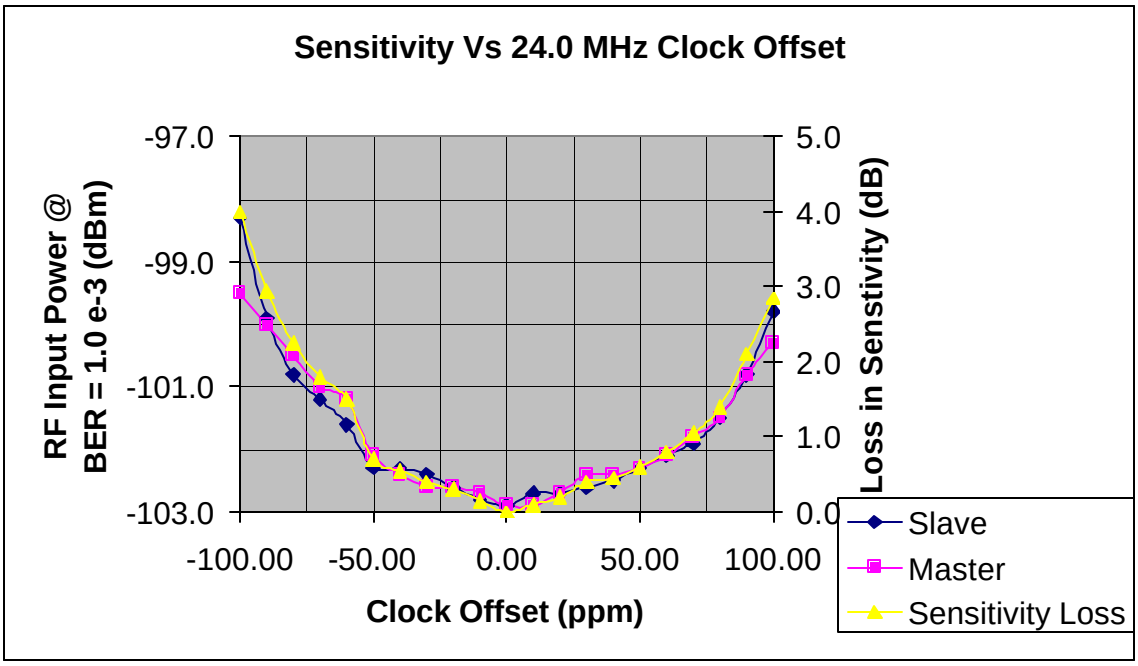


Figure 1: Alpine Sensitivity vs. 24.0 MHz Clock Offset

Crystal frequency offset translates directly to channel frequency offset. In other words, if two radios using the same channel frequency have 24.0 MHz crystals that are 20 ppm different in oscillation frequency, their respective channel frequencies will also be 20 ppm apart. For example, 20 ppm is 48 kHz at 2.4 GHz.

In Alpine, a +/- 30 ppm frequency offset will degrade sensitivity by less than 0.7 dB.

9. Question: How much is sensitivity effected by changes in frequency deviation?

Answer:

Refer to the figure below. Optimal sensitivity occurs at a frequency deviation of +/- 525 kHz.

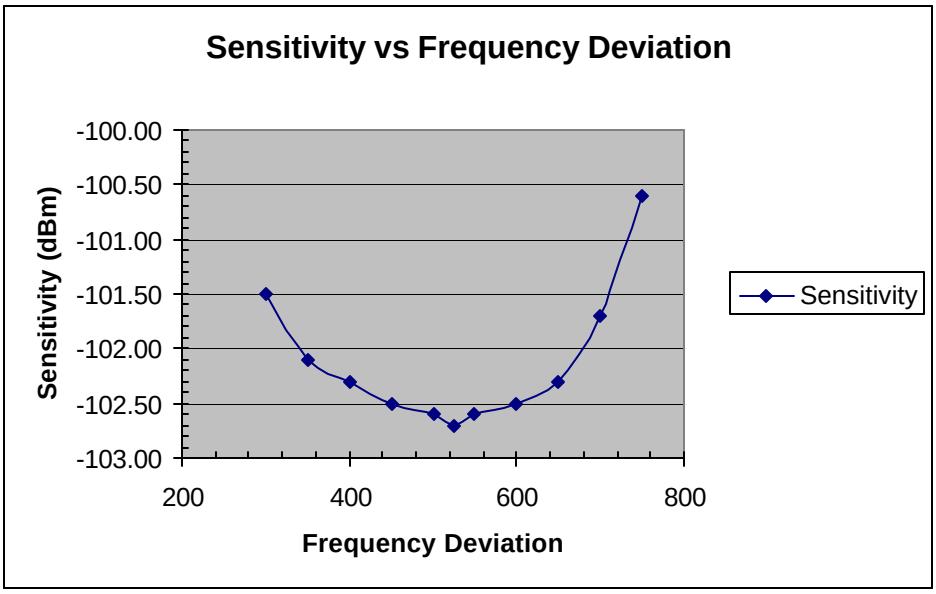


Figure 2: Alpine Sensitivity vs. Frequency Deviation

Reducing frequency deviation below 525 kHz reduces the signal to noise ratio in the demodulator section, increasing BER. Increasing frequency deviation above 525 kHz increases the baseband frequency span. This in turn increases distortion due to the maximum baseband frequency getting closer to the base band filter cutoff frequency. In other words, the base band filters start to distort the received signal.

Registers bits 68[3..0] and 6A[0] control frequency deviation. For more details, refer to the excel file titled: “alpine_lxt821b1_frequency_deviation.xls”.

10. Question: How long does the 24.0 MHz crystal oscillator take to turn on when Alpine is taken out of power down mode?

Answer:

Assuming that the supply voltage is stable at 3.3 Vdc and the temperature is 25 C, the 24.0 MHz crystal oscillator has the following turn on characteristic:

- Time to reach 1.0 Volt peak to peak oscillation amplitude = 250 uS
- Time to reach 3.0 Volt peak to peak oscillation amplitude = 300 uS
- Time for internal digital clock to stabilize = 200 uS

This timing will vary for different crystal manufacturers, temperature, and supply voltage and should be characterized on a manufacturer by manufacturer basis.

For more details, refer to the excel file titled:
“alpine_lxt821b1_24MHz_crystal_oscillator_test1.xls”.

11. Question: What is Alpine's processing gain?

Answer:

Worse case processing gain is around 11 dB for a jammer frequency +/- 650 kHz from the channel center frequency. Refer to the figure below for typical processing gain performance:

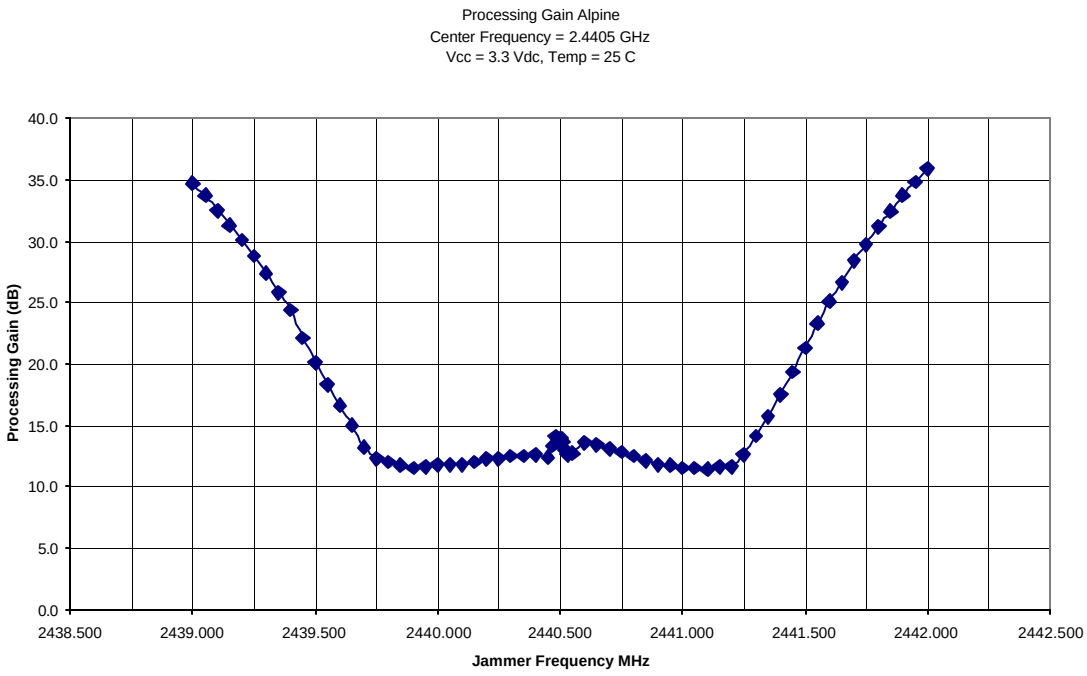


Figure 3: Alpine Processing Gain

The increased processing gain seen at the exact channel frequency is due to the internal DC offset cancellation circuits inside Alpine negating the effect of the co-channel jammer. The overall shape of the curve is a folded mirror image of the baseband frequency response.

12. Question: How long does Alpine take to acquire sync in both the master to slave and slave to master direction?

Answer:

Alpine typically requires around 10 mS to acquire sync in both link directions once taken out of power down. In other words, both link directions will be synced up after 10 mS. Due to the master / slave protocol used by Alpine, the master to slave link must acquire sync before the slave to master link can. This performance assumes the following conditions:

- Slave unit is on all the time. The Master unit is taken out of power down state to initiate link acquisition.
- Sync acquisition threshold = one valid sync word. Loss of sync threshold = 2 consecutive invalid sync words. Increasing these thresholds will degrade sync acquisition time. The FRMCTRL register should be set to 08 or 10 hex.
- RF input power is –97 dBm or greater at both the master and slave unit.

For more details, refer to the excel file titled: “alpine_lxt821b1_sync_acquisition.xls”.

13. Question: What is Alpine's Carrier to Jammer performance?

Answer:

Alpine's carrier to jammer performance is shown in the figure below. It has degraded jammer performance at 1.2 GHz (Fch / 2), 800 MHz (Fch/3), 600 MHz, and 400 MHz.

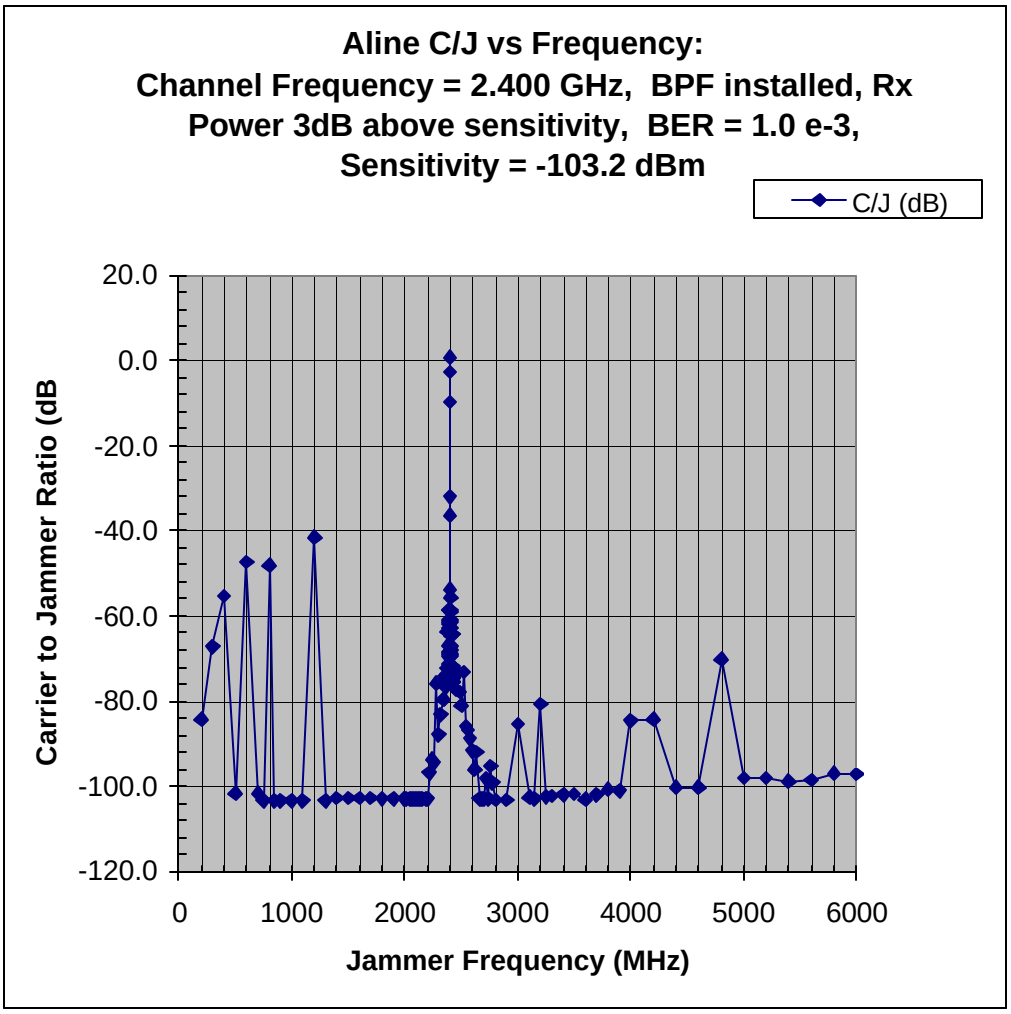


Figure 4: Alpine Carrier to Jammer Ratio

14. Question: What is Alpine's Harmonic Content?

Answer:

Alpine's typical harmonic content is listed in the table below:

2nd Harmonic	3rd Harmonic	4th Harmonic	5th Harmonic
35.0 dB	37.8 dB	52.6 dB	73.9 dB

Table 3: Alpine Harmonic Content

The harmonics listed assumes that a Murata DFC22R44P084LHA band pass filter is installed between Alpine and the antenna port.

These values are worse case assuming a transmit power setting of "20 dBm", a channel frequency range of 2.4030 GHz to 2.4795 GHz, a supply voltage variation of 3.0 to 3.6 Vdc, and a temperature of 25 Celsius.

15. Question: What is best way to use Alpine's Automute feature?

Answer:

Alpine has two degrees of freedom for controlling the automute feature. The AMUTE register selects the pathmetric value required to activate automute. The MTRCWNDW register selects the number of bits used to accumulate a pathmetric value.

The recommended register settings are:

AMUTE[7..0] = 9F: This correlates to a pathmetric threshold of 1F or 31 decimal. Note, AMUTE[7] is an enable bit and does not adjust the threshold value.

MTRCWND[7..0] = 10: This correlates to a 16 bit window sample size.

Basically AMUTE[6..0] sets the activation point and MTRCWND sets the activation speed. These two registers are optimized together to provide:

- Minimal unmuted noise
- Maximum effective range before mute activation
- Maximum activation speed

Refer to the figure below:

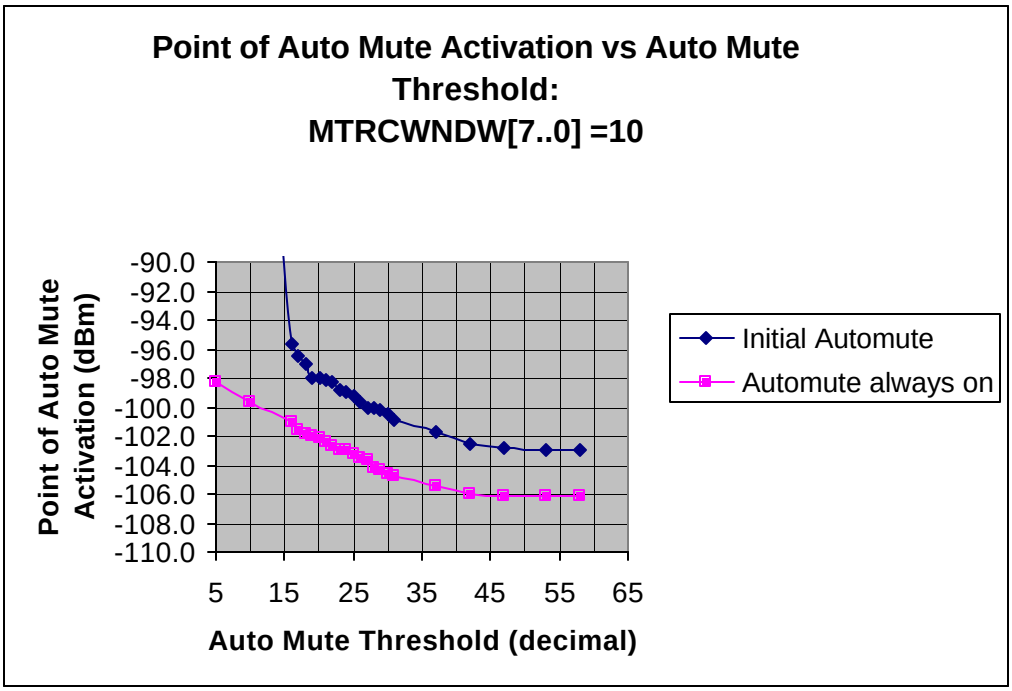


Figure 5: Automute Activation vs Threshold

The vertical axis indicates what RF input power the automute is activated. The upper curve indicates the RF input level were automute just starts to turn on. The lower curve indicates the RF input level were the automute is on all the time. For example, if MTRCWNDW[7..0] = 10 and AMUTE[6..0] = 1F (31 decimal), the automute will start to activate for RF input power levels at –100.8 dBm and the automute will stay on all the time for RF input power level equal to or less than –104.8 dBm.

The performance shown in Figure 5 was taken from an Alpine LXT821B1 using an external bandpass filter. Sensitivity was measured as –102.8 dBm (BER = .001). What is significant is, for this particular radio, humans will start to hear a loss of sound quality when the RF input power level is less than or equal to –101.8 dBm (BER = .0001). This means that the recommended automute settings are very close to optimum; the automute starts to activate at a power level close to but slightly higher than –101.8 dBm.

Activation speed is important for combating specific types of interfering signals. Refer to the figure below:

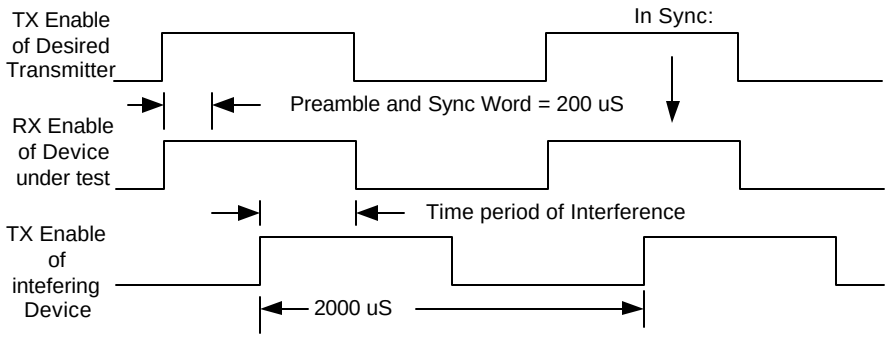


Figure 6: Timing of RX vs Interference

In Figure 6, the timing of an Alpine pair in correct sync is shown with respect to an interfering Alpine that is not in sync. If the time period of interference occurs after the sync word there is a situation were the receiver's payload is corrupted. Despite this, the pair maintains perfect sync. In addition, the synced pair has no indication that anything is wrong except for perhaps an elevated pathmetric value. If the automute activation speed is not fast enough, the end user can perceive unmuted audio errors. The activation speed has been optimized to minimize the time period of interference were unmuted audio errors occur. If the recommended automute settings are used, this interval is around 75 uS.

For more details, refer to the excel worksheets titled "alpine_lxt821b1_automute_lqmon.xls" and "alpine_lxt821b1_automute_interferer.xls"

16. Question: How is the pathmetric (LQMON) value effected by RF input power?

Answer:

Refer to the figure below:

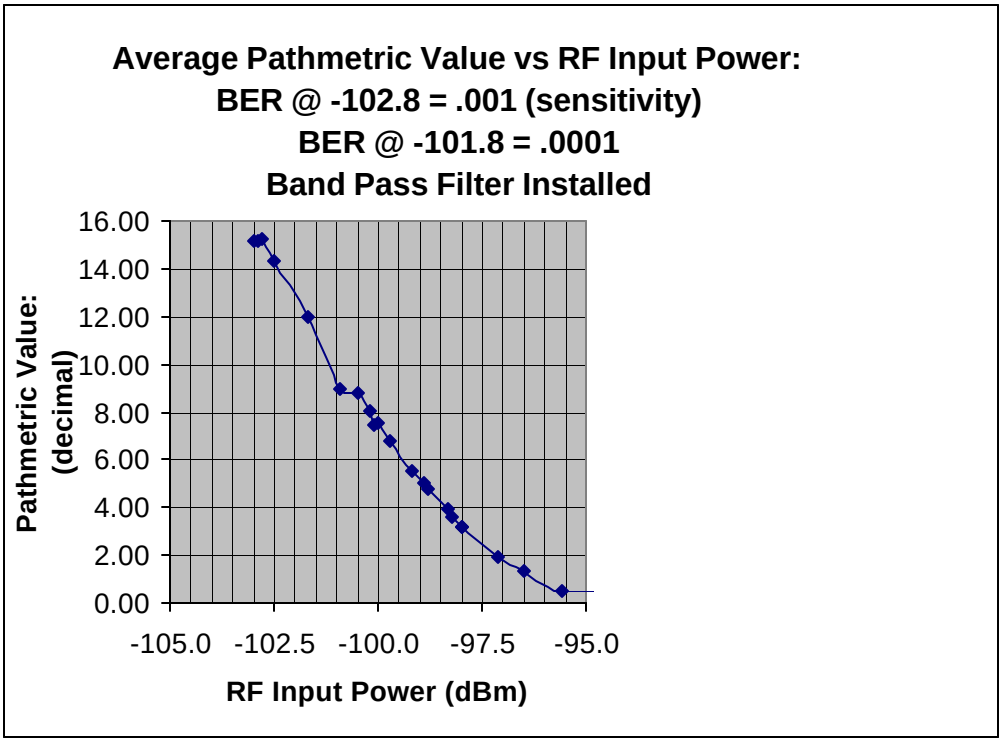


Figure 7: Pathmetric vs RF Input Power

For a bit error rate of .001 (sensitivity) the average pathmetric value is 14.0 (0E hexidecimal). The pathmetric value is not a constant value for any instant in time. The data illustrated in Figure 7 required a sample size of at least 50 measurements to determine average pathmetric for a given RF input power.

17. Question: What is the overall delay between a transmit TXADCPM input and a receive RXADPCM output?

Answer:

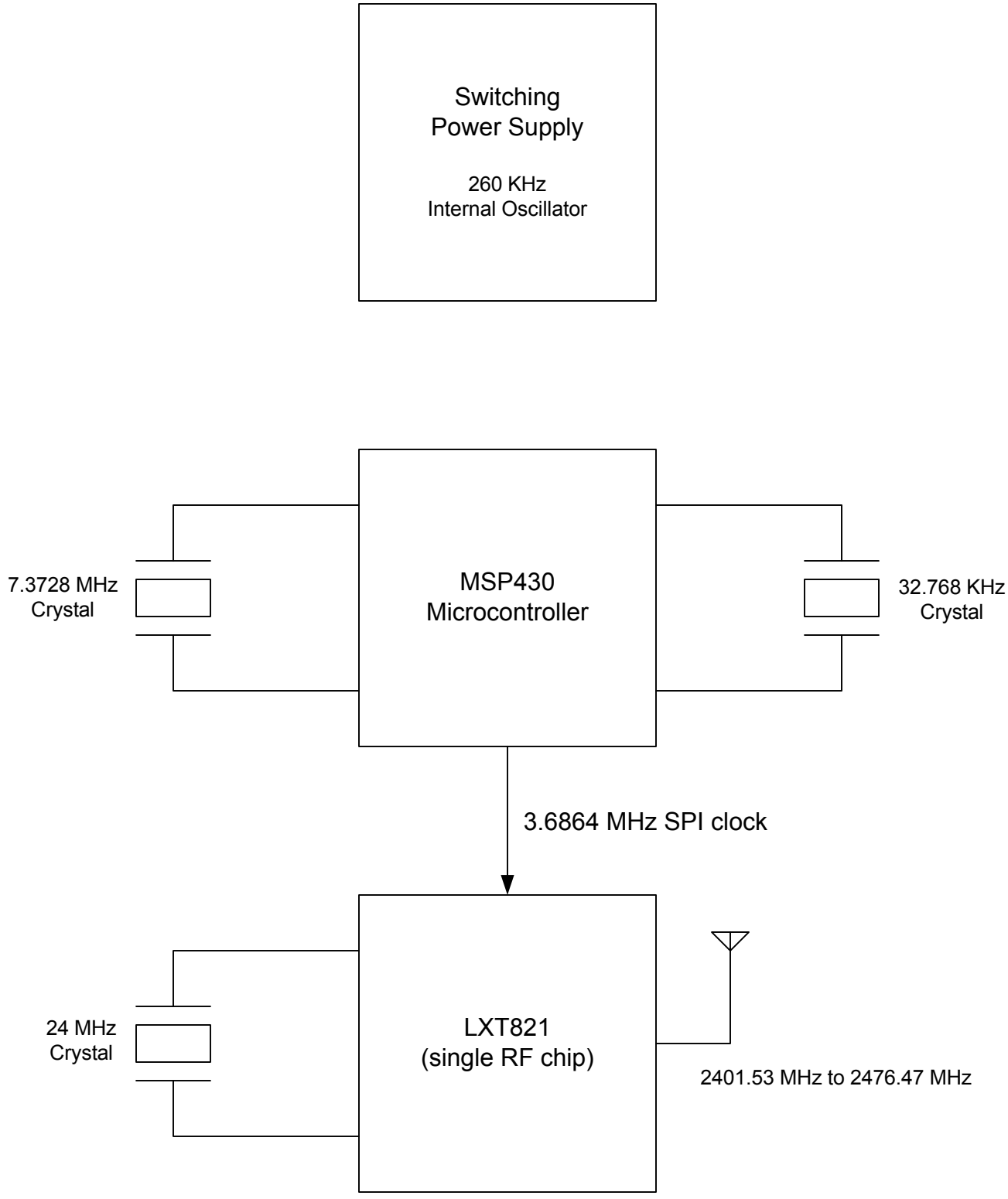
The typical ADPCM data delay for a single link direction is around 2.4 to 2.6 mS; therefore, the Alpine system has a total of 4.8 to 5.2 mS sidetone delay.

18. Question: What is the power spectral density of Alpine?

Answer:

The power spectral density varies from 5.2 dBm to 7.8 dBm depending on the PN code and channel frequency. These values are defined with no band pass filter installed. Assuming a band pass filter is used with an insertion loss of 1.5 dB, the system will have at least 1.7 dB margin with respect to the maximum allowable power spectral density of 8.0 dBm.

DART Clock Diagram



Alpine Bit Encoding and Direct Sequence Spreading

The various segments of the transmitted frame undergo different coding treatment and are spread by different PN sequences.

- The Preamble and Sync Word are spread with the user programmable PN code in PNREG1 and PNREG2 (addresses 0x00 and 0x01).
- The Data Channel and Voice / Fast Data Channel (FDC) Payload are scrambled, run through a rate 1/3 convolutional encoder, and spread with a preset, non-programmable, PN code.
- The Post-amble is treated the same as the Data Channel and Payload except that it is not scrambled; the four post-amble bits are always equal to zero.

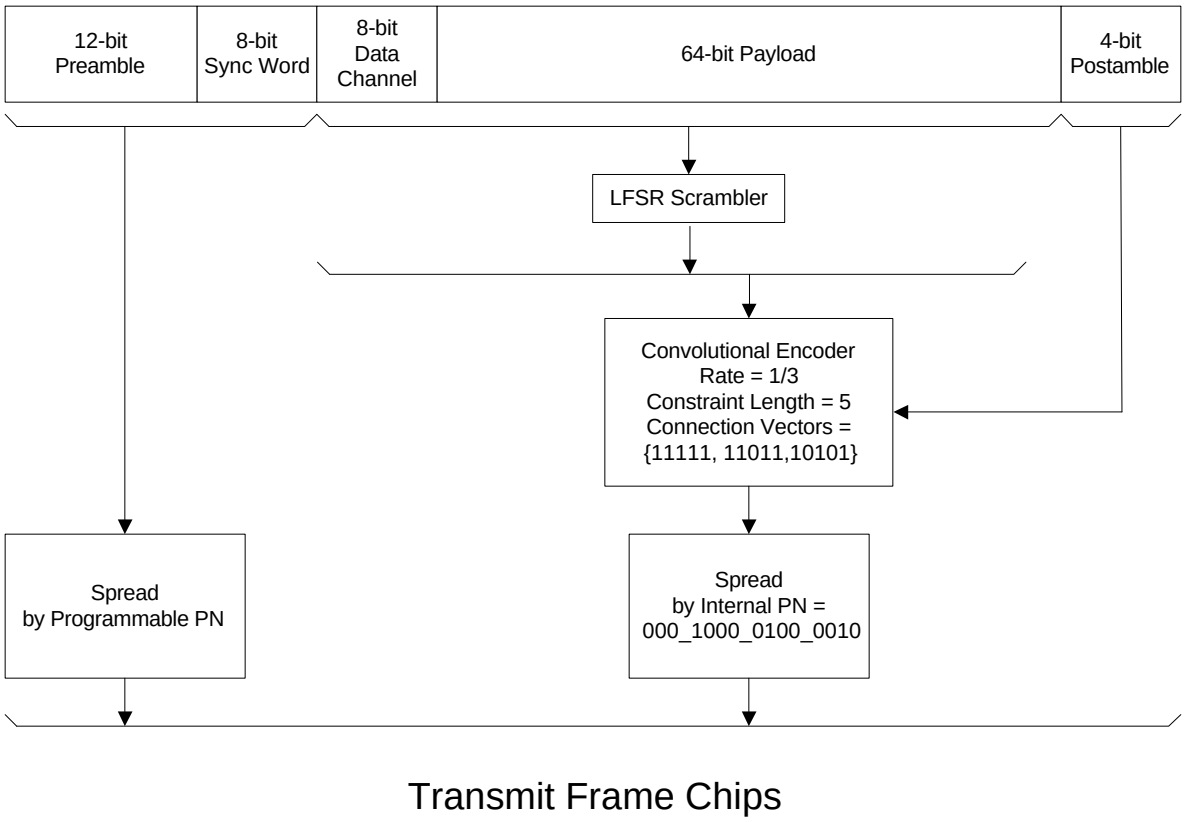


Figure 1: Alpine PN Code and Spreading Definition

Spreading

Each bit is spread by a 15-bit PN code. The spreading is exactly in phase with the start of the bit; start of Most-Significant-Chip coincides with start of bit. The user programmable PN is contained in registers 0x00 and 0x01.

Channel Encoding, Data Channel and Payload

The Data Channel, payload, and postamble are processed through a convolutional encoder and then spread using an internal non-programmable PN sequence. The Alpine receiver uses a Viterbi decoder to make a maximum likelihood estimate of the transmitted data.

The parameter used to make this estimate is the Viterbi pathmetric. It is a measure of the difference between the actual received symbol stream and a hypothesized symbol stream. More exactly: We hypothesize a set of message bits (a data channel value and payload content), calculate the chip stream which corresponds to this set of message bits, that is, we run it through the scrambler, the convolutional encoder, and the spreader, then we measure the difference between this chip stream and the one we actually received. This difference is the Viterbi pathmetric. The maximum likelihood estimate is the one with the lowest pathmetric.

Mathematically, the pathmetric is just the summed Hamming distance over the entire chip set of the message. The Hamming distance is calculated chipwise, that is, a received bit is compared to a hypothesized bit chip by chip. The two can differ in from zero to fifteen chips, thus the Hamming distance contribution from a single bit can range from zero to fifteen. The Viterbi algorithm finds the minimum sum; it finds which message bits will produce the chip set that most closely fits the received chip set.

Payload / Data Channel Coding Example

Here we illustrate the channel coding procedure for the data channel and payload, that is, the portion of the frame that is put through the convolutional encoder. The example will comprise of the first 12 data bits , all equal to zero. This means the TX data channel has been set to zero and at least the first 4 bits of the payload are also zero.. The sequence is: first the data is scrambled, then put through the convolutional encoder, and, last, spread with the payload PN code.

For the LFSR scrambler, see Figure 2:

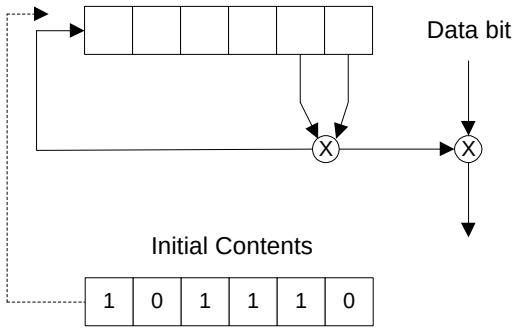


Figure 2: LFSR Scrambler

LFSR Scrambler Contents							Data Bit Out
1	0	1	1	1	0	Initial Contents	N/A
1	1	0	1	1	1		1
0	1	1	0	1	1		0
0	0	1	1	0	1		0
1	0	0	1	1	0		1
1	1	0	0	1	1		1
0	1	1	0	0	1		0
1	0	1	1	0	0		1
0	1	0	1	1	0		0
1	0	1	0	1	1		1
0	1	0	1	0	1		0
1	0	1	0	1	0		1
1	1	0	1	0	1		1

Table 1: LFSR Scrambler I/O Definition

The Data Bit out column is fed into the shifter register of the convolutional encoder. See Figure 3, Alpine Convolutional Encoder:

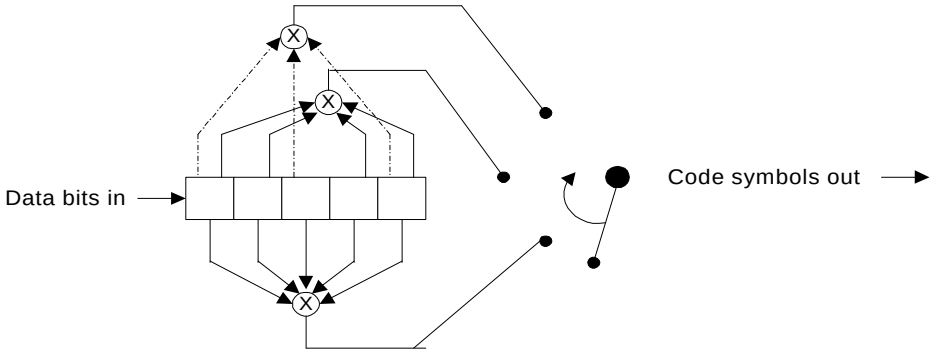


Figure 3: Convolutional Encoder

Shift Reg. Contents						Symbols Out		
0	0	0	0	0	Initial Contents			
1	0	0	0	0		1	1	1
0	1	0	0	0		1	1	0
0	0	1	0	0		1	0	1
1	0	0	1	0		0	0	1
1	1	0	0	1		1	1	0
0	1	1	0	0		0	1	1
1	0	1	1	0		1	0	0
0	1	0	1	1		1	1	1
1	0	1	0	1		1	0	1
0	1	0	1	0		0	0	0
1	0	1	0	1		1	0	1
1	1	0	1	0		1	1	1

Table 2: Convolutional Encoder Shift Register and Symbol Out

The Data Bit Out column from the Figure 2 above is shifted into the far-left column in this table. Remember that the Symbol Out, which consists of three **code bits**, has the transmit period of a single **message bit**, 10 µs. Thus each code bit is 5 chips long.

The last procedure is the spreading via PN code. The payload PN code is: 000100001000010. Separating into groups of 5 chips we see: 00010 00010 00010. It is a 5 chip repeating pattern. Thus a code symbol equal to 101, for example, will spread to 00010 11101 00010. That is, if we use a simple XOR as a spreading function. Alpine does not use just a simple XOR; it inverts the XOR. There is no functional reason for this inversion. The table following shows the chips resultant from the first 12 bits of an all zero Data Channel + payload.

Code Symbol				**Alpine Chips Out**														
1	1	1		1	1	1	0	1	1	1	1	0	1	1	1	1	0	1
1	1	0		1	1	1	0	1	1	1	1	0	1	0	0	0	1	0
1	0	1		1	1	1	0	1	0	0	0	1	0	1	1	1	0	1
0	0	1		0	0	0	1	0	0	0	0	1	0	1	1	1	0	1
1	1	0		1	1	1	0	1	1	1	1	0	1	0	0	0	1	0
0	1	1		0	0	0	1	0	1	1	1	0	1	1	1	1	0	1
1	0	0		1	1	1	0	1	0	0	0	1	0	0	0	0	1	0
1	1	1		1	1	1	0	1	1	1	1	0	1	1	1	1	0	1
1	0	1		1	1	1	0	1	0	0	0	1	0	1	1	1	0	1
0	0	0		0	0	0	1	0	0	0	0	1	0	0	0	0	1	0
1	0	1		1	1	1	0	1	0	0	0	1	0	1	1	1	0	1
1	1	1		1	1	1	0	1	1	1	1	0	1	1	1	1	0	1

Table 3: Transmit Chip Sequence

These chips follow the preamble and sync word ; they begun after 20 bits of data. The timing is diagramed below.

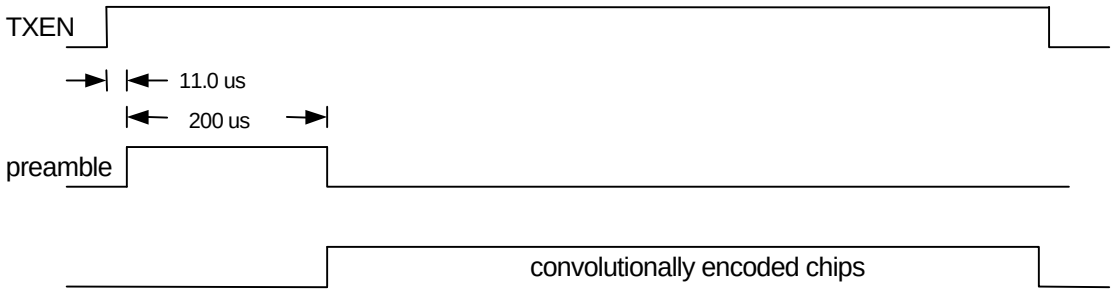


Figure 4 : Transmit Chip Timing