FCC ID: PQ9MCW4

Exhibit 3

Operational/Technical Description

TECHNICAL DESCRIPTION

MCW4
WIRELESS DATA SYSTEM

OVERVIEW

The MCW4 Wireless Data System is a fully integrated digital and analog data control and monitoring system that is linked to a national wireless network. The system features a wide power supply input range, 5 analog inputs, 2 analog outputs, 11 digital input/outputs, I2C bus, RS422/485 and 5V-RS232 serial link, GPS receiver, internal clock/alarms, internal non-volatile memory, internal rechargeable battery, and an advanced power management and monitoring circuitry. All this is housed in a 3 x 4 x 5 inch water proof (NEMA 4) cast aluminum box.

POWER MANAGEMENT CIRCUITRY

External power (8-30 VDC) is applied to a DC-DC converter of the Main Power Supply circuit which current limits the input power to properly charge the internal 6V rechargeable battery. The Main Processor also monitors the charge voltage level of the battery and terminates charging at the proper voltage by switching off the DC-DC converter. In addition, the Main Processor monitors the external voltage, voltage and current levels from the battery (except current delivered to the Radio Modem). Also attached to the battery is a 5VDC Low Dropout Regulator that supplies 5 volt system power. The 5 volt system power is also available to power external circuitry through a Power Switching module. An additional Power Switching module supplies 5 volt power to the GPS Receiver. Both Power Switching modules are current/thermal limited and are turned on and off by the Main Processor.

MAIN PROCESSOR

The heart of the MCW4 is the main processor. It is a fully integrated 12-bit data acquisition system incorporating a high performance self-calibrating multichannel ADC, two 12-bit DACs and programmable 8-bit microprocessor on a single chip. The programmable core is supported by 8K bytes Flash/EE program memory, 640 bytes Flash/EE non-volatile memory for storage of system parameters. Additional microprocessor support functions include Watchdog Timer, Power Supply Monitor, I2C-compatible bus, and Standard UART Serial Port. Normal, idle and power-down operating modes for both the microprocessor core and analog converters allow for flexible power management schemes suited to low power applications.

PIC PROCESSOR

The PIC Processor provides serial switching functions between the different system components and RESET management for the external push button. Additionally, it assists in the re-programmability of the main processor over the wireless link. This is accomplished by first receiving the new operating code over the wireless link and storing it in non-volatile memory. The PIC Processor puts the Main Processor in program mode and then uploads the new stored code into the Main Processor. Upon successful upload, the PIC Processor turns over operation to the Main Processor.

GPS RECEIVER

The GPS receiver is an L1 frequency, 8 channel, continuous tracking GPS receiver. It outputs GPS based position information at a rate of 1 output per second over a serial link to the Main Processor. The Main Processor processes the information and makes it available to the wireless user. Power to the GPS is controlled by a Power Switching Module commanded by the Main Processor. Power can then be cut completely to the GPS to conserve power. The GPS has a battery backed up memory to store ephemeras data to assist in rapid position acquisition.

NON-VOLATILE MEMORY

Over the I2C bus, the processors have access to 224k bytes of non-volatile memory for customer data storage. During program upgrades, this memory also is used to temporarily store the new code.

CLOCK TIMER CIRCUIT

The clock circuit is based on a 2048-bit static CMOS RAM organized as 256 words by 8 bits. Addresses and data are transferred serially via the two-line bidirectional I2C-bus. The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space. The remaining 240 bytes are free RAM locations. Upon an elapsed time or at a specific time, the Clock Timer circuit will produce an interrupt to the PIC processor. This processor will wake up any components that are in power down mode and will vector the program to the appropriate interrupt routine.

SERIAL I/O

The serial link to the customer's equipment is via an RS422/485 interface circuit. This can also provide a 5 volt RS232 serial link capability.

ANALOG INPUTS

The 8 analog inputs are connected to an RC filter before being passed to the 12 bit ADC circuit of the Main Microprocessor. Input voltage range is 0 to 2.5 VDC.

ANALOG OUTPUTS

The Main Microprocessor has two 12 bit DACs. Their output voltage range is 0 to 2.5 VDC. Each of these outputs is protected by a surge suppression circuit.

DIGITAL I/O

There are 11 digital I/O lines. The signal direction for each line is determined by software. I/O voltage range is 0 to 5 VDC TTL levels. Additionally, each digital line is protected by a surge suppression circuit.

I2C BUS

The I2C-bus is for bidirectional, two-line communication between different ICs or external modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines are connected to the positive 5 volt supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

RADIO MODEM

The radio modem operates in the 800 MHz frequency range, and are compatible with DataTAC® wide-area wireless data communication networks. DataTAC® is a packet-switched, narrowband PCS network designed for wide-area wireless data communication networks. The power output is 2 watts. The Main Processor communicates with the Radio Modem via a serial link and a digital activation link.