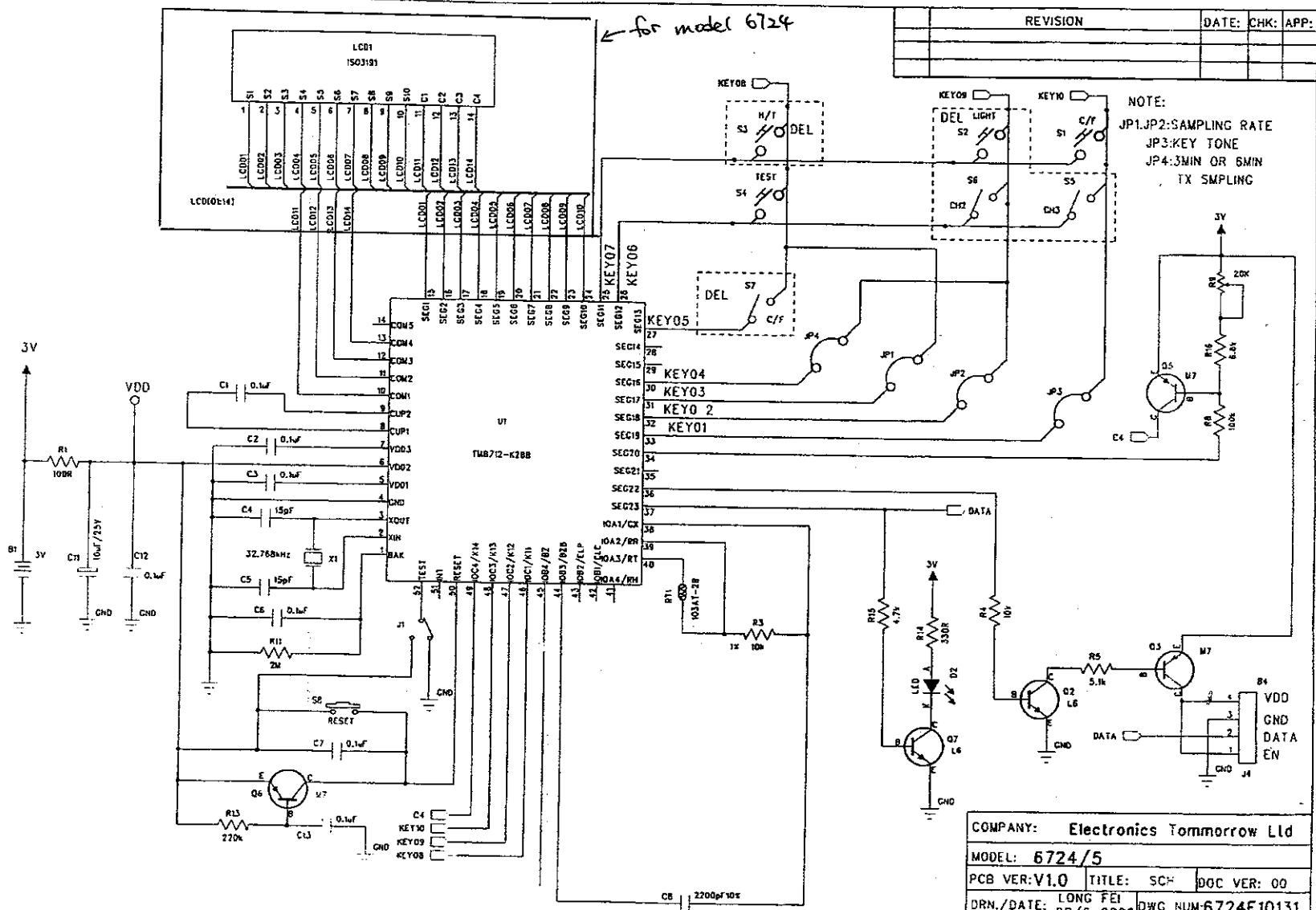


REVISION	DATE:	CHK:	APP:

← for model 6724

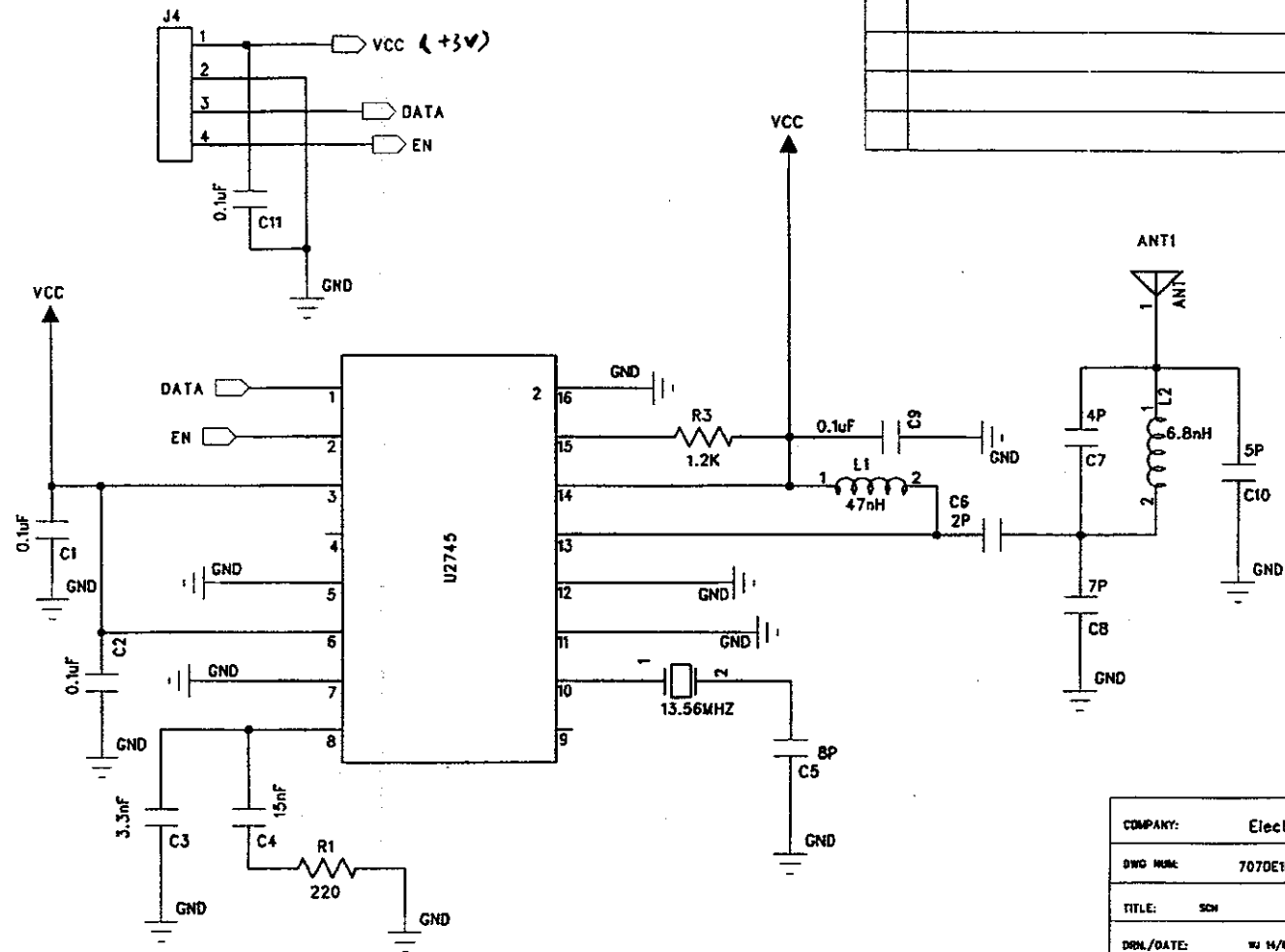


NOTE:
 JP1:JP2:SAMPLING RATE
 JP3:KEY TONE
 JP4:3MIN OR 6MIN
 TX SMPLING

COMPANY:	Electronics Tomorrow Ltd		
MODEL:	6724/5		
PCB VER:	V1.0	TITLE:	SCH
DRN./DATE:	LONG FEI	DWG NUM:	6724E10131
CHK./DATE:	28/6-2002	DOC VER:	00
APP./DATE:	27/7/02		
		LCD:	ISO3191S00V0
<input checked="" type="checkbox"/> TO FILE <input checked="" type="checkbox"/> REL SHEET 1 OF 1 EDD05			

5.12.02

NO.	REVISIONS	DATE:	CHK:	APP:



COMPANY: Electronics Tomorrow	
DWG NO: 7070E10231	REV: v1.0
TITLE: SCH	MODEL: 7070
DRN./DATE: WJ H/8.01	FILE: 70701
CHK./DATE: <i>VBS 10/6/01</i>	IC: U2745B
APP./DATE:	LCD:
<input type="checkbox"/> TO FILE <input type="checkbox"/> REL	SHEET OF: 1/1