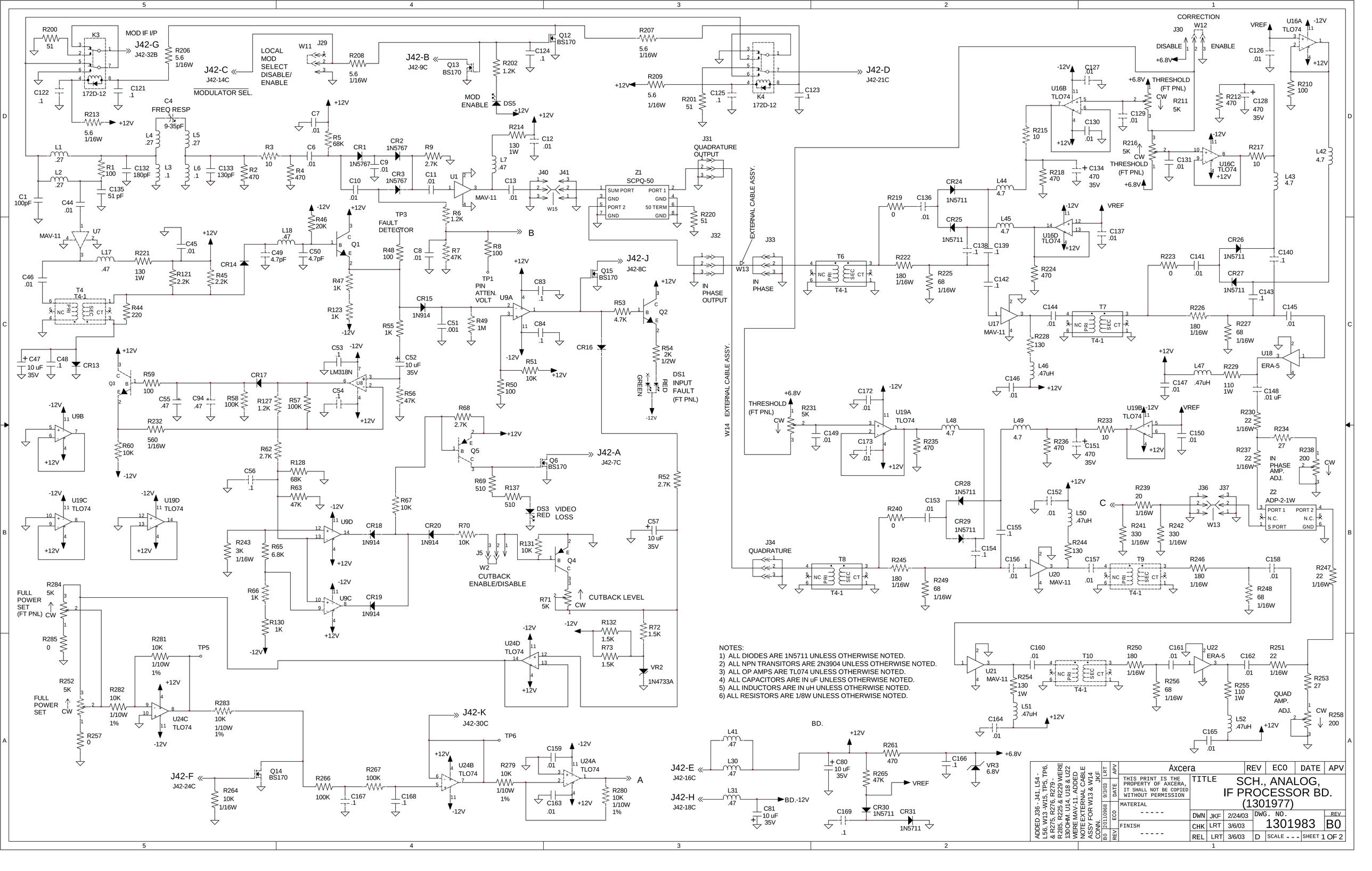
J42-G
J42-32B
MOD IF I/P
J42-C
J42-14C
LOCAL MOD SELECT DISABLE/ ENABLE
MODULATOR SEL.
J42-B
J42-9C
J42-D
J42-21C
J42-A
J42-7C
J42-J
J42-8C
J42-K
J42-30C
J42-E
J42-16C
J42-F
J42-24C
J42-H
J42-18C
EXTERNAL CABLE ASSY.
W14 EXTERNAL CABLE ASSY.
MOD ENABLE
QUADRATURE OUTPUT
IN PHASE OUTPUT
IN PHASE
FAULT DETECTOR
PIN ATTEN. VOLT
DS1 INPUT FAULT (FT PNL)
DS3 VIDEO LOSS
CUTBACK ENABLE/DISABLE
CUTBACK LEVEL
FULL POWER SET (FT PNL)
FULL POWER SET
CORRECTION
DISABLE
ENABLE
THRESHOLD (FT PNL)
IN PHASE AMP. ADJ.
QUAD AMP. ADJ.
SCPQ-50
MAV-11
TLO74
LM318N
ERA-5
ADP-2-1W
172D-12
T4-1
BD.
NOTES:
1) ALL DIODES ARE 1N5711 UNLESS OTHERWISE NOTED.
2) ALL NPN TRANSITORS ARE 2N3904 UNLESS OTHERWISE NOTED.
3) ALL OP AMPS ARE TL074 UNLESS OTHERWISE NOTED.
4) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
5) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.
6) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
ADDED J36 - J41, L54 - L56, W13 -W15, TP5, TP6, & R275, R276, R279 - R285. R225 & R229 WERE 130OHM. U14, U18 & U22 WERE MAV-11. ADDED NOTE EXTERNAL CABLE ASSY FOR W13 & W14 CONN. JKF
B0 20110988
Axcera
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TITLE
SCH., ANALOG, IF PROCESSOR BD. (1301977)
MATERIAL
FINISH
DWN JKF 2/24/03
CHK LRT 3/6/03
REL LRT 3/6/03
DWG. NO. 1301983
REV B0
SCALE
D
SHEET 1 OF 2

LAST USED REF.

C173
R275
W15
DS5
L56
CR31
J41
Q15
U24
TP4
VR3
K4
T10
Z2
S2

C
B
A

-12V U10B +12V
R92 220
R204 39
C69 .01
R203 470
R205 470
+12V
T5 T9-1
C70 .01
R91 2.2K
R168 6.81K 1/10W 1%
R189 1K
R116 470
CR23
U12 MAV-11
L26 .47
R269 130 1W
C68 .01
L25 .27
C170 200pF
C67 .01
R89 100
L24 .27
C65 100pF
C100 100pF
R100 10
R97 10
R98 27
O/P LEVEL
R99 200
CW
R271 5.6 1/16W
R104 10
R107 10
R272 5.6 1/16W
C73 .01
J38
J39
W14
R102 47
R105 47
R273 47
R103 500 (FT PNL) CW
R106 500 (FT PNL) CW
R274 500 (FT PNL) CW
L27 2.7
L54 2.7
L28 2.7
L55 2.7
L53 2.7
L56 2.7
C71 2-8pF
C72 2-8pF
C171 2-8pF
FREQ RESP
U10C -12V +12V
+12V
R270 130 1W
C74 .01
L29 .47
U13 MAV-11
C75 .01
U14 ERA-5
C85 .01
R109 470
R110 47
J35 IF SAMPLE (FT PNL) SMA
C86 .01
R275 110 1W
L32 .47

J42-E
J42-H
J42-A
J42-J
J42-B
J42-C
J42-E
J42-H
J42-D
J42-F
J42-K
J42-G

VIA4204

J42C
1C IF 2 UC
2C
3C
4C VIA 4204
5C
6C ALC AUTO/MAN. SW
7C MODULATION PRES.
8C INPUT FAULT
9C SELECTED IF SOURCE
10C MUTE COMMAND
11C ALC VOLTAGE
12C INTERLOCK
13C BOARD TYPE
14C IF SIGNAL SELECT
15C
16C +12VDC_C4
17C
18C -12VDC_C1
19C
20C
21C MODULATED IF INPUT
22C
23C
24C IF POWER CONTROL
25C
26C
27C
28C
29C
30C DLC VOLTAGE
31C
32C
913289

J42B
1B
2B
3B
4B
5B
6B
7B
8B
9B
10B
11B
12B
13B
14B
15B
16B +12VDC_C4
17B
18B -12VDC_C1
19B
20B
21B
22B
23B
24B
25B
26B
27B
28B
29B
30B
31B
32B MOD. IF OUTPUT
913289

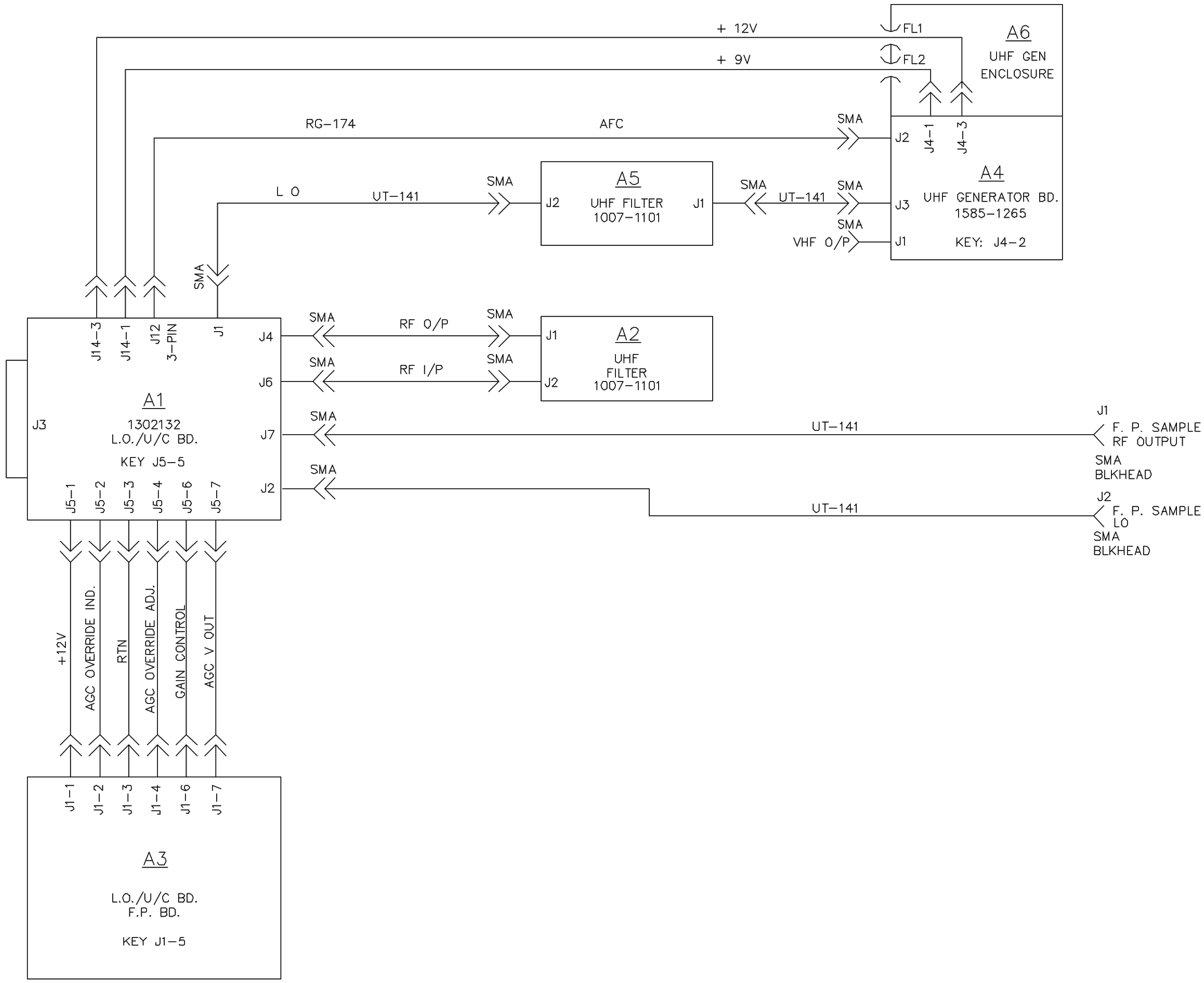
J42A
1A
2A
3A
4A
5A
6A
7A
8A
9A
10A
11A
12A
13A
14A
15A
16A +12VDC_C4
17A
18A -12VDC_C1
19A
20A
21A
22A
23A
24A
25A
26A
27A
28A VIA
29A VIA
30A
31A
32A
913289
VIA4204 1
VIA4204 1

B
R88 470
L19 4.7
CR22 1N914
U11 4N25
R79 1M
DS4 RED
GREEN MUTE (FT PNL)
R78 1.5K
R139 1.5K
+12V
-12V

(FT PNL) MANUAL GAIN
+12V
R87 5K
CW
SW1 SWW246CD7 (FT PNL)
MANUAL
AUTO
TP4 ALC VOLT.
R93 100
R94 220

C58 .47
R86 51
-12V
R82 2.2M
U10D
R85 2K 1/2W
DS2 RED
GREEN ALC FAULT (FT PNL)
+12V
-12V
R77 47K 1/16W
C59 .1
R84 2.7K
+12V
R276 47K 1/16W
U10A
R83 10K
C60 .1
-12V
R80 10K
CR21 1N914
C61 .47
R81 15K

APV	Axcera	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH., ANALOG, IF PROCESSOR BD. (1301977)		
ECO	MATERIAL -----	DWN	JKF	2/24/03	DWG. NO. 1301983 REV B0
REV	FINISH -----	CHK	LRT	3/6/03	
		REL	LRT	3/6/03	D SCALE --- SHEET 2 OF 2



NOTES:

1) ALL WIRES 22AWG UNLESS OTHERWISE NOTED.

REV	ECO	DATE	APV

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MATERIAL — — — —

FINISH — — — —

TITLE: I/C, L.O./ U/C ASSY, UHF LOW PHASE NOISE

DWN	MH	6/11/03	DWG. NO. 1302060	REV A0
CHK	LRT	6/12/03		
REL	LRT	6/12/03	C SCALE ---	SHEET 1 OF 1

LAST USED REF.

C89
CR13
DS2
J14 + J43
K1
L16
Q8
R111
T2
TP7
U14
W3
Z1

IF PROC
IF 2 UC
AFC VOLTAGE
EXT. REF. IND.
AGC #1 VOLT.
PLL LOCK IND.
AGC #2 VOLT.
ALC VOLT.
INTERLOCK
SERIAL CLOCK
SERIAL DATA
SER. LOGIC ENAB.
SYSTEM +12V DC CIRCUIT 5
SYSTEM -12V DC CIRCUIT 1
EXT. 10MHz INPUT
UC RF OUT PUT
SYSTEM 10MHz OUT PUT
MOD. 10MHz INPUT

Z1 LRMS-2
J1 SMA LO I/P
J2 SMA -20dB (FT PNL)
J4 CH. FILTER RF O/P 1 SMA
J6 RF I/P SMA
J7 -20dB SMA (FT PNL)
R5 51
R105 33
R106 27
R107 33
C85 51pF
R2 18
R3 18
R4 18
L3 .15
C83 51pF
C84 51pF
R6 300
R7 300
R8 27
R14 200 IF LEVEL
R12 300
R15 18
R17 300
C7 4.7pF
+5V
R16 47K
Q1 2N3906
Q2 BS170
R23 470
C9 .01
DS1 RED
R22 15K
U2 ERA-5
C10 .001
C11 .001
R18 0
R20 INFINITY
R21 INFINITY
L4 .1uH
R24 110
C69 220pF
R94 100 1/10W 1%
L11 1200 nH
L12 1200 nH
C70 220pF
C71 470pF
C87 .01
C14 .01
+12V
U8 MC78L05ACP
C54 .47
C55 .1
L10 .47uH
C56 47 20V
R59 10
CR6 1N914
CR7 1N914
C15 .01
R60 47K
R28 1K
R32 68K
C18 .001
CR2 1N5767
R33 2.7K
C19 .001
CR3 1N5767
CR4 1N5767
C20 .001
C22 .001
R101 18.2 1/10W 1%
C86 .001
U13 ERA-5
C82 .001
L15 .1uH
R104 110 1W
R102 300 1/16W
R103 300 1/16W
T1 ADTL1-12
C2 .001
C5 .001
R1 100
U1 HELA-10
L1 .47uH
C3 .001
T2
C4 .001
ADTL1-12
L2 .47uH
C6 .001
R41 51
C1 .001
U4A TL082
-12V
LMX2326
GND
CE
CLOCK
DATA
LE
Fo/LD
Vcc 2
Vp
OSC in
Vcc 1
FIN
GND
GND
CPo
FLo
U9
C51 .001
C52 .1
C81 .01
R109 NOT USED
R95 100 1/10W 1%
L13 1200 nH
L14 1200 nH
C72 220pF
C73 220pF
C74 470pF
R110 NOT USED
R108 INFINITY
C30 .01
K1
Q3 BS170
R42 47 1/16W
R44 47 1/16W
C35 .01
C37 .1
U6
CCO-014-T-15-10.000
Q4 BS170
C27 .01
C29 .1
L5 .47uH
L6 .47uH
C24 47 20V
L7 .47uH
C28 47 20V
J10 EXT. W3 INT.
L8 .47uH
J11 ALT INT. 10MHz
R46 100K 1/16W
R48 300 1/16W
C41 .1
U7A TL082
R54 1M
CR5 5082-2811
C44 .01
R55 51 1/16W
L9 .27uH
C46 .001
R96 1M 1/16W
C47 .001
C48 .1
-12V
R53 1.2K
DS2 YELLOW INT. REF. IND
Q5 BS170
Q6 BS170
R112 60.4K 1/10W 1%
C32 .1
R49 60.4K 1/10W 1%
C38 1
C42 .1
U4B TL082
C31 .1
C34 .1
W2 OPERATE SETUP
J9
R43 5K
C W
TP2
R47 220
TP3
R50 220
R51 10K
R52 10K
C43 .1
R56 220
R57 6.8K
U7B TL082
R58 1K
C49 .001
C50 .47
J12 VCXO AFC O/P
C79 .1
U10A LM324D
R62 1K
R63 100K
C61 .001
R69 1K
R70 220
TP6
R72 1K
C60 .47
R64 470K
U10D LM324D
R74 47K
R77 10K
R78 20K
C63 .01
R84 100K
R87 47K
R88 47K
R83 100K
U11C LM324D
C65 .01
R61 220
C59 .01
J5
AGC VOLTAGE OUT
GAIN CONTROL IN
KEY
AGC OVERRIDE ADJ.
GND
AGC OVERRIDE IND
+12V
C57 .01
R100 200
C58 .01
R65 220
C62 .01
AGC #2 OUTER LOOP
AGC #1 INNER LOOP
OUTER LOOP AGC #2
R71 5K
U10B LM324D
TP4
R66 1K
CR8 1N914
R67 10K
CR9 1N914
R75 47K
R76 10K
U10C LM324D
TP5
R68 1K
R73 47K
U14 MAV-11
C88 .01
L16 .47
R111 130 1W
C89 .01
U 12 LM317T
C75 .47
R97 470
R98 470
C76 .1
C77 .01
R99 1.5K
C78 .47
R79 220
INNER LOOP AGC #1 R82 5K
C64 .01
C80 .1
U11A LM324D
TP7
R80 1K
CR10 1N914
U11B LM324D
R81 10K
CR11 1N914
R85 20K
R86 1K
R89 2.2K
R90 47K
R92 10K
R91 10K
CR12
R93 470
1N914
CR13 1N914
Q7 BS170
Q8 BS170
U11D LM324D
HI=OVERDRIVE
C68 .01
J14
+9V
KEY
+12V
RTN
-12V
C66 .01
C67 .01

NOTE:
1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.

R42 WAS 220, R109 & R110 WERE 2K, R49 WAS 10K, C38 WAS 4.7, ADDED R112. PINS U4-2 & -3 TO GND. PIN U4-1 NO CONN. DEL. C36 & C45. JKF

REV	ECO	DATE	APV
B0	20111055	9/19/03	LRT

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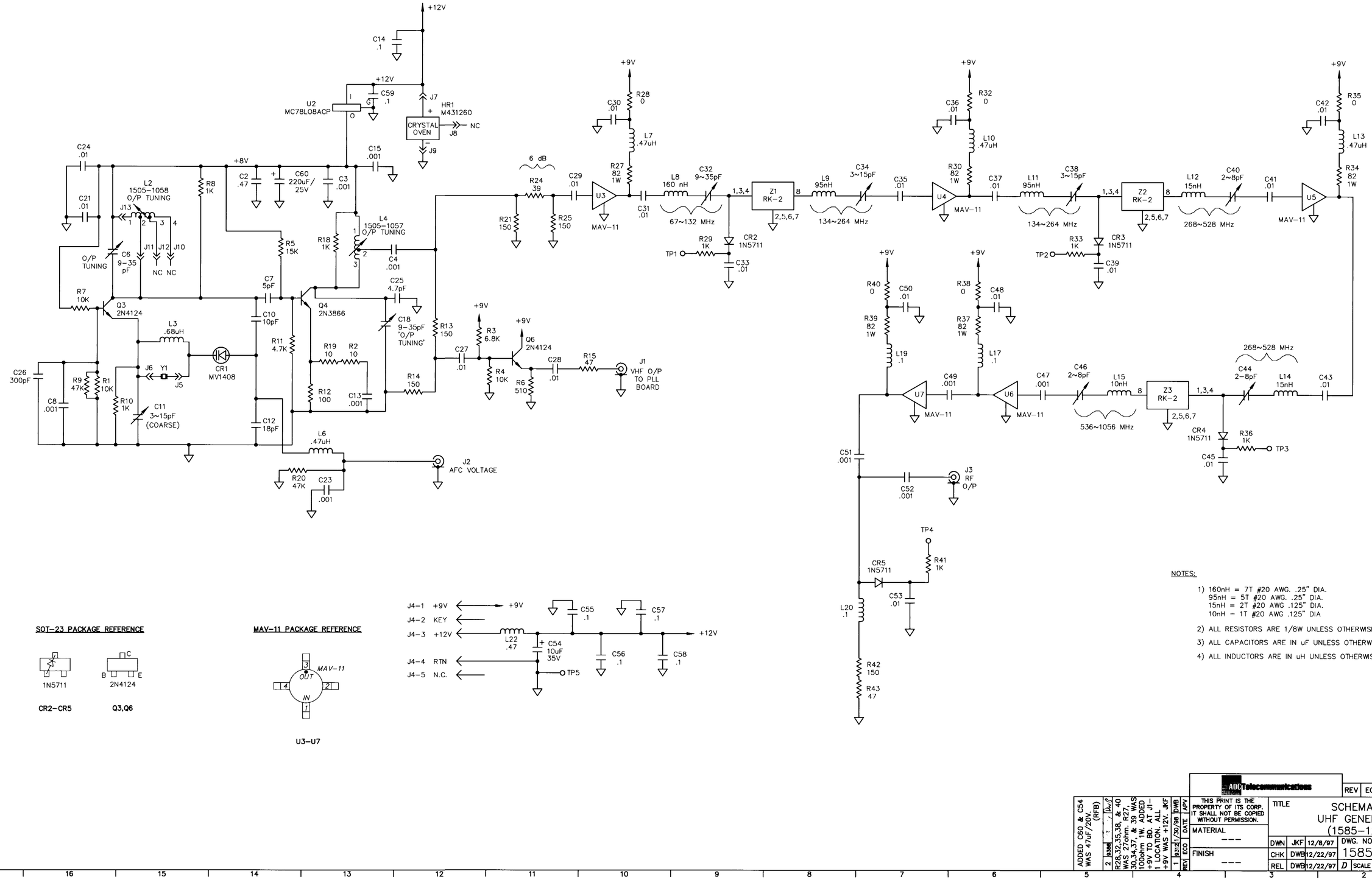
MATERIAL -----

FINISH -----

TITLE SCH., L.O./ UPCONVERTER BD., UHF, LPN. (1302132)

DWN	JKF	3/25/03	DWG. NO. 1302134 REV B0
CHK	LRT	9/3/03	
REL	LRT	9/3/03	D SCALE - - - SHEET 1 OF 1



NOTES:

1) 160nH = 7T #20 AWG. .25" DIA.
   95nH = 5T #20 AWG. .25" DIA.
   15nH = 2T #20 AWG .125" DIA.
   10nH = 1T #20 AWG .125" DIA

2) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.

3) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.

4) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.

REV	ECO	DATE	APV
2	[illegible]	[illegible]	DWB
1	ks22	1/30/98	DWB

ADDED C60 & C54 WAS 47uF/20V. (RFB)

R28,32,35,38, & 40 WAS 27ohm. R27, 30,34,37, & 39 WAS 100ohm 1W. ADDED +9V TO BD. AT J1-1 LOCATION. ALL +9V WAS +12V. JKF

ADC Telecommunications

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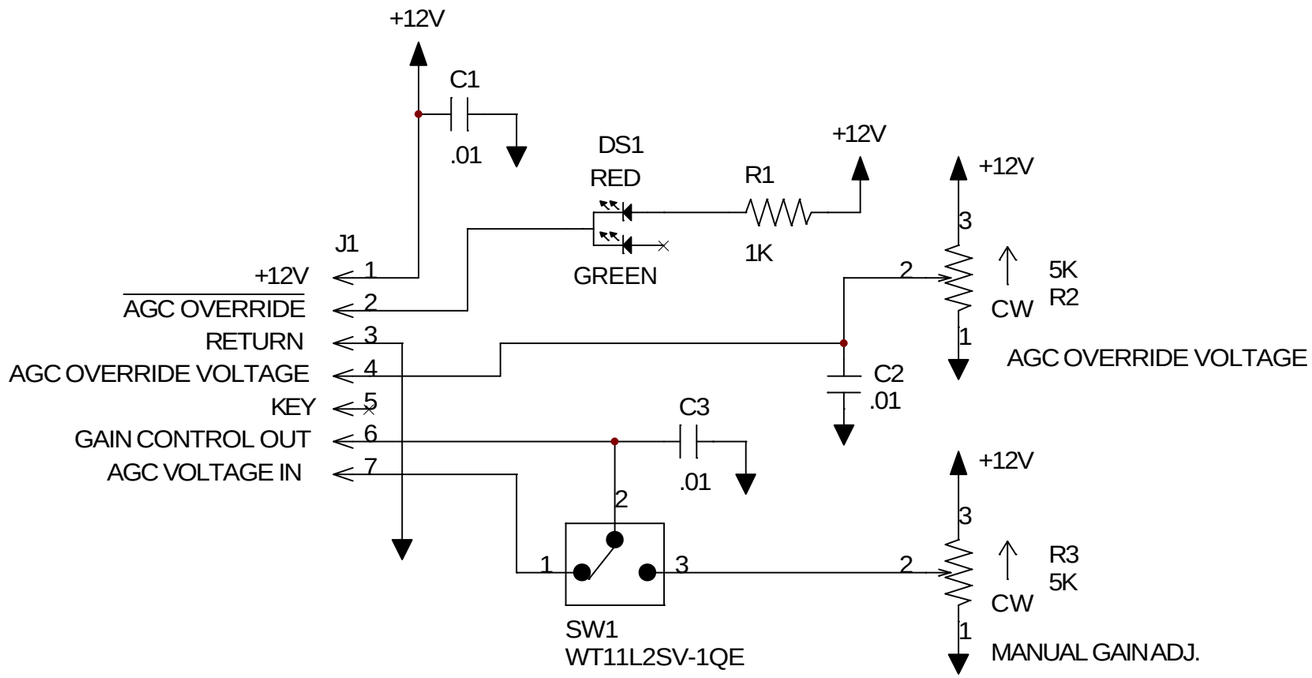
MATERIAL ---

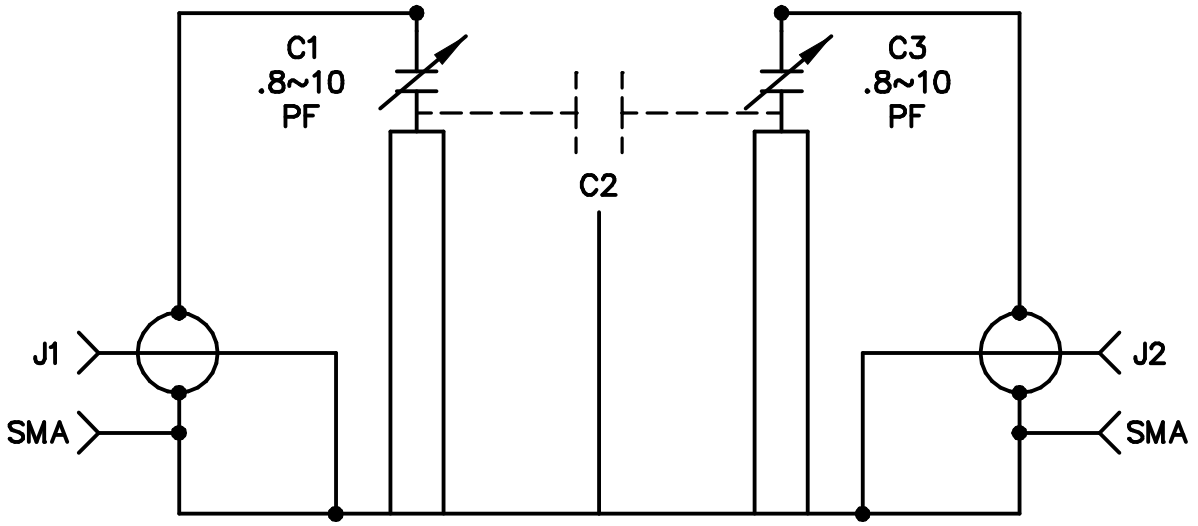
FINISH ---

TITLE SCHEMATIC, UHF GENERATOR (1585-1265)

DWN	JKF	12/8/97	DWG. NO. 1585-3265 REV 2
CHK	DWB	12/22/97	
REL	DWB	12/22/97	D SCALE 1=1 SHEET 1 OF 1



APV	Axcera	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH., FRONT PANEL LED DISPLAY BOARD (1303033)		
ECO	MATERIAL -----	DWN	JKF	7/24/03	DWG. NO. 1303035 / REV A0
REV	FINISH -----	CHK	LRT	7/25/03	
		REL	LRT	7/25/03	B / SCALE - - - / SHEET 1 OF 1



NOTE: C2 IS STRAY CAPACITANCE BETWEEN LINE SECTIONS.

REV	ECO	DATE	APV

ADC

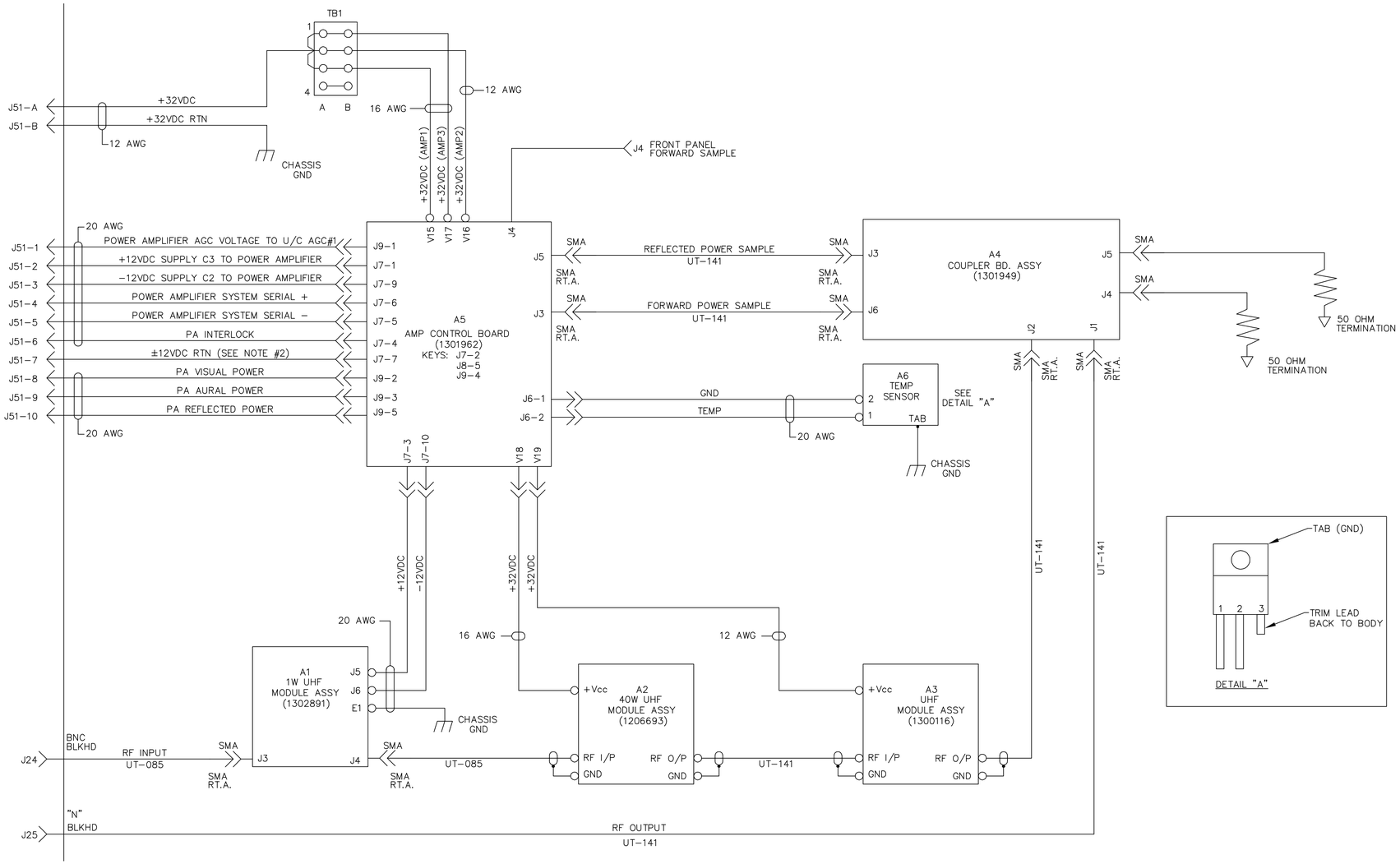
MATERIAL ------

FINISH ------

TITLE **91-00-00-50Z-61**

UHF FILTER

			DWG. NO.	REV
DWN	DD	9/13/83	1007-3101	0
CHK	RWZ	9/13/83		
REL	RWZ	7/20/90	A SCALE ---	SHEET 1 OF 1



NOTE:
1. ALL WIRE IS 18AWG UNLESS OTHERWISE NOTED.
2. THIS CONNECTION MUST BE EQUIPPED WITH LONGER GROUND PIN. (MAKE FIRST BREAK LAST)

REV	ECO	DATE	APV
B0	20110990	9/11/03	JCM

DELETED .141 RIGID BETWEEN A5-J4 AND J1. (SAK)

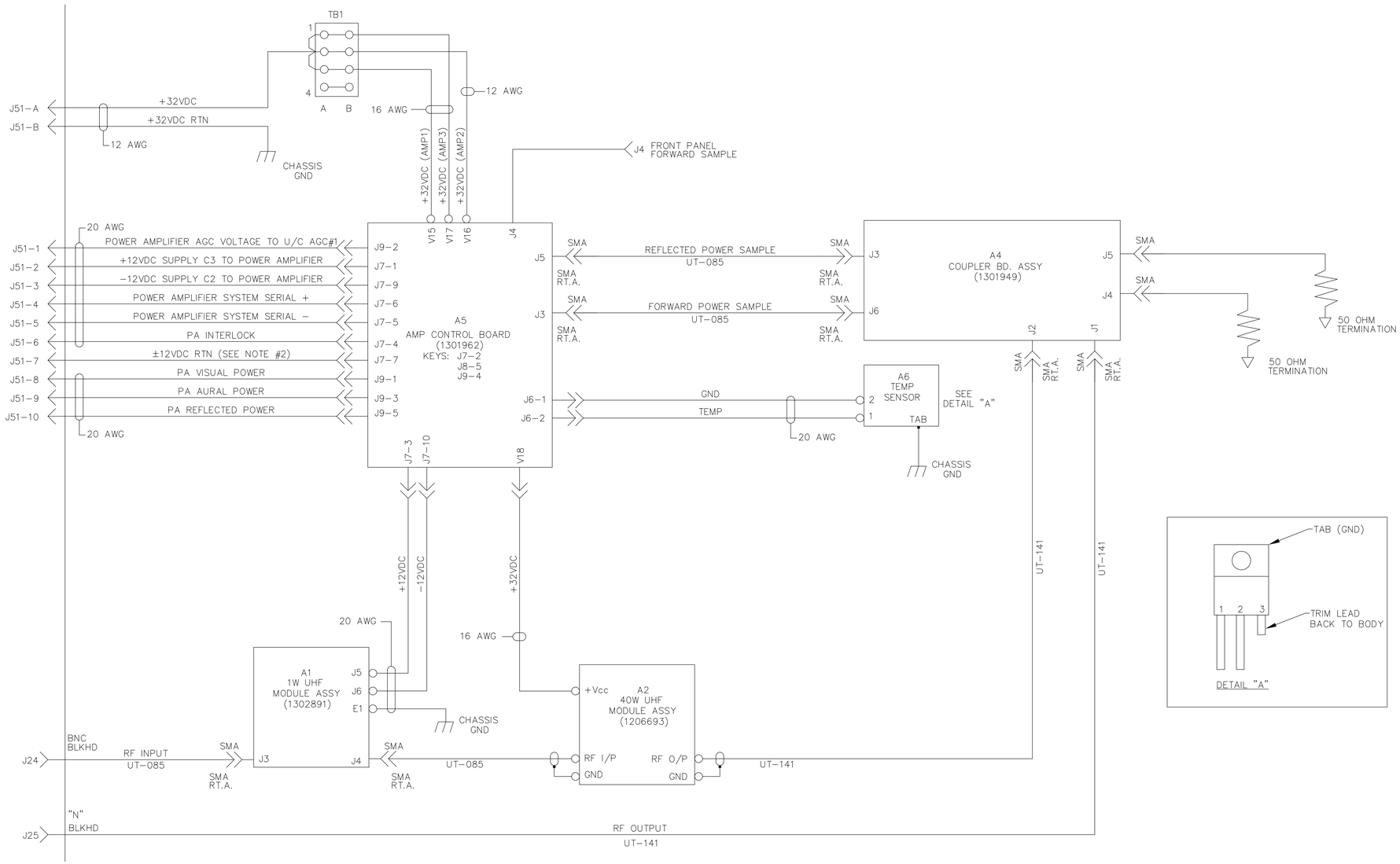
Axcera

MATERIAL: -----

FINISH: -----

TITLE: I/C, PA ASSEMBLY, 100W PIONEER SERIES

DWN	MH	8/13/03	DWG. NO. 1302061 REV B0
CHK	JCM	8/27/03	
REL	JCM	8/27/03	D SCALE --- SHEET 1 OF 1



NOTE:
1. ALL WIRE IS 18AWG UNLESS OTHERWISE NOTED.
2. THIS CONNECTION MUST BE EQUIPPED WITH LONGER GROUND PIN. (MAKE FIRST BREAK LAST)

REV	ECO	DATE	APV
B0	20111102	11/6/03	JCM

A5−J9−2 WAS A5−J9−1.
A5−J9−1 WAS A5−J9−2.
REFLECTED AND FORWARD POWER SAMPLE CABLES WERE UT−141. (RGE)

MATERIAL −−−−−

FINISH −−−−−

TITLE I/C, PA ASSEMBLY, 1KW, DRIVER LX SERIES

DWN	MH	10/21/03	DWG. NO.	REV.
CHK	RT	10/22/03	1303452	B0
REL	JCM	10/22/03	D	SCALE −−− SHEET 1 OF 1

Processor Operation

(1.6V = -12V OK)
(2.72V = -12V missing)
(-.7V = +12V missing)

Serial Address

Fault Monitoring

MC74VHC245DT

MC74HC138A

CD74HC4051M

2-61100-4472

1095823

453-HC373XX

LT1076-ND

PROGRAMMING ENABLED

SERIAL PROGRAMMING PORT

MANUAL MICRO RESET

FIRMWARE CONFIGURATION

ENABLED

DC OK

TEMP

MOD OK

Off Board Wired Connections

J7: +12 Vdc Supply; Key; +12 Vdc to Amp; Device Present; System Serial -; System Serial +; Ground; Ground; -12 Vdc to Amp; -12 Vdc Supply

J8: Device ID1; Device ID2; Device ID3; Device ID4; Key; Device ID5; Device ID6; Device ID7; Device ID8; PS Ctrl

MATERIAL NUMBERS:
1301962 A/D, PIONEER, AMP CTRL
1301963 PCB, PIONEER, AMP CTRL
1301964 SCH, PIONEER, AMP CTRL
1301965 STENCIL FOR 1301963
1301966 FIRMWARE, PIONEER, AMP CTRL

CR27 ANODE WAS CONNECTED TO GND, CATHODE WAS CONNECTED TO R146 & R145. REVERSED CONNECTIONS TO U10B PINS 5 & 6. U15.3 WAS CONNECTED TO CR8. U15.2 TO Q18.1 ADDED. R94 WAS 1.2K. R97 WAS 8.25K. DELETED CR6, V14 THRU V20. ADDED C78 THRU C103, CR29 THRU CR38, E15 THRU E20, J9, J10, J11, Q18, Q19, R167 THRU R176, W1, W2. CHANGED REF. DES. R163 TO R201, R164 TO R203, R166 TO R202, R116 TO R204, R102 TO R205. U28A WAS UNUSED. J8.10 WAS GROUND. TP5 WAS V14. (CR)

C0	20110973	9/23/03	REH

ADDED CR26, CR27, CR28, J7, J8, Q12 THRU Q17, R144 THRU R166, TP4, CHANGED DS1, DS2, DS7 TO SMT, R23, R36 THRU R43, R54 THRU R57 FROM 10K 5% TO 10K 1%, R85 FROM 1K 5% TO 1K 1%, R134, R135, R138, R140 TO 10K, U1 TO CD74HC4051M, U3, U5, U9 TO MC74VHC245DT. DELETED J1, R3, R59. (CR)

B0	20110900	7/31/03	REH

Axcera	REV	ECO	DATE	APV

APV
DATE
ECO
REV

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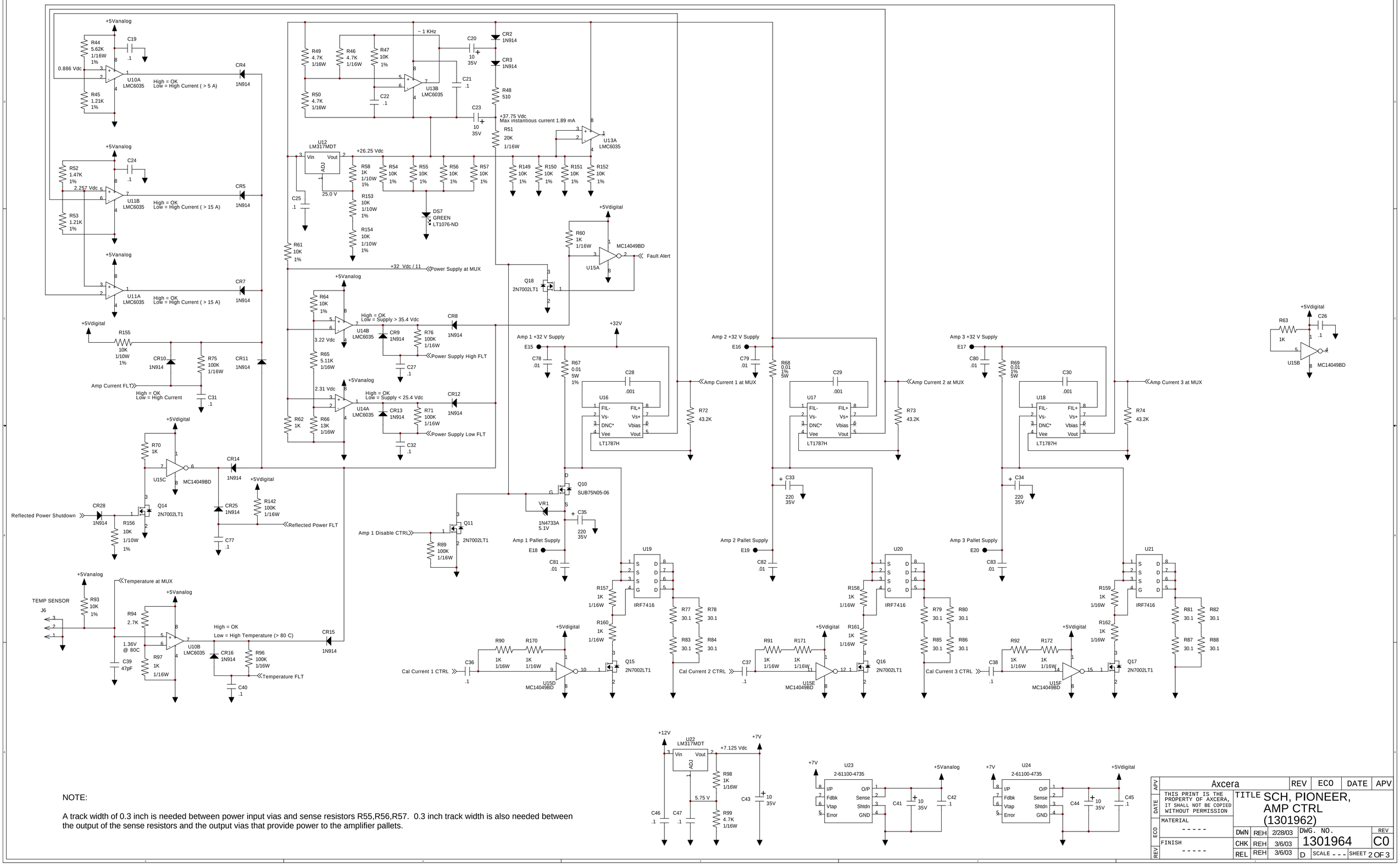
MATERIAL: -----

FINISH: -----

TITLE: SCH, PIONEER, AMP CTRL (1301962)

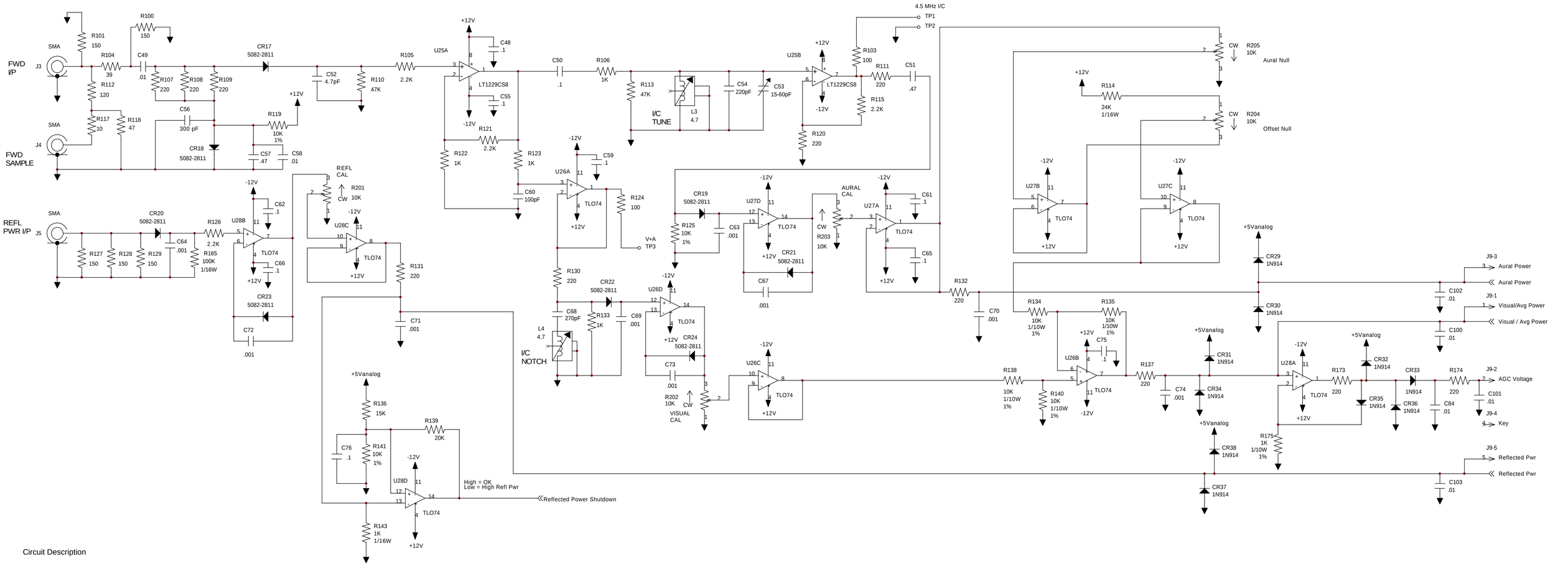
DWN	REH	2/28/03	DWG. NO. 1301964 REV C0
CHK	REH	3/6/03	
REL	REH	3/6/03	D SCALE --- SHEET 1 OF 3



NOTE:

A track width of 0.3 inch is needed between power input vias and sense resistors R55,R56,R57. 0.3 inch track width is also needed between the output of the sense resistors and the output vias that provide power to the amplifier pallets.

	Axcera	REV	ECO	DATE	APV	
APV	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, PIONEER, AMP CTRL (1301962)				
DATE	MATERIAL -----	DWN	REH	2/28/03	DWG. NO. 1301964	REV C0
ECO	FINISH -----	CHK	REH	3/6/03		
REV		REL	REH	3/6/03	D SCALE --- SHEET 2 OF 3	



Circuit Description

Page 1:
Upper center of page one is U4 which is the controller. This in-circuit Atmel microcontroller is operated at 3.6864 MHz. Programming of this device is performed through J2. U4 selects the desired analog channel of U1 through the settings of PA0 - PA3. PA4 of U4 is a processor operating LED that can be flashed to show continued operation.
The outputs of Port A must be set and not changed during an analog input read of channels PA5 - PA7. PA5 is used to monitor the +12 Vdc supply to the board. PA6 is the selected channel of analog switch U1. PA7 is connected to a via for future access.

U6 is our standard serial to RS-485 driver IC. U7 is a watchdog IC used to hold the microcontroller in reset if the supply voltage is less than 4.21 Vdc; (1.25 Vdc < Pin 4 (IN) < Pin 2 (Vcc)). U7 momentarily resets the microcontroller if Pin 6 (!ST) is not clocked every second. A manual reset switch is provided but should not be needed.

Upper right corner U3 is used to determine where the amplifier control board is located. The eight inputs come from the main amp connector and are used to set the SCADA address of the controller. Pull-up resistors set a default condition of logic high.

U5 below U3 is used for getting digital input information of the board. Page two has several monitoring circuits that provide information on the amplifier's status. Many of these circuits automatically shut down the amplifier if a specific fault occurs.

U8 below U5 is used to control four board mounted status LEDs. A FET is turned on to shut current away from the LED to turn it off. U9 below U8 is used to enable different features within software. Actual use is TBD.

Page 2:

In the lower right corner are voltage regulator circuits. U22 should allow for 0.14 amps of power using its 92 C/W rating if Ta = 60C max and Tj = 125C max. 0.26 amps can be obtained from U22 if the mounting pad is 0.5 sqr. inches. The controller will not need this much current.

U23 and U24 are low drop-out voltage regulators with a tolerance greater than or equal to 1%. 100 mA is available from each device but again the controller will not need this much current.

In the upper left section are circuits with U12 and U13. U12 is used to generate a regulated voltage that is about 5 Volts less than the +32 Volt supply. When the +32 Volt supply is enabled, the circuitry around U13B is used to provide gate voltage to Q10 that is 5 volts greater than the source pin of this FET. The gate of Q10 can be turned off by any one of a few different circuits.

U10A is used to turn off the gate of Q10 in the event of high current in amplifier #1. At 0.886 Vdc, the current to amplifier #1 should be about 5.12 Amps. U11 is used to turn of the FET if high current is detected in amplifier #2 or #3. With 2.26 Vdc at pin 5 and pin 3 of U11, the voltage output of current sense amplifier U17 or U18 at high current shut down should be about 13.1 Amps.

U14B is used to turn off the gate of Q10 in the event of high power supply voltage. U14A is used to keep the FET disabled if the power supply voltage is less than 26 volts.

U28D on page 3 is used to turn off the gate of Q10 in the event of high reflected power. U10B turn off the gate of Q1 if the power supply temperature gets too hot.

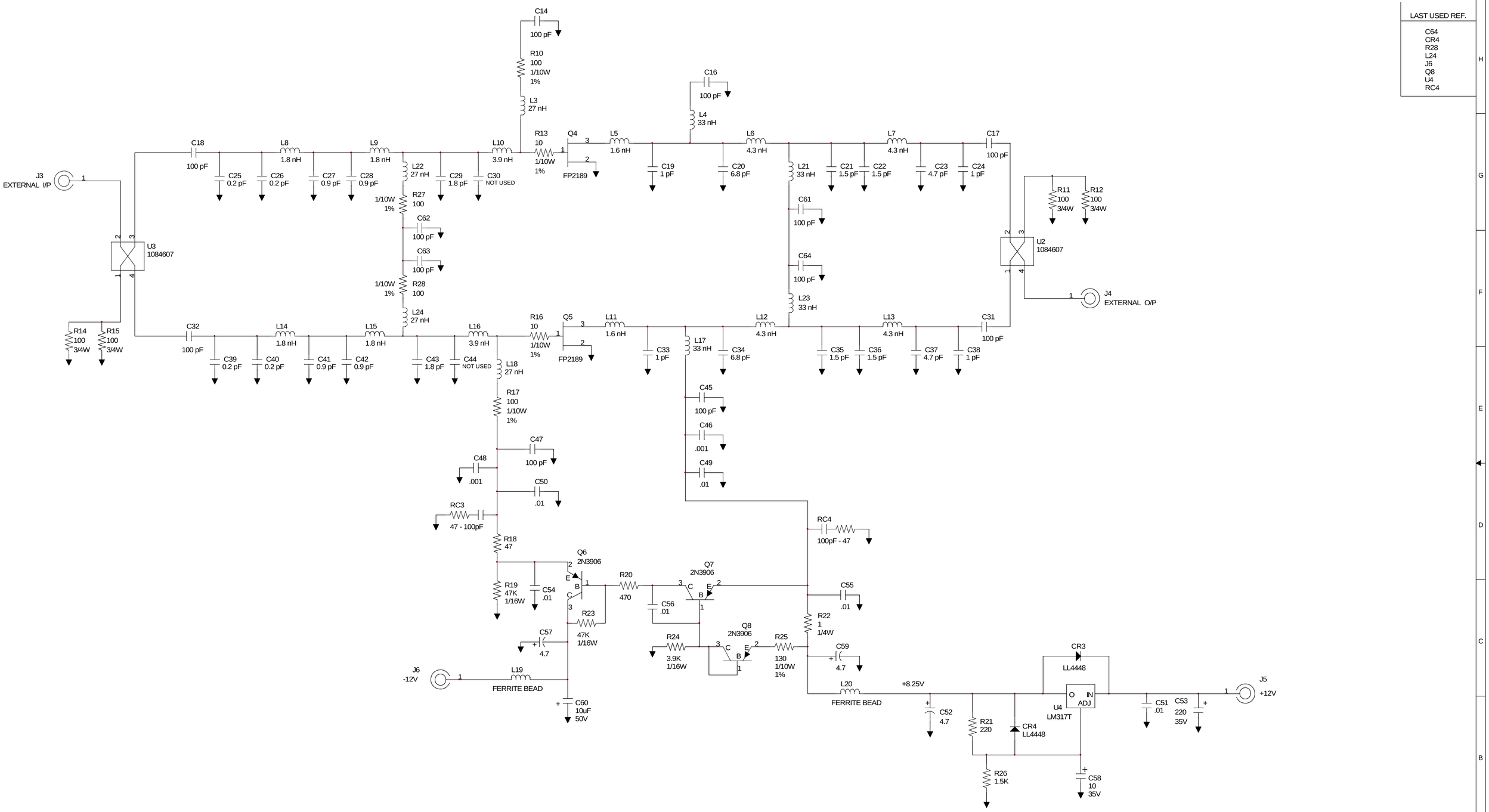
Current Monitoring Sections - A 0.01 ohm 1% 5 Watt thru-hole resistor is used for monitoring the current through several sections of the amplifier. The voltage developed across this resistor is amplified for current monitoring by U16, U17, or U18. The Linear Technology LT1787HVCS8 precision high side current sense amplifier accepts a maximum voltage of 60 Vdc. The 43.2 Kohm resistor from Pin 5 to ground sets the gain of the amplifier to about 17.28. This value is not set with much accuracy since the manufacture internal matches the resistors of this part but their actual resistance value is not closely defined. A trimming resistor is suggested to give a temperature stability of -200ppm/C but instead the microcontroller will determine the exact gain of the circuit and use a correction factor for measurements. Circuit loading components are located in the lower portion of each current monitoring circuit. These components allow for short duration high current loading of the supply. By measuring the current through the sense resistor with and without the additional load, the microcontroller can determine the gain of each circuit. The input to each hex inverter protects the load resistors from prolonged power dissipation. The load resistors are four 30.1 ohm 1% 1206 resistors. For very short duration pulses, a 1206 resistor can handle up to 60 watts. The Atmel processor requires 226 uSec per conversion. A supply voltage of 32 volts will pass 1.06 amps + 1% through the load resistors.

Page 3:

RF power detector circuits. Gain of power measurements will be done through software. Only the Aural Null and Offset Null need to be done through front panel pots.

NOTES:
1) ALL RESISTORS ARE 1/8 WATT UNLESS NOTED OTHERWISE.
2) ALL CAPACITORS ARE uF UNLESS NOTED OTHERWISE.
3) ALL INDUCTORS ARE uH UNLESS NOTED OTHERWISE.

APV	Axcera	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, PIONEER, AMP CTRL (1301962)			
ECO	MATERIAL -----	DWN REH 2/28/03	DWG. NO. 1301964	REV C0	
		CHK REH 3/6/03			
REV	FINISH -----	REL REH 3/6/03	D	SCALE - - -	SHEET 3 OF 3



LAST USED REF.

C64
CR4
R28
L24
J6
Q8
U4
RC4

APV	Axcera	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH., 1 WATT UHF AMPLIFIER (1302761)		
ECO	MATERIAL -----	DWN	JKF	5/12/03	DWG. NO. 1302762 REV A0
REV	FINISH -----	CHK	LRT	9/3/03	
		REL	LRT	9/3/03	D SCALE --- SHEET 1 OF 1

Maschinell erzeugt!
Nicht manuell ändern!

Schutzvermerk nach DIN 34 beachten!
NOTE: copyright protected as in DIN 34.1

OrCAD SCHEMATIC
SN79-308
SCHEMATIC1
G:\EPROI\ORCADWSP\5379308-02\SN79-308.DSN

Detektor-
ausgang
DETECTOR OUT

X801

HF-Eingang
RF INPUT

X802

C851 *** 3)
R819 3) ***
C833 *** 3)
R816 3) ***
R818 3) ***
R800 47
V800 HSMS2800
C818 10p
R810 470k
R813 100
C800 3..10p
Z801
C819 3..10p
L801 ***
C838 100p
R821 15
R822 56
R823 15
V809 BA679
C836 10n
C837 100p
C839 5,6p
C840 100p
V810 BA679
C841 100p
L802 100nH
V811 BA679
L803 100nH
C842 10p
R835 470
R836 470
C843 10p
V812 BCX56
C844 100p
HF-Schirmgehäuse
RF COVER

R826 3,3k
R827 820
R828 820
R829 820
R830 1k
C847 100n
V806 BCW60
R831 15k
V807 4448
R824 270
R825 120
R832 820
C835 470p
C848 100n
R833 15k
V808 TL431ILP
R834 1,8k
C850 ***
Z802

R805 150
R804 150
R802 150
C802 ***
C808 6,8p
C804 15p
C805 18p
V804 MRF182 **
R801 33
C801 180p
C806 10p
C807 ***
C809 6,8p
C810 10n
C811 470p
C812 180p
C813 10u
R843 ***
R803 820
V801 4448
C814 100n
C828 470p
C803 100n
X804
32V
X803
HF-Ausgang
RF OUTPUT
Z803

R807 100
R808 500
C815 100n
R809 470
R806 1,8k
C816 100n
R812 ***
V802 6,8V
R811 1,8k
C817 220u

** 1)
R814 50

R844 ***
C821 10u
R817 820
V803 4448
C820 100n
C822 180p
C823 10n
C824 470p
R820 33
C825 6,8p
C826 6,8p
C827 ***
C829 15p
C830 18p
V805 MRF182 **
C831 10p
C832 ***
C834 180p

1)
BeO
Berylliumoxid

GAIN
CONTROL

X805

R840 3,3k
R839 10k 2)
C849 100p
C845 100p
C846 100p
V813 BCW61
R841 10k
R842 470
V814 4448
R837 10k
R838 10k
"GAIN"

* gedr. Bauelement
PRINTED COMPONENT

** Montage auf Kühlkörper
MOUNTED ON HEATSINK

*** Abgleichwert
FACTORY SET VALUE

2) R839 entfällt, wenn X805 genutzt wird
R839 IS REMOVED WHEN X805 IS USED

3) C833, C851 entfallen bei Bestückung von R816, R818 u. R819
C833, C851 ARE REMOVED WHEN R816, R818, R819 ARE INSTALLED

Leiterplattenbestückung siehe
PC BOARD LAYOUT SEE
51-5379-308-00 (1)

Zust.	Änderung	Datum	Name
02	E185	26.10.98	Sche
01		8.5.98	Sche

	Datum	Name
Bearb	22.04.98	Schenk
Gepr.		
Norm.	4.3.99	Nickel

Urspr.:

TELEFUNKEN Sendertechnik

40W-Modul UHF
40W MODULE UHF

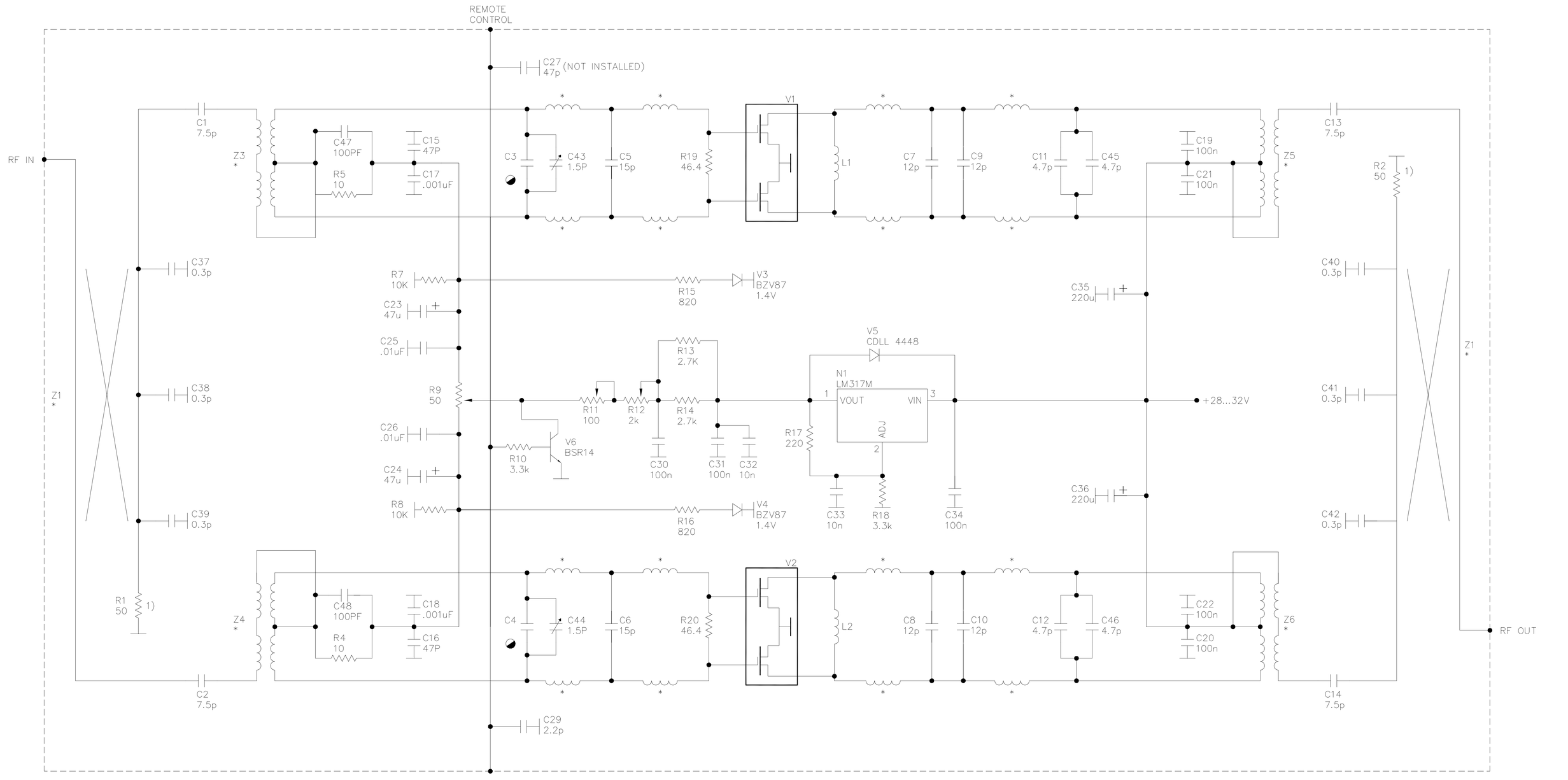
51-5379-308-00 WSP XB

Blatt 1
1 Bl.

Ers. f.:

Ers. d.:

A3L



* PRINTED COMPONENT

FACTORY SET VALUE

PC BOARD LAYOUT SEE
51-5379-309-00 (2)

REV	ECO	DATE	APV
CO	20110221	5/17/02	RE
BO	20100316	04/02/02	LRT

DELETED PTF10159 P/N FROM LDMOS. ADDED C23,C24 & C27. CDD/CR

R15 AND R16 WERE 680 OHMS. PWN

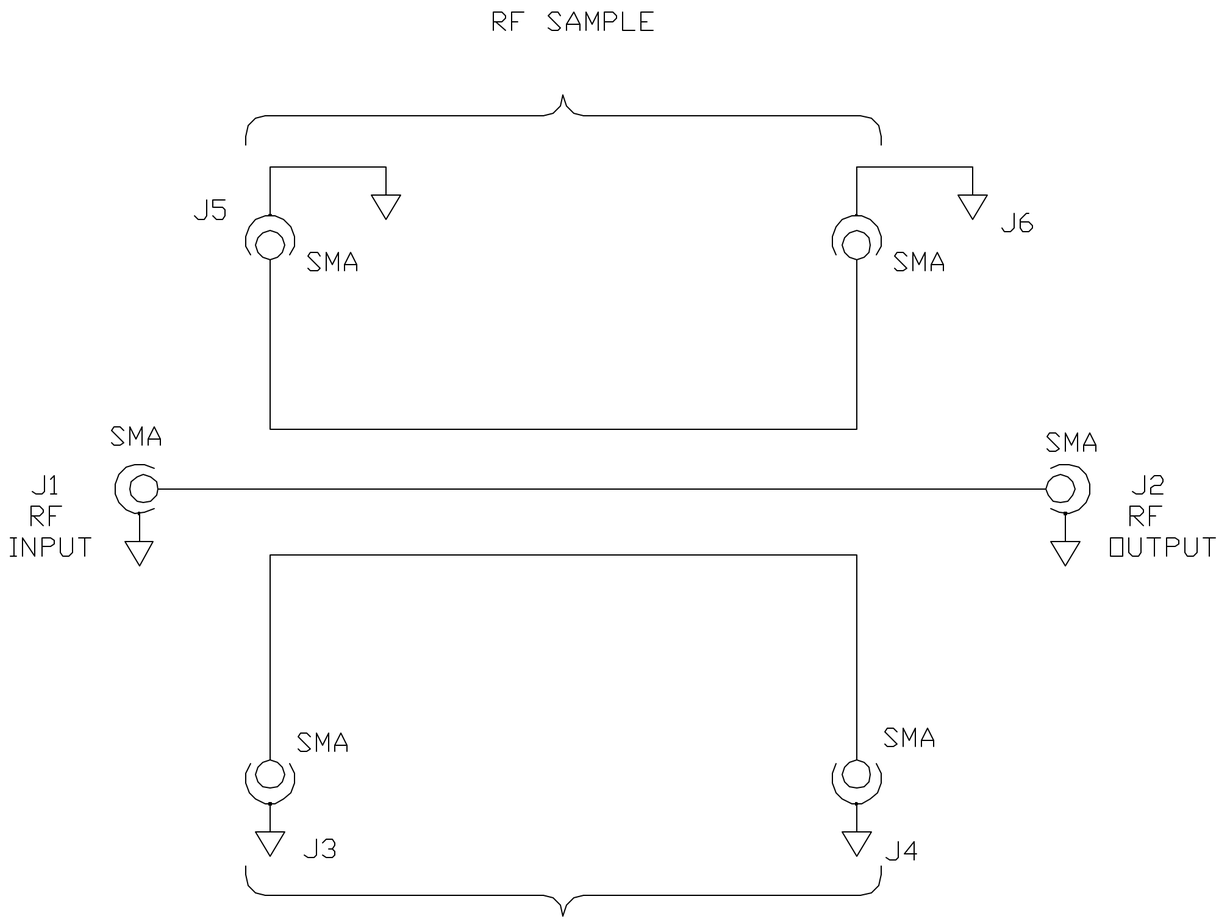
REV	ECO	DESCRIPTION	BY
D0	20110444	CHANGE R3 FROM A 2.2 OHM RESISTOR TO C47, SM., CAP., 100PF, 500WVDC. CHANGE R6 FROM A 2.2 OHM RESISTOR TO C48, SM., CAP., 100PF, 500WVDC. CHANGE R4 FROM A 2.2 OHM RESISTOR TO 1590600OSMT, SM., RES., 10 OHM 5% 1/8W. CHANGE R5 FROM A 2.2 OHM RESISTOR TO 1590600OSMT, SM., RES., 10 OHM 5% 1/8W. CHANGE C17 FROM A 47PF CAP, FIXED CERAMIC, 47 PF TO 1590616OSMT, SM., CAP., .001 UF, 50 WVDC. CHANGE C18 FROM A 47PF CAP, FIXED CERAMIC, 47 PF TO 1590616OSMT, SM., CAP., .001 UF, 50 WVDC. ADD C23, 1301246, SM. CAP, 47MF, 50V, LOW ESR. ADD C24, 1301246, SM. CAP, 47MF, 50V, LOW ESR. ADD C25, 1590616ISMT, SM., CAP., .01 UF, 50 WVDC. ADD C26, 1590616ISMT, SM., CAP., .01 UF, 50 WVDC. PWN	RJ 04/18/02

MATERIAL

FINISH

TITLE AMPLIFIER MODULE

DWN	PWN	04/01/02	DWG. NO. 51-5379-309-00 WSP
CHK	LRT	04/03/02	REV D0
REL	LRT	04/03/02	SCALE D SHEET 1 OF 1



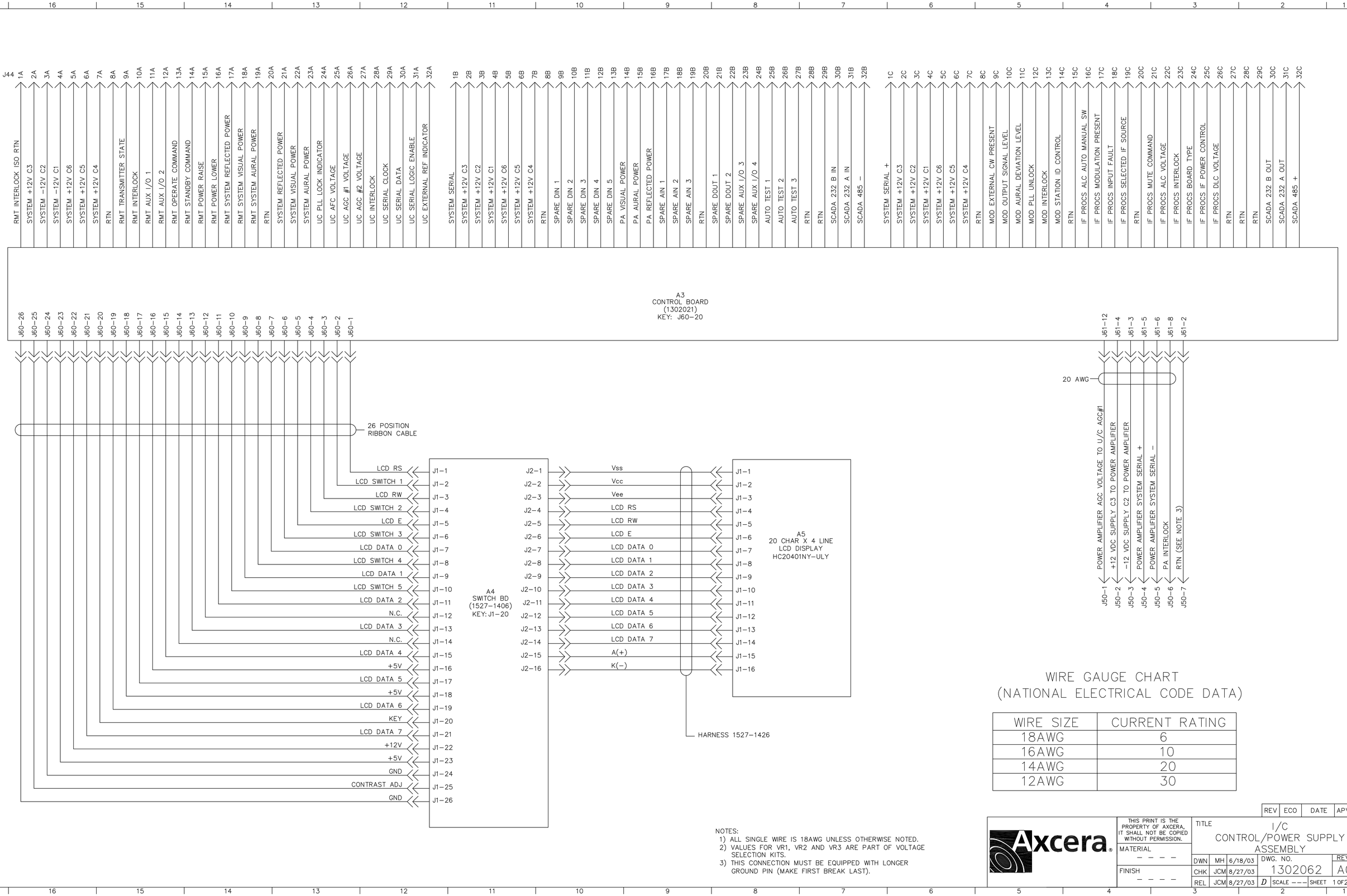
REV	ECO	DATE	APV

MATERIAL — — — —

FINISH — — — —

TITLE
SCHEMATIC
DIRECTIONAL COUPLER
BOARD

DWN	MH	8/11/03	DWG. NO. 1303152	REV A0
CHK	JCM	8/25/03		
REL	JCM	8/25/03	B SCALE — — —	SHEET 1 OF 1



WIRE GAUGE CHART
(NATIONAL ELECTRICAL CODE DATA)

WIRE SIZE	CURRENT RATING
18AWG	6
16AWG	10
14AWG	20
12AWG	30

NOTES:
1) ALL SINGLE WIRE IS 18AWG UNLESS OTHERWISE NOTED.
2) VALUES FOR VR1, VR2 AND VR3 ARE PART OF VOLTAGE SELECTION KITS.
3) THIS CONNECTION MUST BE EQUIPPED WITH LONGER GROUND PIN (MAKE FIRST BREAK LAST).

REV	ECO	DATE	APV

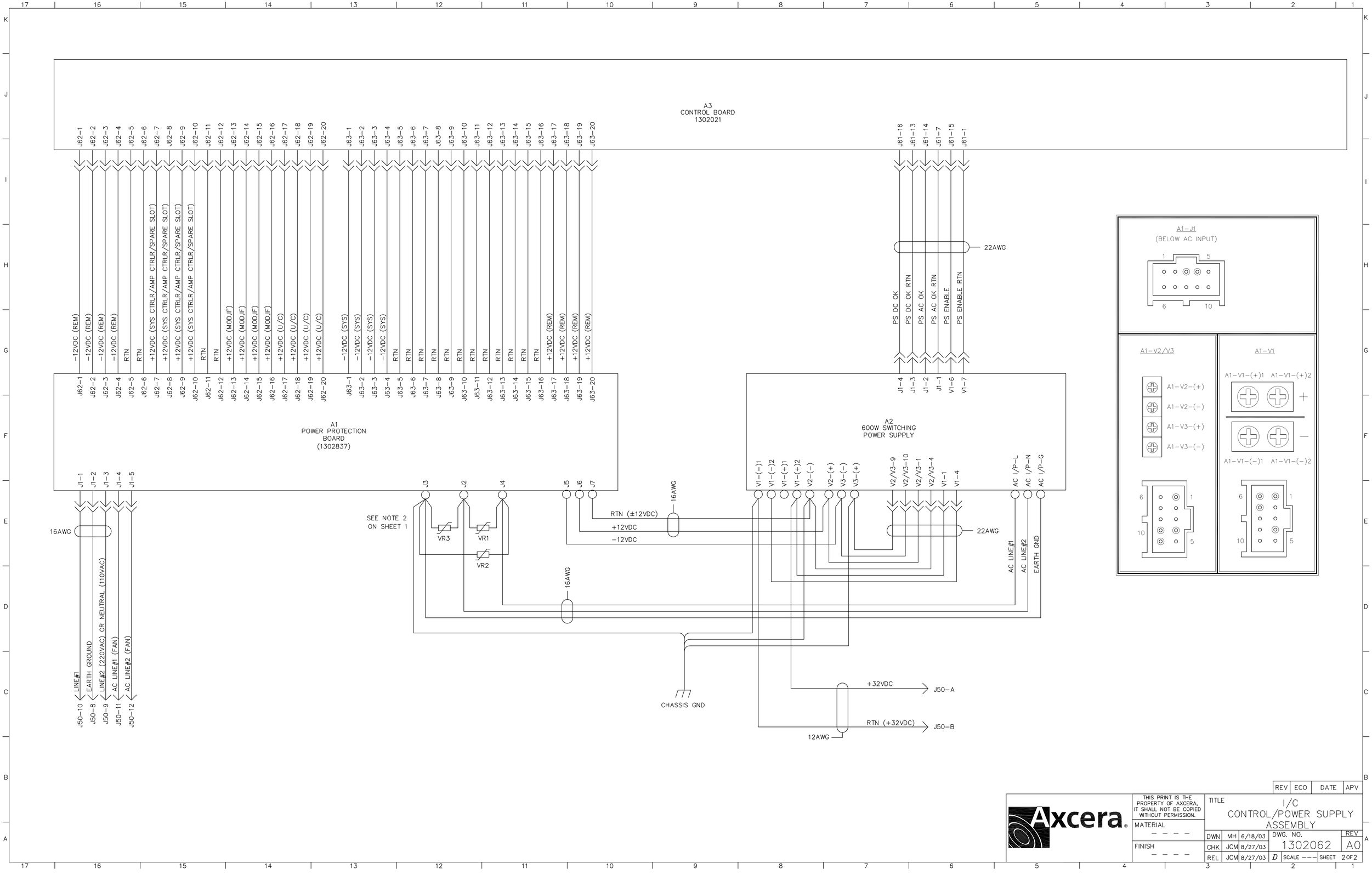
Axcera®

MATERIAL — — — —

FINISH — — — —

TITLE I/C CONTROL/POWER SUPPLY ASSEMBLY

DWN	MH	6/18/03	DWG. NO. 1302062	REV A0
CHK	JCM	8/27/03		
REL	JCM	8/27/03	D SCALE — — —	SHEET 1 OF 2



REV	ECO	DATE	APV

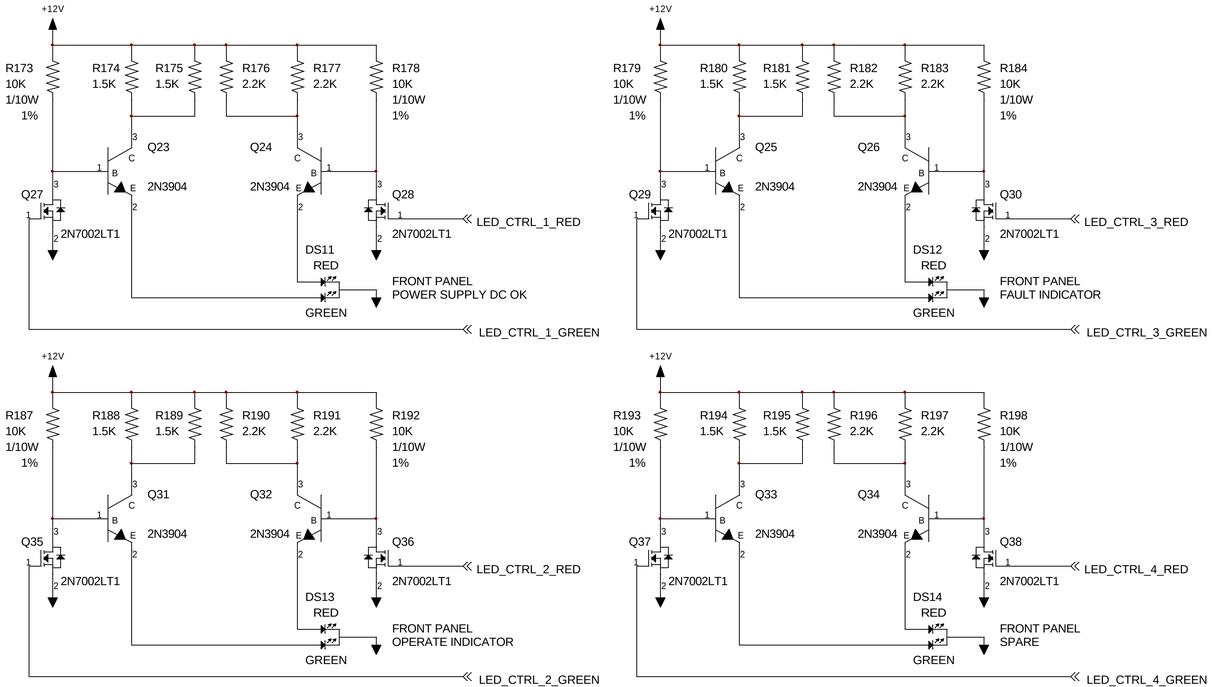
Axcera®

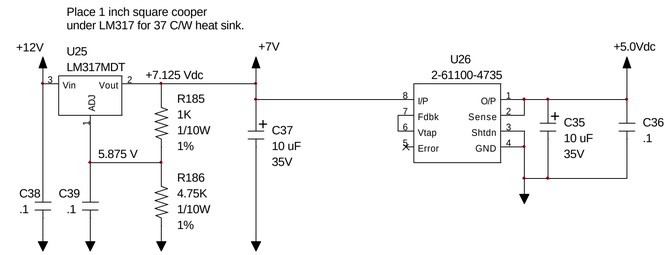
MATERIAL – – – –

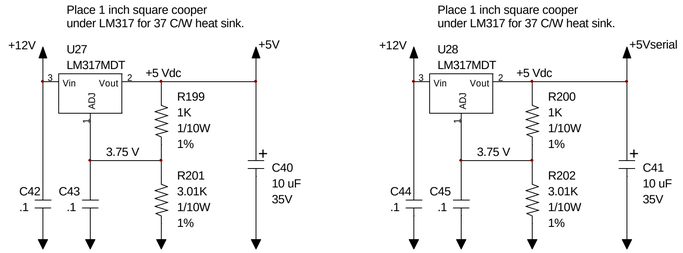
FINISH – – – –

TITLE I/C CONTROL/POWER SUPPLY ASSEMBLY

DWN	MH	6/18/03	DWG. NO. 1302062	REV A0
CHK	JCM	8/27/03		
REL	JCM	8/27/03	D SCALE – – –	SHEET 2 OF 2







Circuit Descriptions:

PAGE 1:

U1 is an Atmel Atmega128 microcontroller. This part is in-circuit programmed using the serial programming port. When the microcontroller is held in reset by either the programming port or the external watchdog IC, a transistor inverts the reset signal while serial programming lines are connected to U1 through analog switch U5.

U2 is a watchdog IC used to hold the microcontroller in reset if the supply voltage is less than 4.21 Vdc; (1.25 Vdc < Pin 4 (IN) < Pin 2 (Vcc)). The watchdog momentarily resets the microcontroller if Pin 6 (!ST) is not clocked every second. A manual reset switch is provided but should not be needed.

Diodes DS1 through DS8 are used for display of auto test results. A test board is used to execute self test routines. When the test board is installed, Auto_Test_1 is held low and Auto_Test_2 is allowed to float at 5 Vdc. This is the signal to start the auto test routines.

U3 and U4 are used to selectively enable various input and output ICs found on page 2 and 3 of the schematic.

U1 has two serial ports available. In this application, one port is used to communicate with transmitter system components where U1 is the master of a RS-485 serial bus. The other serial port is used to provide serial data I/O where U1 is not the master of the data port. A dual RS-232 port driver IC and a RS-485 port driver is also in the second serial data I/O system. The serial ports are wired such that serial data input can come through one of the three serial port channels. Data output is sent out through each of the three serial port channels.

Switch SW1 is used to select either transmitter operation or exciter driver operation. When the switches of SW1 are on, transmitter operation is selected and the power monitoring lines of the transmitter's power amplifier are routed to the system power monitoring lines.

PAGE 2:

Digital output latches are used to control system devices. Remote output circuits are implemented using open drain FETs with greater than 60 Volt drain to source voltage ratings.

Remote digital inputs are diode protected with a 1 Kohm pull-up resistor to 5Vdc. If the remote input voltage is greater than about 2 volts or floating, a FET is turned on and a logic low is applied to the digital input buffer. If the remote input voltage is less than the turn on threshold of the FET (about 2 Vdc), a logic high is applied to the digital input buffer.

Four of the circuits on page two are auxiliary I/O connections wired for future use. They are wired similar to the remote digital inputs but include a FET for digital output operation. To operate these signals as an input, the associated output FET must be turned off. These circuits are also connected to an analog input multiplexer IC.

PAGE 3:

Several ICs are used as input buffers to allow the microcontroller to monitor various digital input values. Most digital inputs use a 10 Kohm pull-up resistor. The buffer IC used for data transfer to the display is wired for read and write control.

PAGE 4:

Each analog input is expected to be between 0 and 5 Vdc. If a signal exceeds 5.1 Vdc, a 0.225 Watt zenor diode clamps the signals voltage. Most signals are calibrated at their source however two dual serial potentiometer ICs are used to calibrate four signals. For these four circuits, the input value is divided in half before it is applied to an op-amp. The serial potentiometer is used to adjust the input signal between 80 and 120% of the input signal. Serial data to the second serial potentiometer is transferred through the first IC.

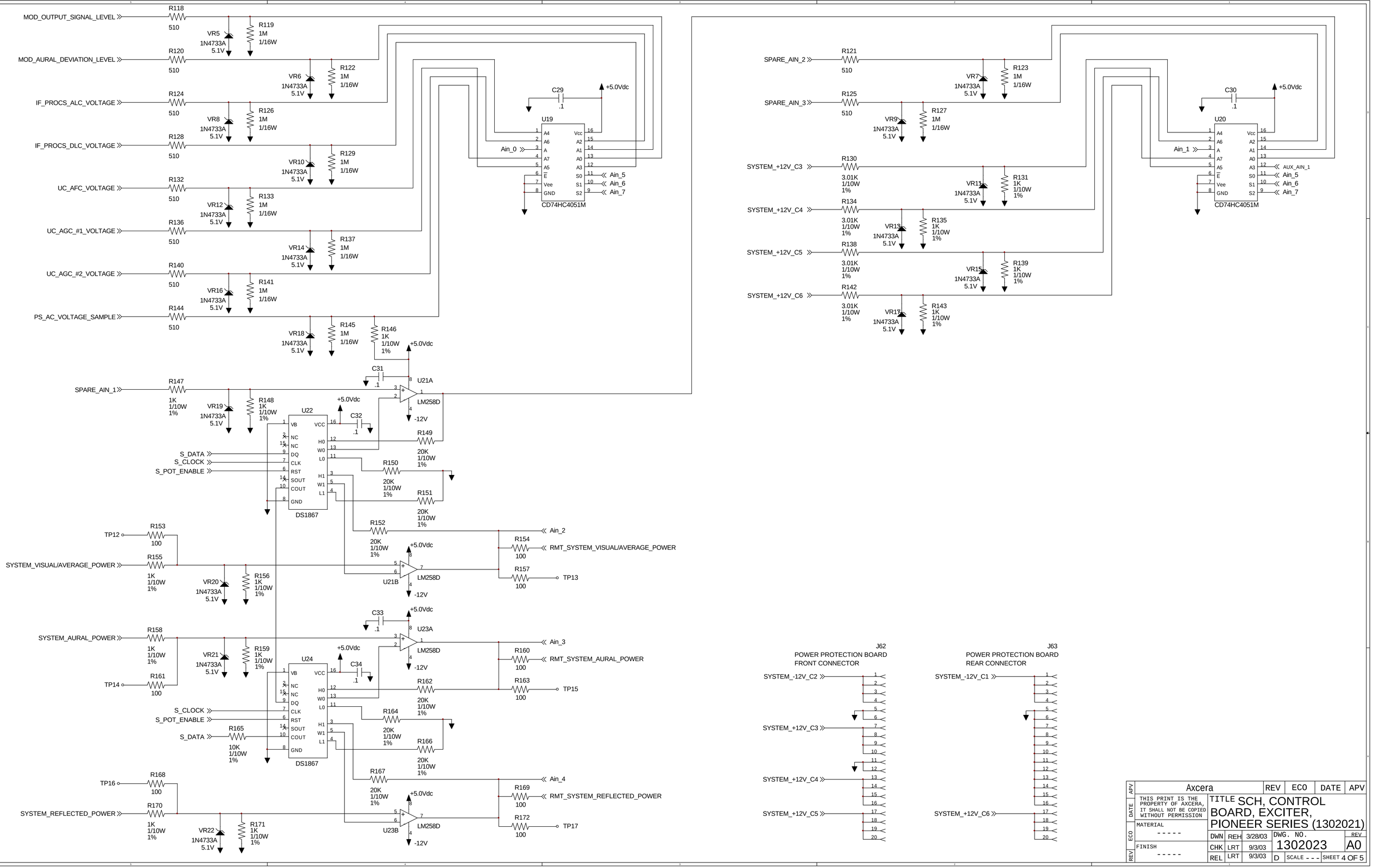
Two 20 position connectors are used to provide power to the backplane. J62 and J63 get power from the power supply after a nominal 3 amp resettable fuse. The Raychem polyswitch resettable fuses may open on a current as low as 2.43 amps at 50C, 3 amps at 25 C or 3.3 amps at 0C. They definately will open when the current is 4.86 amps at 50C, 6 amps at 20C, or 6.6 amps at 0C. Trace widths of these circuits are 0.140" (designed for maximum current).

PAGE 5:

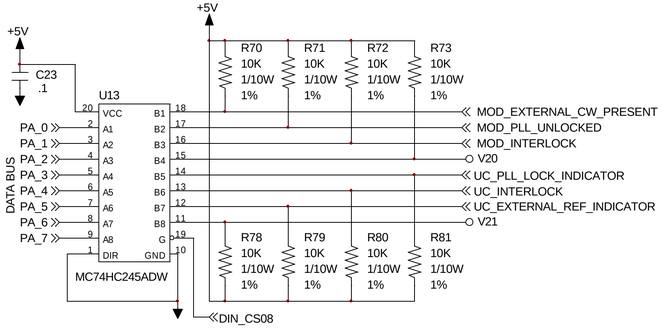
Each of the four LED circuits drive a dual element common cathode LED. To make a good amber color, the current applied to the green element is slightly greater than the red element.

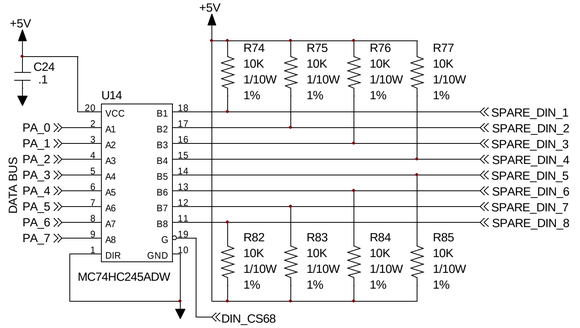
Several voltage regulators are used to power the board. Seven volts is typically applied to board LEDs and to the input of a precision 5.0 volt regulator. The 5.0 volt regulator is used for analog circuits and the microcontroller analog reference voltage. Another two 5 volt regulator circuits are used for most other board circuits.

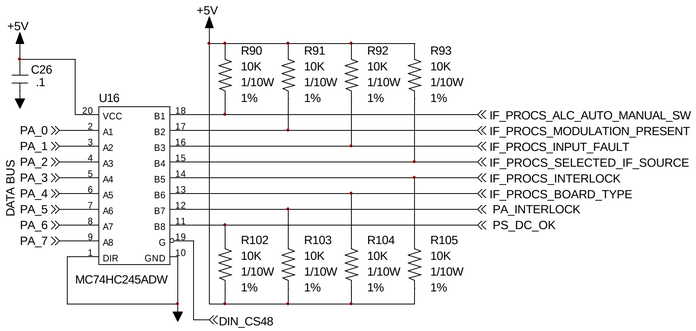
APV	Axcera	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)			
ECO	MATERIAL -----	DWN REH 3/28/03	DWG. NO. 1302023	REV A0	
REV	FINISH -----	CHK LRT 9/3/03			
		REL LRT 9/3/03	D	SCALE ---	SHEET 5 OF 5

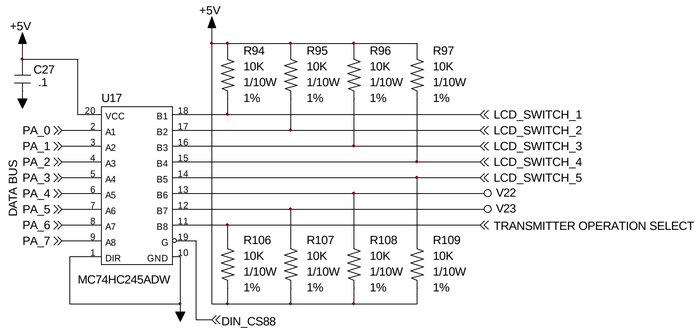


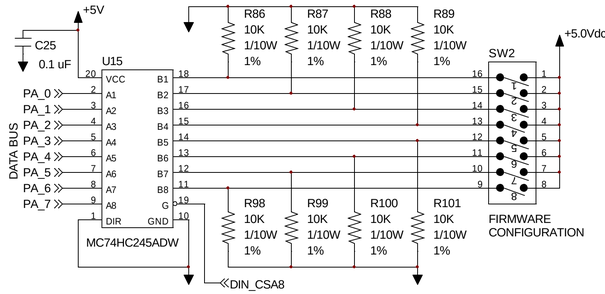
Axcera	REV	ECO	DATE	APV	
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)				
MATERIAL -----	DWN	REH	3/28/03	DWG. NO. 1302023	REV A0
FINISH -----	CHK	LRT	9/3/03		
	REL	LRT	9/3/03	D	SCALE - - - SHEET 4 OF 5

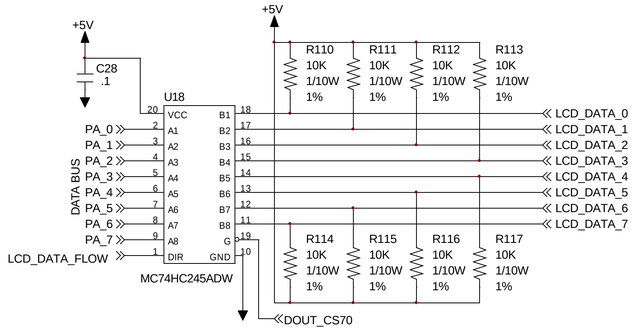




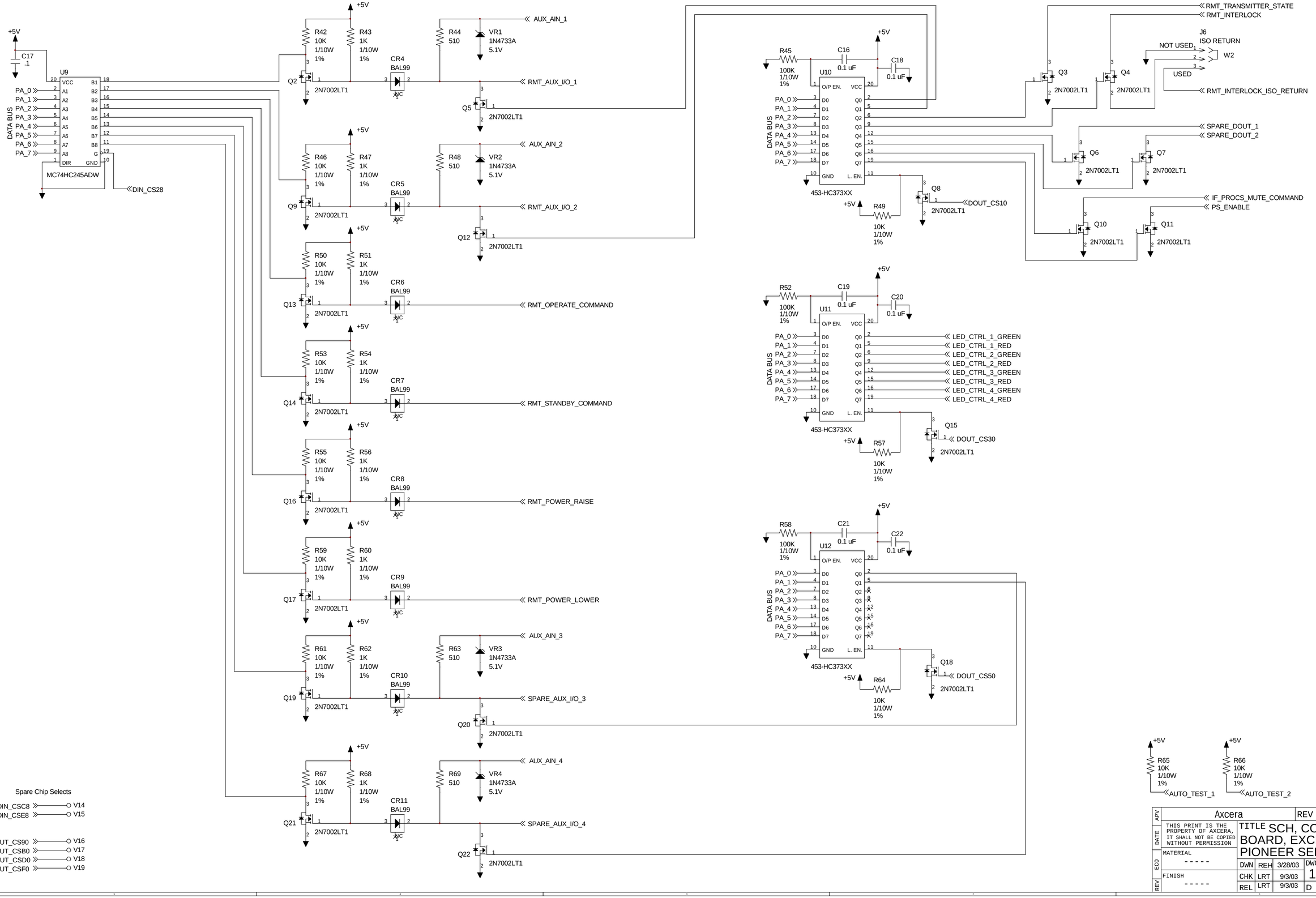




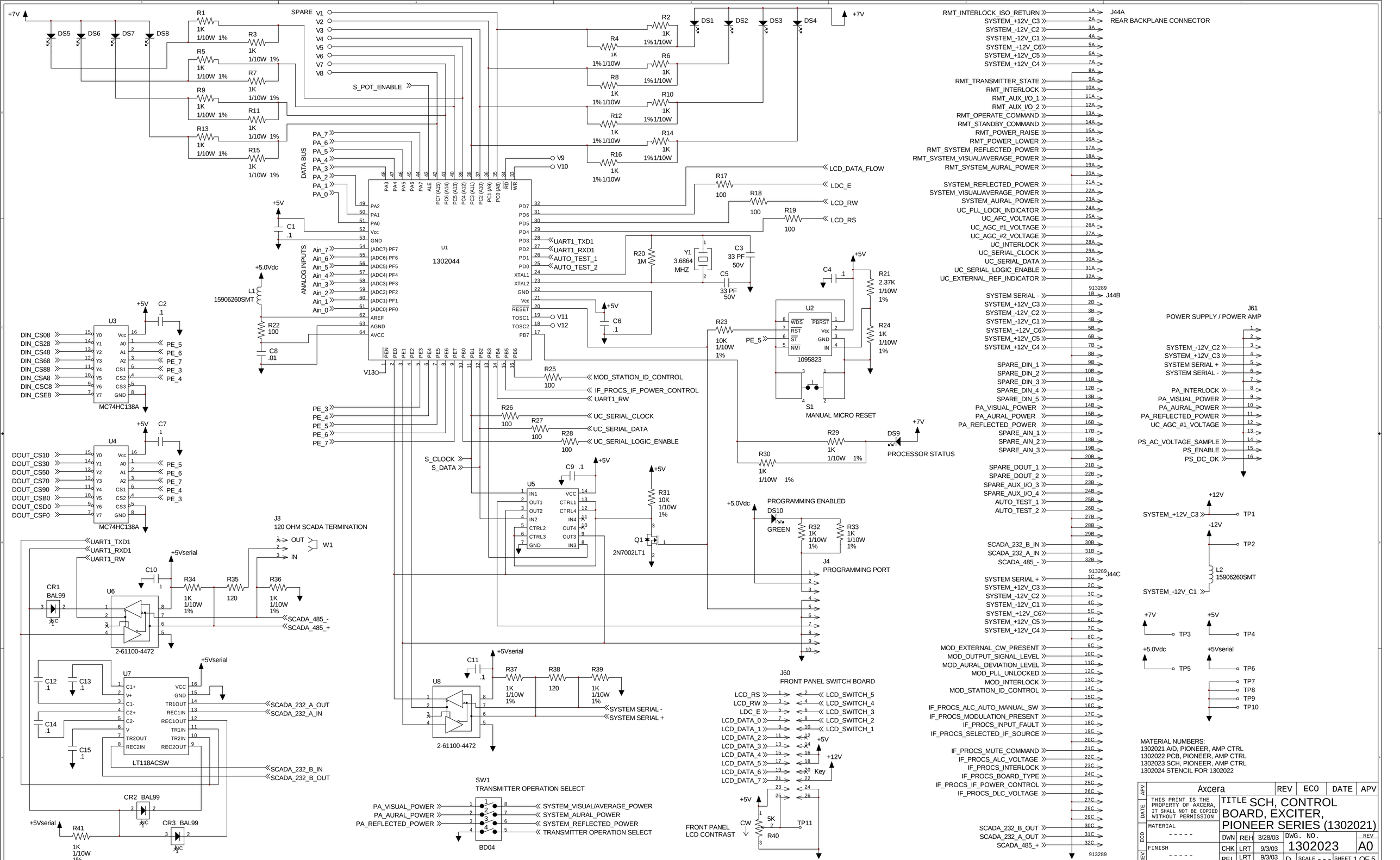




APV	Axcera	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)		
ECO	MATERIAL -----	DWN	REH	3/28/03	DWG. NO. 1302023 REV A0
REV	FINISH -----	CHK	LRT	9/3/03	
		REL	LRT	9/3/03	D SCALE - - - SHEET 3 OF 5



APV	Axcera	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)		
ECO	MATERIAL -----	DWN	REH	3/28/03	DWG. NO. 1302023 REV A0
		CHK	LRT	9/3/03	
REV	FINISH -----	REL	LRT	9/3/03	D SCALE --- SHEET 2 OF 5


+7V
DS5
DS6
DS7
DS8
R1
1K
1/10W 1%
R3
R5
R7
R9
R11
R13
R15
SPARE
V1
V2
V3
V4
V5
V6
V7
V8
S_POT_ENABLE
R2
R4
R6
R8
R10
R12
R14
R16
DS1
DS2
DS3
DS4
DATA BUS
PA_7
PA_6
PA_5
PA_4
PA_3
PA_2
PA_1
PA_0
V9
V10
LCD_DATA_FLOW
LDC_E
LCD_RW
LCD_RS
R17
R18
R19
100
+5V
C1
.1
U1
1302044
ANALOG INPUTS
Ain_7
Ain_6
Ain_5
Ain_4
Ain_3
Ain_2
Ain_1
Ain_0
UART1_TXD1
UART1_RXD1
AUTO_TEST_1
AUTO_TEST_2
R20
1M
Y1
3.6864
MHZ
C3
33 PF
50V
C5
33 PF
50V
+5.0Vdc
L1
15906260SMT
R22
100
C8
.01
C6
.1
V11
V12
V13
C4
.1
R21
2.37K
1/10W
1%
R24
1K
1/10W
1%
R23
10K
1/10W
1%
PE_5
U2
WDS
PBRST
RST
Vcc
ST
GND
NMI
IN
1095823
S1
MANUAL MICRO RESET
R25
100
MOD_STATION_ID_CONTROL
IF_PROCS_IF_POWER_CONTROL
UART1_RW
PE_3
PE_4
PE_5
PE_6
PE_7
R26
R27
R28
UC_SERIAL_CLOCK
UC_SERIAL_DATA
UC_SERIAL_LOGIC_ENABLE
S_CLOCK
S_DATA
C9
.1
U5
R31
10K
1/10W
1%
Q1
2N7002LT1
R29
1K
1/10W
1%
R30
1K
1/10W
1%
DS9
PROCESSOR STATUS
+7V
PROGRAMMING ENABLED
DS10
GREEN
R32
1K
1/10W
1%
R33
1K
1/10W
1%
J4
PROGRAMMING PORT
J3
120 OHM SCADA TERMINATION
OUT
IN
W1
UART1_TXD1
UART1_RXD1
UART1_RW
+5Vserial
C10
.1
R34
1K
1/10W
1%
R35
120
R36
1K
1/10W
1%
CR1
BAL99
U6
2-61100-4472
SCADA_485_-
SCADA_485_+
C11
.1
R37
1K
1/10W
1%
R38
120
R39
1K
1/10W
1%
U8
2-61100-4472
SYSTEM SERIAL -
SYSTEM SERIAL +
C12
.1
C13
.1
C14
.1
C15
.1
U7
LT118ACSW
SCADA_232_A_OUT
SCADA_232_A_IN
SCADA_232_B_IN
SCADA_232_B_OUT
CR2 BAL99
CR3 BAL99
R41
1K
1/10W
1%
U3
MC74HC138A
DIN_CS08
DIN_CS28
DIN_CS48
DIN_CS68
DIN_CS88
DIN_CSA8
DIN_CSC8
DIN_CSE8
PE_5
PE_6
PE_7
PE_4
PE_3
C2
.1
U4
MC74HC138A
DOUT_CS10
DOUT_CS30
DOUT_CS50
DOUT_CS70
DOUT_CS90
DOUT_CSB0
DOUT_CSD0
DOUT_CSF0
C7
.1
J60
FRONT PANEL SWITCH BOARD
LCD_RS
LCD_RW
LDC_E
LCD_DATA_0
LCD_DATA_1
LCD_DATA_2
LCD_DATA_3
LCD_DATA_4
LCD_DATA_5
LCD_DATA_6
LCD_DATA_7
LCD_SWITCH_5
LCD_SWITCH_4
LCD_SWITCH_3
LCD_SWITCH_2
LCD_SWITCH_1
Key
+12V
FRONT PANEL
LCD CONTRAST
CW
5K
R40
TP11
SW1
TRANSMITTER OPERATION SELECT
PA_VISUAL_POWER
PA_AURAL_POWER
PA_REFLECTED_POWER
SYSTEM_VISUAL/AVERAGE_POWER
SYSTEM_AURAL_POWER
SYSTEM_REFLECTED_POWER
TRANSMITTER OPERATION SELECT
BD04
J44A
REAR BACKPLANE CONNECTOR
RMT_INTERLOCK_ISO_RETURN
SYSTEM_+12V_C3
SYSTEM_-12V_C2
SYSTEM_-12V_C1
SYSTEM_+12V_C6
SYSTEM_+12V_C5
SYSTEM_+12V_C4
RMT_TRANSMITTER_STATE
RMT_INTERLOCK
RMT_AUX_I/O_1
RMT_AUX_I/O_2
RMT_OPERATE_COMMAND
RMT_STANDBY_COMMAND
RMT_POWER_RAISE
RMT_POWER_LOWER
RMT_SYSTEM_REFLECTED_POWER
RMT_SYSTEM_VISUAL/AVERAGE_POWER
RMT_SYSTEM_AURAL_POWER
SYSTEM_REFLECTED_POWER
SYSTEM_VISUAL/AVERAGE_POWER
SYSTEM_AURAL_POWER
UC_PLL_LOCK_INDICATOR
UC_AFC_VOLTAGE
UC_AGC_#1_VOLTAGE
UC_AGC_#2_VOLTAGE
UC_INTERLOCK
UC_SERIAL_CLOCK
UC_SERIAL_DATA
UC_SERIAL_LOGIC_ENABLE
UC_EXTERNAL_REF_INDICATOR
913289
J44B
SYSTEM SERIAL -
SYSTEM_+12V_C3
SYSTEM_-12V_C2
SYSTEM_-12V_C1
SYSTEM_+12V_C6
SYSTEM_+12V_C5
SYSTEM_+12V_C4
SPARE_DIN_1
SPARE_DIN_2
SPARE_DIN_3
SPARE_DIN_4
SPARE_DIN_5
PA_VISUAL_POWER
PA_AURAL_POWER
PA_REFLECTED_POWER
SPARE_AIN_1
SPARE_AIN_2
SPARE_AIN_3
SPARE_DOUT_1
SPARE_DOUT_2
SPARE_AUX_I/O_3
SPARE_AUX_I/O_4
AUTO_TEST_1
AUTO_TEST_2
SCADA_232_B_IN
SCADA_232_A_IN
SCADA_485_-
913289
J44C
SYSTEM SERIAL +
SYSTEM_+12V_C3
SYSTEM_-12V_C2
SYSTEM_-12V_C1
SYSTEM_+12V_C6
SYSTEM_+12V_C5
SYSTEM_+12V_C4
MOD_EXTERNAL_CW_PRESENT
MOD_OUTPUT_SIGNAL_LEVEL
MOD_AURAL_DEVIATION_LEVEL
MOD_PLL_UNLOCKED
MOD_INTERLOCK
MOD_STATION_ID_CONTROL
IF_PROCS_ALC_AUTO_MANUAL_SW
IF_PROCS_MODULATION_PRESENT
IF_PROCS_INPUT_FAULT
IF_PROCS_SELECTED_IF_SOURCE
IF_PROCS_MUTE_COMMAND
IF_PROCS_ALC_VOLTAGE
IF_PROCS_INTERLOCK
IF_PROCS_BOARD_TYPE
IF_PROCS_IF_POWER_CONTROL
IF_PROCS_DLC_VOLTAGE
SCADA_232_B_OUT
SCADA_232_A_OUT
SCADA_485_+
913289
J61
POWER SUPPLY / POWER AMP
SYSTEM_-12V_C2
SYSTEM_+12V_C3
SYSTEM SERIAL +
SYSTEM SERIAL -
PA_INTERLOCK
PA_VISUAL_POWER
PA_AURAL_POWER
PA_REFLECTED_POWER
UC_AGC_#1_VOLTAGE
PS_AC_VOLTAGE_SAMPLE
PS_ENABLE
PS_DC_OK
+12V
SYSTEM_+12V_C3
TP1
-12V
TP2
L2
15906260SMT
SYSTEM_-12V_C1
+7V
TP3
+5V
TP4
+5.0Vdc
TP5
+5Vserial
TP6
TP7
TP8
TP9
TP10
MATERIAL NUMBERS:
1302021 A/D, PIONEER, AMP CTRL
1302022 PCB, PIONEER, AMP CTRL
1302023 SCH, PIONEER, AMP CTRL
1302024 STENCIL FOR 1302022
Axcera
REV
ECO
DATE
APV
THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION
MATERIAL
FINISH
TITLE SCH, CONTROL BOARD, EXCITER, PIONEER SERIES (1302021)
DWN REH 3/28/03
CHK LRT 9/3/03
REL LRT 9/3/03
DWG. NO. 1302023
REV A0
D
SCALE - - -
SHEET 1 OF 5

J40A Spare Slot

J40B
V4001 V4003 V4005 V4007 V4009

J40C
RMT_SPARE_1
RMT_SPARE_2
SPARE_DOUT_1
SPARE_DOUT_2
SPARE_DIN_1
SPARE_DIN_2
SPARE_DIN_3
SPARE_DIN_4
SPARE_DIN_5
SPARE_AIN_1
SPARE_AIN_2
SPARE_AIN_3
System_+12Vdc_C3
System_-12Vdc_C1
System_Serial+
System_Serial-

913642

J41A Modulator
MOD_EXTERNAL_CW_PRESENT
MOD_OUTPUT_SIGNAL_LEVEL
MOD_AURAL_DEVIATION_LEVEL
MOD_INTERLOCK
MOD_BASEBAND_AUDIO(+)
MOD_BASEBAND_AUDIO(-)
MOD_COMPOSITE_AUDIO(-)
MOD_COMPOSITE_AUDIO(+)
MOD_SAP/PRO_AUDIO(+)
MOD_SAP/PRO_AUDIO(-)
MOD_VIDEO(-)
MOD_VIDEO(+)
MOD_STATION_ID_CONTROL
System_+12Vdc_C4
System_-12Vdc_C1
SPARE_AUX_I/O_3
SPARE_AUX_I/O_4
MOD_CW_IF_INPUT
MOD_PLL_UNLOCKED

J41B
System_+12Vdc_C3
System_-12Vdc_C1

J41C
MOD_VISUAL_IF_INPUT
MOD_AURAL_IF_OUTPUT
MOD_VISUAL_IF_OUTPUT
MOD_AURAL_IF_INPUT
System_+12Vdc_C4
System_-12Vdc_C1
MOD_COMBINED_IF_OUTPUT
MOD_10_MHz_INPUT

913642

J42A IF Processor

J42B
System_+12Vdc_C4
System_-12Vdc_C1
SPARE_AUX_I/O_3
SPARE_AUX_I/O_4
System_+12Vdc_C4
System_-12Vdc_C1

J42C
MOD_COMBINED_IF_OUTPUT
IF_PROCS_IF_2_UC
V4204
IF_PROCS_ALC_AUTO_MANUAL_SW
IF_PROCS_MODULATION_PRESENT
IF_PROCS_INPUT_FAULT
IF_PROCS_SELECTED_IF_SOURCE
IF_PROCS_MUTE_COMMAND
IF_PROCS_ALC_VOLTAGE
IF_PROCS_INTERLOCK
IF_PROCS_BOARD_TYPE
IF_PROCS_IF_SIGNAL_SELECT
System_+12Vdc_C4
System_-12Vdc_C1
IF_PROCS_MODULATED IF INPUT
IF_PROCS_IF_POWER_CTRL
IF_PROCS_DLC_VOLTAGE

913642

J43 Upconverter
IF_PROCS_IF_2_UC
unused
unused
unused
UC_AFC_VOLTAGE
SPARE_AUX_I/O_3
SPARE_AUX_I/O_4
UC_EXTERNAL_REF_INDICATOR
UC_AGC_#1_VOLTAGE
UC_PLL_LOCK_INDICATOR
UC_AGC_#2_VOLTAGE
IF_PROCS_ALC_VOLTAGE
UC_INTERLOCK
UC_SERIAL_CLOCK
UC_SERIAL_DATA
UC_SERIAL_LOGIC_ENABLE
System_+12Vdc_C5
System_+12Vdc_C5
System_+12Vdc_C5
System_-12Vdc_C1
System_-12Vdc_C1
System_-12Vdc_C1
System_Serial+
System_Serial-
EXT_10_MHz INPUT
UC_RF_OUTPUT
SYSTEM_10_MHz_OUTPUT
MOD_10_MHz_INPUT

J44A Control
RMT_INTERLOCK_ISOLATED_RTN
System_+12Vdc_C3
System_-12Vdc_C2
System_-12Vdc_C1
System_+12Vdc_C6
System_+12Vdc_C5
System_+12Vdc_C4
RMT_TRANSMITTER_STATE
RMT_INTERLOCK
RMT_AUX_I/O_1
RMT_AUX_I/O_2
RMT_SET_TO_OPERATE_CMD
RMT_SET_TO_STAND-BY_CMD
RMT_POWER_RAISE
RMT_POWER_LOWER
RMT_SYSTEM_REFLECTED_PWR
RMT_SYSTEM_VISUAL_PWR
RMT_SYSTEM_AURAL_PWR
SYSTEM_REFLECTED_PWR
SYSTEM_VISUAL_PWR
SYSTEM_AURAL_PWR
UC_PLL_LOCK_INDICATOR
UC_AFC_VOLTAGE
UC_AGC_#1_VOLTAGE
UC_AGC_#2_VOLTAGE
UC_INTERLOCK
UC_SERIAL_CLOCK
UC_SERIAL_DATA
UC_SERIAL_LOGIC_ENABLE
UC_EXTERNAL_REF_INDICATOR

J44B
SPARE_TBD_DIN_[1:8]
System_Serial-
System_+12Vdc_C3
System_-12Vdc_C2
System_-12Vdc_C1
System_+12Vdc_C6
System_+12Vdc_C5
System_+12Vdc_C4
SPARE_DIN_1
SPARE_DIN_2
SPARE_DIN_3
SPARE_DIN_4
SPARE_DIN_5
PA_VISUAL_POWER
PA_AURAL_POWER
PA_REFLECTED_POWER
SPARE_AIN_1
SPARE_AIN_2
SPARE_AIN_3
SPARE_DOUT_1
SPARE_DOUT_2
SPARE_AUX_I/O_3
SPARE_AUX_I/O_4
Auto_Test_1
Auto_Test_2

J44C
SCADA_232_B_IN
SCADA_232_A_IN
SCADA_485-
System_Serial+
System_+12Vdc_C3
System_-12Vdc_C2
System_-12Vdc_C1
System_+12Vdc_C6
System_+12Vdc_C5
System_+12Vdc_C4
MOD_EXTERNAL_CW_PRESENT
MOD_OUTPUT_SIGNAL_LEVEL
MOD_AURAL_DEVIATION_LEVEL
MOD_PLL_UNLOCKED
MOD_INTERLOCK
MOD_STATION_ID_CONTROL
IF_PROCS_ALC_AUTO_MANUAL_SW
IF_PROCS_MODULATION_PRESENT
IF_PROCS_INPUT_FAULT
IF_PROCS_SELECTED_IF_SOURCE
IF_PROCS_MUTE_COMMAND
IF_PROCS_ALC_VOLTAGE
IF_PROCS_INTERLOCK
IF_PROCS_BOARD_TYPE
IF_PROCS_IF_POWER_CTRL
IF_PROCS_DLC_VOLTAGE
SCADA_232_B_OUT
SCADA_232_A_OUT
SCADA_485+

TB02 BASE BAND AUDIO
MOD_BASEBAND_AUDIO(+)
MOD_BASEBAND_AUDIO(-)
MOD_COMPOSITE_AUDIO(+)
MOD_COMPOSITE_AUDIO(-)
MOD_SAP/PRO_AUDIO(+)
MOD_SAP/PRO_AUDIO(-)
MOD_VIDEO(+)
MOD_VIDEO(-)
MOD_VISUAL_IF_INPUT
MOD_AURAL_IF_INPUT
MOD_CW_IF_INPUT
IF_PROCS_MODULATED IF INPUT
EXT_10_MHz INPUT
SYSTEM_10_MHz_OUTPUT
MOD_VISUAL_IF_OUTPUT
MOD_AURAL_IF_OUTPUT
UC_RF_OUTPUT

J3 BNC COMPOSITE AUDIO
J4 BNC SAP/PRO AUDIO
J7 BNC VIDEO INPUT
J17 BNC VIDEO LOOP-THRU
J18 BNC VISUAL IF LOOP-THRU INPUT
J19 BNC AURAL IF LOOP-THRU INPUT
J5 BNC CW IF INPUT
J6 BNC MODULATED IF INPUT
J11 BNC SYSTEM 10 MHz OUTPUT
L1 .27uH
C1 .001
J10 BNC EXTERNAL 10 MHz INPUT
J8 BNC VISUAL IF LOOP-THRU OUTPUT
J9 BNC AURAL IF LOOP-THRU OUTPUT
J23 BNC UPCONVERTER RF OUTPUT

C2 .01 C3 .01 C4 .01 C5 .01 C6 .01 C7 .01 C8 .01 C9 .01
C10 .01 C11 .01 C12 .01 C13 .01 C14 .01
C15 .01 C16 .01 C17 .01 C18 .01 C19 .01 C20 .01 C21 .01 C22 .01 C23 .01 C24 .01

TB30
RMT_TRANSMITTER_STATE
RMT_INTERLOCK
RMT_INTERLOCK_ISOLATED_RTN
RMT_AUX_I/O_1
RMT_AUX_I/O_2
RMT_SET_TO_OPERATE_CMD
RMT_SET_TO_STAND-BY_CMD
RMT_POWER_RAISE
RMT_POWER_LOWER
RMT_SYSTEM_REFLECTED_PWR
RMT_SYSTEM_VISUAL_PWR
RMT_SYSTEM_AURAL_PWR
RMT_SPARE_1
RMT_SPARE_2
System_+12Vdc_C6
System_-12Vdc_C2
KEY
KEY

TB31
KEY
KEY

IF_PROCS_IF_SIGNAL_SELECT
IF_PROCS_DLC_VOLTAGE
UC_AGC_#2_VOLTAGE
SYSTEM_REFLECTED_PWR
SYSTEM_VISUAL_PWR
SYSTEM_AURAL_PWR
System_+12Vdc_C6
System_-12Vdc_C2

J32 SCADA (Input / Loop-Thru)
SCADA_485+
SCADA_485-
SCADA_485+
SCADA_485-
SCADA_232_A_IN
SCADA_232_A_OUT
GND GND
95123-2881

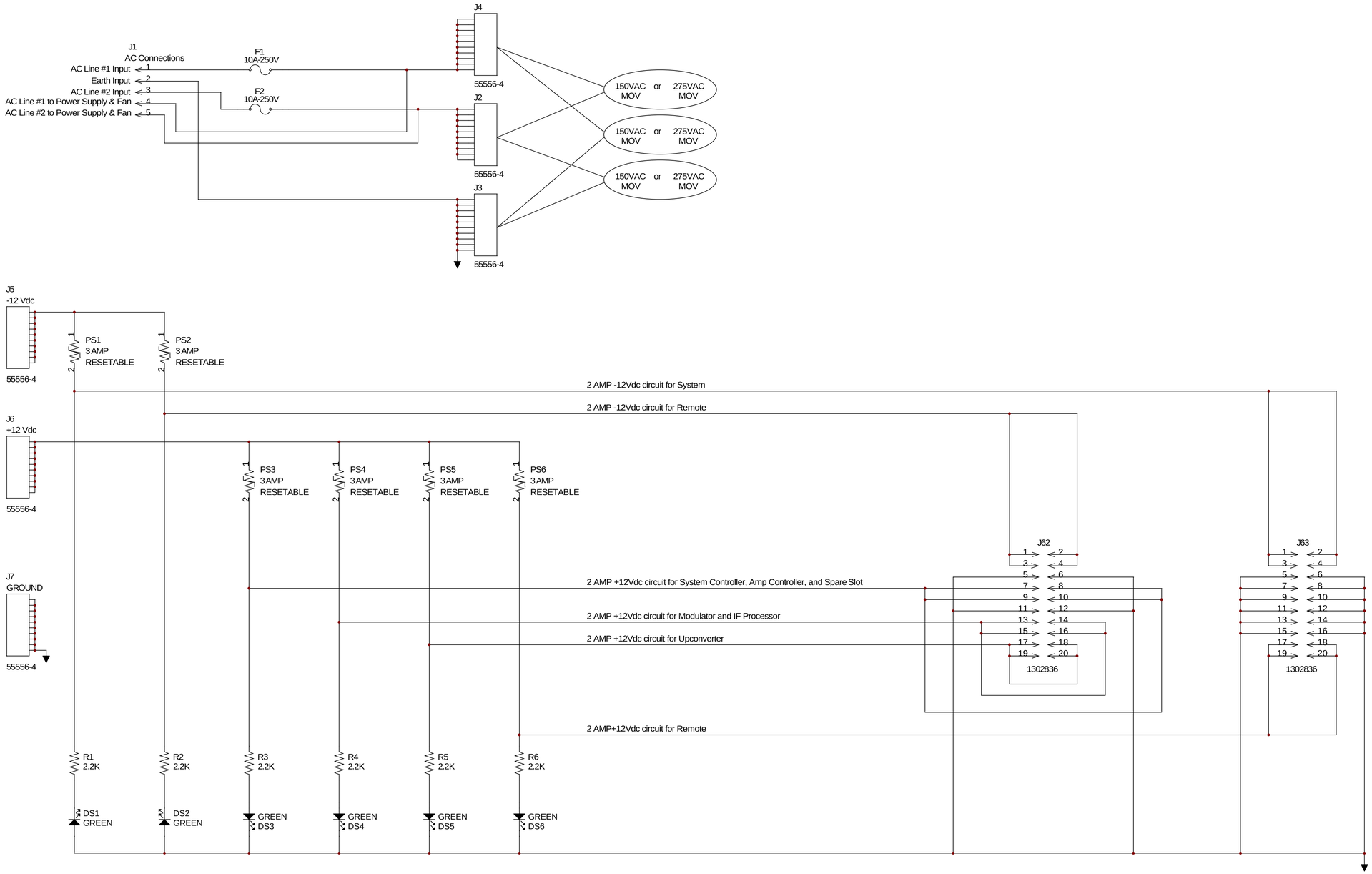
J33 SCADA (Input / Loop-Thru)
SCADA_485+
SCADA_485-
SCADA_485+
SCADA_485-
SCADA_232_B_IN
SCADA_232_B_OUT
GND GND
95123-2881

J34 System RS-485 Serial
UC_AGC_#2_VOLTAGE
System_Serial+
System_Serial-
GND GND
95123-2881

J52
PA_VISUAL_POWER
PA_AURAL_POWER
PA_REFLECTED_POWER
KEY
RTN

Related Part Numbers:
ASSY: 1301941
SCH: 1301995
PCB: 1301993
STENCIL: 1301997

APV	Axcera	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, BACKPLANE BOARD, PIONEER SERIES (1301941)			
ECO	MATERIAL -----	DWN REH 3/03/03	DWG. NO. 1301995		REV A0
REV	FINISH -----	CHK LRT 9/3/03			
		REL LRT 9/3/03	D	SCALE ---	SHEET 1 OF 1



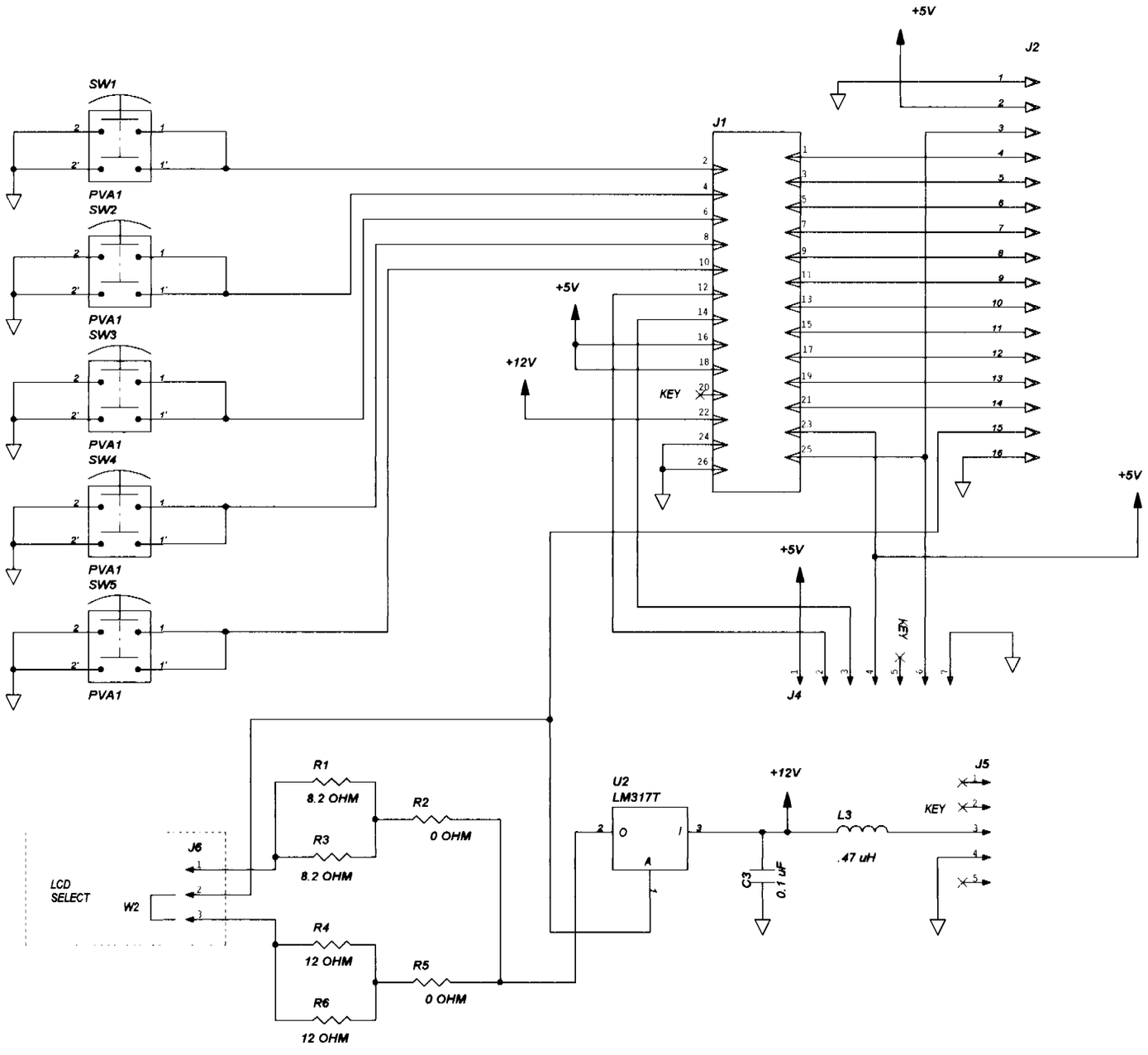
Circuit Design Notes:

1. Track widths of 0.140 inch minimum top and bottom of board shall be used to connections to J1, J2, J3, J4.
2. Track widths of 0.140 inch minimum top of board shall be used to connections to J5 and J6.
3. Track widths of 0.065 inch minimum shall be used to connections to J62 and J63.
4. Track widths of 0.020 inch minimum shall be used to connections between LEDs and resistors.
5. Board BOM needs the following items added to those exported from Orcad:

Part Number	Qty	Description
102071	4	Fuse Clip, PC BD Mnt., 15 Amp

MATERIAL NUMBERS:
1302837 PIONEER, POWER PROTECTION
1302838 PCB, PIONEER, PWR PROTECT
1302839 SCH, PIONEER, PWR PROTECT
1302840 STENCIL FOR 1302838

APV	Axcera	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF AXCERA, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH, PIONEER, PWR PROTECT (1302837)			
ECO	MATERIAL -----	DWN REH 5/29/03	DWG. NO. 1302839		REV AO
	FINISH -----	CHK REH 5/29/03			
REV		REL REH 5/29/03	D	SCALE - - -	SHEET 1 OF 1



DELETED C1, C2, L1, L2, U1, J3, & W1. MOVED W2 FROM J6-1,-2 TO J6 -2,-3. JKF

REV	ECN	DATE	APV
3	8603	11/7/96	RAS
AT J2 W2 WAS W1. (TMY)			
2	8424	9/29/96	JCM
SWITCHED PINS 1 & 2 OF U2. (TMY)			
1	8368	8/27/96	RAS

ITS CORPORATION

MATERIAL ---

FINISH ---

TITLE SCHEMATIC SWITCH BOARD (1527-1406)

DWN	DLM	6/3/96	
CHK	RAS	6/14/96	
REL	RAS	6/14/96	

DWG. NO. 1527-3406 REV 3

B SCALE --- SHEET 1 OF 1