ALIGNMENT PROCEDURE

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
01.01	5 Volt Current	From a 500mA current limited supply, apply 5 volts DC to PL301/4 wrt PL301/2	5v Input current	10mA to 400mA	Input Voltage into PL300 and 7.5 and 10 volts for the radio not required until later. Record value
02.01	PLD Configuration	Select the '*Max Plus 2 - Programming'* menu item. Select the program option	Package response,	Sat/Unsat Verification of the programming process. Examine, Programme, and Verify OK	Using the Altera Max + Plus II programming software package. Choose the PLD program configuration file (.POF) specified in configuration document. Connect the PC to the PLD JTAG interface port via the PL351 connector.
03.01	Processor Initialise	Connect bootload link across PL356/3 to PL356/4. Apply input power. Reset processor using PL356/2 pulled to ground PL356/1 then disconnected. From the PC send a Null character (00H) as per 90775/18/310	The RS232 transmit line. PL359/2.	Sat/Unsat RS232 response : Return of a single 'U' character (55H)	Connect Control Serial port to Processor input port Via PL359/1 0v, PL359/2 Tx, PL359/3 Rx.
03.01.01	*Processor Initialise response failed*	As above.	PL356/18 command_rx_ttl PL356/17 command_tx_ttl	Sat/Unsat RS232 TTL response	Look for fail either side of MAX208 or in processor
03.01.02	*Processor Initialise response still fails*	5v Power only	XTAL1 PL350/40	18.432Mhz signal	Now probing by hand using > 40MHz oscilloscope.
03.02	Load preload32 program	From the PC send the preload32 program as per 90775/18/310 PL359/3 control Rx	The RS232 transmit line. PL359/2	Sat/Unsat RS232 response : Return of a single 'P' character	This test is part of a continues no power break sequence.
03.03	Load Processor Xram test	Send ram test program. Drive as per 90775/18/310 PL359/3 control Rx	The RS232 transmit line. PL359/2	Sat/Unsat	Tests Ram from within Processor prior to loading Ram to test Flash.
03.03.01	*Load Processor port test - Xram fail*	*Follow from load preload32 program. Send port test program.* Drive as per 90775/18/310 PL359/3 control Rx	*The RS232 transmit line. PL359/2*	Sat/Unsat	*2 stage process setting direction and reading values*

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
04.01	Download Flash Test	Follow from load preload32 program Send Flash Test program. Drive as per 90775/18/310	The RS232 transmit line. PL359/2	Sat/Unsat	
04.02	Software Identification	PL359/3 control Rx Drive as per 90775/18/310	The RS232 transmit line. PL359/2	Sat/Unsat	
04.03	Flash A sector test	PL359/3 control Rx Drive as per 90775/18/310	The RS232 transmit line. PL359/2	Sat/Unsat	
04.04	Flash B sector test	PL359/3 control Rx Drive as per 90775/18/310	The RS232 transmit line. PL359/2	Sat/Unsat	
04.05	Store Ftest Results	PL359/3 control Rx Drive as per 90775/18/310	The RS232 transmit line. PL359/2	Sat/Unsat	
04.06	Set Serial Number	PL359/3 control Rx Drive as per 90775/18/310	The RS232 transmit line. PL359/2	Sat/Unsat	
04.07	Download Downloader	PL359/3 control Rx Drive as per 90775/18/310	The RS232 transmit line. PL359/2	Sat/Unsat	
04:08	Software identification	PL359/3 control Rx Drive as per 90775/18/310	The RS232 transmit line. PL359/2	Sat/Unsat	
04.09	Check Boot code area	PL359/3 control Rx Drive as per 90775/18/310	The RS232 transmit line. PL359/2	Sat/Unsat	
04.10	Load Boot Code	PL359/3 control Rx Drive as per 90775/18/310	The RS232 transmit line. PL359/2	Sat/Unsat	
04.11	Copy Boot Code	PL359/3 control Rx Drive as per 90775/18/310	The RS232 transmit line. PL359/2	Sat/Unsat	
04.12	Load Loader Code	PL359/3 control Rx Drive as per 90775/18/310	The RS232 transmit line. PL359/2	Sat/Unsat	
04.13	Load ATE code	PL359/3 control Rx Drive as per 90775/18/310	The RS232 transmit line. PL359/2	Sat/Unsat	
04:14	Software Identification	PL359/3 control Rx Drive as per 90775/18/310	The RS232 transmit line. PL359/2	Sat/Unsat	
05.01	LED red test	Drive RED as per 90775/18/310, PL359/3 control Rx	Optically check Led400 Red.	Sat/Unsat	User input required
05.02	LED green test	Drive GREEN as per 90775/18/310 PL359/3 control Rx	Optically check Led400 Green	Sat/Unsat	User input required

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
05.03	Display output drive L1	Drive PL354/9 high. Drive as per 90775/18/310	All PL354 outputs 3,4, 6,7,8,9,10,11,12,13,14,16	Sat/Unsat Only PL354/9 high	Drive the other outputs low. The PWR output should always be high. All outputs tied to 0v via resistor.
05.04	Display output drive L2	Drive PL354/13 high. Drive as per 90775/18/310	All PL354 outputs 3,4, 6,7,8,9,10,11,12,13,14,16	Sat/Unsat Only PL354/13 high.	Drive the other outputs low. The PWR output should always be high. All outputs tied to 0v via resistor.
05.05	Display output drive L3	Drive PL354/11 high. Drive as per 90775/18/310	All PL354 outputs 3,4, 6,7,8,9,10,11,12,13,14,16	Sat/Unsat Only PL354/11 high.	Drive the other outputs low. The PWR output should always be high. All outputs tied to 0v via resistor.
05.06	Display output drive L4	Drive PL354/12 high. Drive as per 90775/18/310	All PL354 outputs 3,4, 6,7,8,9,10,11,12,13,14,16	Sat/Unsat Only PL354/12 high.	Drive the other outputs low. The PWR output should always be high. All outputs tied to 0v via resistor.
05.07	Display output drive L5	Drive PL354/14 high. Drive as per 90775/18/310	All PL354 outputs 3,4, 6,7,8,9,10,11,12,13,14,16	Sat/Unsat Only PL354/14 high.	Drive the other outputs low. The PWR output should always be high. All outputs tied to 0v via resistor.
05.08	Display output drive TXRX_G	Drive PL354/10 high. Drive as per 90775/18/310	All PL354 outputs 3,4, 6,7,8,9,10,11,12,13,14,16	Sat/Unsat Only PL354/10 high.	Drive the other outputs low. The PWR output should always be high. All outputs tied to 0v via resistor.
05.09	Display output drive TXRX_R	Drive PL354/8 high. Drive as per 90775/18/310	All PL354 outputs 3,4, 6,7,8,9,10,11,12,13,14,16	Sat/Unsat Only PL354/8 high.	Drive the other outputs low. The PWR output should always be high. All outputs tied to 0v via resistor.
05.10	Display output drive STAT-G	Drive PL354/7 high. Drive as per 90775/18/310	All PL354 outputs 3,4, 6,7,8,9,10,11,12,13,14,16	Sat/Unsat Only PL354/7 high.	Drive the other outputs low. The PWR output should always be high. All outputs tied to 0v via resistor.
05.11	Display output drive STAT_R	Drive PL354/4 high. Drive as per 90775/18/310	All PL354 outputs 3,4, 6,7,8,9,10,11,12,13,14,16	Sat/Unsat Only PL354/4 high.	Drive the other outputs low. The PWR output should always be high. All outputs tied to 0v via resistor.
05.12	Display output drive EMG_G	Drive PL354/6 high. Drive as per 90775/18/310	All PL354 outputs 3,4, 6,7,8,9,10,11,12,13,14,16	Sat/Unsat Only PL354/6 high.	Drive the other outputs low. The PWR output should always be high. All outputs tied to 0v via resistor.
05.13	Display output drive EMG_R	Drive PL354/3 high. Drive as per 90775/18/310	All PL354 outputs 3,4, 6,7,8,9,10,11,12,13,14,16	Sat/Unsat Only PL354/3 high.	Drive the other outputs low. The PWR output should always be high. All outputs tied to 0v via resistor.
06.01	Auxiliary output drive TTL_OUT	Drive PL355/3 high. Drive as per 90775/18/310	PL355 outputs 3,4,5,6	Sat/Unsat Only PL355/3 high.	Drive the other outputs low. Outputs tied to 0v via resistor.
06.02	Auxiliary output drive PTT_OUT	Drive PL355/4 high. Drive as per 90775/18/310	PL355 outputs 3,4,5,6	Sat/Unsat Only PL355/4 high.	Drive the other outputs low. Outputs tied to 0v via resistor.
06.03	Auxiliary output drive LED_EMG1	Drive PL355/5 high. Drive as per 90775/18/310	PL355 outputs 3,4,5,6	Sat/Unsat Only PL355/5 high.	Drive the other outputs low. Outputs tied to 0v via resistor.
06.04	Auxiliary output drive LED_EMG2	Drive PL355/6 high. Drive as per 90775/18/310	PL355 outputs 3,4,5,6	Sat/Unsat Only PL355/6 high.	Drive the other outputs low. Outputs tied to 0v via resistor.
07.01	PA output drive PTT_INT High	Drive PL302/9 high. Drive as per 90775/18/310	PL302/9	Sat/Unsat Logic 1	Output tied to 0v via resistor.
07.02	PA output drive PTT_INT Low	Drive PL302/9 low Drive as per 90775/18/310	PL302/9	Sat/Unsat Logic 0	Output tied to 0v via resistor.

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
08.01	Auxiliary Output drive OPTO_OUT float	Drive Opto output low. Drive as per 90775/18/310	PL355/14	Sat/Unsat Logic 1	Leave the OPTO_OUT- output floating PL355/15 PL355/14 is tied high via 100 ohm to 5v.
08.02	Auxiliary Output drive OPTO_OUT low	Drive Opto output low. Drive as per 90775/18/310	PL355/14	Sat/Unsat Logic 0	Ground the OPTO_OUT- output.
08.03	Auxiliary Output drive OPTO_OUT high	Drive Opto output high. Drive as per 90775/18/310	PL355/14	Sat/Unsat Logic 1	Ground the OPTO_OUT- output.
09.01	Display input drive test EMG_IN high	Drive PL354/2 High WRT PL355/12 Read EMG_IN	PL359/2 Control Tx WRT PL359/1	Sat/Unsat Logic 1	Externally drive the pin high and read back through processor to control port.
09.02	Display input drive test EMG_IN Low	Drive PL354/2 Low WRT PL355/12 Read EMG_IN	PL359/2 Control Tx WRT PL359/1	Sat/Unsat Logic 0	Externally drive the pin low and read back through processor to control port.
09.03	Display input drive test FRQ_SW high	Drive PL354/5 High WRT PL355/12 Read FRQ_SW	PL359/2 Control Tx WRT PL359/1	Sat/Unsat Logic 1	Externally drive the pin high and read back through processor to control port.
09.04	Display input drive test FRQ_SW Low	Drive PL354/5 Low WRT PL355/12 Read FRQ_SW	PL359/2 Control Tx WRT PL359/1	Sat/Unsat Logic 0	Externally drive the pin low and read back through processor to control port.
10.01	Auxiliary input drive EMG_IN high	Drive PL355/8 High WRT PL355/12 Read EMG_IN	PL359/2 Control Tx WRT PL359/1	Sat/Unsat Logic 1	Externally drive the pin high and read back through processor to control port.
10.02	Auxiliary input drive EMG_IN Low	Drive PL355/8 Low WRT PL355/12 Read EMG_IN	PL359/2 Control Tx WRT PL359/1	Sat/Unsat Logic 0	Externally drive the pin low and read back through processor to control port.
10.03	Auxiliary input drive Fix_IN high	Drive PL355/9 High WRT PL355/12 Read FIX_IN	PL359/2 Control Tx WRT PL359/1	Sat/Unsat Logic 1	Externally drive the pin high and read back through processor to control port.
10.04	Auxiliary input drive Fix_IN Low	Drive PL355/9 Low WRT PL355/12 Read FIX_IN	PL359/2 Control Tx WRT PL359/1	Sat/Unsat Logic 0	Externally drive the pin low and read back through processor to control port.
10.05	Auxiliary input drive TTL_IN high	Drive PL355/10 High WRT PL355/12 Read TTL_IN	PL359/2 Control Tx WRT PL359/1	Sat/Unsat Logic 1	Externally drive the pin high and read back through processor to control port.
10.06	Auxiliary input drive TTL_IN Low	Drive PL355/10 Low WRT PL355/12 Read TTL_IN	PL359/2 Control Tx WRT PL359/1	Sat/Unsat Logic 0	Externally drive the pin low and read back through processor to control port.
10.07	Auxiliary input drive 1PPS_IN high	Drive PL355/11 High WRT PL355/12 Read 1PPS_IN	PL359/2 Control Tx WRT PL359/1	Sat/Unsat Logic 1	Externally drive the pin high and read back through processor to control port.
10.08	Auxiliary input drive 1PPS_IN Low	Drive PL355/11Low WRT PL355/12 Read 1PPS_IN	PL359/2 Control Tx WRT PL359/1	Sat/Unsat Logic 0	Externally drive the pin low and read back through processor to control port.
10.09	Auxiliary inputs drive OPTO_IN High	Drive PL355/17 high WRT pin 16 tied to 0v, Read OPTO_IN	PL359/2 Control Tx WRT PL359/1	Sat/Unsat Logic 1	Externally drive the pin high and read back through processor to control port.
10.10	Auxiliary inputs drive OPTO_IN Low	Drive PL355/17 low WRT pin 16 tied to 0v, Read OPTO_IN	PL359/2 Control Tx WRT PL359/1	Sat/Unsat Logic 0	Externally drive the pin low and read back through processor to control port.

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
11.01	Auxiliary Analogue input level test.	Drive PL355/1 to 3V 0.1% WRT/2 , Read Analogue input	PL359/2 Control Tx WRT PL359/1	ADC Value 602 to 626	Externally drive the pin and read value back through processor to control port. Store the Value in Flash.
11.02	PA PA_PWR_MON input level test.	Drive PL302/7 to 2V 0.1% WRT/3 , Read Analogue input	PL359/2 Control Tx WRT PL359/1	ADC Value 402 to 418	Externally drive the pin and read value back through processor to control port. Store the Value in Flash.
	Note Other Analogue inputs to be tested when in the radio section.				10v_mon, 7v5_mon, Temp, Rss, RXFB_DC to be used when in radio section) 5v_LNA antenna SK500 loaded with 250 ohm 50mA. Power in @ 30v i/p
12.01	Serial Duart B handshaking Output Comms test.	Request UUT to send a message at 38K4 via Duart B with full handshaking from PL355/23,24,25,26	Monitor RS232 serial output on PL355/23,24,25,26	Sat/Unsat	
12.02	Serial Duart B handshaking Input Comms test.	Request UUT to send a pass on a message received at 38K4 via Duart B with full handshaking from PL355/23,24,25,26	Monitor RS232 serial output on PL359/2	Sat/Unsat	
12.03	Serial TXD1 Port2 Output Comms test.	Request UUT to send a message at 38K4 from internal source TXD1 via the PLD route matrix to Port2 Tx.	Monitor RS232 serial output on PL355/20	Sat/Unsat	
12.04	Serial RXD1 Port2 Input Comms test.	Request UUT to pass on a message received at 38K4 on Port2 Rx PL355/22 via the PLD route matrix to internal destination RXD1.	Monitor RS232 serial output on PL359/2	Sat/Unsat	
12.05	Serial TXD1 Port1 Output Comms test.	Request UUT to send a message at 38K4 from internal source TXD1 via the PLD route matrix to Port1 Tx.	Monitor RS232 serial output on PL355/19	Sat/Unsat	
12.06	Serial RXD1 Port1 Input Comms test.	Request UUT to pass on a message received at 38K4 on Port1 Rx PL355/21 via the PLD route matrix to internal destination RXD1.	Monitor RS232 serial output on PL359/2	Sat/Unsat	

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
12.07	Serial Duart A Output P1 Comms test.	Request UUT to send a message at 38K4 from internal source Duart A via the PLD route matrix to Port1 Tx.	Monitor RS232 serial output on PL355/19	Sat/Unsat	
12.08	Serial Duart A Input P1 Comms test.	Request UUT to pass on a message received at 38K4 on Port1 Rx PL355/21 via the PLD route matrix to internal destination Duart A.	Monitor RS232 serial output on PL359/2	Sat/Unsat	
12.09	Serial Duart A Output P2 Comms test.	Request UUT to send a message at 38K4 from internal source Duart A via the PLD route matrix to Port2 Tx.	Monitor RS232 serial output on PL355/21	Sat/Unsat	
12.10	Serial Duart A Input P2 Comms test.	Request UUT to pass on a message received at 38K4 on Port2 Rx PL355/22 via the PLD route matrix to internal destination Duart A.	Monitor RS232 serial output on PL359/22	Sat/Unsat	
12.11	Serial GPS1_RX1 Output Comms test.	Request UUT to send a message at 38K4 from internal source Duart A via the PLD route matrix to GPS1_RX1.	Monitor 5v RS232 serial output on SK400/5	Sat/Unsat	
12.12	Serial GPS1_TX1 Input Comms test.	Request UUT to pass on a message received at 38K4 on GPS_TX1 SK400/3 via the PLD route matrix to internal destination Duart A.	Monitor RS232 serial output on PL359/2	Sat/Unsat	Connect PL356 pins 5 to 6 and 7 to 8 and 9 to 10
12.13	Serial GPS1_RX2 Output Comms test.	Request UUT to send a message at 38K4 from internal source Duart A via the PLD route matrix to GPS1_RX2.	Monitor 5v RS232 serial output on SK400/5	Sat/Unsat	

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
12.14	Serial GPS1_TX2 Input Comms test.	Request UUT to pass on a message received at 38K4 on GPS_TX2 SK400/1 via the PLD route matrix to internal destination Duart A.	Monitor RS232 serial output on PL359/2	Sat/Unsat	Connect PL356 pins 5 to 6 and 7 to 8 and 9 to 10
12.15	Serial GPS2_RXDA Output Comms test.	Request UUT to send a message at 38K4 from internal source Duart A via the PLD route matrix to GPS1_RXDA SK401/5.	Monitor RS232 serial output on SK401/5	Sat/Unsat	
12.16	Serial GPS2_TXDA Input Comms test.	Request UUT to pass on a message received at 38K4 on GPS_TX1 SK401/3 via the PLD route matrix to internal destination Duart A.	Monitor RS232 serial output on PL359/2	Sat/Unsat	Connect PL356 pins 11 to 12 and 13 to 14 and 15 to 16
12.17	Serial GPS2_RXDB Output Comms test.	Request UUT to send a message at 38K4 from internal source Duart A via the PLD route matrix to GPS2_RXDB SK401/11.	Monitor RS232 serial output on SK401/11	Sat/Unsat	
12.18	Serial GPS2_TXDB Input Comms test.	Request UUT to pass on a message received at 38K4 on GPS_TX2 SK401/9 via the PLD route matrix to internal destination Duart A.	Monitor RS232 serial output on PL359/2	Sat/Unsat	Connect PL356 pins 11 to 12 and 13 to 14 and 15 to 16
12.19	GPS1 input drive 1PPS_IN and battery input test high.	Connect SK400/6 and 4 together. Drive High by connecting PL356/19 to 21.	PL359/2 Control Tx WRT PL359/1	Sat/Unsat Logic 1	Externally drive the pin high and read back through processor to control port. Connect PL356 pins 5 to 6 and 7 to 8 and 9 to 10
12.20	GPS1 input drive 1PPS_IN and battery input test low	Connect SK400/6 and 4 together. Drive low by disconnecting PL356/19 to 21.	PL359/2 Control Tx WRT PL359/1	Sat/Unsat Logic 0	Externally drive the pin low and read back through processor to control port. Connect PL356 pins 5 to 6 and 7 to 8 and 9 to 10
12.21	GPS2 input drive 1PPS_IN and battery input test high	Connect SK401/15 and 18 together. Drive High by connecting PL356/19 to 21.	PL359/2 Control Tx WRT PL359/1	Sat/Unsat Logic 1	Externally drive the pin high and read back through processor to control port. Connect PL356 pins 11 to 12 and 13 to 14 and 15 to 16

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
12.22	GPS2 input drive 1PPS_IN and battery input test low	Connect SK401/15 and 18 together. Drive Low by connecting PL356/19 to 21.	PL359/2 Control Tx WRT PL359/1	Sat/Unsat Logic 0	Externally drive the pin low and read back through processor to control port. Connect PL356 pins 11 to 12 and 13 to 14 and 15 to 16
13.01	7V5B Input Current.	PL301/6=7.5V wrt PL301/2(0V)	PL301/6 current	0 to 50mA	
13.02	5V Voltage TCVR	PL301/6=7.5V wrt PL301/2(0V)	PL351/42 voltage wrt PL351/14 (0V)	4.975V to 5.025V	
13.03	5V_EC Voltage - Off	Set EC low (Econ off mode)	PL351/30 voltage wrt PL351/14 (0V)	0.0V to 0.050V	**PL301/6=7.5V and PL301/4=5V wrt PL301/2(0V) for this and all remaining tests unless other wise stated, use control serial port for commands**.
13.04	5V_EC Voltage - On	Set EC high (Econ Mode)	PL351/30 voltage wrt PL351/14 (0V)	4.925V to 5.000V	
13.05	5V_RX Voltage - Off	Set EC low	PL351/40 voltage wrt PL351/14 (0V)	0.0V to 0.50V	
13.06	5V_RX Voltage - On	Set Receive mode	PL351/40 voltage wrt PL351/14 (0V)	4.925V to 5.000V	
13.07	7V5_RX Voltage - Off	Set Econ mode	PL351/12 voltage wrt PL351/14 (0V)	0.0V to 0.050V	
13.08	7V5_RX Voltage - On	Set Receive mode	PL351/12 voltage wrt PL351/14 (0V)	7.250V to 7.550V	
13.09	7V5_TX Voltage – Off	Set Econ mode	PL351/20 voltage wrt PL351/14 (0V)	0.0V to 0.050V	
13.10	7V5_TX Voltage – On	Set Transmit mode	PL351/20 voltage wrt PL351/14 (0V)	7.25V to 7.55V	
13.11	7V5_EC Voltage – Off	Set Econ off mode	PL351/22 voltage wrt PL351/14 (0V)	0.0V to 1.500V	
13.12	7V5_EC Voltage - On	Set Econ mode	PL351/22 voltage wrt PL351/14 (0V)	7.25V to 7.55V	
13.13	HV_EC Voltage - Off	Set EC control line LOW	PL351/18 voltage wrt PL351/14 (0V)	0V to 1.5V	

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
13.14	HV_EC Voltage - On	Set EC control line HIGH	PL351/18 voltage wrt PL351/14 (0V)	22.00V to 24.00V	
13.15	10V_TX off	Set SW10V_TX off	PL351/49 voltage wrt PL351/14 (0V)	1.0 to 0 volts	Testing FET switch in PSU section via processor control
13.16	10V_TX on	Set SW10V_TX on	PL351/49 voltage wrt PL351/14 (0V)	10.5 to 9.5 volts	
13.17	2V5_REF Voltage		PL351/41 voltage wrt PL351/14 (0V)	2.475V to 2.525V	
13.18	TEMP Voltage		PL351/39 voltage wrt PL351/14 (0V)	1.4V to 1.8V	
14.01	RF MOD 0	PL359/3 control Rx	PL351/ 36 voltage wrt PL351/14 (0V)	2.15 to 2.35 V	Set DAC to limits to test voltage swing
14.02	RF MOD 255	PL359/3 control Rx	PL351/ 36 voltage wrt PL351/14 (0V)	4.35 to 4.65 V	Set DAC to limits to test voltage swing
14.03	VCO_CT 0	PL359/3 control Rx	PL351/ 24 voltage wrt PL351/14 (0V)	> 22.0V	Set DAC to limits to test voltage swing
14.04	VCO_CT 255	PL359/3 control Rx	PL351/ 24 voltage wrt PL351/14 (0V)	< 3.0V	Set DAC to limits to test voltage swing
14.05	IMAGE 1 0	PL359/3 control Rx	PL351/ 16 voltage wrt PL351/14 (0V)	> 15.0 V	Set DAC to limits to test voltage swing
14.06	IMAGE 1 255	PL359/3 control Rx	PL351/ 16 voltage wrt PL351/14 (0V)	< 1.0 V	Set DAC to limits to test voltage swing
14.07	RX TUNE 0	PL359/3 control Rx	PL351/ 28 voltage wrt PL351/14 (0V)	> 15.0 V	Set DAC to limits to test voltage swing
14.08	RX TUNE 255	PL359/3 control Rx	PL351/ 28 voltage wrt PL351/14 (0V)	< 1.0 V	Set DAC to limits to test voltage swing
14.09	LO TUNE 0	PL359/3 control Rx	PL351/ 26 voltage wrt PL351/14 (0V)	> 15.0 V	Set DAC to limits to test voltage swing
14.10	LO TUNE 255	PL359/3 control Rx	PL351/ 26 voltage wrt PL351/14 (0V)	< 1.0 V	Set DAC to limits to test voltage swing
14.11	DIS TUNE 0	PL359/3 control Rx	PL351/ 32 voltage wrt PL351/14 (0V)	> 15.0 V	Set DAC to limits to test voltage swing
14.12	DIS TUNE 255	PL359/3 control Rx	PL351/ 32 voltage wrt PL351/14 (0V)	< 1.0 V	Set DAC to limits to test voltage swing

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
15.01	VCO Coarse Tune Calibration (Receive) 137.000MHz	Set to Receive on 137MHz		Sat / Unsat	Adjust DAC B until the dc voltage at TP6 is as near as possible to 5.1V.
15.02	TP6 Voltage at 137MHz	Set to Receive on 137MHz	TP6	> 5.0 V	
15.03	Gain at 137 MHz	Set to Receive on 137MHz		< 1.2 V / MHz	Adjust frequency up and down and measure o/p.
15.04	DAC B value at 137 MHz	Set to Receive on 137MHz	TP6	242 to 252	Note the resultant DAC value and save for curve fit.
15.05	VCO Coarse Tune Calibration (Receive) 145.000MHz	Set to Receive on 145MHz	TP6	Sat / Unsat	Adjust DAC B until the dc voltage at TP6 is as near as possible to 5.7V.
15.06	TP6 Voltage at 145MHz	Set to Receive on 145MHz	TP6	> 5.7 V	
15.07	Gain at 145 MHz	Set to Receive on 145MHz	TP6	< 1.25 V / MHz	
15.08	DAC B value at 145 MHz	Set to Receive on 145MHz	DAC B Value as given by the Test System	232 to 243	Note the resultant DAC value and save for curve fit.
15.09	VCO Coarse Tune Calibration (Receive) 155.000MHz	Set to Receive on 155MHz	TP6	Sat / Unsat	Adjust DAC B until the dc voltage at TP6 is as near as possible to 6.5V.
15.10	TP6 Voltage at 155MHz	Set to Receive on 155MHz	TP6	> 6.6 V	
15.11	Gain at 155 MHz	Set to Receive on 155MHz	TP6	< 1.35 V / MHz	
15.12	DAC B value at 155 MHz	Set to Receive on 155MHz	DAC B Value as given by the Test System	218 to 230	Note the resultant DAC value and save for curve fit.
15.13	VCO Coarse Tune Calibration (Receive) 165.000MHz	Set to Receive on 165MHz	TP6	Sat / Unsat	Adjust DAC B until the dc voltage at TP6 is as near as possible to 7.2V.

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
15.14	TP6 Voltage at 165MHz	Set to Receive on 165MHz	TP6	> 7.25 V	
15.15	Gain at 165 MHz	Set to Receive on 165MHz	TP6	< 1.4 V / MHz	
15.16	DAC B value at 165 MHz	Set to Receive on 165MHz	DAC B Value as given by the Test System	201 to 215	Note the resultant DAC value and save for curve fit.
15.17	VCO Coarse Tune Calibration (Receive) 173.000MHz	Set to Receive on 173MHz	TP6	Sat / Unsat	Adjust DAC B until the dc voltage at TP6 is as near as possible to 7.8V.
15.18	TP6 Voltage at 173MHz	Set to Receive on 173MHz	TP6	> 8.0 V	
15.19	Gain at 173 MHz	Set to Receive on 173MHz	TP6	< 1.5 V / MHz	
15.20	DAC B value at 173 MHz	Set to Receive on 173MHz	TP6	181 to 198	Note the resultant DAC value and save for curve fit.
15.21	VCO Coarse Tune Curve Fit (Receive)			Sat / Unsat	Using the data obtained in Tests 15.01 to 15.20 fit a straight line between adjacent calibration points and determine the DAC values for the EEPROM locations specified in MTR026, Table 9 (RX COARSE TUNE). The value calculated for each location should be centred on the range of frequencies covered by that location. For example, the DAC value for VHF FREQ = 138MHz is calculated for 139.000MHz (VCO frequency 184.000MHz). The DAC values obtained for the test frequencies used in Tests 15.01 to 15.2 should be directly loaded into the relevant EEPROM locations. All interpolated DAC values should be rounded up to the next integer value above the calculated value (even if this is itself an integer) and then loaded into the relevant EEPROM locations. The value stored for 172MHz (i.e. the result of Test 02.05) should be repeated for 174MHz.

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
16.01	VCO Coarse Tune Calibration (Transmit) 137.000MHz	Set to Transmit on 137MHz	TP6 DAC B Value as given by the Test System	233 to 249	Adjust DAC B until the dc voltage at TP6 is as near as possible to 4.9V. Note the resultant DAC value and save for curve fit.
16.02	VCO Coarse Tune Calibration (Transmit) 145.000MHz	Set to Transmit on 145MHz	TP6 DAC B Value as given by the Test System	214 to 234	Adjust DAC B until the dc voltage at TP6 is as near as possible to 5.7V. Note the resultant DAC value and save for curve fit.
16.03	VCO Coarse Tune Calibration (Transmit) 155.000MHz	Set to Transmit on 155MHz	TP6 DAC B Value as given by the Test System	184 to 214	Adjust DAC B until the dc voltage at TP6 is as near as possible to 6.7V. Note the resultant DAC value and save for curve fit.
16.04	VCO Coarse Tune Calibration (Transmit) 165.000MHz	Set to Transmit on 165MHz	TP6 DAC B Value as given by the Test System	138 to 184	Adjust DAC B until the dc voltage at TP6 is as near as possible to 7.7V. Note the resultant DAC value and save for curve fit.
16.05	VCO Coarse Tune Calibration (Transmit) 173.000MHz	Set to Transmit on 173MHz	TP6 DAC B Value as given by the Test System	6 to 114	Adjust DAC B until the dc voltage at TP6 is as near as possible to 8.5V. Note the resultant DAC value and save for curve fit.
16.06	VCO Coarse Tune Curve Fit (Transmit)			Sat / Unsat	Using the data obtained in Tests 16.01 to 16.05 fit a straight line between adjacent calibration points and determine the DAC values for the EEPROM locations specified in MTR026, Table 9 (TX COARSE TUNE). The value calculated for each location should be centred on the range of frequencies covered by that location. For example, the DAC value for VHF FREQ = 138MHz is calculated for 139.000MHz. The DAC values obtained for the test frequencies used in Tests 03.01 to 03.05 should be directly loaded into the relevant EEPROM locations. All interpolated DAC values should be rounded up to the next integer value above the calculated value (even if this is itself an integer) and then loaded into the relevant EEPROM locations. The value stored for 172MHz (i.e. the result of Test 03.05) should be repeated for 174MHz.

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
17.01	LOCK Output (Out of Lock)	Set to Receive on 154MHz Set DAC A as Test 04.01 Set DAC B to 00	PL351,38 (LOCK) as measured by the DMM	< 1 V	Checks LOCK indication with loop out of lock.
17.02	LOCK Output (In Lock)	Set to Receive on 154MHz Set DAC A as Test 04.01 Set DAC B as Test 02.03	PL351,38 (LOCK) as measured by the DMM	> 4 V	Checks LOCK indication with loop locked.
18.01	Reference Oscillator Alignment	Set to Transmit on 154MHz Set DAC B as Test 16.03	Frequency of SK502 Output as measured by the Counter	-77Hz to +77Hz	Increase DAC C until UUT draws between 100mA and 130mA from 10V supply. **Do not** set DAC C > 40. Adjust DAC A for the value which gives the nearest frequency to 154.000MHz. Check the frequency is within specified limits. Store the DAC A value for use in later tests. Calculate the fractional error, E, of the output frequency from the formula: E = (Output Frequency / 154MHz) - 1 Save the value of E for use in later tests.
18.02	Reference Oscillator DAC Value	As per 90775/13/310	DAC A Value as given by the Test System	43 to 130	Note the value of DAC A from Test 18.01 and check it is within specified limits. Store value in all 256 locations allocated to Reference Oscillator
19.01	2nd LO Alignment	Set to Receive on 154MHz TEST = Logic 1 Set DAC A as Test 18.01 Set DAC B as Test 16.03 SK502 Input = Freq. See Note Level -30dBm Unmodulated	SK502 (IFO) Frequency as measured by the Counter	-50Hz to +50Hz	Adjust DAC F (2nd LO) for the value which gives the nearest frequency to 455kHz. Check the frequency is within specified limits. SK502 Frequency is determined by the formula: Freq. = 154.025 + 199.025 E MHz Where E, the reference oscillator fractional frequency error, has been defined in Test 18.01. The 154MHz frequency measured in Test 18.01, the SK502 input frequency and the 455kHz output frequency should all be measured using the same Frequency Standard. Store the DAC F value for use in later tests.

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
19.02	2nd Local Oscillator DAC Value	As per 90775/13/310	DAC F Value as given by the Test System	122 to 182	Note the value of DAC F from Test 19.01 and check it is within specified limits. Store value in all 64 locations allocated to 2nd Local Oscillator
20.01	Demodulator Alignment	Set to Receive on 154MHz Set DAC A as Test 18.01 Set DAC B as Test 16.03 Set DAC F as Test 19.01 SK502 Input = Freq. 154.025MHz Level -60dBm Unmodulated	PL351,43 (RXS) as measured by the DMM	2.4V to 2.6V	Adjust DAC G for dc voltage closest to 2.5V. Check the voltage is within specified limits. Store the DAC G value for use in later tests.
20.02	Demodulator DAC Value	As per 90775/13/310	DAC G Value as given by the Test System PL351/43 (RXS) voltage w.r.t. 0V	155 to 189	Note the value of DAC G from Test 20.01 and check it is within specified limits. Store value in all 32 locations allocated to Discriminator
20.03	Receive Audio Level (25kHz BW)	Set to Receive on 154MHz Set DAC A as Test 18.01 Set DAC B as Test 16.03 Set DAC F as Test 19.01 Set DAC G as Test 20.01 Synthesizer Frequency = 199.025MHz SK502 Input =Freq. 154.025MHz Level -60dBm Mod. 1kHz, Dev. 5kHz	PL351,43 (RXS) as measured by the Audio Analyzer	1.0V pk-pk to 2.0V pk-pk	Check that the audio level is within specified limits and record. Calculate the required Correction Factor to be stored in EEPROM:- Gain = (Measured Audio Level) / (1.3V pk-pk) Correction Factor = 256 / (Gain + 1) Store the value for the Correction Factor, rounded to the nearest integer, in all 32 locations allocated to Receive Audio Level (25kHz BW)

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
20.04	Receive Audio Level (12.5kHz BW)	Set to Receive on 154MHz BWS = Logic 1 Set DAC A as Test 18.01 Set DAC B as Test 16.03 Set DAC F as Test 19.01 Set DAC G as Test 20.01 SK502 Input =Freq. 154.025MHz Level -60dBm Mod. 1kHz Dev. 2.5kHz	PL351,21 (RXFB) as measured by the Audio Analyser	0.5Vpk-pk to 1.0V pk-pk	Check that the audio level is within specified limits and record. Calculate the required Correction Factor to be stored in EEPROM:- Gain = (Measured Audio Level) / (1.0V pk-pk) Correction Factor = 256 / (Gain + 1) Store the value for the Correction Factor, rounded to the nearest integer, in all 32 locations allocated to Receive Audio Level (12.5kHz BW)
20.05	RXS POT calibration 25kHz bandwidth	As per 90775/13/310	PL351,21 (RXFB)	0.928 to 0.948 v p-p	
20.06	RXS POT DAC value 25kHz bandwidth	As per 90775/13/310	Pot DAC value	127 to 179	
20.07	RXS POT calibration 12.5kHz bandwidth	As per 90775/13/310	PL351,21 (RXFB)	0.928 to 0.948 v p-p	
20.08	RXS POT DAC value 12.5kHz bandwidth	As per 90775/13/310	Pot DAC value	50 to 78	
20.09	RXS DC level 25kHz bandwidth	As per 90775/13/310	PL351,21 (RXFB)	2.24 to 2.44 v	
20.10	RXS DC level 12.5kHz bandwidth	As per 90775/13/310	PL351,21 (RXFB)	2.19 to 2.49 v	
21.01	RX Signal Strength Indication (Large Signal)	Set to Receive on 154.025MHz Set DAC A as Test 18.01 Set DAC B as Test 16.03 Set DAC F as Test 19.01 Set DAC G as Test 20.01 SK502 Input = Freq. 154.025MHz Level -60dBm Unmodulated	PL351,11 (RSS) as measured by the DMM	3V to 9.999V	Check RSS voltage for large rf input. Allow 50ms for settling before reading RSS output level.

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
21.02	RX Signal Strength Indication (No Signal)	Set to Receive on 154.025MHz Set DAC A as Test 18.01 Set DAC B as Test 16.03 Set DAC F as Test 19.01 Set DAC G as Test 20.01 SK502 Input = No signal	PL351,11 (RSS) as measured by the DMM	0.25 V to 2 V	Check RSS voltage for no rf input. Allow 50ms for settling before reading RSS output level.
22.01	Rx Tune 136.025MHz	Set to Receive on 136. 025MHz Set DAC A as Test 18.01 Set DAC B as Test 16.01 Set DAC F as Test 19.01 Set DAC G as Test 20.01 SK502 Input = Freq. 136.025MHz Level -75dBm Unmodulated	DAC D Data as given by the Test System PL351,11 (RSS)	229 to 240	Vary DAC D for maximum output at PL351,11 (RSS). Allow 50ms for settling before reading RSS output. Store DAC D value for use in later tests.
22.02	Image Filter Notch 136.025MHz	Set to Receive on 136. 025MHz Set DAC A as Test 18.01 Set DAC B as Test 16.01 Set DAC D as Test 22.01 Set DAC F as Test 19.01 Set DAC G as Test 20.01 SK502 Input =Freq. 226. 025MHz Level Variable Unmodulated	DAC C Data as given by the Test System PL351,11 (RSS)	143 to 174	1. Set the rf level at SK502 (10dB steps) to give an output level at RSS of > 3.0V. 2. Adjust DAC C data to reduce the RSS output. 3. If the RSS output falls to below 2.2V, increase the rf level at SK502 to give an output at RSS of 3.0V to 3.5V, and continue Step 2. 4. When the RSS output reaches a minimum, note the corresponding value of DAC C. Store DAC C value for use in later tests. Allow 50ms for settling before reading RSS output.
22.03	Rx Tune 154. 025MHz	Set to Receive on 154.025MHz Set DAC A as Test 18.01 Set DAC B as Test 16.03 Set DAC F as Test 19.01 Set DAC G as Test 20.01 SK502 Input =Freq. 154. 025MHz Level -75dBm Unmodulated	DAC D Data as given by the Test System PL351,11 (RSS)	178 to 200	Vary DAC D for maximum output at PL351,11 (RSS). Allow 50ms for settling before reading RSS output. Store DAC D value for use in later tests.

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
22.04	Image Filter Notch 154. 025 MHz	Set to Receive on 154.025MHz Set DAC A as Test 18.01 Set DAC B as Test 16.03 Set DAC D as Test 22.03 Set DAC F as Test 19.01 Set DAC G as Test 20.01 SK502 Input =Freq. 244.025MHz Level Variable Unmodulated	DAC C Data as given by the Test System PL351,11 (RSS)	119 to 156	1. Set the rf level at SK502 (10dB steps) to give an output level at RSS of > 3.0V. 2. Adjust DAC C data to reduce the RSS output. 3. If the RSS output falls to below 2.2V, increase the rf level at SK502 to give an output at RSS of 3.0V to 3.5V, and continue Step 2. 4. When the RSS output reaches a minimum, note the corresponding value of DAC C. Store DAC C value for use in later tests. Allow 50ms for settling before reading RSS output.
22.05	Rx Tune 173.975MHz	Set to Receive on 173.975MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 Set DAC F as Test 19.01 Set DAC G as Test 20.01 SK502 Input =Freq. 173.975MHz Level -75dBm Unmodulated	DAC D Data as given by the Test System PL351,11 (RSS)	94 to 146	Vary DAC D for maximum output at PL351,11 (RSS). Allow 50ms for settling before reading RSS output. Store DAC D value for use in later tests.
22.06	Image Filter Notch 173.975MHz	Set to Receive on 173.975MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 Set DAC D as Test 22.05 Set DAC F as Test 19.01 Set DAC G as Test 20.01 SK502 Input =Freq. 173.975MHz Level Variable Unmodulated	DAC C Data as given by the Test System PL351,11 (RSS)	85 to 137	1. Set the rf level at SK502 (10dB steps) to give an output level at RSS of > 3.0V. 2. Adjust DAC C data to reduce the RSS output. 3. If the RSS output falls to below 2.2V, increase the rf level at SK502 to give an output at RSS of 3.0V to 3.5V, and continue Step 2. 4. When the RSS output reaches a minimum, note the corresponding value of DAC C. Store DAC C value for use in later tests. Allow 50ms for settling before reading RSS output.

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
22.07	RF Tune Curve Fit			Sat / Unsat	Using the DAC D results from Tests 22.01, 22.03, and 22.05 fit a straight line between calibration points and determine the DAC values for EEPROM locations specified in MTR026, Table 12 - RX TUNE. The value calculated for each location should be centred on the range of frequencies covered by that location. For example, the DAC value for VHF FREQ 137MHz is calculated for 137.500MHz. The DAC D values obtained at the test frequencies should be directly loaded into the relevant EEPROM locations. All interpolated DAC values should be rounded down to the next integer value below the calculated value and then loaded into the relevant EEPROM locations. The value stored for 173MHz (i.e. the result of Test 22.05) should be repeated for 174MHz.
22.08	Image Filter Curve Fit			Sat / Unsat	Using the DAC C results from Tests 22.02, 22.04, and 22.06 fit a straight line between calibration points and determine the DAC values for EEPROM locations specified in MTR026, Table 12 - RX IMAGE. The value calculated for each location should be centred on the range of frequencies covered by that location. For example, the DAC value for VHF FREQ 137MHz is calculated for 137.500MHz. The DAC C values obtained at the test frequencies should be directly loaded into the relevant EEPROM locations. All interpolated DAC values should be rounded down to the next integer value below the calculated value and then loaded into the relevant EEPROM locations. The value stored for 173MHz (i.e. the result of Test 22.06) should be repeated for 174MHz.

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
23.01	Rx Sensitivity at 136.025MHz	Set to Receive on 136.025MHz Set DAC A as Test 18.01 Set DAC B as Test 16.01 Set DAC C as Test 22.02 Set DAC D as Test 22.01 Set DAC F as Test 19.01 Set DAC G as Test 20.01 SK502 Input = Freq. 136.025MHz Level –113dBm Mod. 1kHz Dev. 3kHz	PL351,43 (RXS) via AF Filter SK502 Input Level as given by RF Signal Generator 1	>=20dB	Measure the SINAD, Psophometrically weighted, at the AF Filter output. Filter de-emphasis selected.
23.02	Rx Sensitivity at 154.025MHz	Set to Receive on 154.025MHz Set DAC A as Test 18.01 Set DAC B as Test 16.03 Set DAC C as Test 22.04 Set DAC D as Test 22.03 Set DAC F as Test 19.01 Set DAC G as Test 20.01 SK502 Input =Freq. 154.025MHz Level –113dBm Mod. 1kHz Dev. 3kHz	PL351,43 (RXS) via AF Filter SK502 Input Level as given by RF Signal Generator 1	>=20dB	Measure the SINAD, Psophometrically weighted, at the AF Filter output. Filter de-emphasis selected.
23.03	Rx Sensitivity at 173.975MHz	Set to Receive on 173.975MHz Set DAC A as Test 18.01 Set DAC B as Test 16.01 Set DAC C as Test 22.06 Set DAC D as Test 22.05 Set DAC F as Test 19.01 Set DAC G as Test 20.01 SK502 Input =Freq. 173.975MHz Level –113dBm Mod. 1kHz Dev. 3kHz	PL351,43 (RXS) via AF Filter SK502 Input Level as given by RF Signal Generator 1	>=20dB	Measure the SINAD, Psophometrically weighted, at the AF Filter output. Filter de-emphasis selected.

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
23.04	Rx Sensitivity at 173.975MHz 12.5 kHz bandwidth	Set to Receive on 173.975MHz BWS = Logic 1 Set DAC A as Test 18.01 Set DAC B as Test 16.01 Set DAC C as Test 22.06 Set DAC D as Test 22.05 Set DAC F as Test 19.01 Set DAC G as Test 20.01 SK502 Input =Freq. 173.975MHz Level -107dBm Mod. 1kHz Dev. 1.5kHz	PL351,43 (RXS) via AF Filter SK502 Input Level as given by RF Signal Generator 1	>=20dB	Measure the SINAD, Psophometrically weighted, at the AF Filter output. Filter de-emphasis selected..
24.01	Wideband Frequency Response @ 8kHz	Set to Receive on 154.025MHz Set DAC A as Test 18.01 Set DAC B as Test 16.03 Set DAC C as Test 22.04 Set DAC D as Test 22.03 Set DAC F as Test 19.01 Set DAC G as Test 20.01 SK502 Input =Freq. 154.025MHz Level -60dBm Mod. (a) 1kHz, (b) 8kHz Dev. 5kHz	PL351,43 (RXS) Level as measured by the Audio Analyser	0.0dB to -5 dB	Checks the receiver frequency response for 8kHz modulation in a 25kHz channel. Measure RXS level with 1kHz modulation and store the result. Repeat the measurement with 8kHz modulation. Result is the RXS level at 8kHz modulation with respect to the RXS level at 1kHz modulation.
24.02	Wideband Frequency Response @ 6kHz	Set to Receive on 154.025MHz Set DAC A as Test 18.01 Set DAC B as Test 16.01 Set DAC C as Test 22.04 Set DAC D as Test 22.03 Set DAC F as Test 19.01 Set DAC G as Test 20.01 SK502 Input = Freq. 154.025MHz Level -60dBm Mod. 6kHz Dev. 5kHz	PL351,43 (RXS) Level as measured by the Audio Analyser	0.0dB to -3.5 dB	Checks the receiver frequency response for 6kHz modulation in a 25kHz channel. Result is with respect to the RXS level measured at 1kHz modulation in Test 24.01.

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
24.03	Wideband Frequency Response @ 8kHz 12.5kHz Bandwidth	Set to Receive on 154.025MHz BWS = Logic 1 Set DAC A as Test 18.01 Set DAC B as Test 16.03 Set DAC C as Test 22.04 Set DAC D as Test 22.03 Set DAC F as Test 19.01 Set DAC G as Test 20.01 SK502 Input = Freq. 154.025MHz Level -60dBm Mod. 8kHz Dev. 5kHz	PL351,43 (RXS) Level as measured by the Audio Analyser	-20 to -90 dB	Checks the receiver frequency response for 8kHz modulation in a 12.5kHz channel. This test verifies that the 12.5kHz filter is correctly selected by the receiver. Result is with respect to the RXS level measured at 1kHz modulation in Test 24.01.
24.04	Rx Hum and Noise at 173.975MHz	Set to Receive on 173.975MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 Set DAC C as Test 22.06 Set DAC D as Test 22.05 Set DAC F as Test 19.01 Set DAC G as Test 20.01 SK502 Input = Freq. 173.975MHz Level -60dBm Mod. 1kHz Dev. (a) 3kHz, (b) OFF	PL351,43 (RXS) via AF Filter as measured by the Audio Analyser	30.0dB to 99.0dB	(a) Measure the audio level at the AF filter output with 3kHz deviation at SK502. (b) Repeat with carrier only at SK502. Result is the level obtained in (a) with respect to that obtained in (b). Filter de-emphasis selected.
24.05	Rx Distortion	As per 90775/13/310		< 5 %	
25.01	Squelch Calibration No Signal 25kHz Bandwidth	Set to Receive on 173.975MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 Set DAC C as Test 22.06 Set DAC D as Test 22.05 Set DAC F as Test 19.01 Set DAC G as Test 20.01	PL351,33 (CSQ) Number of pulses as measured by the Counter	187 to 237	Measure the Pulse Repetition Rate at PL351,33 (CSQ) with no signal at SK502. Calculate and record the number of pulses that would occur in a 26ms window ($WSquel_{NS}$). Save the value of $WSquel_{NS}$ for use later.

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
25.02	Squelch Calibration Sig = -116dBm 25kHz Bandwidth	Set to Receive on 173.975MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 Set DAC C as Test 22.06 Set DAC D as Test 22.05 Set DAC F as Test 19.01 Set DAC G as Test 20.01 SK502 Input = Freq. 173.975MHz Level = -116dBm Mod. 1kHz Dev. 4.5kHz	PL351,43 (RXS) via AF Filter PL351,33 (CSQ) Number of pulses as measured by the Counter	28 to 100	Measure the Pulse Repetition Rate at PL351,33 (CSQ). Calculate and record the number of pulses that would occur in a 26ms window ($WSquel_{-116dBm}$). Save the value of $WSquel_{-116dBm}$ for use later.
25.03	Squelch Calibration No Signal 12.5kHz Bandwidth	Set to Receive on 173.975MHz BWS = Logic 1 Set DAC A as Test 18.01 Set DAC B as Test 16.05 Set DAC C as Test 22.06 Set DAC D as Test 22.05 Set DAC F as Test 19.01 Set DAC G as Test 20.01	PL351,33 (CSQ) Number of pulses as measured by the Counter	87 to 137	Measure the Pulse Repetition Rate at PL351,33 (CSQ) with no signal at SK502. Calculate and record the number of pulses that would occur in a 26ms window ($NSquel_{NS}$). Save the value of $NSquel_{NS}$ for use later.
25.04	Squelch Calibration Sig = -116dBm 12.5kHz Bandwidth	Set to Receive on 173.975MHz BWS = Logic 1 Set DAC A as Test 18.01 Set DAC B as Test 16.05 Set DAC C as Test 22.06 Set DAC D as Test 22.05 Set DAC F as Test 19.01 Set DAC G as Test 20.01 SK502 Input = Freq. 173.975MHz Level= -116dBm Mod. 1kHz Dev. 2.25kHz	PL351,43 (RXS) via AF Filter PL351,33 (CSQ) Number of pulses as measured by the Counter	6 to 58	Measure the Pulse Repetition Rate at PL351,33 (CSQ). Calculate and record the number of pulses that would occur in a 26ms window ($NSquel_{-116dBm}$). Save the value of $NSquel_{-116dBm}$ for use later.
25.05	Squelch Data			Sat / Unsat	Recall $WSquel_{-116dBm}$ and $NSquel_{-116dBm}$ Load squelch data into Flash as follows :- In the four Wsquel locations store $WSquel_{-116dBm}$ In the four Nsquel locations store $NSquel_{-116dBm}$

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
26.01	RX Current Consumption	Set to Receive on 173.975MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 Set DAC C as Test 22.06 Set DAC D as Test 22.05 Set DAC F as Test 19.01 Set DAC G as Test 20.01 SK502 Input = Freq. 173.975MHz Level -60dBm Mod. 1kHz Dev. 3kHz	Current into PL301,6 (7V5B) as measured by the DMM	150mA to 120mA	Checks the 7.5V current in receive mode.
26.02	Economise Current Consumption	Set all DACs to 0 Programme the Synthesiser with the STANDBY STATUS WORD as specified in MTR026, Section 4.3.2.2	Current into PL301,6 (7V5B) as measured by the DMM	120 to 100mA	Checks the 7.5V current in economise mode.
27.01	TX Power 154.000MHz RF Level Calibration 10mW Nominal	Set to Transmit on 154.000MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 PL301,8 (10V_TX) = 10V	SK502 Output Power as measured by the Modulation Analyser	5mW to 20mW	Adjust DAC C for closest to nominal Output Power and within the specified limits. Store DAC C value for use in future tests.
27.02	TX Power 154.000MHz DAC Value, 10mW Nominal		DAC C Value as given by the Test System	30 to 50	Note the value of DAC C from Test 27.01 and check it is within specified limits.

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
27.03	Tx Power Curve Fit, 10mW Nominal			Sat / Unsat	Produce DAC values for the other frequencies by multiplying the 154 MHz value from Test 27.01 by a scaling factor as follows (round to the nearest integer):- DAC value (136MHz) = DAC value (154MHz) x 0.9 DAC value (144MHz) = DAC value (154MHz) x 0.93 DAC value (164MHz) = DAC value (154MHz) x 1.07 DAC value (174MHz) = DAC value (154MHz) x 1.07 Fit a straight line between calibration points for 10mW output and thus derive DAC values for EEPROM locations specified in MTR026, Table 10 - PA LEVEL (HIGH).The value calculated for each location should be centred on the range of frequencies covered by that location. For example, the DAC value for 138MHz is calculated for 139MHz. The DAC C values at the test frequencies and from the above scaling calculations should be directly loaded into the relevant EEPROM locations. All interpolated DAC values should be rounded up to the next integer value below the calculated value and then loaded into the relevant EEPROM locations.
28.01	TX Power 136.000MHz RF Level Calibration 0.5 W Nominal	Set to Transmit on 136.000MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 PL301,8 (10V_TX) = 10V	SK502 Output Power as measured by the Modulation Analyser	0.4 W to 0.6 W	Adjust DAC C for closest to nominal Output Power and within the specified limits. Store DAC C value for use in future tests.
28.02	TX Power 136.000MHz DAC Value, 0.5 W Nominal		DAC C Value as given by the Test System	65 to 85	Note the value of DAC C from Test 28.01 and check it is within specified limits.
28.03	TX Power 144.000MHz RF Level Calibration 0.5 W Nominal	Set to Transmit on 144.000MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 PL301,8 (10V_TX) = 10V	SK502 Output Power as measured by the Modulation Analyser	0.4 W to 0.6 W	Adjust DAC C for closest to nominal Output Power and within the specified limits. Store DAC C value for use in future tests.

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
28.04	TX Power 144.000MHz DAC Value, 0.5 W Nominal		DAC C Value as given by the Test System	65 to 85	Note the value of DAC C from Test 28.03 and check it is within specified limits.
28.05	TX Power 154.000MHz RF Level Calibration 0.5 W Nominal	Set to Transmit on 154.000MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 PL301,8 (10V_TX) = 10V	SK502 Output Power as measured by the Modulation Analyser	0.4 W to 0.6 W	Adjust DAC C for closest to nominal Output Power and within the specified limits. Store DAC C value for use in future tests.
28.06	TX Power 154.000MHz DAC Value, 0.5 W Nominal		DAC C Value as given by the Test System	65 to 85	Note the value of DAC C from Test 28.05 and check it is within specified limits.
28.07	TX Power 164.000MHz RF Level Calibration 0.5 W Nominal	Set to Transmit on 164.000MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 PL301,8 (10V_TX) = 10V	SK502 Output Power as measured by the Modulation Analyser	0.4 W to 0.6 W	Adjust DAC C for closest to nominal Output Power and within the specified limits. Store DAC C value for use in future tests.
28.08	TX Power 164.000MHz DAC Value, 0.5 W Nominal		DAC C Value as given by the Test System	65 to 85	Note the value of DAC C from Test 28.07 and check it is within specified limits.
28.09	TX Power 174.000MHz RF Level Calibration 0.5 W Nominal	Set to Transmit on 174.000MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 PL301,8 (10V_TX) = 10V	SK502 Output Power as measured by the Modulation Analyser	0.4 W to 0.6 W	Adjust DAC C for closest to nominal Output Power and within the specified limits. Store DAC C value for use in future tests.
28.10	TX Power 174.000MHz DAC Value, 0.5 W Nominal		DAC C Value as given by the Test System	65 to 85	Note the value of DAC C from Test 28.09 and check it is within specified limits.

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
28.11	Tx Power Curve Fit, 0.5 W Nominal			Sat / Unsat	Using the data from Tests 28.01, 28.03, 28.05, 28.07 and 28.09 fit a straight line between calibration points for 500mW output and thus derive DAC values for EEPROM locations specified in MTR026, Table 10 - PA LEVEL (HIGH).The value calculated for each location should be centred on the range of frequencies covered by that location. For example, the DAC value for 138MHz is calculated for 139MHz. The DAC C values obtained at the test frequencies should be directly loaded into the relevant EEPROM locations. All interpolated DAC values should be rounded up to the next integer value below the calculated value and then loaded into the relevant EEPROM locations. The value stored for 172MHz (i.e. the result of Test 28.09) should be repeated for 174MHz.
29.01	TX Power 136.000MHz RF Level Calibration 2.0 W Nominal	Set to Transmit on 136.000MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 PL301,8 (10V_TX) = 10V	SK502 Output Power as measured by the Modulation Analyser	1.8 W to 2.2 W	Adjust DAC C for closest to nominal Output Power and within the specified limits. Store DAC C value for use in future tests.
29.02	TX Power 136.000MHz DAC Value, 2.0 W Nominal		DAC C Value as given by the Test System	125 to 145	Note the value of DAC C from Test 29.01 and check it is within specified limits.
29.03	TX Current 136.000MHz	Set to Transmit on 136.000MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 Set DAC C as Test 29.01 PL301,8 (10V_TX) = 10V	Current into PL301,8 (10V_TX) as measured by the DMM	100 to 700 mA	Set DAC C as Test 29.01 result.
29.04	TX Power 144.000MHz RF Level Calibration 2.0 W Nominal	Set to Transmit on 144.000MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 PL301,8 (10V_TX) = 10V	SK502 Output Power as measured by the Modulation Analyser	1.8 W to 2.2 W	Adjust DAC C for closest to nominal Output Power and within the specified limits. Store DAC C value for use in future tests.

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
29.05	TX Power 144.000MHz DAC Value, 2.0 W Nominal		DAC C Value as given by the Test System	125 to 145	Note the value of DAC C from Test 27.04 and check it is within specified limits.
29.06	TX Current 144.000MHz	Set to Transmit on 144.000MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 Set DAC C as Test 29.04 PL301,8 (10V_TX) = 10V	Current into PL301,8 (10V_TX) as measured by the DMM	100 to 700 mA	Set DAC C as Test 29.04 result.
29.07	TX Power 154.000MHz RF Level Calibration 2.0 W Nominal	Set to Transmit on 154.000MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 PL301,8 (10V_TX) = 10V	SK502 Output Power as measured by the Modulation Analyser	1.8 W to 2.2 W	Adjust DAC C for closest to nominal Output Power and within the specified limits. Store DAC C value for use in future tests.
29.08	TX Power 154.000MHz DAC Value, 2.0 W Nominal		DAC C Value as given by the Test System	125 to 145	Note the value of DAC C from Test 27.07 and check it is within specified limits.
29.09	TX Current 154.000MHz	Set to Transmit on 154.000MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 Set DAC C as Test 29.07 PL301,8 (10V_TX) = 10V	Current into PL301,8 (10V_TX) as measured by the DMM	100 to 700 mA	Set DAC C as Test 29.07 result.
29.10	TX Power 164.000MHz RF Level Calibration 2.0 W Nominal	Set to Transmit on 164.000MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 PL301,8 (10V_TX) = 10V	SK502 Output Power as measured by the Modulation Analyser	1.8 W to 2.2 W	Adjust DAC C for closest to nominal Output Power and within the specified limits. Store DAC C value for use in future tests.
29.11	TX Power 164.000MHz DAC Value, 2.0 W Nominal		DAC C Value as given by the Test System	125 to 145	Note the value of DAC C from Test 29.10 and check it is within specified limits.

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
29.12	TX Current 164.000MHz	Set to Transmit on 164.000MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 Set DAC C as Test 29.10 PL301,8 (10V_TX) = 10V	Current into PL301,8 (10V_TX) as measured by the DMM	100 to 700 mA	Set DAC C as Test 29.10 result.
29.13	TX Power 174.000MHz RF Level Calibration 2.0 W Nominal	Set to Transmit on 174.000MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 PL301,8 (10V_TX) = 10V	SK502 Output Power as measured by the Modulation Analyser	1.8 W to 2.2 W	Adjust DAC C for closest to nominal Output Power and within the specified limits. Store DAC C value for use in future tests.
29.14	TX Power 174.000MHz DAC Value, 2.0 W Nominal		DAC C Value as given by the Test System	125 to 145	Note the value of DAC C from Test 29.13 and check it is within specified limits.
29.15	TX Current 174.000MHz	Set to Transmit on 174.000MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 Set DAC C as Test 29.13 PL301,8 (10V_TX) = 10V	Current into PL301,8 (10V_TX) as measured by the DMM	100 to 700 mA	Set DAC C as Test 29.13 result.
29.16	Tx Power Curve Fit, 2.0 W Nominal			Sat / Unsat	Using the data from Tests 29.01, 29.04, 29.07, 29.10 and 29.13 fit a straight line between calibration points for 2.0W output and thus derive DAC values for EEPROM locations specified in MTR026, Table 10 - PA LEVEL (HIGH).The value calculated for each location should be centred on the range of frequencies covered by that location. For example, the DAC value for 138MHz is calculated for 139MHz. The DAC C values obtained at the test frequencies should be directly loaded into the relevant EEPROM locations. All interpolated DAC values should be rounded up to the next integer value below the calculated value and then loaded into the relevant EEPROM locations. The value stored for 172MHz (i.e. the result of Test 29.13) should be repeated for 174MHz.

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
30.01	FM Deviation Calibration 136.000MHz	Set to Transmit on 136.000MHz Set DAC A as Test 18.01 Set DAC B as Test 16.01 Set DAC C as Test 29.01 PL301,8 (10V_TX) = 10V PL351,31(MAF) = Freq. (i) 5kHz (ii) 50Hz Level 1.3V pk-pk Sinewave centred on +2.5V dc	SK502 Output Deviation as measured by the Modulation Analyser	Sat / Unsat	Set DIGIPOT 2 to 128 initially. (i) Set PL351,31(MAF) frequency to 5kHz. Adjust DIGIPOT 1 for 4.85kHz ± 50Hz deviation. (ii) Set PL351,31(MAF) frequency to 50Hz. Adjust DIGIPOT 2 for 4.85kHz ± 50Hz deviation. Repeat Steps (i) and (ii) alternately until neither DIGIPOT value changes to meet the deviation limits. Deviation measurement should be peak to peak deviation divided by 2. Save final values of DIGIPOT_1 and DIGIPOT 2 for use in future tests.
30.02	VCO_MOD Calibration Value, 136.000MHz		DIGIPOT 1 Value as given by the Test System	171 to 200	Note the value of DIGIPOT 1 from Test 30.01 and check it is within specified limits.
30.03	REF_MOD Calibration Value, 136.000MHz		DIGIPOT 2 Value as given by the Test System	148 to 176	Note the value of DIGIPOT 2 from Test 30.01 and check it is within specified limits.
30.04	FM Deviation Calibration 154.500MHz	Set to Transmit on 154.000MHz Set DAC A as Test 18.01 Set DAC B as Test 16.03 Set DAC C as Test 29.07 PL1,17 PL351,31(MAF) = Freq. (i) 5kHz (ii) 50Hz Level 1.3V pk-pk Sinewave centred on +2.5V dc	SK502 Output Deviation as measured by the Modulation Analyser	Sat / Unsat	Set DIGIPOT 2 to 128 initially. (i) Set PL351,31(MAF) frequency to 5kHz. Adjust DIGIPOT 1 for 4.85kHz ± 50Hz deviation. (ii) Set PL351,31(MAF) frequency to 50Hz. Adjust DIGIPOT 2 for 4.85kHz ± 50Hz deviation. Repeat Steps (i) and (ii) alternately until neither DIGIPOT value changes to meet the deviation limits. Deviation measurement should be peak to peak deviation divided by 2. Store final values of DIGIPOT_1 and DIGIPOT 2 for use in future tests.
30.05	VCO_MOD Calibration Value, 154.000MHz		DIGIPOT 1 Value as given by the Test System	122 to 150	Note the value of DIGIPOT 1 from Test 30.04 and check it is within specified limits.
30.06	REF_MOD Calibration Value, 154.000MHz		DIGIPOT 2 Value as given by the Test System	133 to 158	Note the value of DIGIPOT 2 from Test 30.04 and check it is within specified limits.

Test No.	Parameter	Stimulus	Monitor	Limit	Notes
30.07	FM Deviation Calibration 174.000MHz	Set to Transmit on 174.000MHz Set DAC A as Test 18.01 Set DAC B as Test 16.05 Set DAC C as Test 29.13 PL301,8 (10V_TX) = 10V PL351,31(MAF) = Freq. (i) 5kHz (ii) 50Hz Level 1.3V pk-pk Sinewave centred on +2.5V dc	SK502 Output Deviation as measured by the Modulation Analyser	Sat / Unsat	Set DIGIPOT 2 to 128 initially. (i) Set PL351,31(MAF) frequency to 5kHz. Adjust DIGIPOT 1 for 4.85kHz ± 50Hz deviation. (ii) Set PL351,31(MAF) frequency to 50Hz. Adjust DIGIPOT 2 for 4.85kHz ± 50Hz deviation. Repeat Steps (i) and (ii) alternately until neither POT value changes to meet the deviation limits. Deviation measurement should be peak to peak deviation divided by 2. Store final values of DIGIPOT_1 and DIGIPOT 2 for use in future tests.
30.08	VCO_MOD Calibration Value, 174.000MHz		DIGIPOT 1 Value as given by the Test System	78 to 100	Note the value of DIGIPOT 1 from Test 30.07 and check it is within specified limits.
30.09	REF_MOD Calibration Value, 174.000MHz		DIGIPOT 2 Valueas given by the Test System	116 to 138	Note the value of DIGIPOT 2 from Test 30.07 and check it is within specified limits.
30.10	VCO_MOD Curve Fit			Sat / Unsat	Using the DIGIPOT 1 data from Tests 30.01, 30.04, and 30.07 fit a straight line between calibration points and determine the (DIGIPOT 1) data values for EEPROM locations specified in MTR026, Table 11 (VCO). Note that the frequencies given in Table 11 are the lower bounds and the relevant data values are determined for 0.5MHz above these, at the centre of the location's frequency range. For example, the DIGIPOT 1 value for VHF FREQ. = 137MHz is calculated for 137.5MHz. The measured DIGIPOT 1 values should be directly loaded into the relevant EEPROM locations. All the interpolated DIGIPOT 1 values should be rounded down to the next integer value below the calculated value and then loaded into the relevant EEPROM locations. The value stored for 173MHz (DIGIPOT 1 result of Test 30.07) should be repeated for 174MHz.