# Operational Description

The transmit chain of the SR528 consists of a direct LO modulation transmit path for GSM (GMSK). The LO is modulated directly by the baseband signal by a digital delta-sigma modulator. The modulated output of the modulator is mixed with a DC voltage and the resultant output is then converted to a single ended waveform via an on chip balun. The RF output power level is adjusted to an appropriate level via the on chip RF attenuator.
The RF ports of the transmitter are single-ended and matched to 50Ω. No off-chip RF baluns or filters are required.

**Frequency Sources**

There are two frequency sources on the SR528. The first is the RF frequency synthesizer, which serves as the LO for both receive and transmit chains. The VCO for the synthesizer is fully integrated and no calibration is required as this is all performed automatically on the SR528. During reception or transmission in normal operation, the frequency synthesizer is operated at twice the desired channel of operation in PCS and DCS modes and at four times the desired channel of operation in EGSM and USGSM modes. On-chip dividers (÷2 for PCS/DCS and ÷4 EGSM/USGSM) reduce the frequency of the signal. The outputs of these dividers are buffered before being applied to the up or down converters. The loop filter of the frequency synthesizer is fully integrated. This reduced component count and form factor minimizes the number of sensitive components in the design.

The second frequency source is the Digitally Controlled Crystal Oscillator (DCXO). The DCXO is designed to accept a crystal with fundamental frequency of 26MHz. After power-on of the chip, the DCXO starts oscillating. It continues oscillating until power-off or programming of doze mode.
The reference oscillator can be used with a 26MHz crystal. In this configuration, the reference frequency is controlled by on-chip capacitor banks that can be switched in via the RCB. This allows for precise tuning of the crystal when implemented with a conventional Automatic Frequency Control (AFC) loop.
The SR528 can also be supplied with an external reference such as a 26MHz VCTCXO or other frequency source.
The reference clock signal generated in the chip is buffered before being sent to the Phase Locked Loop in the frequency synthesizer block. Either a square wave or a clipped sine wave can be selected. The buffer is capable of driving a reference clock line with a load capacitance of 10pF.
There are two 26MHz reference clock output ports on the SR528, REF OUT and REF2 OUT. Each output is independently controlled by its enable ports, REF EN and REF2 EN.