Medtronic MINIMED

SPECIFICATION

Doc Desc:

MMT-3160 PPC Hardware Design Description

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A	5-8087	Production Release	LT		
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TABLE OF CONTENTS

1.0 PURPOSE

The purpose of this document is to describe design details of the MMT-3160 Personal Programming Communicator (PPC) board hardware.

2.0 SCOPE

This document covers the design of the MMT-3160 PPC electronic hardware.

3.0 ASSOCIATED DOCUMENTS

3.1	9013174	Schematics, MMT-3160 PPC
3.2	9013175	Schematics, PLD Circuit, MMT-3160 PPC
3.3	6053154	Layout, MMT-3160 PPC
3.4	ES1160	Specifications, MMT-3160 PPC Hardware/Software Interface
3.5	RD1142	Requirements, MMT-3160 PPC Hardware
3.6	DD1008	Design Description, Processor IC

4.0 DEFINITIONS AND ABBREVIATIONS

4.1	ADC	Analog to Digital Converter
4.2	EEPROM	Electrical Erasable Programmable Read Only Memory
4.3	IC	Integrated Circuit
4.4	I/O	Input/Output
4.5	IrDA	Infrared Data Association
4.6	IU	Implant Unit - An Medtronic MiniMed product
4.7	LCD	Liquid Crystal Display
4.8	PPC	Personal Programming Communicator
4.9	RAM	Random Access Memory
4.10	ROM	Read Only Memory
4.11	UART	Universal Asynchronous Receiver Transmitter
4.12	EL	Electro luminescent
4.13	EMI	Electro-Magnetic Interference
4.14	ESD	Electro Static Discharge
4.15	PCB	Printed Circuit Board
4.16	CPLD	Complex Programmable Logic Device

5.0 OVERVIEW

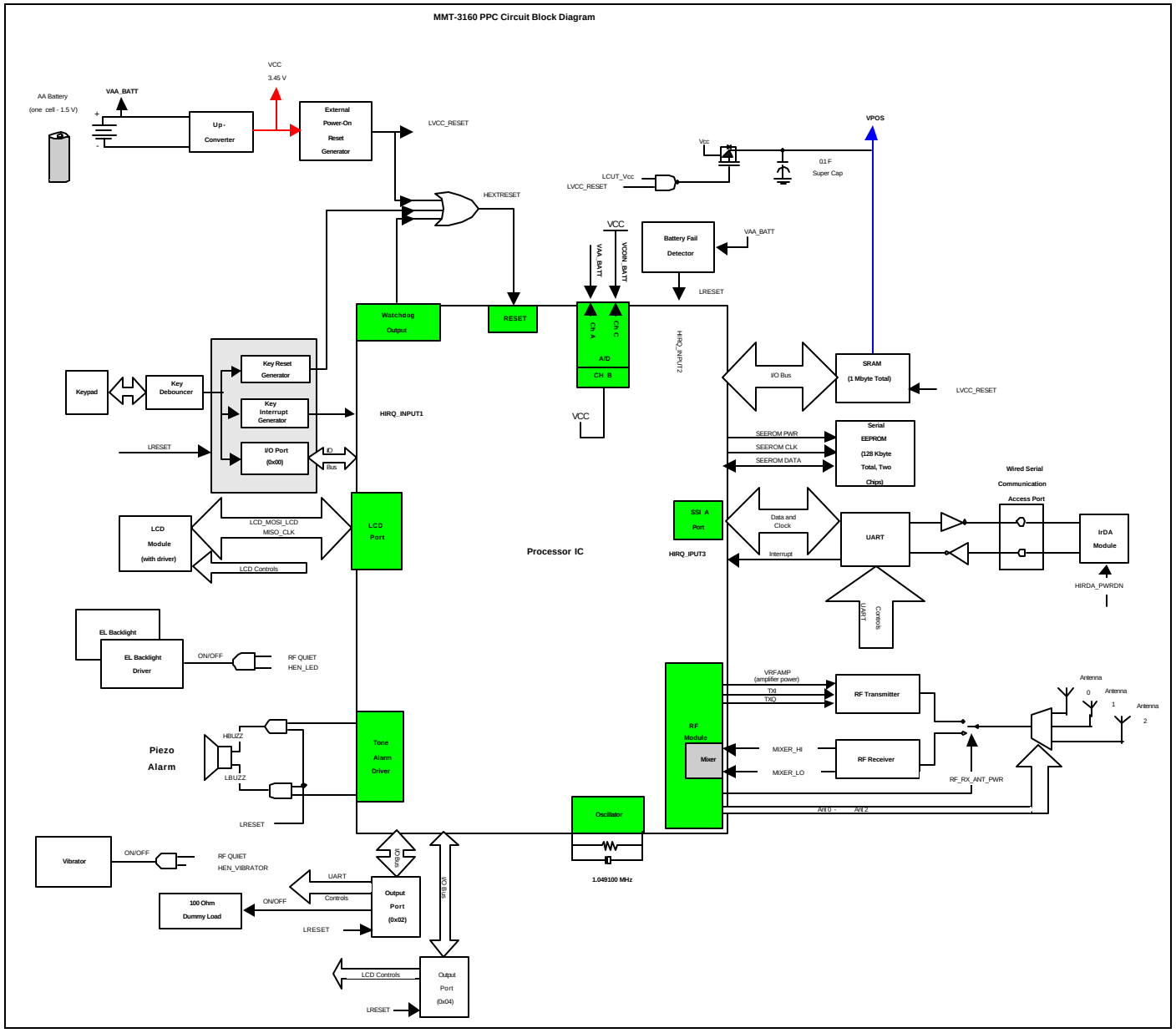
5.1 The PPC device is used to communicate with Medtronic MiniMed implantable devices such as Implantable Glucose Monitor (IGM) and implantable insulin pumps, collectively called Implant Unit (IU).

5.2 The PPC device is to be carried externally by a patient who has an implant unit.

5.3 The circuit contains an up-converter, external serial ROM (SEEPROM), vibrator for vibrational alarm, piezo for tone alarm, RF circuitry for 131KHz telemetry, processor of the system (Medtronic MiniMed custom Processor IC), external SRAM, power manager, external IO, LCD, EL backlight, UART/IrDA port, keypad connector, interrupt generator and other supporting logic circuitry. Block diagram of the PPC is given in *Figure 1: PPC Block Diagram*

5.4 This device is considered an incremental upgrade to the existing MMT-315x PPC. Therefore, it is an intention to make necessary improvements based on the MMT-315x models yet keeping the software changes minimal. For this reason, major circuit design and component selections are carried over from the MMT-315x models where possible.

Figure 1: PPC Block Diagram



6.0 DETAILED DESIGN DESCRIPTION

6.1 Power

6.1.1 The main source of power to the entire circuit is a single AA battery (the main battery - VAABATT). This voltage is up converted to +3.45 V as VCC by a switching type up-converter. VCC is the main operating power for the circuit.

6.1.2 A secondary operating power, VPOS, is connected to the system's external SRAM as its supply voltage. As will be discussed more in subsequent sections, VPOS is derived from VCC, backed up by a super cap, and used to power the SRAM in long term memory backup mode and to power the entire circuit when the up-converter is shutdown temporarily in some situations.

6.1.3 A 0.1 Farad super capacitor (C5, the backup capacitor or the super cap) is connected to VPOS. When VCC is normally supplied by the up-converter, it charges the super cap and keeps it in the charged state. When the up-converter no long supplies VCC, either due that the up-converter is being temporarily shut down (during RF reception, for example) or due to depleted main battery (including battery removal), the super cap will support both VCC and VPOS until either the VCC voltage goes down to 2.87V or when the processor asserts HCUT_VCC, whichever comes first. At that time, a switch (Q1) will cut off the connection between VCC and VPOS. From that point on, the super cap will only supply for VPOS to keep the external SRAM powered for as long as the charge in the capacitor will last. See table below for more details.

6.1.4 Also counted as a supply voltage is LCD_VCC. This is the output of a low dropout linear regulator U16. The nominal level is set to 2.87V. This voltage is used to power the LCD module only.

6.1.5 The AA battery source is brought in through connector CN5.

6.1.6 The AA battery voltage is connected to ADC channel "A" of the processor for voltage monitoring.

6.1.7 The VCC voltage is connected to ADC channel "B" internally to the processor IC for voltage monitoring.

6.1.8 In selecting the nominally 3.45V VCC voltage and the nominally 2.87V LCD_VCC voltage, the following are the major considerations.

6.1.8.1 VCC should be low voltage for low power operation. Some components selected are of low voltage rated components with the recommended maximum supply voltage of 3.6 V.

6.1.8.2 VCC should be high enough to provide adequate working voltage differential so that there is enough stored energy for orderly shutdown after battery removal. Working voltage differential here is the difference between the initial VCC voltage and the final VCC voltage at which low VCC is detected (LVCC_RESET asserts, at which the circuit is in hardware controlled system power-down state).

6.1.8.3 VCC should be high enough to provide adequate working voltage differential so that there is enough stored energy for long-term memory backup. Working voltage differential here is the difference between the initial VPOS voltage entering memory backup mode and the specified minimum external SRAM data retention voltage.

6.1.8.4 VCC should be high enough to provide adequate working voltage differential so that there is enough stored energy for circuit backup during the short periods when the up-converter is shut down in RF QUIET mode.

The voltage differential here is the difference between the initial VCC voltage when the up-converter is shut down and the voltage at which LCD_VCC is out of regulation. When LCD_VCC is out of regulation, LCD contrast change might be noticeable by the user, which is undesirable.

6.1.9 *Table 1: Powers* shows more details on the powers.

Table 1: Powers	
VCC voltage (main power)	3.45 V, +/-100 mV, supporting a max load of 30 ohm connected to it, with battery voltage of 1.15 V to 1.8 V measured at the input of the up-converter
main power source (AA battery)	One AA battery (nominally 1.5 V), typically alkaline type, lithium AA cell with voltage up to 1.8V acceptable
VPOS voltage (secondary power)	Within 50mV of VCC when VCC is at normal level
LCD_VCC	2.87 V +/-3%

6.2 Power Management

6.2.1 The functions of the power management circuit are as followed: a) to provide proper power-up reset; b) to provide backup power for the on-board SRAM; c) to provide interrupt signal to inform the processor when battery is low; d) and to provide adequate time for orderly system shut-down when the main battery is dead or removed.

6.2.2 Battery Voltage and VCC Voltage Monitoring By The Processor

6.2.2.1 The AA battery voltage, VAABATT, is connected to ADC channel “A” of the processor for voltage monitoring by the processor.

6.2.2.2 It is expected that the software will make battery voltage measurements and provide warning of low battery at a voltage level higher than the depleted battery voltage level which will be detected by the hardware. To ensure enough pre-warning of low battery conditions, it is expected that the measurements would be done under load, using dummy load R30.

6.2.2.3 The dummy load is a 100 ohm load connected to VCC for a typical load current of 34.5 mA from VCC. Because of the high load, for battery life consideration, it is not recommended that this load is used often. Battery voltage measurement of once per day under this load is recommended.

6.2.2.4 The VCC voltage is connected to ADC channel “B” internally to the processor IC for voltage monitoring by the processor.

6.2.2.5 ADC channel “C” was used in MMT315x models to measure the backup coin battery voltage. Coin battery is not used in this circuit. This channel is now connected to VCC so that MMT315x model software can run on this hardware without changing with respect to this item.

6.2.2.6 VCC is a regulated voltage of nominally 3.45 V. If this voltage is out of range, it might be caused by the following: a) the battery voltage is too low, typically below 0.9V; b) the up-converter circuit has problem; c) the entire circuit is taking too much power (typically greater than 60mA at 3.45 V, this current is also battery condition dependent).

6.2.2.7 VCC can be measured periodically, but not necessarily under load, for the purpose of detecting faulty conditions. It should be noted that this measurement should not be relied upon for battery voltage tracking. This is because when VCC is too low, most likely the battery is already deeply depleted. It should be enough to rely on the hardware VCC voltage detection for power management purposes.

6.2.3 Hardware Battery Voltage Detector And Depleted Battery State

6.2.3.1 A battery voltage detector is implemented with U7, R4, R5, R6 and C76. The output signal is named LRESET (low asserted). The designed detection threshold is 1.0 V on battery voltage falling and 1.16 V on voltage rising. At 1.0 V battery voltage, VCC is still in the normal level of 3.45 V, but the battery cannot support heavy loads. When the battery gets close to this level, activating high load activities such as turning on the vibrator would most likely cause the battery voltage to dip below this threshold level, which will trigger a hardware low battery shutdown, but with enough time provided for orderly shutdown. For this reason, it is expected that the software would do regular battery voltage measurements and issue low battery warning at a higher level so that enough warning is provided before this state.

6.2.3.2 U7 is a voltage comparator (MAX837EUS, Maxim). The internal threshold is typically 1.204V +/-1%. In order to have the detection battery voltage threshold of 1.0 V, which is lower than the internal threshold, VCC is used as the reference point instead of the normally used system ground.

6.2.3.3 R6 is used to provide hysteresis. In the event of battery voltage rising (battery insertion, for example), the detection threshold is determined by the facts that R4 connects to VAABATT (battery voltage), R5 connects to VCC and R6 connects to GND (because LRESET is asserted at that point). In the event of battery voltage falling (battery natural depletion or battery removal), the detection threshold is determined by the facts that R4 connects to VAABATT (battery voltage), R5 connects to VCC and R6 also connects to VCC (because LRESET is de-asserted at that point). This way, the circuit will only starts operating (when LRESET de-asserts) when the battery voltage is high and VCC is up to the normal level in battery insertion event; and the circuit will only stops operating as the battery drops really low. See Table 3: Other Battery Detector Parameters for more details.

6.2.3.4 This hysteresis also ensures that LRESET is clean of glitches as the battery voltage rises and falls.

6.2.3.5 Because of the hysteresis, when a battery is inserted, or when the battery has gradually depleted, the circuit might be in a state such that the up-converter is fully operational, but the system is locked from powering up due to the assertion of LRESET. The voltage at which the circuit is allowed to start normal operation is the rising battery voltage threshold. This design prevents an oscillation condition that when a very weak battery is inserted, the system starts to boot up, then higher power demand from the very weak battery causes a rapid battery voltage drop, causing LRESET to be asserted, the system is then put back to power-down state.

6.2.3.6 HRESET, the inverted state of LRESET, is used as a power-fail interrupt signal to the processor. This interrupt signal is fed directly to the HIRQ_INPUT2 input of the processor. The software is expected to

perform orderly shutdown when it receives this interrupt. In this design, because the use of the super cap, the time for the software to perform orderly shutdown is ample. However, it is expected that the software will perform that orderly shutdown timely so that more energy stored in the super cap will be used for long-term backup of the external SRAM.

6.2.3.7 In order to save more energy for long-term SRAM backup, the software is expected to perform timely orderly shutdown, then asserts the signal LCUT_VCC (I/O port 0x02, bit 2). The assertion of LCUT_VCC disconnects VPOS from VCC in a uni-directional fashion, meaning current can go from VCC to VPOS (if VCC is still high) but not the other way around. The connecting PFET gate, Q1, is turned off when LCUT_VCC is asserted, but the intrinsic diode in the PFET would still conduct in the VCC to VPOS direction (with a diode drop in voltage). In the battery removal case, VCC will drop very rapidly when LCUT_VCC is asserted, but the VPOS voltage level will stay. In the case when battery depletes gradually, low VAABATT will cause the assertion of LRESET, which should trigger orderly shutdown. In turn, it will lead to the assertion (software controlled) of LCUT_VCC and the turning off of Q1. At that time, VCC might still be at normal level because that the up-converter can operate down to 0.9 V of VAABATT, so VCC is still supplying VPOS with PFET diode conduction.

6.2.3.8 After orderly shutdown, the software is expected to check the state of LRESET by reading the corresponding I/O bit periodically. It should not attempt to resume normal operation as long as LRESET is asserted. This is because while the initial assertion of LRESET causes an interrupt to the processor, the asserted level would not prevent the processor from attempting to resume normal operation, even though the attempt would not be successful because the lock-out of the devices as listed in Table 2: Depleted Battery State by the asserted LRESET.

6.2.3.9 LRESET is connected to input port 0x00, bit 6 for software reading.

6.2.3.10 When LRESET is asserted, it immediately disables the output ports, which in turn shuts down all high power devices. This is to save more energy in the super cap for orderly shutdown and SRAM backup. Refer to *Table 2: Depleted Battery State* for more information.

Table 2: Depleted Battery State
Key press no longer generates key board interrupt to the processor
5-key reset no longer works
UART disabled, IrDA module shut down
The output ports, 0x02 and 0x04, are cleared
LCD is held in un-selected and reset state
Backlight is disabled
Vibrator is disabled
The 100-ohm dummy load is disabled

Table 3: Other Battery Detector Parameters	
Battery voltage falling detection threshold	1.0 V
Battery voltage rising detection threshold	1.16 V
Time between battery removal and LRESET assertion	Approximately 20 microseconds
When LRESET is asserted:	See table above
Major design considerations	♦ Static power consumption ♦ Voltage detection threshold: on rising, high enough so the circuit would only be allowed to operate when VCC is good and stable; on falling, low enough so the battery energy would be fully utilized, but high enough so power would be available for orderly shutdown (especially high enough so that in any situation, orderly shutdown can be completed before hardware controlled low VCC system power-down would happen) ♦ Immunity to noise, especially due to ESD events ♦ Hysteresis – to avoid oscillation condition due to battery voltage fluctuation
Major components	♦ U7 – Chosen because of low static power consumption, push-pull output, small package.

6.2.4 Hardware VCC Voltage Detector And System Power-down State

6.2.4.1 The VCC voltage detector is comprised of U16, R47, R48, C80 and C75.

6.2.4.2 U16 is an integrated micro-power voltage regulator and voltage detector. U16, in conjunction with R47 and R48, sets the output voltage, LCD_VCC, as well as the threshold for the LVCC_RESET signal.

6.2.4.3 The output voltage, LCD_VCC, is set to:

Voutput = 1.23(1+R47/R48) = 1.23(1+365K/274K) = 2.87 V, +/-3%

6.2.4.4 C80 is a low ESR capacitor needed by U16. C75 provides noise immunity of LVCC_RESET, especially in the event of ESD. For enhanced noise immunity, U16 is well decoupled with a 0.1 uF VCC bypass capacitor placed very close to its VCC pin.

6.2.4.5 This detector detects low VCC voltage level. The threshold is set to:

Vth = 0.925(Vout) = 0.925 X 2.87 = 2.65 V (typ)
Vth = 0.965(Vout) = 0.965 x 2.87 x (1+3%) = 2.85 V (max)
Vth = 0.885(Vout) = 0.885 x 2.87 x (1-3%) = 2.46 V (min)

6.2.4.6 The output of this detector is LVCC_RESET.

6.2.4.7 When VCC falls below the set threshold, LVCC_RESET is asserted. The assertion of this signal disables essentially the entire circuit, with the exception of the processor oscillator. However, the processor is not operational because this signal also holds the processor in reset state by setting HEXTRESET high.

6.2.4.8 In addition, the assertion of this signal disables the accessing of the external SRAM for the purpose of preventing the corruption of the SRAM content by uncontrolled address and data line state changes due to out of spec VCC level.

6.2.4.9 This signal also turns off the VCC to VPOS gate, Q1, if this has not be done so by the processor setting LCUT_VCC. This is the latest time for the circuit to enter memory backup mode. The earlier time would be when the software asserts LCUT_VCC after orderly shutdown.

6.2.4.10 When VCC falls below this threshold, it means that the battery has depleted to a level that it cannot produce a regulated VCC. At this point, it is assumed that the system has been in low battery shutdown state because low battery (LRESET asserted) should have been detected before this point.

Table 4: Hardware VCC Voltage Detector And System Power-Down State

VCC voltage detector output signal	LVCC_RESET
VCC voltage detection threshold	2.85 V (max) 2.65 V (typ) 2.46 V (min)
When LVCC_RESET asserted:	♦ External SRAM, U9, cannot be accessed; SRAM I/O lines tri-stated ♦ Q1 turned off to preserve VPOS power ♦ HEXTRESET is set to static high so processor is held in reset (note that the processor will not operation until this signal is low, or called released from reset state)
Major design considerations	♦ Static power consumption ♦ Low dropout voltage regulation ♦ Linear voltage regulator output (LCD_VCC): VCC voltage detection threshold follows this setting ♦ LCD_VCC has to be capable of powering the LCD module ♦ VCC voltage detection threshold: high enough so VPOS can backup the SRAM for the specified duration, low enough so VCC fluctuation would not cause premature circuit reset ♦ Immunity to noise in the event of ESD (because the output signal, LVCC_RESET, affects the entire circuit operation)
Major component selection considerations	♦ U16 – Max6349TLUT: This part was chosen mainly for its low static state power and the fact that it has a built-in voltage detector. This part is to be active all the time so power consumption is a major consideration. This part has a pre-programmed output voltage, but this is

Table 4: Hardware VCC Voltage Detector And System Power-Down State	
VCC voltage detector output signal	**LVCC_RESET**
	over-ridden by the use of the output voltage setting resistor divider. Lower than the pre-programmed output and detection voltage is desired here. Availability was a factor in selecting this part over other parts in the same family. Push-pull detector output wins over open-drain output to save a pull-up resistor. Low dropout is a must. The 100mA+ output has no problem of powering the LCD module.

6.2.5 Backup Capacitor, Memory Backup and Circuit Power Backup

6.2.5.1 Memory Backup and Circuit Power Backup are implemented with components C5, Q1 and U10. SP1 is for test purposes.

6.2.5.2 A double layer capacitor (super cap), C5, is used as a power backup cell, which supplies VPOS. This source is used to power the external memory in memory backup mode, when the AA battery is absent (depleted or removed) and is used to power the entire circuit when the up-converter is temporarily turned off during RF QUIET mode.

6.2.5.3 The time in RF QUIET mode when the up-converter is shut down, and the super cap is powering the entire circuit is referred to as the circuit power backup mode, or simply circuit backup mode.

6.2.5.4 RF QUIET mode is enabled by setting bit 4 of I/O port 0x04.

6.2.5.5 Q1 connects VCC and VPOS. During normal circuit operation, Q1 is turned on so VCC charges the super cap as well as supplying VPOS.

6.2.5.6 When VCC falls below the low VCC threshold (assertion of LVCC_RESET), or when the processor asserts LCUT_VCC, Q1 is turned off. The connection is cut in the direction of VPOS to VCC, but the direction of VCC to VPOS is still somewhat open by the diode conduction in the PFET.

6.2.5.7 In RF QUIET mode, when the up-converter is shut down by the action of turning on the RF receiver, the software must not assert LCUT_VCC. Doing so will cause a total loss of VCC power.

6.2.5.8 Memory backup duration is required to be a minimum of 1 hour. Actual memory backup duration is calculated as follows:

Table 5 : Power Backup Calculations								
Memory backup time with NEC SuperCap, 0.1F, 5.5V								
SuperCap Use as Memory Backup								
nominal capacitance (F)	capacitance change factor (%)	actual capacitance (F)	starting backup voltage (V)	ending backup voltage (V)	net backup voltage (V)	total charge Q (C)	averaged power consumption I (uA)	calculated backup time (hour)
Fs		Fa	Vi	Vf	Vn	C	I	t

Table 5 : Power Backup Calculations								
Memory backup time with NEC SuperCap, 0.1F, 5.5V								
SuperCap Use as Memory Backup								
	% of spec value	(spec value) x (%)			(Vi - Vf)	(Fa) x (Vn)		((C*1000000)/I)/3600
based on initial cap value								
0.1	-20	0.08	3.45	1.8	1.65	0.132	1	36.7
0.1	-20	0.08	3.45	1.8	1.65	0.132	5	7.3
0.1	-20	0.08	3.3	1.8	1.5	0.12	1	33.3
0.1	-20	0.08	3.3	1.8	1.5	0.12	5	6.7
0.1	-20	0.08	3	1.8	1.2	0.096	1	26.7
0.1	-20	0.08	3	1.8	1.2	0.096	5	5.3
worst case in cap value based on spec								
0.1	-50	0.05	3.45	1.8	1.65	0.0825	1	22.9
0.1	-50	0.05	3.45	1.8	1.65	0.0825	5	4.6
0.1	-50	0.05	3.3	1.8	1.5	0.075	1	20.8
0.1	-50	0.05	3.3	1.8	1.5	0.075	5	4.2
0.1	-50	0.05	3	1.8	1.2	0.06	1	16.7
0.1	-50	0.05	3	1.8	1.2	0.06	5	3.3
lower memory data retention voltage								
0.1	-50	0.05	3.45	1.3	2.15	0.1075	1	29.9
0.1	-50	0.05	3.45	1.3	2.15	0.1075	5	6.0
0.1	-50	0.05	3.3	1.3	2	0.1	1	27.8
0.1	-50	0.05	3.3	1.3	2	0.1	5	5.6
0.1	-50	0.05	3	1.3	1.7	0.085	1	23.6
0.1	-50	0.05	3	1.3	1.7	0.085	5	4.7

6.2.5.9 This super cap also serves the purpose of lessening the burden on the up-converter and the battery in supporting short high power bursts.

6.2.5.10 Another function, as discussed earlier, of the super cap is providing the time for orderly shutdown at battery removal.

6.2.5.11 High power devices such as the vibrator and the backlight, are disabled by hardware in circuit backup mode, when the up-converter is shutdown.

6.2.5.12 The high power dummy load has higher priority RF QUIET mode. This means that if the dummy load is turned on, the up-converter is inhibited from shutting down for that duration.

6.2.5.13 All hardware disabled devices, including the up-converter, during circuit backup mode would automatically be enabled, without affecting the software set states, once RF receive becomes inactive.

6.2.5.14 The software is expected not to perform other tasks, which could result in the consumption of higher than available total charge as specified in Table 5 : Power Backup Calculations, during circuit power mode. Consumption in term of charge is calculated by Q=I * t.

6.2.5.15 The software is expected to de-assert LCUT_VCC during normal operation, only to be asserted after orderly shutdown.

6.2.5.16 The solder pad, SP1, and signal SUPERCAP are provided for ATS testing. In board level testing, SP1 is to be left open so the super cap can be tested by the ATS through the use of the signal SUPERCAP, which is brought to the board-edge connector. After testing, SP1 is to be shorted with solder. It is designed this way because in board level testing, circuit power consumption tests might have to deal with sub-milliamp current measurements. Having a super cap connected in the circuit would make such test difficult because of the relatively long super cap charging period. Isolating the super cap also makes the testing of the super cap itself easier.

6.2.5.17 Circuit power backup calculation is as shown in Table 7: Backup Capacitor, SRAM Backup and Circuit Power Backup.

Table 6: Circuit Power Backup Time Calculation

SuperCap Use as Power Source During RF Receive

nominal capacitance (F)	capacitance change factor (%)	actual capacitance (F)	starting backup voltage (V)	ending backup voltage (V)	net backup voltage (V)	total charge Q (C)	averaged power consumption I (uA)	calculated backup time (second)
based on initial cap value								
0.1	-20	0.08	3.45	3	0.45	0.036	1000	36
worst case in cap value based on spec								
0.1	-50	0.05	3.45	3	0.45	0.0225	1000	22.5

Table 7: Backup Capacitor, SRAM Backup and Circuit Power Backup	
Super cap	0.1 F (nominal)
VCC cannot drop below this voltage in circuit power backup mode to avoid noticeable change in LCD contrast	2.95 V
SRAM data retention voltage	1.8V minimum
In circuit power backup mode:	♦ RF RX on ♦ Up-converter shut down ♦ Vibrator disabled ♦ Backlight disabled ♦ Dummy load on would disable this mode for the duration
Major design considerations	♦ The backup power has to be able to backup SRAM for a minimum of 1 hour. ♦ The backup power has to be able to support circuit operation for a minimum of 1.5 seconds during circuit power backup mode. In this backup mode, VCC cannot drop below 2.95 V to avoid noticeable change in LCD contrast. In other words, LCD_VCC should not be out of regulation. ♦ No coin cell because of higher cost, bigger size and it is perishable. ♦ No lithium rechargeable coin cell because the size of such would be too big for one that can support the operation of the circuit. Such design would need more parts too. ♦ The PFET gate must have low Ron to minimize VCC drop during circuit power backup. ♦ Long-term reliability. Have to use high design margins. ♦ U10 was not integrated into the CPLD because this part has to be powered by VPOS, and this is because the PFET Q1 has to be turned off (need a high voltage level to do that) when VCC is gone.
Major component selection considerations	♦ NEC super cap, 0.1F, C5: This part was selected because NEC is reputable in quality. Manufacturer test data show long-term reliability. This part is a desirable surface-mount part, designed for auto pick-n-place and regular reflow process. Cheap in price. Good availability. Low ESR. 5.5V rated. Essentially no limit on charging current and charging cycle. Another major factor is this part meets the 5.5 mm max height requirement (height restriction because of spacing between PC board and back cover). ♦ ZETEX ZXM61P02 PFET, Q1: Small package, low Ron.

6.3 Up-converter

6.3.1 The up-converter is constructed around a switching controller, U24, Linear Technology LT1307, with switching coil, L6, and diode D2. Feedback is provided by R31 and R32. Input and output filtering is provided by C72, C68, C73 and C61. Loop control is by R33 and C63. Shutdown is controlled by LUC_SHDN from the CPLD, with pull-up RP1G.

6.3.2 The up-converter up converts the voltage of the single AA battery (nominally 1.5 V) to a nominal voltage of 3.45 V.

6.3.3 The output voltage of the up-converter is set by selecting the resistance ratio of R58 and R60. The formula is:

$$V_{out}=1.22(1+R58/R60)\ V.$$

6.3.4 This is a switching type up-converter. The switching frequency is between 550 kHz and 750 kHz, nominally 600 kHz. However, under light load, the up-converter utilizes burst mode, resulting a wide noise spectrum.

6.3.5 For best RF performance, during RF reception, it is expected that the software will set the RF QUIET mode, in that, the up-converter is shutdown during the RF receive windows.

6.3.6 During RF transmit, the transmit current is high enough to put the up-converter in the fixed 600KHz switching frequency mode (instead of burst mode), resulting low harmonic noise at 131KHz (the RF center primary frequency).

6.3.7 Minimum start-up voltage of this up-converter is guaranteed to be no greater than 1.00 V (0.92 V typical) with starting load of no more than 100 ohm load at the output.

6.3.8 Typical efficiency of this up-converter is 70% to 80%, depending on load and input voltage.

6.3.9 This up-converter switching controller can tolerate reversed battery input voltage up to 1.8V. Furthermore, because of the external switching diode, the rest of the circuit would experience no negative current flow when the reversed battery voltage is applied. This provides protection against accidental reversed battery insertion.

6.3.10 Shutdown of the up-converter is controlled by the LUC_SHDN signal from the CPLD, with the 10Kohm pull-up. LUC_SHDN is the combined result of RF QUIET mode bit and RF RX state.

6.3.11 For proper start-up, the output of LUC_SHDN must be tri-stated before VCC gets to the operating level, and defaults to high level once VCC gets to that operating level. At start-up, LUC_SHDN needs to be tri-stated because the /SHDN pin of the switching controller needs to be at or above Vin in order to operate. As battery is inserted, VCC follows Vin, and if the LUC_SHDN output is tri-stated, because of the 10K pull-up, the /SHDN pin will follow VCC (which follows Vin). As Vin reaches the startup voltage, the up-converter starts to operate and produce VCC.

6.3.12 This design takes advantage of the high impedance nature of CPLD outputs (the Xilinx CPLD selected) at low voltage for the purpose of saving parts.

Table 8: Up-Converter	
Input voltage (VAABATT)	AA battery
Output voltage (VCC) and load regulation	3.45 V nominal, 3.35 to 3.6 V range input[1] of 1.15 minimum, load up to 30 ohm at VCC: VCC = 3.35 to 3.60 V input of 1.10 minimum, load up to 30 ohm at VCC: VCC = 3.30 to 3.60 V input of 1.00 minimum, load up to 100 ohm at VCC: VCC = 3.35 to 3.60 V
Type	Current mode PWM
Switching frequency	600KHz nominal, 550KHz to 750KHz range
Minimum start-up input voltage	1.0 V max with start-up load of no more than 100 ohm at VCC
output ripple	less than 80 mVpp
Major design considerations	♦ Low startup voltage ♦ Can support a minimum of 110mA at 3.45V, with input of 1.15V and up ♦ Reversed battery insertion protection ♦ High efficiency ♦ Has shutdown capability ♦ Noise consideration ♦ Can handle the worst start up conditions: with a totally discharged 0.1F super cap, battery voltage as low as 1.15 V
Major component selection considerations	♦ Linear Technology LT1307, switching controller, U24: This part was selected because it meets the major requirements quite well. ♦ CoilCraft DO1608C inductor, 10uH, L6: Low profile, small SMD package, high rated current, low cost. ♦ Motorolla MBR0530 power diode: High current, high voltage, small SMD package.

6.4 Processor

6.4.1 A Medtronic MiniMed custom processor is used as the system processor. This Processor IC, U8, incorporates an low power 8086 processor core and much custom support logics, including ADC, RF module, sensor module and pump module.

6.4.2 Refer to DD1008 for details of the Processor IC.

6.5 PLD

6.5.1 A Xilinx Complex Programmable Logic Device (cPLD), U27, is used to integrate all integratable support logics. The integration reduces part count, thus lowers cost and required board space. This also enhances manufacturability and product reliability.

6.5.2 This is a low power, low voltage in-circuit re-programmable device.

[1] Voltage measured at the input of the up-converter, not at the battery.

6.5.3 A 100-pin flat-pack package is selected, over a smaller super fine pitch BGA package, because this package eases up the requirement on the layout tool and leads to the reduction in PC board fabrication cost.

6.6 Clock

6.6.1 The system clock is generated by the on-chip (Processor IC) oscillator in conjunction with an external 1.049100 MHz, +/-525 Hz (+/-500 PPM) crystal, XTAL1.

6.6.2 The clock frequency is 1.049100 MHz, +/-525 Hz (+/-500 PPM). This clock supports the 131KHz RF frequency.

6.6.3 The accuracy and drift of the clock is important in this design because the system design requires that this device is to be in sync with the companion implant unit for telemetry communication.

6.6.4 To keep this device and the implant unit in sync even with the allowable clock tolerance of +/-525 Hz, the clock stealer function of the processor should be used by the software design.

6.6.5 Even with the tight clock tolerance and the use of clock stealer in the processor, significant time drift may still exist between the two devices, depending on the elapsed time between telemetry communications. Software will deal with the expected time drift.

6.6.6 The crystal, XTAL1, Micro Crystal CC4V-T2, was selected for its availability in the selected frequency, tight tolerance, low drift and small package. This exact crystal is also used in the companion implant units, again, for minimum relative time drift.

6.7 Reset

6.7.1 The Processor IC, U8, can be reset by one of several ways: (a) 5-key reset (KEYRESET). (b) Watchdog reset (HWDRESET). (c) Power-on reset (LVCC_RESET).

6.7.2 The reset of the processor is initiated by a logic high signal to its HEXTRESET pin. The reset is level sensitive, meaning a high level will hold it in reset and a subsequent low level will release it from the reset.

6.7.3 The 5-key reset is generated whenever all five keys on the keypad are pressed simultaneously. Logics in the PLD generate a high HEXTRESET level as long as all five keys are being pressed.

6.7.4 The watchdog reset is generated when the processor does not service the watchdog timer in a timely manner. The watchdog reset signal from the processor is OR'ed with the other reset signals inside the PLD and outputs as HEXTRESET.

6.7.5 The power-on reset signal, LVCC_RESET, is generated by the VCC level detector U16. This signal is also OR'ed with the other reset signals inside the PLD and outputs as HEXTRESET.

6.7.6 It should be noted that HEXTRESET does not affect the content of the external SRAM.

6.7.7 R1 is used on the HEXTRESET line to isolate the output from the PLD so production ATS can reset the board (device-under-test). C70 is used for noise immunity purpose, especially for ESD induced noise.

6.8 External Interrupts

6.8.1 There are three external interrupts to the processor: key interrupt, power interrupt and UART interrupt.

6.8.2 The key interrupt is generated by any key press and is fed to the HIRQ_INPUT1 input of the Processor IC.

6.8.3 The power interrupt is generated by the AA-battery voltage detector, U7, with the signal named HRESET (inverted signal of LRESET). This signal is fed to the HIRQ_INPUT2 input of the Processor IC.

6.8.4 The UART interrupt is generated by the UART chip, U22. This interrupt signal is fed to the HIRQ_INPUT3 input of the Processor IC. A UART interrupt is generated on serial communication events such as data received, transmission buffer empty, etc.

Table 9: External Interrupts (IRQs)

Processor Input	Function and Signal Name	Active Level
HIRQ_INPUT1	key interrupt (HIRQ_KBD)	active high
HIRQ_INPUT2	power interrupt (HRESET)	active high
HIRQ_INPUT3	UART interrupt (HIRQ_UART)	active high

6.9 External RAM

6.9.1 An 8-Mbit, 512K x 16 bit, low power SRAM chip, U9 is provided as the external SRAM memory for the system.

6.9.2 The memory can be accessed either byte-wide or word-wide, controlled by LXRAMLO and LXRAMHI from the processor.

6.9.3 Memory access is further controlled by signal LVCC_RESET. When LVCC_RESET is asserted, memory access is denied. This is designed to prevent memory access during unstable VCC periods and to tri-state the memory chip outputs so they are not driving low impedance inputs when VCC is absent in backup mode.

6.9.4 These memory chip is powered by power signal VPOS. This power is derived from VCC as it is available and from the super cap when VCC is not available in backup mode.

6.9.5 Address lines used are A1 to A17 and HPUMP_FIRE (function as bank switch line) from the Processor. HXRAM_A18 and HXRAM_CS are derived from LXRAM1 and LXRAM2 from the processor. This is needed because the processor was originally designed to access two lower density SRAM chips.

6.9.6 The chip selected can be a NanoAmp N08L163WC2AB or SamSung K6F8016U6A. These chips were selected because of their low operating power, low static power, high density and small package. Low static power is an important criteria because the backup time required. These chips typically draws less than 1uA in static mode. To guarantee specified memory backup duration, boards have to be 100% tested for backup mode current.

6.9.7 U6 needs VPOS powering because it is needed to keep the SRAM chip disabled while VCC is rising or dropping, and VPOS ensures U6 would provide that stable signal. When VCC is low or in some “half-good-half-bad” states, LVCC_RESET will stay low, guaranteed by U16.

Table 10: External SRAM	
Total memory	1M bytes or 512K words
Organization	byte-wide or word-wide
Address lines used	A1 to A17 from the Processor
Bank select line used	HPUMP_FIRE from the Processor
Chip select	LXRAM1, LXRAM2 from the Processor, combined to form HXRAM_CS, in conjunction with LVCC_RESET
Memory write control	LWRITE, LXRAMLO and LXRAMHI from the Processor
Memory read control	LREAD, LXRAMLO and LXRAMHI from the Processor
Memory range	Bank 0: 0x20000 to 0x9FFFF Bank 1: 0x20000 to 0x9FFFF

6.10 Serial ROM

6.10.1 Two Atmel serial EEPROM (SEEPROM) chips, U12 and U13, provide the memory space for data and program code storage.

6.10.2 The addresses for the two SEEPROM chips are set to 000 and 001 by hard wiring.

6.10.3 The capacity of the SEEPROM chips are 512K bits (64K bytes) each, organized as 512 pages of 128-bytes each, with a total serial ROM memory of 128K bytes.

6.10.4 Interface to the SEEPROM chips is a dedicated port of the Processor. Interfacing signal lines include SEEROM_PWR (power), SEEROM_CLK (clock) and SEEROM_DATA (data).

6.10.5 The SEEPROM chips are so connected that they can be written to as well as read from during run time by the system processor.

6.10.6 The SEEPROM chips can also be fully accessed by an external EEPROM programmer. This is done by accessing the SEEROM_PWR, SEEROM_CLK and SEEROM_DATA lines via test connector. This provides a way for an ATS to program this memory space during board testing.

6.10.7 Pull-up is needed for SEEROM_DATA because this is an open-drain output (when it is used as an output) on the chip.

6.10.8 The software, working in conjunction with respective hardware in the processor, is responsible for removing the power to the serial ROM chips when they are not in use.

6.10.9 Refer to ES1160 for information on how to access this serial ROM memory.

Table 11: Serial EEPROM	
Total memory	128K bytes (2 chips x 64K byte each)
Organization	512 pages, 128 bytes per page
Memory device addresses	address 0 and address 1 (hard-wired)
Interface	Atmel 2-wire serial

6.11 RF

6.11.1 The communication link between the IU and the PPC is RF telemetry at 131.075 kHz. The RF telemetry subsystem is composed of analog and digital modules. The digital module includes a modulator/demodulator, a control, and a timing logic circuit that are all integrated in the Processor IC.

6.11.2 The analog module consists of a RF front-end circuit and a mixer. The mixer is also integrated in the Processor IC. The RF front-end circuit is implemented on the PPC board. The RF front-end circuit consists of a transmitter and a receiver, which is in-turn composed of a band-pass filter and a 3-stage amplifier.

6.11.3 Select-In-Test (SIT) capacitors are provided for the tuning of the antenna, the filter, the second amplifier stage. SIT capacitor tuning allows the use of standard tolerance capacitors and inductors instead of high cost tight tolerance parts.

6.11.4 There are three logical antennas orientated in such way that the X, Y and Z directions are covered to minimize range dependency on orientation. The three logical antennas are housed in two physical packages. These antennas are custom designed parts for this application.

6.11.5 ANT0, ANT1 and ANT2 are antenna selection signals, fully controlled by software. There is no automatic hardware antenna selection mechanism, therefore, software is fully responsible for selecting the antenna which yields the best field strength at a given time. Only one antenna shall be selected at a time.

6.11.6 More performance details of the RF circuit are to be presented in a separate document.

Table 12: RF Circuit Signals

Receiver Output	MIXER_HI (mixer high) MIXER_LOW (mixer low)
Transmitter Input	TXI TXQ
Control/Power	RF_RX_ANA_PWR (transmit/receive control) VRF_AMP (receiver power)
Antenna Selection Control	ANT0 for selecting antenna 0, low=select ANT1 for selecting antenna 1, low=select ANT2 for selecting antenna 2, low=select

6.12 External I/O Ports

6.12.1 There is one external input port and two external output ports. These ports are implemented in the PLD.

6.12.2 The address for the input port is 0x00.

6.12.3 The addresses for the output ports are 0x02 and 0x04.

6.12.4 The input port is a typical tri-statable port.

6.12.5 The output ports are each constructed resettable D-flipflog (D-FF). The design is such that the bit settings are latched, and on power-up and when battery is low, they are all set to an independent default state. The design is necessarily this way because the data bus is a shared bus so needing the latching; when battery is detected low, all high power devices need to be shutdown immediately to save energy for backup; on power-up and before the process fully booted and the circuit is initialized, all high power devices should be off (it is especially not desirable to have the vibrator on when the processor is booting). The default state depends on the function of the bit. For example, bit 3 of 0x02 is HIRDA_SHDN, this bit is default HIGH because high level shuts down the IR transceiver. Another example is LSHDN_MAX3100, this bit is default LOW because low level shuts down the MAX3100 UART chip.

6.12.6 In order to achieve the default states, yet keeping the bit setting convention as in MMT315x models, double inversion (before and after the D-FF) and is used for some bits.

6.12.7 Connected to the input port are key signals and power management signals. Note that bit 5 (VCC) and bit 7 (LVCC_RESET) have no real function because VCC is detected by hardware and when LVCC_RESET is asserted, the entire circuit is disabled. Software is not expected to be able to use these two bits for any meaningful function. Bit 5 was the LPFO bit in MMT315x models, so connecting it to VCC makes this backward compatible.

6.12.8 The output ports control various devices. See Table 13 for details.

6.12.9 The output ports are controlled by HRESET (inverted LRESET). When LRESET is asserted (VAABATT falls below the programmed threshold), the output ports are cleared, achieving the purposes described in the paragraphs above.

6.12.10 Table 13: I/O Ports below lists the bit assignments of the ports.

Table 13: I/O Ports

Port Address	Bit	Signal	Description	State
0x00 (input)	0	DOWNKEY	DOWN key	low = key pressed
	1	UPKEY	UP key	low = key pressed
	2	SELKEY	SEL key	low = key pressed
	3	ACTKEY	ACT key	low = key pressed
	4	HIDDENKEY	HIDDEN key	low = key pressed
	5	VCC	Considered NOT USED	
	6	LRESET	dead main battery	low = battery voltage low
	7	LVCC_RESET	Low VCC signal	low = VCC is low, circuit shutdown by hardware
0x02 (output)	0	LCS_MAX3100	UART chip select	Default: high low = UART selected
	1	LSHDN_MAX3100	UART chip shut-down	Default: low low = UART shutdown
	2	LCUT_VCC	Cuts VPOS from VCC	Default: high High = VPOS isolated (cut) from VCC

Table 13: I/O Ports				
Port Address	**Bit**	**Signal**	**Description**	**State**
				low = VPOS connected to VCC Note: The states here are actual electrical states. To the software, writing a “0” to this bit CUTs the VCC connection, writing a “1” to this bit MAKEs the VCC connection.
	3	HIRDA_PWRDN	IrDA module power down	Default: high high = IRDA shutdown
	4	not used		
	5	not used		
	6	not used		
	7	not used		
0x04 (output)	0	LCS_LCD	LCD chip select	Default: high low = selected
	1	LRESET_LCD	LCD reset	Default: low Low = LCD reset
	2	HEN_LCD_INSCK	LCD clock loop-back	Default: low high = LCD clock loop back
	3	not used		
	4	HEN_QUIET	Quiet RF mode control	Default: low High = RF QUIET mode - EL backlight and vibrator disabled during RF reception
	5	HEN_LED	LCD EL backlight enabled	Default: low High = EL backlight enabled
	6	HEN_VIBRATOR	Vibration motor enabled	Default: low High = vibrator enabled
	7	DUMMY_LOAD	100 ohm dummy load ON (intended to used to load the AA battery during AA battery voltage measurement, can be used for other purposes)	Default: low High = dummy load turned on (RF QUIET mode temporarily disabled)

6.13 Keypad

6.13.1 Connector CN4 is the connector for the 5-key keypad. This connector accepts flex cable only. It is a “bottom contact” connector.

6.13.2 IC chip MAX6818, U23, is an integrated key interface device, key de-bouncer and ESD suppresser.

6.13.3 The de-bounce duration is 20 ms minimum, 40 ms typical.

6.13.4 A key interrupt generator is integrated in the PLD. This circuit generates a reset signal (KEYRESET) if all keys are pressed simultaneously. It generates a key interrupt signal (HIRQ_KBD) whenever any one or more keys are pressed. This interrupt is fed directly to the HIRQ_INPUT1 input of the processor.

6.13.5 R49 and C81 are added to the HIDDEN key line to provide additional suppression of short pulses caused by ESD so that ESD event would not trigger a 5-key reset.

6.13.6 R45 is used for the purpose of limiting ESD current, thus reduces ESD induced noise to the main circuit. The value of resistor has to be kept low because the 32-100Kohm pull-up in the de-bouncer chip. The worst case is when all 5 keys are depressed, resulting the lowest effective pull-up resistance of 6.5Kohm. Rated input HIGH threshold for the de-bouncer is 2.2 V. With R45 = 4.75Kohm, the worse case voltage appear at the inputs, when all 5 keys are pressed, is 1.45V, which is below the 2.2V threshold.

6.13.7 The states of keys are monitored by input port 0x00, bits 0 to 4. The Processor is expected to read the port to determine which key was pressed after receiving a key interrupt. See *Table 14* below for key and I/O bit assignments. A low state indicates key press.

Table 14: Key and I/O Bit Assignments

PORT	BIT	SIGNAL	DESCRIPTION
0x00 (input port)	0	LDOWNKEY	DOWN key
	1	LUPKEY	UP key
	2	LSELKEY	SEL key
	3	LACTKEY	ACT key
	4	LHIDDENKEY	HIDDEN key

6.14 Buzzer

6.14.1 Connector CN2 is for the connection of the connection of the piezo type alarm buzzer.

6.14.2 The buzzer is driven with signals HBUZZ and LBUZZ from the Processor IC. These signals are gated by the signal LRESET inside the PLD, meaning that the buzzer is disabled when the battery is low.

6.14.3 Volume and frequency controls are done in the processor per software control. See ES1160 for more details.

6.14.4 Absolute sound level is frequency and case design dependent.

Table 15: Buzzer Alarm Circuit Parameters

driving voltage	VCC (3.45 V)
driving signal	HBUZZ and LBUZZ
frequency	programmable
volume	2 levels

6.15 Vibration Motor

6.15.1 Connector CN3 is provided for the connection of a 1.3V DC vibration motor, which is used as a secondary alarm device. JP1 is a set of pads on the PC board for mounting the vibration motor.

6.15.2 The vibration motor is driven by an N-MOSFET BSS123, Q8, which is in-turn controlled (on/off) by bit 6 of I/O port 0x04 in conjunction with RF QUIET mode signals.

6.15.3 In RF QUIET mode, the vibration motor is disabled immediately when the up-converter is shut down, then when the up-converter is turned back on, a small delay is imposed (by hardware logic) on the re-enabling of the vibration motor. This is to make sure that the up-converter is fully operational before the vibrator is turned on again.

6.15.4 The power for the motor is the AA battery direct.

Table 16: Vibration Motor Circuit Parameters

driving voltage	VAABATT (battery voltage direct)
motor current	35 mA typical at 1.3V
motor RPM	7300 rpm nominal
ON/OFF control	bit 6 of I/O port 0x04 in conjunction with RF QUIET mode signals

6.16 AA Battery Measurement Dummy Load

6.16.1 R30 is a 100-ohm dummy load connected to VCC. This load is controlled by bit 7 of output port 0x04 through the N-FET Q9. To turn on the load, set this I/O bit logic high.

6.16.2 The intended purpose of this dummy load is for loaded AA battery voltage measurement. However, this load can be used for other purposes. Note that this load is controlled by an I/O bit, and the I/O port will be disabled when LRESET is asserted (low battery).

6.17 LCD Module and Support Circuit

6.17.1 The LCD module connects to the main board through connector CN1. The LCD panel (with LCD driver), the EL backlight panel and the support components such as contrast setting resistors and bias generator caps are all integrated the LCD module.

6.17.2 The LCD driver is Motorola MC141800B. The LCD panel assembly is manufactured by PICVUE, with the glass layout custom designed by Medtronic MiniMed.

6.17.3 Communication to the LCD module is done using I^2C serial communication protocol. The communication lines are LCD_MISO, LCD_MOSI and LCD_OUTSCK, directly from the SSI_B port of the processor. Refer to ES1160 for details on communicating to the LCD.

6.17.4 The current LCD module design is to use the internal oscillator of the LCD driver. A minor re-design (just populate a resistor) can make it back to use the 64KHz LCD clock from the processor.

6.17.5 For best RF performance, it is recommended to set the internal LCD clock to 90KHz.

6.17.6 Chip select for the LCD is bit 0 of I/O port 0x04 (LCS_LCD). To select the LCD driver chip, set this I/O bit logic low.

6.17.7 Chip reset for the LCD is bit 1 of I/O port 0x04 (LRESET_LCD). To reset the LCD driver chip, set this I/O bit logic low.

6.17.8 The LCD should be initialized as specified in Table 18: LCD Initialization Table, and follow the order as shown.

Table 17: LCD Circuit Parameters	
Processor-LCD communication port	SSI B
Communication format	I^2C
Clock frequency	90KHz, to be selected by commands to the LCD driver
LCD chip select (LCS_LCD)	I/Oport 0x04, bit 0
LCD reset (LRESET_LCD)	I/Oport 0x04, bit 1

Table 18: LCD Initialization Table	
Command byte (in order shown) (hex) // (binary)	**Descriptions**
0x32, //00110010b	normal display frequency
0x7A, //01111011b	;internal oscillator
0x7C, //01111010b	;set frequency
0x08, //00001000b	frequency is 90KHz
0x7F, //01111111b	oscillator on
0x38, //00111000b	bias 1:9
0x2B, //00101011b	dc dc converter on
0x2D, //00101101b	internal regulator on
0x6D, //01101101b	set temperature coefficient
0x31, //00110001b	internal contrast on
0x17, //00010111b	contrast
0x2F, //00101111b	smart bias divider
0x22, //00100010b	col0 to seg0 mapping
0x25, //00100101b	row0 to com63 mapping
0x29, //00101001b	display on
0x21, //00100000b	5x converter
0x36, //00110110b	master clear ram
0x00, //0	Dummy write
0x08, //00001000b	page 9
0x37, //00110111b	master clear icons
0x00, //0	dummy
0x3F, //00111111b	normal display mode
0x44, //01000100b	disable page mask
0x46, //01000110b	disable icon mask

Table 18: LCD Initialization Table	
Command byte (in order shown) (hex) // (binary)	**Descriptions**
0x41, //01000001b	set page mask
0x00, //00000000b	all pages
0x64, //01100100b	waveform type b
0x68, //01101000b	6 phase smart icon
0x3C, //00111100b	end command
0x80, //	FIRST_COLUMN
0x08, //	PAGE_9
0x48, //	WRITE_LCD_MEMORY
0x01, //1	
0xFF, //11111111b	
0xFF, //11111111b	
0x3C, //00111100b	end command
0x80, //	FIRST_COLUMN
0x04, //4	
0x48, //	WRITE_LCD_MEMORY
0x01, //1	
0xFF, //11111111b	
0xFF, //11111111b	
0x3C, //00111100b	end command
0x41, //01000001b	page mask
0xFF, //11111111b	
0x3C, //00111100b	end command
0x45, //01000101b	enable page mask
0x44, //01000100b	disable page mask
0x3C, //00111100b	end command
0x3C, //00111100b	end command

6.18 EL Backlight

6.18.1 An Electro luminescent (EL) backlight panel is used to illuminate the LCD in low light level conditions.

6.18.2 The EL panel is driven by a driver comprised of L1, U2 and C4. U2 is the EL driver chip, Sipex SP4422. It converts the VCC voltage into approximately 300 Hz, 140 VACpp which is applied to the EL element.

6.18.3 The ON/OFF control of the backlight is HEN_LED, bit 5 of I/O port 0x04, in conjunction with RF QUIET mode signals.

6.18.4 In RF QUIET mode, the EL backlight is disabled immediately when the up-converter is shut down, then when the up-converter is turned back on, a small delay is imposed (by hardware logic) on the re-enabling of the backlight. This measures is to make

sure that the up-converter is fully operational and VCC is up-to-the-level before the high power backlight is turned on again.

6.18.5 C4 is the frequency setting capacitor. It affects the frequency, thus the brightness and power consumption. The selection of frequency setting has to take into account of the switching inductance such that the inductor is not operating in a saturated mode.

Table 19: EL Circuit Parameters	
source voltage	VCC
EL panel voltage	140 VAC pp nominal
EL panel voltage frequency	300 Hz nominal
ON/OFF control	bit 5 of I/Oport 0x04 in conjunction with RF QUIET mode signals

6.19 IrDA Port

6.19.1 An IrDA port for communicating with an external computer is provided. The port is comprised of a UART chip, U22, and an IrDA transceiver module, D1.

6.19.2 The data transfer rate through this port is fixed at 115.2 Kbit/s. This port complies with IrDA 1.2 Low Power standard.

6.19.3 The SSI_A port of the processor is used for this serial communication.

6.19.4 To use this port, the UART IC must be configured properly by the application software. Refer to ES1160 for details.

6.19.5 Both the UART IC and the IrDA transceiver can be powered down to save power. See *Table 20* below.

6.19.6 Whenever external data is received by the IrDA transceiver, the UART IC generates a UART interrupt. This interrupt is fed directly to IRQ3 input of the processor.

6.19.7 When the UART is in shutdown state, its oscillator is stopped. When the UART is taken out of shutdown state (LSHDN_MAX3100 set high), it will take a minimum of 100ms to start up the oscillator. The software is expected to allow for the startup time.

Table 20: IrDA Port	
power source voltage	VCC (3.45V)
communication port of the processor	SSI A
baud rate	115.2 Kbit/s, fixed
protocol	IrDA 1.2 Low Power
UART chip select	bit 0 of I/Oport 0x02, logic high
UART shut-down control	bit 1 of I/Oport 0x02, logic low to shut down
IrDA transceiver ON/OFF control	bit 3 of I/Oport 0x02, logic low to enable transceiver, logic high to disable transceiver

6.20 Battery Life

Battery life depends on system design. Below is an example based on an existing IGMS system. Actual battery life calculation will be done in the system level.

MMT3160 PPC (Used as IGMS PPC) POWER CONSUMPTION WORKSHEET

	CURRENT @ VBATT=1.25 V	CALCULATED POWER @1.25V	DUTY TIME PER DAY	DUTY CYCLE	ITEM TOTAL	COMMENT
MMT3160 generic	(mA)	(mW)	(second)		(mW.Hr)	(per day)
ICON only mode with backlight off	0.6	0.8	85932	0.994583	17.9	23.87 hours (about 8 minutes in Menu Screen mode)
Menu screen with backlight off	2.5	3.1	360	0.004167	0.3	6 minutes (glucose value viewing)
Menu screen with backlight on	80	100.0	90	0.001042	2.5	1.5 minute (glucose value viewing time)
RF reception (interval)	2.5	3.1	72	0.000833	0.1	0.05 second per minute, 72 seconds per day
RF reception (messages)	2.5	3.1	10	0.000116	0.0	10 seconds
RF transmission (messages)	40	50.0	10	0.000116	0.1	10 seconds
Vibrator on with menu screen	42	52.5	15	0.000174	0.2	15 seconds
TOTAL PPC consumption in mW.Hr per day					21.1	(mW.Hr)
Battery capacity to 1.15 V in mW.Hr					2100.0	(mW.Hr)
Battery life (day)					99.3	(day)
Battery life (week)					14.2	(week)

TOTAL PPC consumption in mW.Hr per day without the use of vibrator alarm					20.9	(mW.Hr)
Battery capacity to 1.15 V in mW.Hr					2100.0	(mW.Hr)
Battery life (day)					100.4	(day)
Battery life (week)					14.3	(week)

6.21 Test Connector

6.21.1 Selected signals are routed to two board edge connectors for production test purposes. J2 has mostly RF related signals while J1 has the rest of the signals of interest.

6.21.2 *Table 21* lists the signals.

Table 21: Signals at Test Connector

Connector Pins	Signal Names	Signal Descriptions
	HBUZZ	
	LBUZZ	
	HTSTCLKEN	
	TSTCLKIN	
	HTPON	
	VIB_TP	
	SEEROM_CLK	
	SEEROM_PWR	
	SEEROM_DATA	
	IN_ACTKEY	
	IN_SELKEY	
	IN_UPKEY	
	IN_DOWNKEY	
	IN_HIDDENKEY	
	PADCLK	
	SER_TX_TP	
	SER_RX_TP	
	RF_RX_ANA_PWR	
	VPOS	
	VAABATT	
	VCC	
	HEXRESET	
	TXI	
	+1.2V_AMP1	
	TXQ	
	VRFAMP	
	RFI	
	RFVCC	
	ANT0	
	ANT1	
	RF_RX_SIGNAL	
	RF_RX_ANA_PWR_TP	

Table 21: Signals at Test Connector		
Connector Pins	**Signal Names**	**Signal Descriptions**
	+0.6V_AMP1	
	RFQ	
	ANT2	
	TDO	
	TCK	
	TDI	
	TMS	
	HPRG_PORT_EN	

6.22 PLD Programming

This section is not to be the concern of PPC application software because the application software is not responsible for programming the on-board PLD.

6.22.1 In order for the PPC circuit to function at all, the on-board PLD must first be programmed with the appropriate logic file.

6.22.2 To program the on-board PLD

6.22.3 Connect the following signals found on the edge connector, J1, of the PPC board to the corresponding signals on the programmer:

- TDO
- TCK
- TDI
- TMS
- HPRG_PORT_EN
- VCC
- (GND)

6.22.4 Pull the HPRG_PORT_EN input to VCC at the programmer.

6.22.5 Program according to manufacturer specification.

7.0 XILINX COOLRUNNER PLD PROGRAMMING

Note: The “MMT3160” name is just an example.

7.1 Schematic to EDIF File Conversion

7.1.1 Use OrCad 9.2 with XUNIFIED library for OrCad from Xilinx.

7.1.2 Create EDIF 200 netlist from OrCad. File name will be MMT3160.EDN

7.2 Programming

7.2.1 Use Xilinx Project Navigator, release 4.2i.

7.2.2 Before invoking the Navigator, set up the following files in the MMT3160 project directory

7.2.3 Change the MMT3160.EDN file name to MMT3160.EDF.

7.2.4 Copy and existing .UCF pin file and name it SCHEMATIC1.UCF. This name is a default name used by Navigator.

7.2.5 Invoke Navigator.

7.2.6 Close old project.

7.2.7 Start new project. Enter project name “MMT3160”. Select device property: “CoolRunner XPLA3 CPL”, “XCR3064XL VQ100”, “EDIF”. Note the project location displayed.

7.2.8 With the cursor highlight “XCR3064XL VQ100-EDIF” in the Sources in Project window, select Add Source from Project drop down menu. Select “MMT3160.EDF” to add. Remove old source file before adding the new source file.

7.2.9 The Sources of Project window should display “MMT3160” “XCR3064XL VQ100-EDIF” and “schematic1(MMT3160.EDF)”. If not, check to make sure that the MMT3160.EDF file is not changed (somehow it happens, evident of only a 1Kbyte file). If it is changed, copy the .EDN file to make the .EDF file again.

7.2.10 In the Source window, use the cursor to highlight “schematic1(MMT3160.EDF)”. In the Process window, open up Design Entry Utility then the User Constrains.

7.2.11 Run the first “Edit Implementation Constrain” under User Constrain” in the Process window. The txt file named schematic1.ucf in the MMT3160 project directory should be opened with NotePad. Edit or verify the content. Refer to file sample attached. Make sure each pin assignment line ends with a semi-colon. Make sure to enter the pin number starting with a “P”, e.g. “LOC=P40”.

7.2.12 Save the file and exit NotePad. Navigator will continue the process.

7.2.13 Right click on the second “Edit Implementation Constrains (Constrains Editor)”. Select “Rerun All”. Verify all pins.

7.2.14 Open the “Implement Design” menu.

7.2.15 Highlight the “Implement Design” menu then right click. Select “Property”.

7.2.16 Enter or select the properties as specified the Process Properties table below.

7.2.17 Open the “Generate Programming File” menu.

7.2.18 Highlight the “Generate Programming File” menu then right click. Select “Property”.

7.2.19 Highlight “Configure Device (impact)” in “Generate Programming File” menu. Right click and select ReRun or Rerun All. Utility program IMPACT should be invoked.

7.2.20 Connect the JTAG signals from the programming cable (Insight, JTAG Cable, Model IJC-2). Connect power to DUT. Pull HPRG_PORT_EN signal of DUT high to enable programming.

7.2.21 In IMPACT, when ready, do the following

7.2.21.1 In the EDIT dropdown menu, select “Select All”

7.2.21.2 In the OPERATIONS menu, select “Program”, check the “Erase Before Program” and the “Verify” items. Click on OK to run.

7.2.21.3 Verify that programming completes without error.

7.3 Setting for Programming PLD

Table 22: Process Properties for Implement Design	
Xilinx CoolRunner PLD Programming Configurations – "Implement Design" Configurations	
Speed Grade	-10
Implementation User Constrain File	(leave empty)
Implementation Template	Optimize speed
Use Timing Constraints	Checked
Use Location Constraints	Always
Output Slew Rate	Slow
Default Power-up Value of Registers	Low
Exhaust fit mode	(Unchecked)
Use multi-level logic optimization	Checked
Use fast input for input registers	(Unchecked)
Function block input limit	38
Collapsing input limit	32
Collapsing Pterm limit	Template controlled
Use foldback NAND	(Unchecked)
Reserve ISP pins	(Unchecked)

- Use Cable Reset to reset cable.
- Don't have multiple IMPACT active
- Put board in reset
- Enable PLD programming
- Make sure VCC is good

Table 23: Process Properties for Generate Programming File	
Xilinx CoolRunner PLD Programming Configurations – "Generate Programming File" Configurations	
Signature/User Code	(leave empty)
Jedec Test Vector File	(unchecked)
Pull-up unused I/O pins	checked

8.0 HARDWARE CHANGES AS COMPARED TO MMT315X PPC

Table 24: Hardware Changes as Compared to MMT3150 PPC

	MMT3160	MMT315x	Associated changes	Benefit from the change	Trade-off from the change
Backup cell	0.1 Farad Super Cap	40mA.hr, 3V lithium coin cell	♦ Eliminated a perishable component ♦ Eliminated the need for coin cell holder ♦ Auto pick-n-place of this component instead of manual coin cell insertion	♦ Can back up the VCC for normal circuit operation when up-converter is shutdown for noise reduction during RF activity ♦ Lessen the burden on the up-converter and the battery by supporting high current bursts ♦ Cheaper component ♦ Cheaper assembly cost ♦	♦ Shorter SRAM backup time ♦
External SRAM backup time	Exceeds the 1-hour requirement	3 years	♦	♦	♦ Would have to set up the PPC again if system is without power for longer than the guaranteed backup time
VCC backup time when up-converter is shut down	2 seconds at 2 mA consumption with no circuit operation interruption or LCD brightness effect	Less than 300 ms at 2mA	♦ Enable quiet RF reception mode (by turning off up-converter) ♦ Eliminated the high cost up-converter circuit shield	♦ Improved RF range ♦ More time for orderly shutdown on low battery interrupt ♦ Lower component cost ♦ Lower part count	
Processor IC	Use BGA prepackaged MMT custom processor IC	Same IC but bare die, put on the board with chip-on-board process	♦ Eliminated the problem prone chip-on-board process	♦ Cheaper assembly cost ♦ More reliable product (chip-on-board was proven to be prone of problems such as scratched die, broken wire-bonds, etc) ♦ Improved reworkability	

Table 24: Hardware Changes as Compared to MMT3150 PPC					
	MMT3160	**MMT315x**	**Associated changes**	**Benefit from the change**	**Trade-off from the change**
LCD power	2.86 V regulated	VCC	♦ Added an extra voltage regulator, however, this is not really an extra component because the built-in voltage detector replaces the voltage detector used in the MMT3150 PPC ♦ Added 74LV367 chip as a level shifter	♦ Lower power consumption by the LCD	♦ Higher part count (the level shifter)
LCD clock	Use LCD's internal oscillator with internal frequency setting resistor, 90KHz clock	Use 64KHz clock, generated by the processor	♦ LCD clock frequency is now 90KHz, reduce the harmonic noise in RF pass band	♦ Improved RF performance	♦
LCD panel	New design		♦ Eliminated the manual contrast adjust process	♦ Lower component cost ♦ Improved contrast ♦ Improved appearance due to the change of polarizer ♦ Improved viewing due to better centering the LCD active area in the case window ♦	♦
LCD module	Pre-assembled	Solder to the board	♦ Connect to the board using a flex connector ♦ Added a new custom designed flex, a flex connector, a custom designed LCD support, a custom designed PSA piece ♦ Eliminated the	♦ Improved reworkability if LCD is defective ♦ Improved assembly process ♦ Improved yield ♦ Improved product reliability (the assembly process of soldering the LCD to the main board was proven	♦

Table 24: Hardware Changes as Compared to MMT3150 PPC					
	MMT3160	**MMT315x**	**Associated changes**	**Benefit from the change**	**Trade-off from the change**
			bezel, the double-sided foam, the custom designed EL connecting flex, the bezel mounting screws, the gluing process of the bezel to the LCD panel	to be prone of LCD damages) ♦ Reduced overall assembly cost ♦	
ESD immunity	Enhanced		♦ Added resistors, capacitors and a EMI choke to keypad circuit, to LCD circuit, to reset circuit, to piezo circuit and to battery negative terminal	♦ Reduce the chances of ESD induced damage ♦ Reduce the chances of ESD induced system reset	• Higher part count • Higher component cost
External SRAM chip	One 8Mbit chip, BGA package	Two 4Mbit chips, SSOP packages	♦ 1 part vs 2 parts ♦ BGA package	♦ Reduced part count ♦ Reduced component cost ♦ Reduced board space needed	• Possibly increased assembly difficulty because of BGA package
PC board	One board	Two boards (RF and Digital)	♦ Eliminated one pc board ♦ Eliminated four board mounting spacer ♦ Eliminated the board sandwiching process ♦ Eliminated two inter-board connectors ♦ Eliminated the testing of one board ♦ Enabled automatic writing of calibration data into the serial ROM by the ATS, replacing the manual data entry process	♦ Reduced part count (the bare pc board is a component) ♦ Reduced component cost ♦ Reduced assembly cost ♦ Reduced test time ♦ Improved product reliability by eliminating the inter-board connector ♦ Improved reworkability	
ATS test connectors	Pre-fab'ed board edge connector (not a component)	Test points	♦	♦ Easier connection for the ATS ♦ Improved ATS connection reliability	♦

Table 24: Hardware Changes as Compared to MMT3150 PPC					
	MMT3160	**MMT315x**	**Associated changes**	**Benefit from the change**	**Trade-off from the change**
				♦ Reduced ATS cost	
Antenna	Three functional antennas (two physical parts)	One loop antenna	♦ Auto pick-n-place of the antennas, eliminating the manual soldering ♦ Pick up more noise from LCD due to unshielded antennas	♦ Longer RF range ♦ Less RF range orientation dependency ♦ Reduced assembly cost	♦ Higher component cost (two parts vs one part, unit cost comparable) ♦ Lower EMI immunity because the new antennas has no EMI shielding ♦
RF circuit	New topology		♦ Eliminated on high price inductor ♦ Enabled the use of higher tolerance parts ♦ Eliminated RF shields	♦ Lower component cost ♦ Higher yield due to easier tuning ♦ Longer range ♦ Less orientation dependency	♦ Higher part count ♦
Up-converter shielding	Not shielded	Shielded	♦ Eliminated the manual process of soldering the shield	♦ Lower component cost ♦ Lower part count ♦ Lower assembly cost	♦
Up-converter shutdown	Enabled	Not an option	♦ The QUIET mode bit was already available in MMT3150, but not used ♦ In MMT3160, if QUIET mode is set by software, the hardware will automatically shut down the up-converter if RF receive is active	♦ Longer RF range	♦
Power input/output caps	Battery input: 47uF, X5R type, non-polarized, 1210 case size VCC output: 47uF, X5R type, non-polarized, 1210 case size	Battery input: 68uF, tantalum type, polarized, “C” case size VCC output: two 220uF, tantalum type, non-polarized, “D” case size	♦ Reduced board space needed ♦ These components can be placed where they should be for better noise suppression because no more height restriction	♦ Lower part count ♦ Lower component cost ♦ Improved noise suppression because the components can be place where they should be	♦

Table 24: Hardware Changes as Compared to MMT3150 PPC					
	MMT3160	**MMT315x**	**Associated changes**	**Benefit from the change**	**Trade-off from the change**
CPLD (Complex Programmable Logic Device)	Used	Not used	♦ Eliminated almost all standard logic components ♦ Added this CPLD part ♦ Enabled the single board design due to the freeing up of board space ♦ Require the need to program the CPLD ♦	♦ Lower part count ♦ Improved product reliability ♦ Lower assembly cost ♦	♦ Higher component cost ♦ Added the process of programming the CPLD
LPFO (Low Power Fail Output)	Eliminated (where this bit was in the input port is now tied to VCC so the software might not need to change for this hardware change)	Used, but this signal provided no real function	♦	♦ None	♦ None
ANT0, ANT1, ANT2	Used to control the selection of antennas	Not used	♦ Enabled antenna selections	♦	♦
Piezo sound	Disabled when battery is low	Straight from the processor	♦ Added a gate (in the CPLD) to disable the sound	♦ No annoying sound when battery is low and the processor is not in control	♦ (adding the gate is not adding a physical component because the CPLD has enough free gates for this)
Piezo connection	Wire and connector	Custom flex	♦ Added connector on board ♦ Piezo is procured as an assembly, with wire and connector pre-assembled ♦ Eliminated the need to manually solder the flex onto the board ♦ Eliminated the custom flex ♦ Eliminated the	♦ Improved product reliability ♦ Reduced part count ♦ Reduced component cost ♦ Reduced assembly cost ♦ Improved reworkability	♦

Table 24: Hardware Changes as Compared to MMT3150 PPC					
	MMT3160	**MMT315x**	**Associated changes**	**Benefit from the change**	**Trade-off from the change**
			manual soldering of the flex onto the piezo		
Serial ROM	Two BGA parts	Two leadless parts	♦ Smaller footprint ♦ BGA package	♦ Free up some board space	♦ Possibly increased assembly difficulty because of BGA package
EL inductor	4.7mH Murata part	4.7mH CoilCraft part	♦ Small package	♦ Free up some board space	♦
Dummy load	100 ohm	150 ohm	♦ Dummy load current now 34.5 mA and is the highest load in the circuit.	♦ This ensures that low battery detection provides enough pre-warning of low battery condition to the user	♦ (This is a high power load, but should not lead to shorter battery life as compare to MMT3150 because the overall device power consumption is now lower)
Backlight and vibrator on/off control	Have delay, backlight and vibrator cannot be on at the same time	No delay, vibrator and backlight can be on at the same time	♦ Added delay circuit ♦ Added control logic ♦ The on delay prevents the loading of the super cap when the up-converter is just taken out of shutdown and not yet fully in stable operation ♦ The two high current devices not being on at the same time reduces the power circuit burden and reduces the chances of premature low battery condition	♦ Extended battery life ♦	♦ In night-time use, the user would observe backlight being turned off when the vibrator is on
Vibrator mounting	Soldered on-board	Taped to the module	♦ Eliminated the need for vibrator sleeve ♦ Eliminated double-sided foam pieces ♦ Eliminated the vibrator module	♦ Reduced part count ♦ Reduced component cost ♦ Reduced assembly cost ♦ Improved product reliability	♦

Table 24: Hardware Changes as Compared to MMT3150 PPC					
	MMT3160	**MMT315x**	**Associated changes**	**Benefit from the change**	**Trade-off from the change**
			assembly ♦ Eliminated the need to manually install the vibrator assembly onto the module and carefully dress the vibrator wires ♦ Added the need to manually solder the vibrator onto the board		
Vibrator	1.6 V (1 V up operational)	3.6 V	♦ Drive with battery voltage direct ♦	♦ Reduced the burden of battery and up-converter ♦ Reduced power consumption ♦ Reduced chances of vibrator induced premature low battery condition	♦ Lower RPM

9.0 HARDWARE CHANGES INDUCED SOFTWARE CHANGES AS COMPARED TO MMT-315X PPC

Table 25: Hardware Changes Induced Software Changes As Compare to MMT315x PPC

Hardware change	Required software changes	Recommended software changes	Comments
Three antennas	If only one antenna is to be used, the other two antennas have to be disabled by setting the ANT bits accordingly	Dynamically selecting one of the antennas which has the best orientation with the implant unit for optimum range performance	See HW/SW interface document for ANT bit setting
QUIET mode		Use QUIET mode during telemetry for better RF performance	RF reception continuous period is limited to less than 1.3 seconds
HCUT_VCC		Assert this signal after orderly shutdown upon low-battery interrupt to preserve energy in super cap for SRAM backup	
LPFO		Eliminate the monitoring of this bit and associated activities.	Or no change needed
Low-battery interrupt by LRESET and orderly shutdown			Much more time than before for orderly shutdown
1-hour guaranteed memory backup time instead of 3yr		Save more setup parameters in serial ROM or the implant unit so loss of memory does not require the user to enter new setup data??	The need to set up the date and time might be unavoidable unless date and time information is saved in the implant unit as well. The implant unit is already saving the time (???)
New LCD panel	Set LCD to use internal oscillator with internal frequency setting resistor, frequency 90KHz Disable LCD clock in the processor		

10.0 PC BOARD LAYOUT

Figure 2: MMT3160 PPC Bottom View

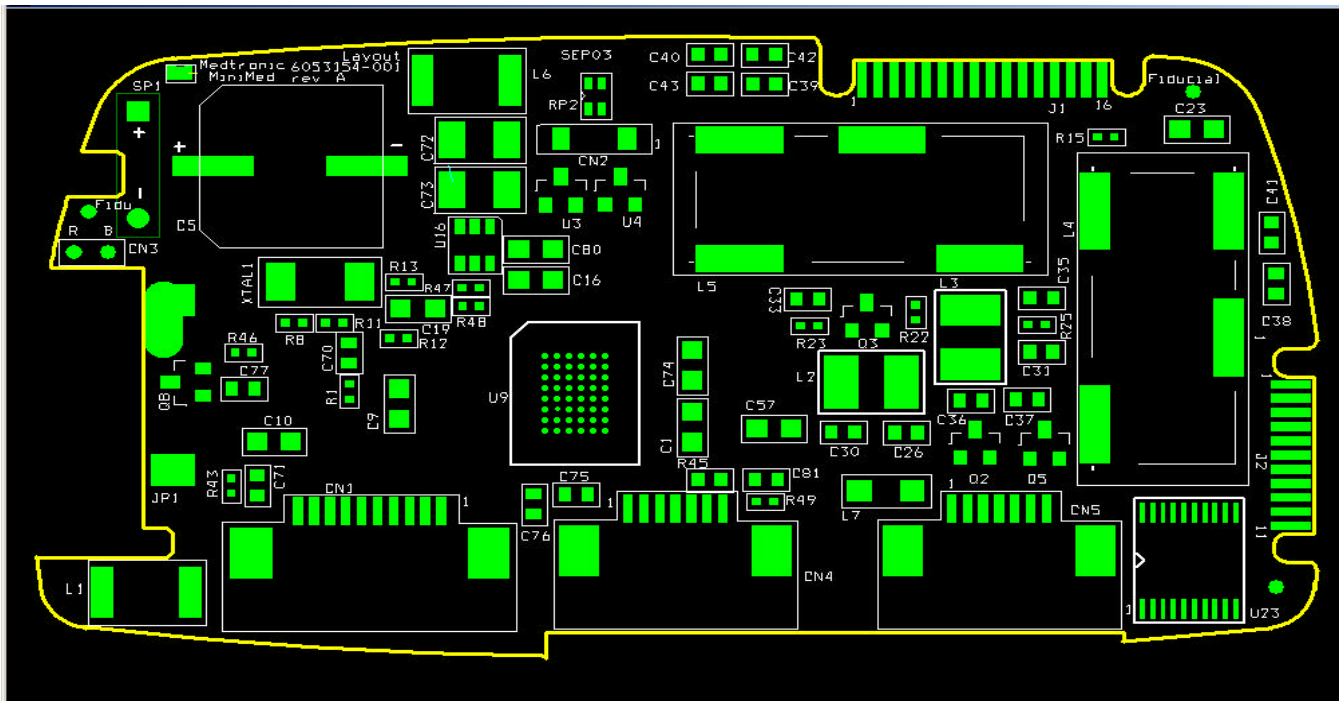


Figure 3: MMT3160 PPC Top Side View