Digital Board Hardware description

A) Overview

The Alpha One Pager is a POCSAG alpha-numeric pager. It has two key and 16 character (14-segment type) LCD display. It is controlled by Samsung KS57C21116 4-bit MCU. The POSCAG data is received by the decoder SM8212B and will store to the memory (RAM) of the MCU. The user can use the key to read the received message. The message will display the LCD glass and will scroll if more than 16 character. When the new user message is arrived, the pager can set the alert signal to user such as buzzing sound or vibration from vibrator.

B) POCSAG decoder

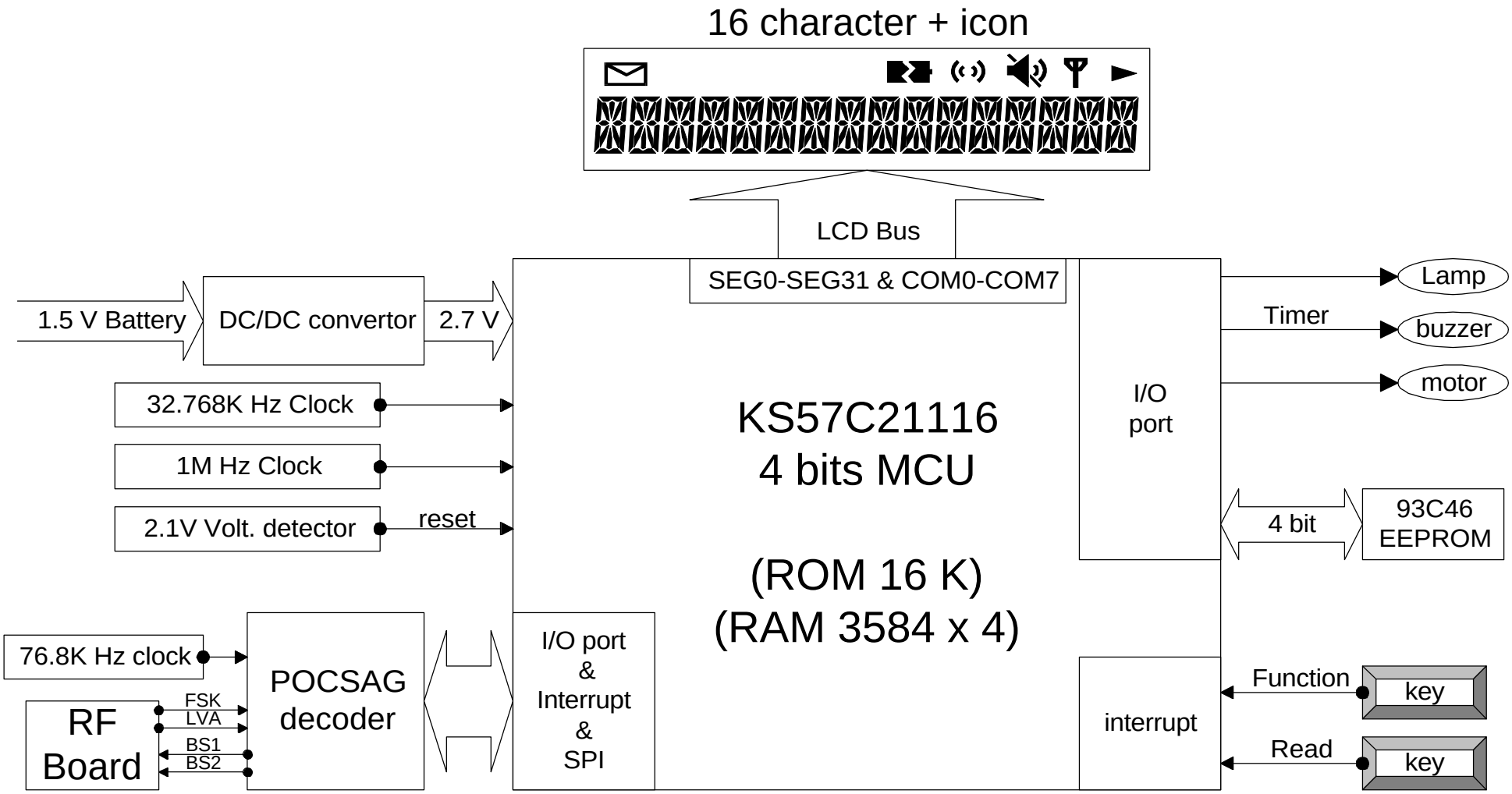
The POCSAG decoder SM8212M is used to connect the RF board to MCU of the digital board. The decoder will control the RF board ON & OFF and receive the FSK data. The decoder will decode the FSK signal and acknowledge the MCU if CAP code is correct. When the new message arrive, the decoder will generate the interrupt to the MCU. The decoder will also generate the low battery signal to the MCU if voltage is below 1.1V. The 76.8K Hz crystal is used to drive the POCSAG decoder.

C) MCU

The core MCU is Sumsung KS57C21116 which will handle all the work of pager. The MCU will has a initial procedure that will read setting from EEPROM and setup the I/O device. The MCU will receive the RF signal thu RF board and POCSAG decoder. After MCU receive the signal with respect address, it will turn the buzzer on or motor on to acknowledge the user. The user can access the pager by the key input to read the message from the LCD. The 1M Hz and 32.768K Hz crystal is used to drive the MCU. The DC/DC convertor step up the 1.5V to 2.7V from battery to supply the MCU, decoder and EEPROM. A 2.1V voltage detector is used as reset circuit to the MCU.

D) I/O DEVICE

LCD -	The fully ON LCD display profile is shown on the block diagram. It contains 16 14-segment character and five icon on the top. It can check in the test mode.
EEPROM -	93C46, 1K bit serial EEPROM, is used to save the configuration information.
Buzzer & Motor -	is used to acknowledge the user.
Lamp -	is used to see the LCD in darkness place.



Block diagram of 6015N digital board

Technical Description and Block diagram of 6015 pager - RF part

A) Theory of Operation

The RF demodulation process is based on conventional double conversion superheterodyne method. The first IF (intermediate frequency) is selected to be 21.4MHz. The second IF is 455KHz. The demodulation process is done by the FM-IF IC (KA8514) or TA31145. The FM-IF IC includes voltage regulator, low battery detection circuit, mixer, oscillator, FSK comparator and limiting IF amplifier. The operation principles of this paging receiver are depicted in Fig. 1 and the schematics.

B) Antenna Circuit and Amplifier

Antenna of the pager is constructed by silver plated copper loop. By proper tuning a variable capacitor, the loop antenna will be matched to the amplifier and hence the signal picked up would be amplified. The amplified RF signal is then applied to a mixer through a wide-band SAW filter. The SAW filter is mainly used for first image signal suppression.

C) First Local Oscillator and Mixer

The oscillating signal is generated by a crystal oscillator with one stage of frequency multiplier. The LO signal is then mixed with the RF signal by mixer to generate the 21.4MHz IF signal. The 21.4MHz crystal filter is used to filter the 21.4MHz IF signal with second image rejection purpose.

D) FM-IF Circuit

The FM-IF IC converts the 21.4MHz IF signal to 455KHz second IF by the internal second mixer with externally connected crystal of either 20.945MHz. Ceramic filters are used to improve the adjacent channel rejection response. The 455KHz IF signal will then be amplified, limited and discriminated by a ceramic resonator to the base-band analogue signal. Inside the chip there is a level comparator for converting the analogue signal to the digital data. Besides, the chip can power up the whole RF front end with a regulated 1Vdc. With the low voltage alarm function, the MCU can detect the battery from running flat.

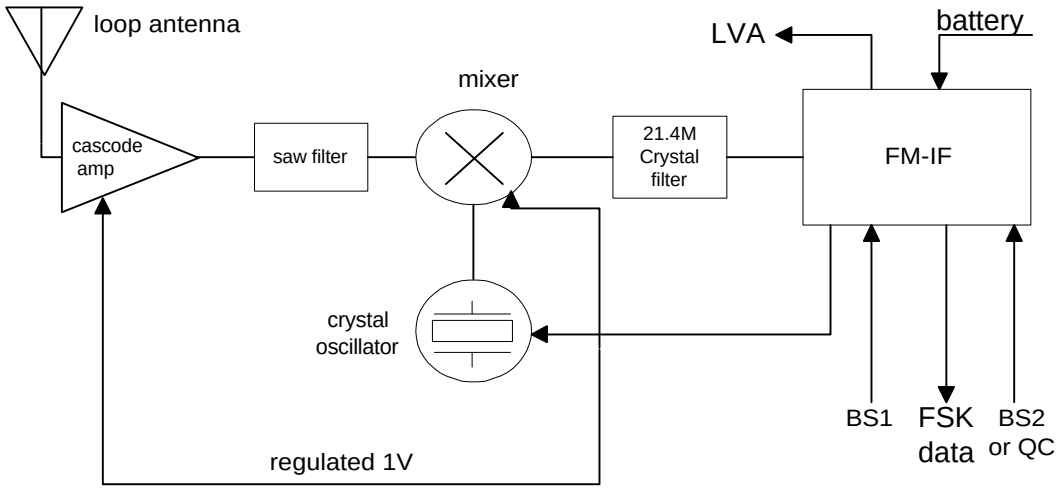


Figure 1: Block diagram of 2-level FSK RF demodulation architecture.

E) Frequency of the first and second local oscillator

Here attached the frequency of the first local oscillator,

e.g. 1. for 928MHz pager sample, the frequency generated from the local oscillator is 75.550MHz and its harmonic.

2. for 932MHz pager sample, the frequency generated from the local oscillator is 75.883MHz and its harmonic.

The second local oscillator is fixed at 20.945MHz.