THEORY OF OPERATION

(MODEL:FR-230)

□. FREQUENCY GENERATION CIRCUITRY

The frequency generation circuit is composed of the synthesizer IC 301 and the VCO. The block diagram illustrates the interconnect and support circuitry used in the design. Refer to the schematic for reference designator.

The supply for the synthesizer is regulated 4.0 volts which also serves the rest of the radio. In addition to the VCO, The synthesizer must interface with the logic and AF filter circuitry. Programming for the synthesizer is accomplished through the clock, data and strobe signals (pin 6, 7 and 8) from the microprocessor IC502.

A serial data is sent whenever the synthesizer is programmed. A 4.0 volt DC signal from pin 5 indicates to the microprocessor that the synthesizer is locked. While unlock is indicated by a low voltage on this pin. The audio signal from the AF filter is modulated by D302 of VCO.

PLL FREQUENCY SYNTHESIZER

The U401 PLL IC includes all the functions such as the phase comparator, the programmable divider, the lock detector, and reference oscillator.

The synthesizer uses a 21.25 MHz crystal (X401) to provide the reference frequency for the system. The other reference oscillator components external to the U401 are C404, C405, TC401, C406.

The loop filter, comprised of R404, R403, C403, R402, C402, R401 and C401 provides the necessary DC steering voltage for the VCO as well as filtering of spurious signals from the phase detector. The pre-scaler for the loop is internal to U401 with the value determined by the frequency band of operation.

The TCXO(21.25MHz) is the temperature compensation circuit to maintain the frequency within the allowable error range even under a low temperature of -20□.

The phase comparator send out the output power to the loop filter through 14th pin of the U401. When phase comparator detects phase difference, LD terminal (pin 5) outputs "LOW". When phase comparator locks, LD terminal outputs "HIGH".

V C O

The VCO, in conjunction with the synthesizer (IC401), oscillates 462.5625 MHz to 467.7125 MHz in the transmit mode and 440.8625 MHz to 446.0125 MHz in the receive mode. The VCO consists of the colpitts oscillator of the Q302. A sample of the RF signal from the enabled oscillator is routed from Q303, C312, through to the pre-scaler input (U401 pin 16). After frequency comparison in the synthesizer, a resultant control voltage is received at the VCO. This voltage is a DC voltage between 1.0 and 3.7 volts when the PLL is locked on frequency.

In the receive mode, the RF signal through Q303 is the local oscillator RF injection and it is applied to the first mixer at Q103.

In the transmit mode, the RF signal at Q303 is run to the input of the pre-drive transistor (Q304 base). This RF signal is the Tx RF injection. Also in transmit mode, The audio signal to be frequency modulated onto the carrier is received by the transmit VCO modulation circuitry at audio in.

During receiving, a relative low frequency should be oscillate compared to transmission. Therefor, the D301 is adversely biased by the Q303, and as a result, the C311 which is added in serial to the resonance circuit of the VCO is added to oscillate the desired reception frequency.

□. RECEIVER

The receiver of the UHF consists of 4 major blocks each: the Front-end ,the Mixer , the First IF and the second IF/Demodulator IC.

FRONT - END

The UHF Front-end contains two separate circuits ; the RF Amplifier and SAW Filter. The RF Amplifier, consist of two transistor Q101 and Q102 is the cascode in all-bipolar form which is also referred to as common·emitter-common·base (CE-CB) connection. This Amplifier get approximately 20dB gain owing to high output impedance , a noise figure of approximately 3dB and is supplied by the receive 4.0V line.

The SAW Filter is BPF of high stability and reliability with good performance and no adjustment and is fixed-tuned design to eliminate the need for tuning and to provide narrow-band operation. The 3dB bandwidth is approximately 6MHz, centered on 465MHz with an insertion loss of approximately 4dB.

The net-gain from the Front-end selection is approximately 20dB in the centre of the band, falling to approximately 4dB at band edges, with a centre band noise figure of approximately 5.5dB.

MIXER

The Mixer operates with a local oscillator drive level minimum -4dBm. The mixer provides excellent isolation between the ports and operates over a large bandwidth. The received signal is mixed down to 21.7MHz, the frequency of the first IF.

FIRST IF

The first IF consists of a 21.7MHz crystal filter and amplifier. The crystal filter provides selectivity, second image protection and intermodulation protection with an approximately 3dB band with of 3.75kHz for 12.5kHz models. The IF Amplifier, Q102, provides approximately 20dB of gain at 21.7MHz.

SECOND IF/DEMODULATOR IC

The Second IF/Demodulator IC, KA3361, accepts the 21.4MHz IF input and mixes it with a second local oscillator signal derived from an external crystal of 21.25MHz. This produces a second IF of 450kHz which is filtered externally by a ceramic filter and passed back into the IC for amplification.

The signal is passed to a quadrature detector for demodulation and, after being filtered, is pass to the output. The IC, along with some external components, controls the squelch sensitivity, squelch tail, and hysteresis. Internal variable resistor, VR101, controls the noise squelch setting.

□. TRANSMITTER

The FR-230 transceiver contain five basic circuits : a Pre-Driver, Driver, Final Amplifier, Antenna Switch and a Harmonic Filter. Refer to the block diagram and the schematic for more information.

POWER AMPLIFIER

The Power Amplifier consists of three stages : a Pre-Diver, Driver, Power Amplifier. It requires a supply voltage of 6.0 volts, and is capable of supplying maximum 0.5W(ERP).

ANTENNA SWITCH

The antenna switch circuit consists of two pin diodes (D101 and D303),In the transmit mode, TXB+ LINE is applied to the circuit to bias the diodes "on". The shunt diode (D101) shorts out the receiver port and the PI network, which operates as a quarter wave transmission line and transforms the low impedance of the shunt diode to a high impedance at the input of the harmonic filter.

In the receive mode, The diodes are both off, hence, there exists a low attenuation path between the antenna and receiver ports.

HARMONIC FILTER

The harmonic filter consists of part of C101, C102, L101, C103, L102, C104, L103 and C105. The design of the harmonic filter is 5th order chevyshev filter with 0.1dB ripple. This type filter has the advantage that it can give greater attenuation in the stop-band for a given ripple level.

□. AUDIO PATHS

RX AUDIO PATH

Audio processing for the RX audio is achieved via U101. After de-emphasis and volume adjustment by MCU.(pin 29, 30, 31), it is fed to the Audio Power Amplifier, U201. This is a Bridged-tied Load amplifier with a fixed gain of 40dB, developing 300mW output at less than 10% harmonic distortion into the 8Ω internal loudspeaker with nominal 6V battery and supply. Maximum audio power output is greater than 1W.

TX AUDIO TONES

The TX audio is fed from the microphone to Mic Amp, U202C, 202D which contains the pre-emphasis components. The output level is adjusted by the Max Deviation circuit, VR201, and fed to the TX VCO.