SECTION 6

CIRCUIT DESCRIPTION

6.1 OVERVIEW

Section 6 describes the circuit operation of the logic board. This section is intended for use by engineering and service personnel.

6.2 CIRCUIT DESCRIPTION

Refer to Figure 6-1 for the block diagram of the Integra-TR Logic Board.

6.2.1 MICROPROCESSOR CIRCUIT

The microprocessor contains two Z84015 CMOS low power Intelligent Peripheral Controllers (IPC). Each IPC is an 8-bit microprocessor integrated with CTC, SIO, PIO Clock Generator Controller and Watch Dog Timer.

One of the Z84015s (U17) is used in the normal mode. The other Z84015 (U21) is used in the evaluation mode and only the CTC, SIO and PIO sections are used. The CPU section is disabled.

The first Z84015 Clock Generator uses a 19.6608 MHz crystal that provides a CPU clock rate of 9.8304 MHz for both Z84015s. The 9.8304 MHz clock is further divided by 2 to feed all 8 CTC (4 in each Z84015).

The 64K-memory space of the Z84015 is divided into two blocks of 32k each. The lower 32K are used for the firmware program and the upper 32K by the CMOS RAM (U18). The memory IC used for the program is a CMOS FLASH (U22) with 1024 sectors of 128 bytes each.

The dual Z84015 circuit provides up to 8 Counter Timer Channels (CTC), 4 Serial Input/Output (SIO) and 32 Parallel In-put/Output (PIO) lines.

The CPU also provides the clock for the CPLD modem.

6.2.2 RS232

The RS232 IC (U15) is used to interface the application DE-9 connector to the SIO_B section of U17, and the set-up DE-9 connector to the SIO_A section of U21. Two receivers remain enabled in sleep mode to ensure fast wakeup.

6.2.3 MODEM

The modem section is used to interface the serial digital data to the transceiver.

The CPLD modem IC (U16) with a programmable Raise-Cosine filter (U10) operates in DRCMSK mode at 2400, 4800, 9600, and 19200 bits/sec. It incorporates a 7-bit hardware scrambler and uses Differential (NRZI) encoding in DRCMSK mode to minimize data pattern-sensitivity. An electronic potentiometer U5B

(E-Pot), controlled by CPU U17, is used to set the transmitter deviation by amplitude adjustment of the baseband signal. Electronic potentiometer U5C is also provided to fine adjust the RF carrier frequency.

6.2.4 TRANSMIT & RECEIVE DATA

Transmit Data from the RS-232 port is level-shifted to TTL by U15 and passed through the CPU for further processing and conversion from asynchronous to synchronous format. The CPLD modem, U16, takes the digital data stream from SIO-A of the CPU and synthesizes to the constant-amplitude analog baseband signal. The synthesized data stream is filtered by U10, buffered by U9B, and applied to radio module TXA at P1-6.

Received signals are applied to the RXA pin on P1-13 and amplified by U3A. U3A gain is set by the electronic potentiometer, U5D, and filtered by U10. The same filter circuit is used for transmission and reception. Two analog multiplexer/demultiplexer gates (U8A and B) controlled by TX_EN line are used for sharing. The filter U10 cut-off frequency is programmable by the CPLD, based on the data rate. The analog signal is buffered by U1D and fed to Peak Detectors U3C, U3D, and U3B, and to slicer circuit U1C via U1B. The raw data is passed to the CPLD modem (U16) for de-scrambling and receive clock recovery. The resulting synchronous bit stream is fed to CPU SIO-A for further processing and conversion to asynchronous format before delivery to the RS-232 driver and to the user port.

6.2.5 INTEGRA-TR A/D AND DIGIPOT

An 8 channel, 8-bit successive approximation A/D converter, type ADC0838 (U4), is interfaced to CPU (U17) and Peripheral (U21).

CH0 and CH1 are connected to the positive and negative peak detector of the modem section. The software can read the positive or negative value of an RX signal, or using the differential mode, the actual peak-to-peak RX signal value.

CH3 is used to measure the radio RSSI signal which was amplified by U7A.

CH4 is connected to the radio diagnostic signal (P3-14). This pin is used to output an analog signal corresponding to the power output and the reflected signal.

CH5 is connected to U6 (LM50), a temperature sensor with a -40 to +125°C range.

CH6 is used to read the SWB+ voltage after proper scaling into the 0-5 V range.

CH7 and CH8 are connected to EXT SIGNAL 1 and 2. A 2:1 divider and protection circuit is inserted between both external signals and the A/D.

The External Signal (pins 1 and 2) is also connected to U21 at PB6 and PB7 through transistors Q3 and Q4 and can be used for Analog Input or Digital Output.

EXT_SIGNAL 2 is also connected to the Rx test point RX-TP through U8A (74HC4066). Under software control, the RX-TP (scaled down by 2) is available on the power connector for trouble-shooting purposes.

A 4-channel digital potentiometer type (U5) is used to adjust the RX Signal, TX Modulation, Carrier Frequency and Carrier Detect Threshold.

An 8 channel, 8-bit successive approximation A/D converter, type AD0838 (U9), is interfaced to CPU (U18) and Peripheral (U20).

U19 generates a power-on reset for the CPU and U6 is a temperature sensor used by the firmware to compensate for variations in RSSI.

The RSSI signal from the transceiver is amplified and filtered by U7A. The signal is compared to a threshold value set by digital potentiometer (U5A). The output of the comparator (U7B) is used to change the hold time of both peak detectors at the beginning of the receive packet.

6.2.6 WAKE-UP CIRCUIT

The wake-up circuit for the Integra-TR consists of a 50 ms monostable circuit that is triggered by the rising edge of a Sleep signal from CPU (U17). The falling edge of this 50 ms pulse (end of pulse) is connected to the NMI of the CPU and will wake up the CPU from Sleep mode after 50 ms.

When exiting SLEEP mode on a \NMI, the CPU firmware will increment a counter, then return to Sleep until it reaches a limit set by a software parameter. When the programmed count is reached the CPU will wake up the radio and the RS232 driver, program the synthesizer, and watch for channel activity.

While in sleep mode (during the 50 ms pulse), an active RTS from either communication port will reset (terminate) the 50 ms pulse so that its falling edge will restart the CPU immediately.

The CPU will check to see if either RTS signal is valid each time it is restarted by the \NMI. The firmware will only start the sleep timer after checking that all “wakeup” inputs are inactive.

6.2.7 POWER SUPPLY

The 13.3-volt DC power input is protected by a 3-amp fuse and reverse-protected by a diode.

A 5 volt, low voltage regulator (U12) is used to power all digital functions and another 5 volt, low voltage regulator is used to control the analog +5V_SW voltage in the sleep mode.

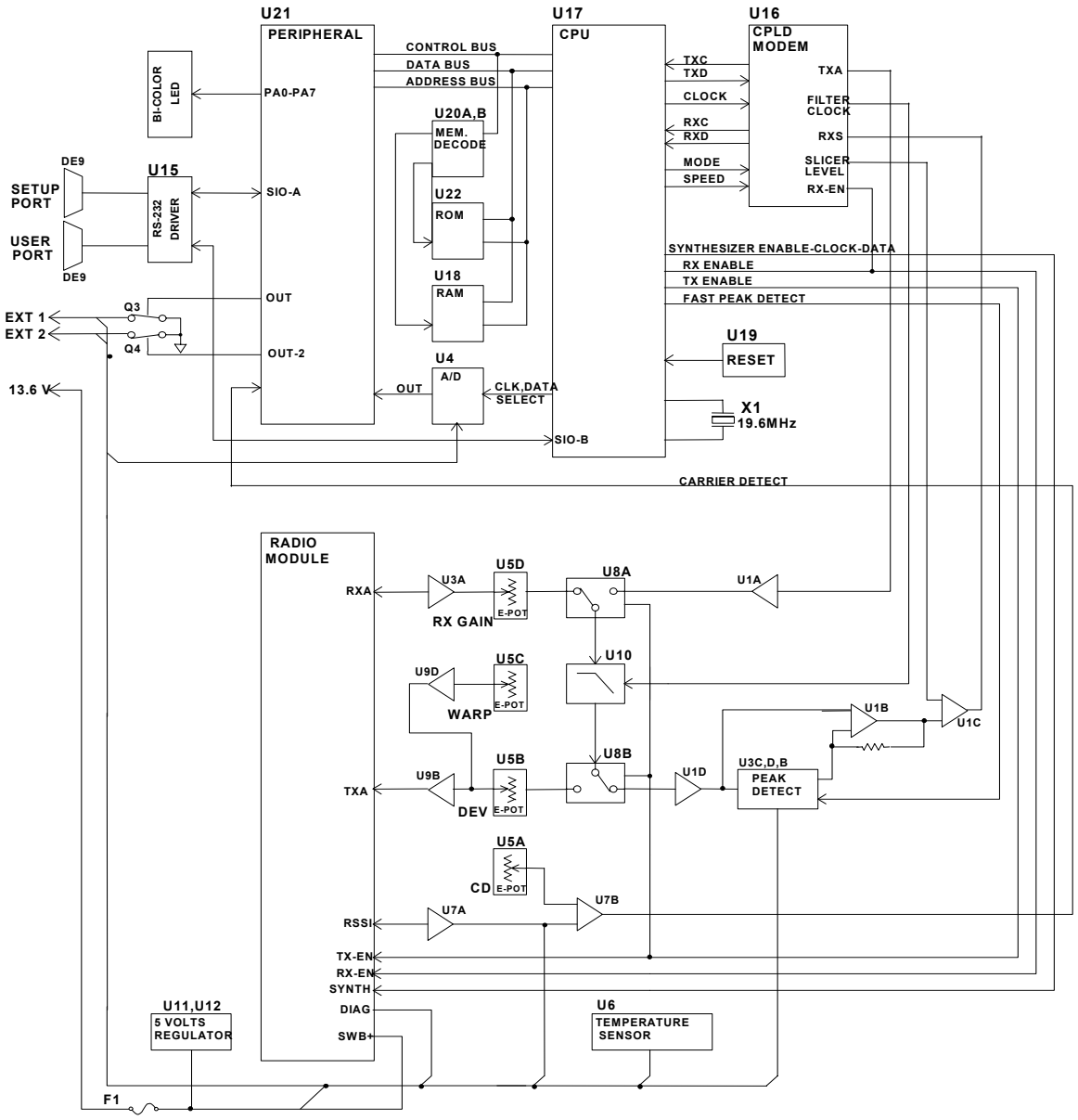

Figure 6-1 Logic Board Block Diagram