Delivery Specifications

Product Description	LTE Cat. M1 Module
Customer Part Number	TBD
WNC Model Name	DLSS-WI01
FCC ID	NKR-DLSSWI01
IC	4441A-DLSSWI01
Version	V1.0
Manufacturer	Wistron NeWeb Corporation Address: 20 Park Avenue II Road, Hsinchu Science Park, Hsinchu 308, Taiwan, R.O.C. Tel: +886-3-666-7799
Production Plant	Wistron NeWeb Corporation Address : 5 Lihsin Rd. VI, Hsinchu Science Park, Hsinchu 300, Taiwan Tel: +886-3-666-7799
Production Country	Taiwan

About this Data Sheet

Purpose and Scope

The DLSS-WI01 is a complete LTE Cat M1/NB1/NB2 module with baseband, RF and memory, targeted at narrow band low data rate M2M and IoT devices for wide deployment. This document provides technical information about DLSS-WI01 LGA module. DLSS-WI01 is based on Sequans's Monarch 2 platform.

Who Should Read this Document?

This document is intended for engineers who develop User Equipment (UE) for LTE systems.

Changes in this Document

This revision is the first version.

Table 1: Revision history

Revision	Date	Changes from the previous version
1.0	Jul. 2024	• Initial Version

Table of Contents

1 General Description

The WNC DLSS-WI01 is an LTE Cat M1/NB1/NB2 module based on Sequans' second-generation Monarch 2 chip platform. The DLSS-WI01 is a complete module solution, including a Single-SKU™ RF front end capable of operating on every GSM band worldwide, and an integrated EAL5+ Secure Element (SE) capable of hosting the SIM inside the module with zero compromise on security while lowering cost and reducing complexity. The DLSS-WI01 features a very small and cost-effective form factor that requires no external components.

The DLSS-WI01 leverages Sequans's 15-plus years of experience in 4G+ technologies and incorporates Sequans's carrier-approved LTE protocol stack and a software suite among the most mature in the industry. The DLSS-WI01 inherits Monarch's already certified LTE-M and NB-IoT stack and delivers significantly improved performance and lower power consumption thanks to Sequans's second-generation Monarch 2 chip and the new module architecture.

1.1 Frequency Bands

The DLSS-WI01 supports the following bands:

- B1 (2100);
- B2 (1900 PCS);
- B3 (1800+);
- B4 (AWS-1);
- B5 (850);
- B8 (900 GSM);
- B12 (700 a);
- B13 (700 c);
- B14 (700 PS);
- B17 (700 b);
- B18 (800 Lower);
- B19 (800 Upper);
- B20 (800 DD);
- B25 (1900+);
- B26 (850+);
- B28 (700 APT);
- B66 (AWS-3);
- B71 (600)
- B85 (700 a+).
- B106 (LMR) -> 897.5 - 900.5 MHz in the US according to the FCC rules

1.2 Applications

DLSS-WI01 is ideal for adding LTE-M and/or NB-IoT LTE connectivity to narrow band, low data rate M2M and IoT devices such as utility meters, industrial sensors, health and fitness appliances, asset trackers, and many additional devices in smart home, smart city, and wearable applications.

DLSS-WI01 can also be used as a slim modem controlled by an external MCU via its UART. Alternatively, the DLSS-WI01 can execute applets on its embedded MCU.

1.3 Block Diagram

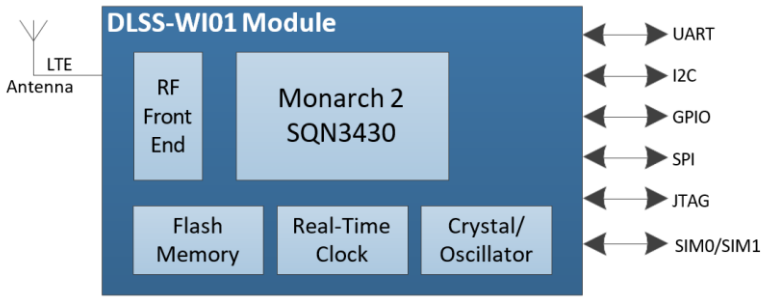

Figure 1: DLSS-WI01 Block Diagram

Note: Two distinct antennas are required in the design. LTE and GNSS RF paths share the same RF front-end block after an RF switch. To get the best GNSS performance, both an external SAW filter and a LNA are strongly recommended.

1.4 General Features

Physical Characteristics	LGA module, 120 pads. Size: 16.3 × 17 × 2.3 mm (hardware Rev. 3)
Temperature Range	Operation temperature range: -40 to +85 °C Storage: MSL3
Power Supply	Voltage range for RF compliance: 2.5 to 5.5 V Functional voltage range: 2.2 to 5.5 V
Tx Power	+23 dBm in each band
Interfaces	• Dual (U)SIM Card Interface: support for external, removable or fixed UICC. Support for integrated UICC (iUICC) with a dedicated p/n; • 4x High-Speed UART Interfaces with flow control, up to 921600 bauds; • GPIOs, I2C, SPI, PWM, Pulse Counter, I2S/PCM, ADC;
SMS	Text and PDU modes
Firmware Upgrade	UART interface, FOTA, support of full and differential firmware upgrade

RoHS	All hardware components are fully compliant with EU RoHS directive, bromine-free
LTE Feature	• 3GPP LTE Release 13/14 Cat M1/NB1/NB2 compliant; • LTE Cat M1: 1.1 Mbps / 0.3 Mbps UL/DL throughput; • LTE Cat NB1: 62.5 kbps / 27.2 kbps UL/DL throughput; • LTE Cat NB2: 160 kbps / 120.7 kbps UL/DL throughput.

1.5 Available Part Numbers

DLSS-WI01's ECCN is 5A991.

Table 2: Available Part Numbers

Available Part Number	Hardware Version	Software Build (ATI1)	UE Version (ATI1)	PTCRB Model Name / Model	SVN	Availability Status
GP02RBAQRF		LR 8.2.0.2	UE 8.2.0.2	DLSS-WI01	15	Available, OTP unlocked

2 Interfaces

The DLSS-WI01 provides electric interfaces connecting it to the external parts, such as communication I/O ports, GPIO and antenna RF I/O. This chapter provides information about all these interfaces.

Power supply pins and details thereof are detailed in section Electrical, RF and Thermal Characteristics.

Important: Please refer to this data sheet's companion MS-Excel file for details on each pin's:

- Default assigned function;
- State during low power modes;
- Configurability with AT commands;
- Pull status and requirements.

2.1 Pin Assignment

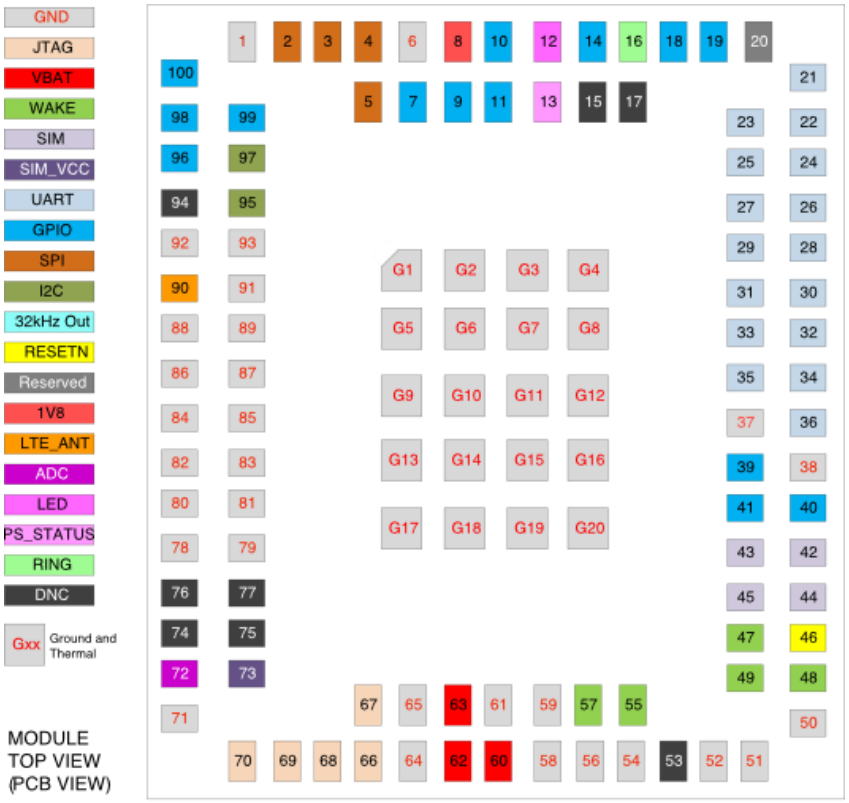

Figure 2: DLSS-WI01 Module Pads Assignments

2.2 UART

When the DLSS-WI01 is used as a slim modem, it has three UARTs available. The default function for each UART is as follows:

- UART0: data and control from external MCU via AT commands
- UART1: debug and upgrade
- UART2: modem console

This default configuration can be overridden.

Attention: Although possible, configuring two different UARTs as console will cause the kernel log messages to randomly appear on either one of them.

Note: See section Power for behavior of I/Os in Deep Sleep mode.

Table 3: UART Signals

Pad #	Pad Name	Primary Function	Alternate Function [4]	Power Group	Direction	Pad type [5]	Reset state
36	GPIO12/ TXD0	TXD0	GPIO12	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		In for primary function, UART0					
34	GPIO13/ RXD0	RXD0	GPIO13	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		Out for primary function, UART0					
35	GPIO14/ CTS0	CTS0	GPIO14	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		Out for primary function, UART0					
33	RTS0	RTS0	N/A	PMU_5V	In	IN	High-Z
		Wake signal enabled by default.					
32	TXD1	TXD1	N/A	PVDD_1V8	In	BIDIR	High-Z, 2 mA
		UART1					
30	RXD1	RXD1	N/A	PVDD_1V8	Out	BIDIR	Out-1, 2 mA
		UART1					
31	CTS1	CTS1	N/A	PVDD_1V8	Out	BIDIR	Out-1, 2 mA
		UART1					
29	RTS1	RTS1	N/A	PMU_5V	In	IN	High-Z
		Wake signal enabled by default.					
28	GPIO15/ TXD2	TXD2	GPIO15	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		In for primary function, UART2					

[4] Alternate functions will be available in future versions via SW upgrade.

[5] UART pad types's electrical characteristics are detailed in Table 21 and Table 22.

Pad #	Pad Name	Primary Function	Alternate Function [4]	Power Group	Direction	Pad type [5]	Reset state
26	GPIO16/ RXD2	RXD2	GPIO16	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		Out for primary function, UART2					
27	GPIO17/ CTS2/ DCD0	GPIO17	CTS2/ DCD0	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		UART2					
25	GPIO18/ RTS2/DSR0	GPIO18	RTS2/ DSR0	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		UART2					

High-Speed UARTs Flow Control Signals

- CTS0, CTS1, CTS2 : Clear-To-Send signals of resp. UART0, UART1, UART2, (active low). To be connected to the CTS of the remote UART device. See Figure 3.

  Leave CTS unconnected if hardware flow control is not used.

- RTS0, RTS1, RTS2 : Ready-To-Send signals of resp. UART0, UART1, UART2, (active low). To be connected to the RTS of the remote UART device. Tie to a 1 kΩ pull-down when flow control is not used. If connected to an external part (like a RS 232 driver), the user must insure that the part presents a low level to the DLSS-WI01 See Figure 3.

Figure 3 represents the typical implementation for hardware flow control.

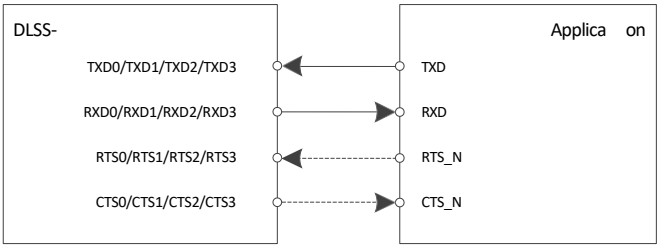

Figure 3: UART Convention and Flow Control

Note: Please refer to *Module Integration Guide* for details on UART connections.

2.3 USIM Interfaces

2.3.1 SIM0 Interface

This is the main external SIM interface. It can be used with removable or non-removable SIM cards or with soldered SIM chips. The modem manages the SIM's power supply to keep consumption as low as possible.

Note: See Section Power for behaviour of I/Os in Deep Sleep mode.

[4] Alternate functions will be available in future versions via SW upgrade.

[5] UART pad types's electrical characteristics are detailed in Table 21 and Table 22.

Table 4: SIM0 Signals

Pad #	Pad Name	Primary Function	Power Group	Direction	Pad type [3]	Reset State	Comment
42	SIM0_CLK	SIM0_CLK	PVDD_1V8	Out	BIDIR	Out-0, 2 mA	Main SIM
45	SIM0_DETECT [4]	SIM0_DETECT	PMU_5V	In	IN	High-Z	Main SIM
44	SIM0_IO	SIM0_IO	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA	Main SIM
43	SIM0_RSTN	SIM0_RSTN	PVDD_1V8	Out	BIDIR	Out-0, 2 mA	Main SIM
73	SIM0_VCC [5]	SIM0_VCC	PVDD_1V8	Out	SUPPLY	Out-0, 2 mA	Main SIM

2.3.2 SIM1 Interface

This DLSS-WI01's interface to a second SIM is typically meant for soldered SIM chips (since it lacks SIM detect and SIM VCC). If the board makes use of a single SIM, it should be connected to the main SIM interface (see Section SIM0 Interface above).

Note: See Section Power for behavior of I/Os in Deep Sleepmode.

Table 5: SIM1 Signals

Pad #	Pad Name	Primary Function	Alternate Function [9]	Power Group	Direction	Pad Type [10]	Reset state
40	GPIO26/ SIM1_CLK	GPIO26	SIM1_CLK	PVDD_1V8	Out	BIDIR	Out-0, 2 mA
41	GPIO27/ SIM1_RESETN	GPIO27	SIM1_RESETN	PVDD_1V8	Out	BIDIR	Out-0, 2 mA
39	GPIO25/ SIM1_IO	GPIO25	SIM1_IO	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA

Important: Both SIM0 and SIM1 interfaces use 1.8 V signaling.

2.4 I²C

Note: See Section Power for behavior of I/Os in Deep Sleep mode.

[6] USIM pad type electrical characteristics are detailed in Table 21 and Table 22.

[7] SIM0_DETECT is active high (high when a card is present, low when no card is present). It can be configured as a WAKEpin via software command.

8 See range of values in Table 15.

9 Alternate functions will be available in future versions via SW upgrade.

10 Pad type electrical characteristics are detailed in Table 21.

Table 6: I²C Pad Details

Pad #	Pad Name	Primary Function	Alternate Function [8]	Power Group	Direction	Pad type [9]	Reset State
95	GPIO23/ I2C_SDA	GPIO23	I2C_SDA	PVDD_1V8	In/Out	BIDIR	High-Z
97	GPIO24/ I2C_SCL	GPIO24	I2C_SCL	PVDD_1V8	In/Out	BIDIR	High-Z

2.5 PCM

Note: See section Power for behavior of I/Os in Deep Sleep mode.

Table 7: PCM Pad Details

Pad #	Pad Name	Primary Function	Alternate Function [10]	Power Group	Direction	Pad type [11]	Reset State
96	GPIO4/ PCM_CLK	GPIO4	PCM_CLK	PVDD_1V8	In/Out	BIDIR	High-Z
98	GPIO3/ PCM_RXD	GPIO3	PCM_RXD	PVDD_1V8	In/Out	BIDIR	High-Z
99	GPIO5/ PCM_FS	GPIO5	PCM_FS	PVDD_1V8	In/Out	BIDIR	High-Z
100	GPIO6/ PCM_TXD	GPIO6	PCM_TXD	PVDD_1V8	In/Out	BIDIR	High-Z

2.6 SPI

Note: See section Power for behavior of I/Os in Deep Sleep mode.

Table 8: SPI Pad Details

Pad #	Pad Name	Primary Function	Alternate Function [12]	Power Group	Direction	Pad type [13]	Reset state
3	GPIO7/ SPI_SDI	GPIO7	SPI_SDI	PVDD_1V8	In/Out	BIDIR	High-Z
4	GPIO8/ SPI_SDO	GPIO8	SPI_SDO	PVDD_1V8	In/Out	BIDIR	High-Z

11 Alternate functions will be available in future versions via SW upgrade.

12 I²C pad types's electrical characteristics are detailed in Table 21.

13 Alternate functions will be available in future versions via SW upgrade.

14 PCM pad types's electrical characteristics are detailed Table 21.

15 Alternate functions will be available in future versions via SW upgrade.

16 SPI pad types' elctrical characteristics are detailed in Table 21.

Pad #	Pad Name	Primary Function	Alternate Function [12]	Power Group	Direction	Pad type [13]	Reset state
2	GPIO9/ SPI_CLK	GPIO9	SPI_CLK	PVDD_1V8	In/Out	BIDIR	High-Z
5	GPIO10/ SPI_CSN1	GPIO10	SPI_CSN1	PVDD_1V8	In/Out	BIDIR	High-Z
7	GPIO11/ SPI_CSN2	GPIO11	SPI_CSN2	PVDD_1V8	In/Out	BIDIR	High-Z

2.7 GPIO

33 GPIOs are available on the DLSS-WI01 the first 28 are named GPIO1 to GPIO28 and the last five GPIO31 to GPIO35. The GPIOs listed in Table 9 are not enabled by default. Their states are controlled by software.

Table 9: GPIO pads detail

GPIO Range	Default State
GPIO3 to GPIO11	Disabled
GPIO17 to GPIO28	Disabled
GPIO31 to GPIO32	Disabled

The GPIOs are documented in this data sheet according to their shared or assigned function. In addition to the GPIO, five wake signals are also available (see section Other Signals).

2.8 Other Signals

Table 10: GND and DNC pads

Pads Type	Pads Number
GND	1, 6, 37, 38, 50, 51, 52, 54, 56, 58, 59, 61, 64, 65, 71,78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 91, 92, 93
DNC (Reserved)	15, 17, 53, 74, 75, 76, 77, 94

Note: See Section Power for behavior of I/Os in Deep Sleep mode.

15 Alternate functions will be available in future versions via SW upgrade.

16 SPI pad types' electrical characteristics are detailed in Table 21.

17 Functions will be available in future versions via SW upgrade.

Table 11: Other Signals (No Interface)

Pad #	Name	Primary Function	Alternate Function [17]	Power Group	Direction	Pad Type [18]	Reset State
72	ADC1	ADC1 (see below)	N/A	N/A	In	IN	N/A
		Analogue-Digital Converter (ADC, IN)					
12	GPIO1/ STATUS_LED	STATUS_LED	GPIO1	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		Primary Function: Status LED (STATUS_LED, OUT)					
13	GPIO2/ PS_STATUS	PS_STATUS	GPIO2	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		Primary Function: Power Saving status (PS_STATUS, OUT) enabled by default. Active high.					
14	GPIO28/DTR0	GPIO28 (see Note 14)	DTR0	PVDD_1V8	In/Out	BIDIR	High-Z
19	GPIO31/ PWM0/ PULSE0/ 19M2_OUT	GPIO31 (see Note 14)	PWM0/ PULSE0/ 19M2_OUT	PVDD_1V8	In/Out	BIDIR	High-Z
18	GPIO32/ PWM1/ PULSE1	GPIO32 (see Note 14)	PWM1/ PULSE1	PVDD_1V8	In/Out	BIDIR	High-Z
9	GPIO33/ TX_IND	TX_IND	GPIO33	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		Primary Function: Transmission indicator (TX_IND, OUT). Active high.					
10	GPIO34/ ANT_TUNE0	ANT_TUNE0	GPIO34	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		Primary Function: Antenna tuning (ANT_TUNE0, OUT)					
11	GPIO35/ ANT_TUNE1	ANT_TUNE1	GPIO35	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		Primary Function: Antenna tuning (ANT_TUNE1, OUT)					
20	RESERVED/ FFF_FFH	RESERVED	N/A	PVDD_1V8	N/A	BIDIR	High-Z, 2 mA
		Boot mode selection (FFF_FFH, IN). This pad needs a pull-down resistor by default.					
15, 17, 53, 74, 75. 76. 77, 94	RESERVED	RESERVED	N/A	PVDD_1V8	N/A	BIDIR	N/A
		Do not connect					
46	RESETN	RESETN	N/A	PMU_5V	In	IN	In, Pull-up
		Module HW reset signal. Active low. The minimum duration of a reset pulse on the RESETN signal is 100 µs.					

18 Pad type's electrical characteristics are detailed in Table 21 and Table 22.

Pad #	Name	Primary Function	Alternate Function [14]	Power Group	Direction	Pad Type [15]	Reset State
16	RING0	RING0	N/A	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		UART0 ring line (RING0, OUT). Enabled by default with inverted polarity.					
48	WAKE0	WAKE0	N/A	PMU_5V	In	IN	High-Z
		Wake #0 input line (WAKE0, IN), disabled by default.					
47	WAKE1	WAKE1	N/A	PMU_5V	In	IN	High-Z
		Wake #1 input line (WAKE1, IN), disabled by default.					
49	WAKE2	WAKE2	N/A	PMU_5V	In	IN	High-Z
		Wake #2 input line (WAKE2, IN), disabled by default.					
55	WAKE3	WAKE3	N/A	PMU_5V	In	IN	High-Z
		Wake #3 input line (WAKE3, IN), disabled by default.					
57	WAKE4	WAKE4	N/A	PMU_5V	In	IN	High-Z
		Wake #4 input line (WAKE4, IN), disabled by default.					

2.8.1 ADC Specifications

The ADC1 pin 72 has the following specifications:

Table 12: ADC Specifications

Parameter	Value	Unit
Resolution	14	bit
Dynamic Range	75	dB
Signal-to-Noise Ratio (SNR)	68	dB
Effective Number of Bits	11	bit
Input Signal Bandwidth	1.4	MHz
Full-scale Voltage	1.8	V
Input Resistance	40	kΩ

2.9 JTAG

Note: See Section Power for behavior of I/Os in Deep Sleep mode.

[17] Functions will be available in future versions via SW upgrade.

[18] Pad type's electrical characteristics are detailed in Table 21 and Table 22.

[19] JTAG pad type's electrical characteristics are detailed in Table 21.

Table 13: JTAG pads Details

Pad #	Pad Name	Primary Function	Power Group	Direction	Pad type [19]	Reset State
69	JTAG_TCK	JTAG_TCK	PVDD_1V8	In	IN	In, Pull-down, Schmitt-trigger
67	JTAG_TDI	JTAG_TDI	PVDD_1V8	In	IN	In, Pull-up
68	JTAG_TDO	JTAG_TDO	PVDD_1V8	Out	BIDIR	Out, 0
66	JTAG_TMS	JTAG_TMS	PVDD_1V8	In	IN	In, Pull-up
70	JTAG_TRSTN	JTAG_TRSTN	PVDD_1V8	In	IN	In, Pull-down

Note: The DLSS-WI01 does not support boundary scan (IEEE 1149.1) for production testing.

2.10 Antenna

Table 14: Antenna pad Details

Pad #	Pad Name	Direction	Comments
90	LTE_ANT	In/Out	Main Antenna, for Rx and Tx

3 Electrical, RF and Thermal Characteristics

3.1 Power

Important: Details about power consumption can be found in the Software Release note corresponding to the product's software version installed.

3.1.1 Power Pads Characteristics

Note: Pad 1V8 is the reference voltage for I/Os. It can be used to provide power to small devices (100 mA maximum usage). This voltage is not available when the modem is in Deep Sleep mode. When the modem is in standby the voltage drops to 1.62 V as per Table 15.

Table 15: Power Pads

Pad #	Pad Name	Power Group	Direction	Min Value	Typical Value	Max Value
8	1V8 (see Note above)	PVDD_1V8	Out	1.62 V	1.8 V	1.98 V
73	SIM_VCC [17]	PVDD_1V8	Out	1.62 V	1.8 V	1.98 V
60, 62, 63	VBAT	N/A	In	2.2 V		5.5 V

Note: Reference VBAT voltage range is 2.5 V to 5.5 V for RF-compliant operation and 2.2 V to 5.5 V for functional operation with possible degradation of RF performances.

Note: The DLSS-WI01 does not use any boost or step-up DC/DC converters.

3.1.2 Power-Up and Reset Sequences

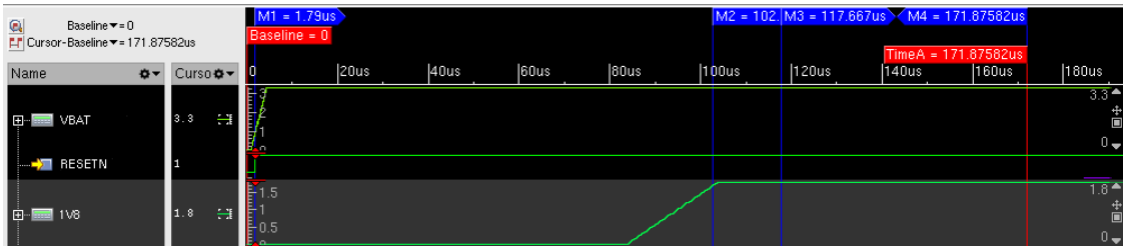

Figure 4: Typical Timing Diagram for Power-Up Sequence

Important: The 1V8 power signal can remain low up to 370 µs after the VBAT rising edge

[17] See also Section USIM Interfaces.

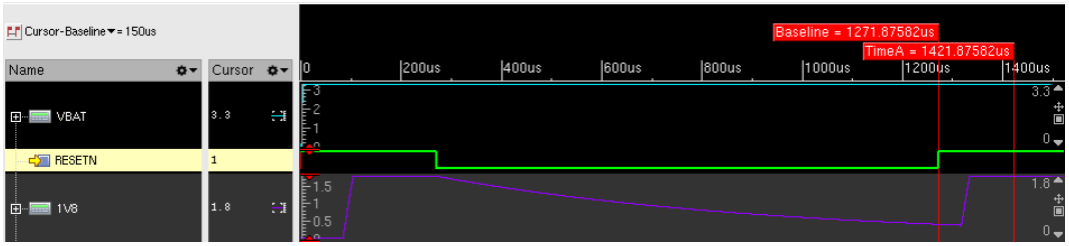

Figure 5: Typical Timing Diagram for Reset Sequence

Note: since RESETN is pulled-up internally, RESETN does not need to be held low after VBAT is established, as shown in Figure 5. There is no timing condition between RESETN and VBAT.

Note: RESETN minimum duration for reliable detection is 100 µs

3.1.3 Power States

Figure 6 represents the electrical states of the module and their transitions.

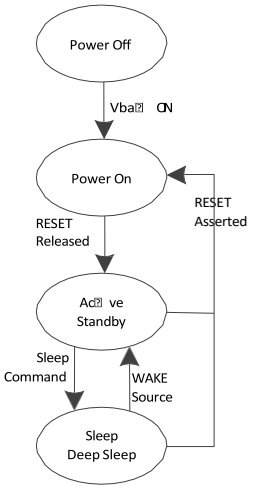

Figure 6: Electrical States and Transitions

There are four possible power modes:

- Active mode: operational, UART on, RF on, LCPU/MCPU/DSP are running. Power consumption depends on workload and transmit power level.
- Standby mode: Same as active mode, except RF off.
- Sleep mode: MCPU/LCPU/DSP are power gated, UART off, RAM content is salvaged. Power level 300 µA circa.
- Deep Sleep Mode: Only the power management unit (PMU) stays active. Power level 1 µA.

More information is given in the table below:

Table 16: Power Modes Description

Power Mode	LTE Mode	Available Interfaces
Active	Connected (RF on)	All interfaces
Standby	Connected (RF off)	All interfaces
Sleep	Short eDRX idle duration RRC Idle	WAKE pins (including RTS0/1)

Power Mode	LTE Mode	Available Interfaces
Deep Sleep	PSM idle, Long eDRX idle duration, radio-off, airplane	WAKE pins (including RTS0/1)

3.1.4 PVDD_1V8 BIDIR Pads State in Deep Sleep mode

In Deep Sleep mode, the Digital PVDD_1V8 bi-directional I/Os are completely powered off and behave like 50 MΩ high-impedance pins.

3.1.5 PMU_5V IN Pads State in Deep Sleep mode

In Deep Sleep mode the digital PMU_5V inputs are completely powered off and behave like 180 MΩ high-impedance pins.

Table 17 gives the values of the measured leakage current (measurements taken on silicon) for the PMU wake inputs.

Table 17: Measured Leakage Current for the PMU Wake Inputs

Minimum	Typical	Maximum
3 nA	4 nA	12 nA

Table 18 shows values of the external pull-up/pull-down resistor to be used at the PMU wake inputs pads.

Table 18: External Pull-up/Pull-down Resistor at PMU Wake Input Pads

Minimum	Typical	Maximum
1 kΩ	10 kΩ	100 kΩ

Table 19 details the PMU wake input pulses detection mechanism timings.

Table 19: PMU Wake Input Pulses Detection Mechanism Timings

Maximum pulse width guaranteed to be ignored	Minimum pulse width guaranteed to be recognised
11.1 ns	100 µs

Table 20 provides the internal pull-up current range at RESETN.

Table 20: Internal Pull-Up Current at RESETN Pad

Minimum	Typical	Maximum
73.5 nA	100 nA	160.5 nA

3.2 Digital I/O Characteristics

This section details the voltage and current characteristics of the various I/O pads of the DLSS-WI01.

The I/Os belong either one of two power groups:

- PVDD_1V8
- PMU_5V

The operational voltage range of both power groups is described in Table 21 and Table 22.

CAUTION: Designers must ensure that the input voltage on any of the I/O pads never exceeds the V_{IH} of the power group they belong to.

See Table 21 for the digital I/O characteristics of the different I/O pads. Refer to each interface of the DLSS-WI01 in chapter Interfaces for the power group and I/O pad type of each pad. Note that IN pads are inputs only whereas BIDIR can be both inputs and outputs.

Table 21: DC Ratings for Digital I/Os, PVDD_1V8 Power Group

Symbol	Minimum	Maximum	Unit
V_{IH} Input HIGH level	1.26	3.3	V
V_{IL} Input LOW level	0	0.54	V
V_{OH} Output HIGH voltage	1.44	1.8	V
V_{OL} Output LOW voltage	0	0.36	V
I_{RPU} Input pull-up resistor current	15		µA
R_{RPU} Input pull-up resistance	27	34	kΩ
I_{RPD} Input pull-down resistor current	15		µA
R_{RPD} Input pull-down resistance	27	34	kΩ
V_H Input hysteresis	0.18		V
I_{PAD} Input leakage current, non-tolerant	-1	1	µA
I_{OZ} Off-State leakage current		1	µA

Table 22: DC Ratings for Digital I/Os, PMU_5V Power Group

Symbol	Minimum	Maximum	Unit
V_{IH} Input HIGH level	0.8	VBAT + 0.6 (max. 5.5)	V
V_{IL} Input LOW level	0	0.2	V

The total capacitance of the DLSS-WI01 is 115 µF. Total inductance is 5.3 µH.

3.3 RF Performance

Important: For proper operation, the VSWR at the antenna pad must be better than 2:1 in conducted mode and 3:1 in radiated mode. A higher value could result either in poor RF performance, reduced Tx power or increased sideband/harmonic emission levels. Very high VSWRs can permanently damage the power amplifier.

It is recommended to add a DC blocking capacitor in series with the module RF input/ output pad (#90).

3.3.1 RF Sensitivity

The DLSS-WI01 exhibits the following typical RF sensitivity at 2.5 V:

Table 23: RF Sensitivity

Technology	Band	Output Power Loss
LTE-M	Low Bands: B5, B8, B12, B13, B14, B17, B18, B19, B20, B26, B28, B71,B106 (hardware Rev. 3 only), B85	-105 dBm
	High bands: B1, B2, B3, B4, B25, B66	-106 dBm
NB-IoT	Low Bands: B5, B8, B12, B13, B14, B17, B18, B19, B20, B26, B28, B71,B106 (hardware Rev. 3 only), B85	-108 dBm
	High bands: B1, B2, B3, B4, B25, B66	-108 dBm

3.3.2 RF Output Power

The DLSS-WI01 maximum output power within the recommended operating range (from 2.5 to 5.5 V) is given in Table 24.

Table 24: RF Max Output Power

Bands	Output Power
All Bands	23 dBm ± 1 dB

3.3.3 RF performance at 2.2 V

While it is not recommended to operate the DLSS-WI01 in the range 2.2 to 2.5 V, the RF section will continue to work normally, albeit with reduced TX output power as shown in Table 25 below.

Table 25: RF Performance at 2.2 V compared to 2.5 V

Temperature	Sensitivity Loss	Output Power Loss
-30 °C	No loss	1.1 dB
25 °C	No loss	1.1 dB
85 °C	No loss	1.7 dB

3.4 Power Supply Dimensioning

This section provides guidance to designers working on the power supply or selecting a suitable battery to power the DLSS-WI01.

3.4.1 Overview

The current consumption of the DLSS-WI01 peaks before every TX sub-frame as shown in Figure 7. In this figure, the time division is 50 µs. Around 150 µs from the start, two current pulses peaking 34% higher than the average current consumption during the 23 dBm TX tone which follows can be observed.

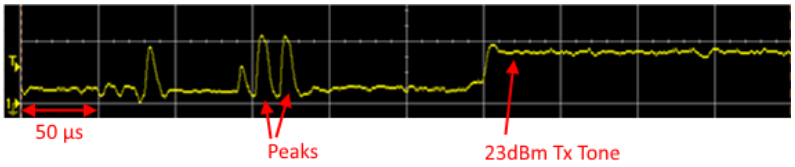

Figure 7: Current Consumption in TX Sub-Frame

3.4.2 Peak Current Measurement Method

WNC recommends to use the setup represented in Figure 8 for peak current measuring. This setup was used to record the measurements presented in Table 26.

Note that:

1. Voltage probes are placed close to module VBAT input;
2. Voltage probes accuracy is calibrated using a current probe;
3. A large capacitance C_{batt} is placed close to the VBAT pin to simulate a battery and screen the device from the parasitic inductances of the cables and tracks;
4. 2 × 22 µF capacitors (C_{ext}) are placed between the voltage probes and the module VBAT input to soften the current peaks.

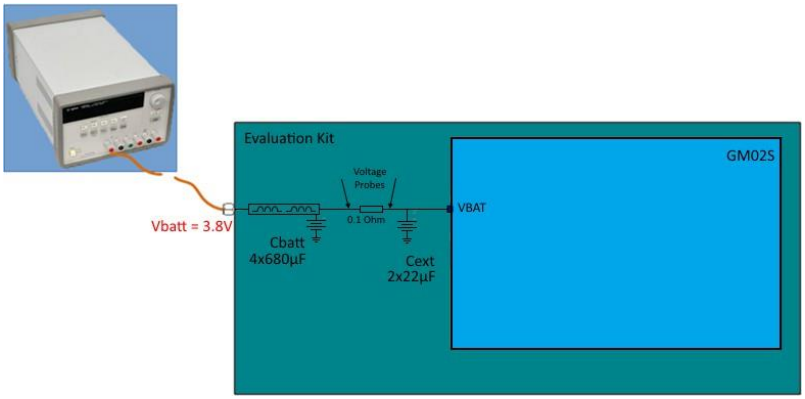

Figure 8: Setup for Current Peak Measurement

3.4.3 Peak Current Measurement

Table 26 gives the peak current values measured on the setup shown on Figure 8 for different voltages and temperatures.

Table 26: Peak Current Measurements

Input Voltage	T = -40°C	T = -30°C	T = +25°C	T = +85°C
5.5 V	328 mA	305 mA	263 mA	268 mA
3.8 V	475 mA	438 mA	444 mA	479 mA
2.5 V	705 mA	667 mA	679 mA	741 mA
2.2 V	676 mA	640 mA	652 mA	717 mA

3.4.4 Margin

Important: It is recommended that designs potentially sensitive to the current peaks described in this section use the recommended C_{ext} 2 × 22 µF and dimension the power supply with an extra 20% margin w/r to the values provided in this section.

3.4.5 Module's Total Capacitance and Inductance

The module's sum of internal capacitance (positive side tolerance) is 115 µF. The module's sum of internal inductance (positive side tolerance) is 5.3 µH.

3.5 Maximum Electrical Ratings

Table 27: Maximum Electrical Ratings

Parameter	Minimum	Maximum
Supply Voltage VBAT	-0.2 V	5.5 V
I/Os in Power Group PVDD_1V8	-0.2 V	4.125 V
I/Os in Power Group PMU_5V	-0.2 V	6.0 V

3.6 Thermal Considerations

Special attention needs to be given to thermal dissipation.

The outer layers of the host board must be covered in as many wide copper areas as possible, and those must be stitched with evenly spaced ground vias. Care must be taken that no air gap exists along the thermal path from the DLSS-WI01 to the dissipating copper area(s). Gaps can be filled with heat conducting materials such as *GapPad™*.

The Gxx pads should be tied to a large ground plane on the customer's PCB layer 1. It is also recommended to have the Gxx pads area on the PCB stitched with through ground vias to improve thermal dissipation.

If the host board is piggybacked over a larger board, the aforementioned heat dissipation considerations should be applied to both the main and the daughter board.

4 Mechanical Characteristics

4.1 Package Description

The module footprint is (16.3 ± 0.15) mm × (17.0 ± 0.15) mm. See below for the other dimensions.

The DLSS-WI01 weighs 1.43 g.

4.1.1 Hardware Module Dimensions

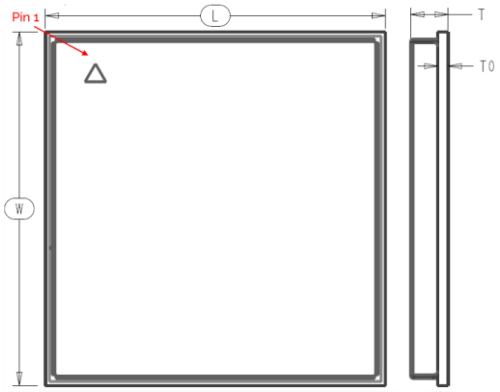

Figure 9: Module Top and Side Views

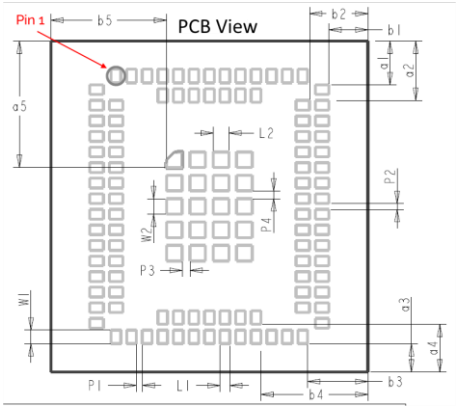

Figure 10: Module PCB Views

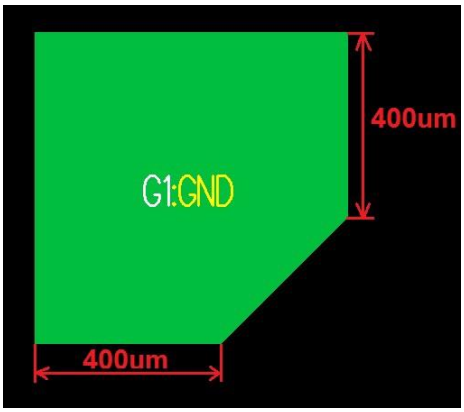

Figure 11: Details of chamfered central ground pad G1

Table 28: Module Dimensions (mm)

Dimension	Value (mm)
L	16.3 ± 0.15
W	17.0 ± 0.15
T	2.3 max (2.2 typical)
T0	0.8 max
L1	0.5 ± 0.1
W1	0.7 ± 0.1
L2	0.8 ± 0.1
W2	0.8 ± 0.1
a1	2.25 ± 0.1
a2	3.05 ± 0.1
a3	1.45 ± 0.1
a4	2.45 ± 0.1
a5	6.5 ± 0.1
b1	2.0 ± 0.1
b2	3.0 ± 0.1
b3	3.1 ± 0.1
b4	5.5 ± 0.1
b5	5.95 ± 0.1
P1	0.3 ± 0.1
P2	0.3 ± 0.1
P3	0.4 ± 0.1
P4	0.4 ± 0.1

4.1.2 Laser Marking

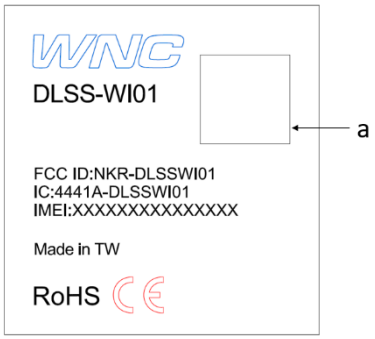

Figure 12: DLSS-WI01 Laser Marking

Notes:

1. The triangle in the bottom-right corner provides pin #1 location.
2. FCC ID: NKR-DLSSWI01
3. IC: 4441A-DLSSWI01
4. IMEI:*XXXXXXXXXXXXXXX*
5. 2D marked “a” refer to IMEI Barcode

4.2 Environmental Conditions

DLSS-WI01 operating conditions:

- Temperature (PCB temperature as measured by on-board thermistor):
  - Operational: -40°C to +85°C;
  - RF compliant: -30°C to +85°C
- Humidity: 10% to 85% (non-condensing)

4.3 Packing

The DLSS-WI01 is delivered in Tape-and-Reel. Details are provided in the figures below.

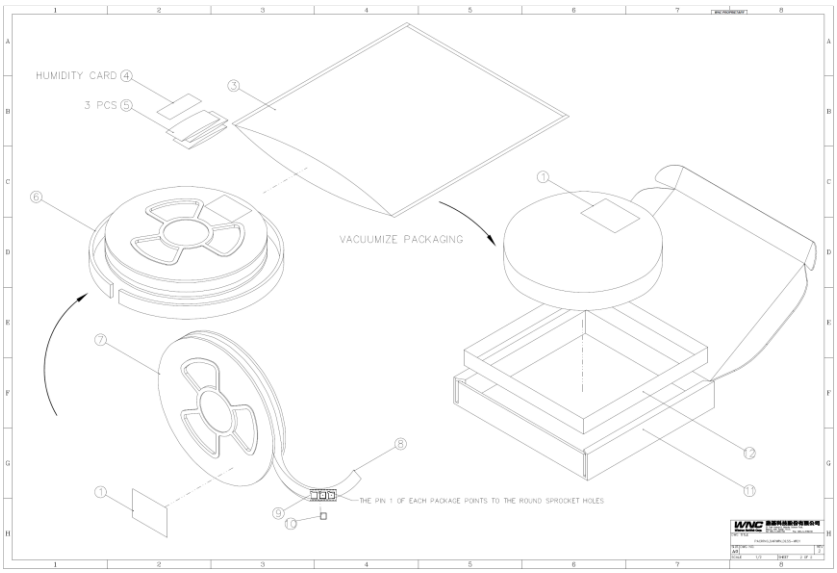

Figure 13: Packing Modules in Reels

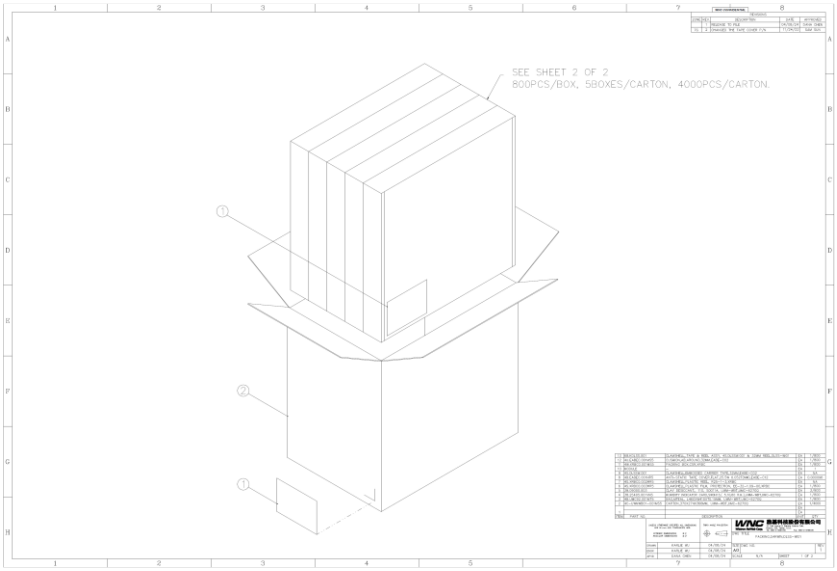

Figure 14: Packing Reels in Boxes

The full box set weights about 5.95 kg.

4.4 Storage and Mounting

The DLSS-WI01 module is Moisture Level 3 rated as per JEDEC industrial standard.

The DLSS-WI01 is JEDEC J-STD-033D compliant and can be stored at T < 40 °C and relative humidity < 90%.

The DLSS-WI01 can withstand up to three reflows at a maximum of 250 °C.

Table 29: Reflow Profile

Profile Feature	
Solder Paste Alloy	Sn 96.5/Ag 3.0/Cu 0.5 (Lead Free solder paste)
Peak Package Body Temperature	235 °C to 245 °C
Fusion Time	Temp: over 220°C Duration: 60 ~ 90 s
Pre-heat / Soak	Temp: 150 ~ 200 °C Time: 60 ~ 120 s
Ramp-up Rate	< 3 °C/s
Ramp-down Rate	-3 to 0 °C/s
Air composition	N_2, O_2 contents less than 1,500 ppm

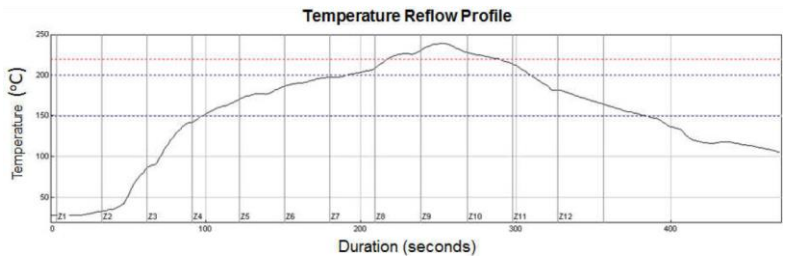

Figure 15: Reflow Profile Parameters

Recommended stencil thickness: 0.1 to 0.13 mm (prefer 0.1 mm). More detail on the PCB land pattern will be provided in a future edition of the document.

Following reflow soldering, the DLSS-WI01 can be washed with deionised RO water to remove any remaining flux. The module then needs a single backing at 125 °C during 16 hours. The module's package may be slightly discoloured during baking.

4.5 Reliability Specifications for Hardware Rev. 3

The DLSS-WI01 has been tested against WNC's industrial reliability specification as described in Table 30.

Table 30: Reliability Test Plan

Item	Test conditions	Standard	#Samples	Result
Preconditioning	(a) Bake: 125°C / 24 hours (b) MSL3: 30°C/60% RH, 192 hrs (c) SAT (CSAM & TSCAN) (d) X-ray (e) Reflow 3 cycles at Tp: 250 ±2°C (f) SAT (CSAM & TSCAN)	JESD22-A113	225	PASS

Item	Test conditions	Standard	#Samples	Result
TC	Temperature Shock Cycling (TC): -40°C to +85°C air to air, 20 minutes, ramp rate 20°C/minute, 1000 cycles	JESD22-A104	25	PASS
THB	Temperature Humidity Bias Test +85°C, 85 % RH, V_{cc} Max, Read Point at 168/500/1,000 hrs	JESD22-A101	25	PASS
HAST	1. 130/100 °C, 85% RH, Vcc max 2. Electrical test	JESD22-A110	25	PASS
Environmental Testing - A Cold	Environmental Testing Test A Cold. -40°C, 500 hrs	IEC60068-2-1 JESD22-A119	25	PASS
Environmental Testing - B Dry Heat	Environmental Testing Test B Dry Heat. +85°C, 500 hrs	IEC60068-2-2 JESD22-A103	25	PASS
HTOL	High Temperature Operating Test 75°C, V_{cc} max, Tx: 50% / Rx: 50%. Read Point at 283/500/1,000 hrs	N/A	50	PASS
LTOL	Low Temperature Operating Test <50°C, V_{cc} max, Tx: 50% / Rx: 50%. Read Point at 283 hrs	JESD22-A108	25	PASS

High Temperature Storage Test (HST)	150 °C/1,000 hours	JESD22-A103	25	PASS
Intermittent Operating Life (IOL)	• Power on/off • 75 °C • 5,000 cycles	N/A	25	PASS
Power and Temperature Cycling	Test Condition A – -40 to +85 °C	JESD22-A105	25	PASS
Shock	Mechanical Shock (MS) (Half Sine, 500G, 1.0 ms, 1 shock for each ±axis)	DIN IEC 68-2-27	15	PASS
Drop	Drop Test: 1. Height: 80 cm; 2. Concrete or steel; 3. All surfaces and edges; 4. 1,500 g / 0.5 ms	DIN IEC 68-2-31 ETS 300019-2-7	15	PASS
Vibration	Vibration Test (Vib) Sweep-Sine Vibration. Sinusoidal, 10 ~ 500 Hz, 1.0 octave/ min, 10 sweep cycles for 2 hr for each axis.	DIN IEC 68-2-6 EIA/TIA 571 §4.1.1.2	15	PASS
ESD	HBM Start: ±1000V, Stop:± 1500V	JS-001JESD22- A114	12	PASS
	CDM Start: ±250V, Stop: ±500V	JS-002STM5.3.1	12	PASS
TCT	Temperature Change Test 10 cycles; 1 cycle has the following steps (roughly 7+ hrs): • Ramp from ambient (23°C) to -40°C at 3°C/min. • 3 hrs at - 40°C • Ramp to 85°C at 3°C/min • 3 hrs at 85°C Ramp from 85°C to 23°C at 3°C/ min	IEC60068-2-14	25	PASS