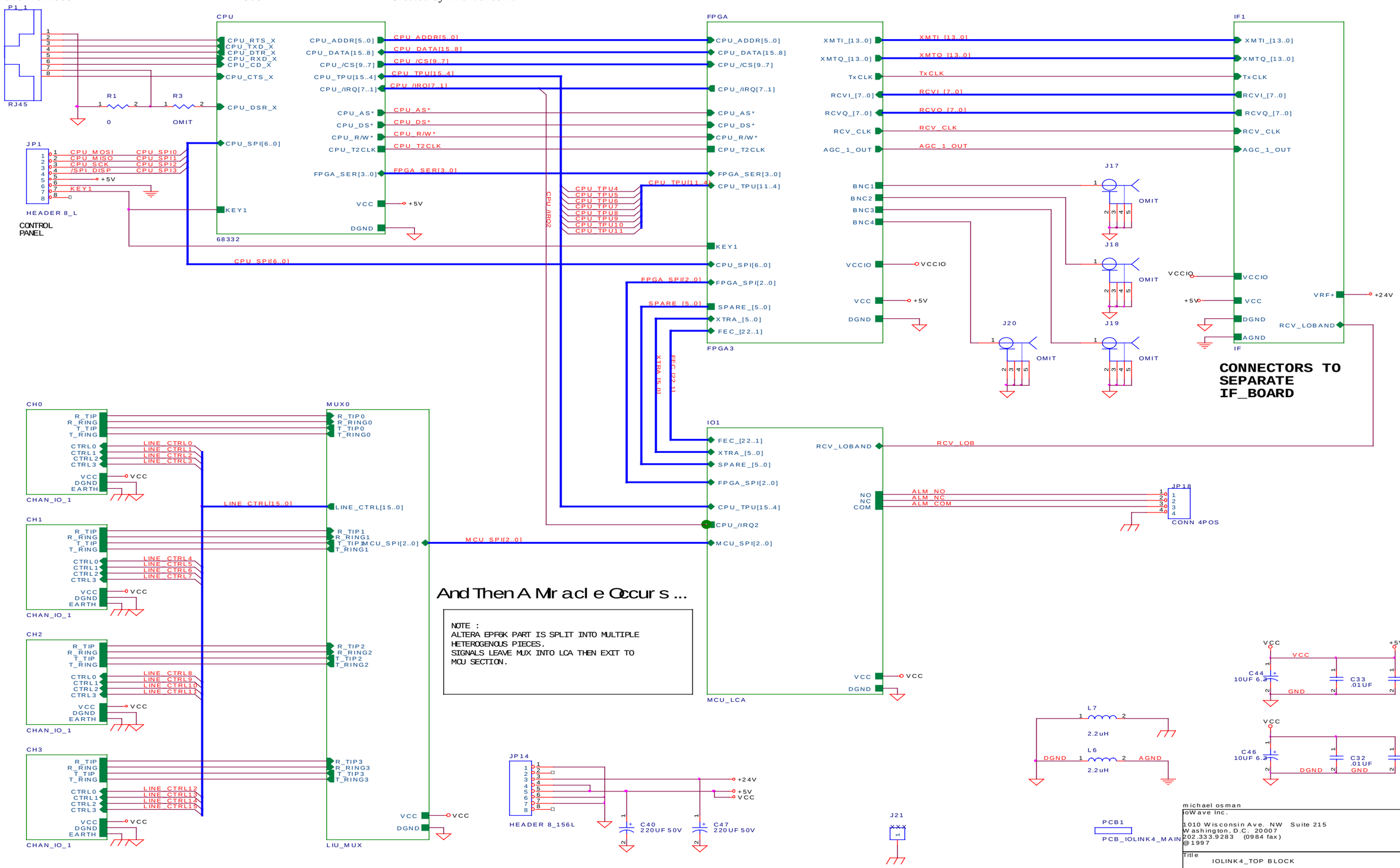
IOWAVE INC.
1010 WISCONSIN AVE. NW SUITE 250
WASHINGTON, DC 20007
202-333-9283

IoLink4

List of Figures :


P1_1
RJ45
CPU
CPU_RTS_X
CPU_TXD_X
CPU_DTR_X
CPU_RXD_X
CPU_CD_X
CPU_CTS_X
CPU_DSR_X
CPU_SPI[6..0]
KEY1
R1
R3
0
OMIT
JP1
CPU_MOSI
CPU_MISO
CPU_SCK
/SPI_DISP
CPU_SPI0
CPU_SPI1
CPU_SPI2
CPU_SPI3
+5V
KEY1
HEADER 8_L
CONTROL PANEL
68332
CPU_ADDR[5..0]
CPU_DATA[15..8]
CPU_/CS[9..7]
CPU_TPU[15..4]
CPU_/IRQ[7..1]
CPU_AS*
CPU_DS*
CPU_R/W*
CPU_T2CLK
FPGA_SER[3..0]
VCC
+5V
DGND
CPU_IRQ2
CPU_TPU4
CPU_TPU5
CPU_TPU6
CPU_TPU7
CPU_TPU8
CPU_TPU9
CPU_TPU10
CPU_TPU11
CPU_TPU[11..4]
FPGA
CPU_ADDR[5..0]
CPU_DATA[15..8]
CPU_/CS[9..7]
CPU_/IRQ[7..1]
CPU_AS*
CPU_DS*
CPU_R/W*
CPU_T2CLK
FPGA_SER[3..0]
CPU_TPU[11..4]
KEY1
CPU_SPI[6..0]
FPGA_SPI[2..0]
SPARE_[5..0]
XTRA_[5..0]
FEC_[22..1]
FPGA3
XMTI_[13..0]
XMTQ_[13..0]
TxCLK
RCVI_[7..0]
RCVQ_[7..0]
RCV_CLK
AGC_1_OUT
BNC1
BNC2
BNC3
BNC4
VCCIO
VCC
+5V
DGND
J17
J18
J19
J20
OMIT
IF1
XMTI_[13..0]
XMTQ_[13..0]
TxCLK
RCVI_[7..0]
RCVQ_[7..0]
RCV_CLK
AGC_1_OUT
VCCIO
VCC
+5V
DGND
AGND
VRF+
+24V
RCV_LOBAND
IF
CONNECTORS TO SEPARATE IF_BOARD
CH0
CH1
CH2
CH3
R_TIP
R_RING
T_TIP
T_RING
CTRL0
CTRL1
CTRL2
CTRL3
LINE_CTRL0
LINE_CTRL1
LINE_CTRL2
LINE_CTRL3
LINE_CTRL4
LINE_CTRL5
LINE_CTRL6
LINE_CTRL7
LINE_CTRL8
LINE_CTRL9
LINE_CTRL10
LINE_CTRL11
LINE_CTRL12
LINE_CTRL13
LINE_CTRL14
LINE_CTRL15
VCC
DGND
EARTH
CHAN_IO_1
LINE_CTRL[15..0]
MUX0
R_TIP0
R_RING0
T_TIP0
T_RING0
R_TIP1
R_RING1
T_TIP1
T_RING1
R_TIP2
R_RING2
T_TIP2
T_RING2
R_TIP3
R_RING3
T_TIP3
T_RING3
LIU_MUX
MCU_SPI[2..0]
IO1
FEC_[22..1]
XTRA_[5..0]
SPARE_[5..0]
FPGA_SPI[2..0]
CPU_TPU[15..4]
CPU_/IRQ2
RCV_LOBAND
RCV_LOB
NO
NC
COM
ALM_NO
ALM_NC
ALM_COM
JP18
CONN 4POS
MCU_LCA
And Then A Mir acl e Occur s ...
NOTE :
ALTERA EPF6K PART IS SPLIT INTO MULTIPLE HETEROGENOUS PIECES.
SIGNALS LEAVE MUX INTO LCA THEN EXIT TO MCU SECTION.
JP14
HEADER 8_156L
+24V
+5V
VCC
C40
220UF 50V
C47
220UF 50V
J21
XXX
PCB1
PCB_IOLINK4_MAIN
L7
2.2uH
L6
2.2uH
C44
10UF 6.3
C33
.01UF
C73
0.1uF
C46
10UF 6.3
C32
.01UF
C140
0.1uF
michael osman
IoWave Inc.
1010 Wisconsin Ave. NW Suite 215
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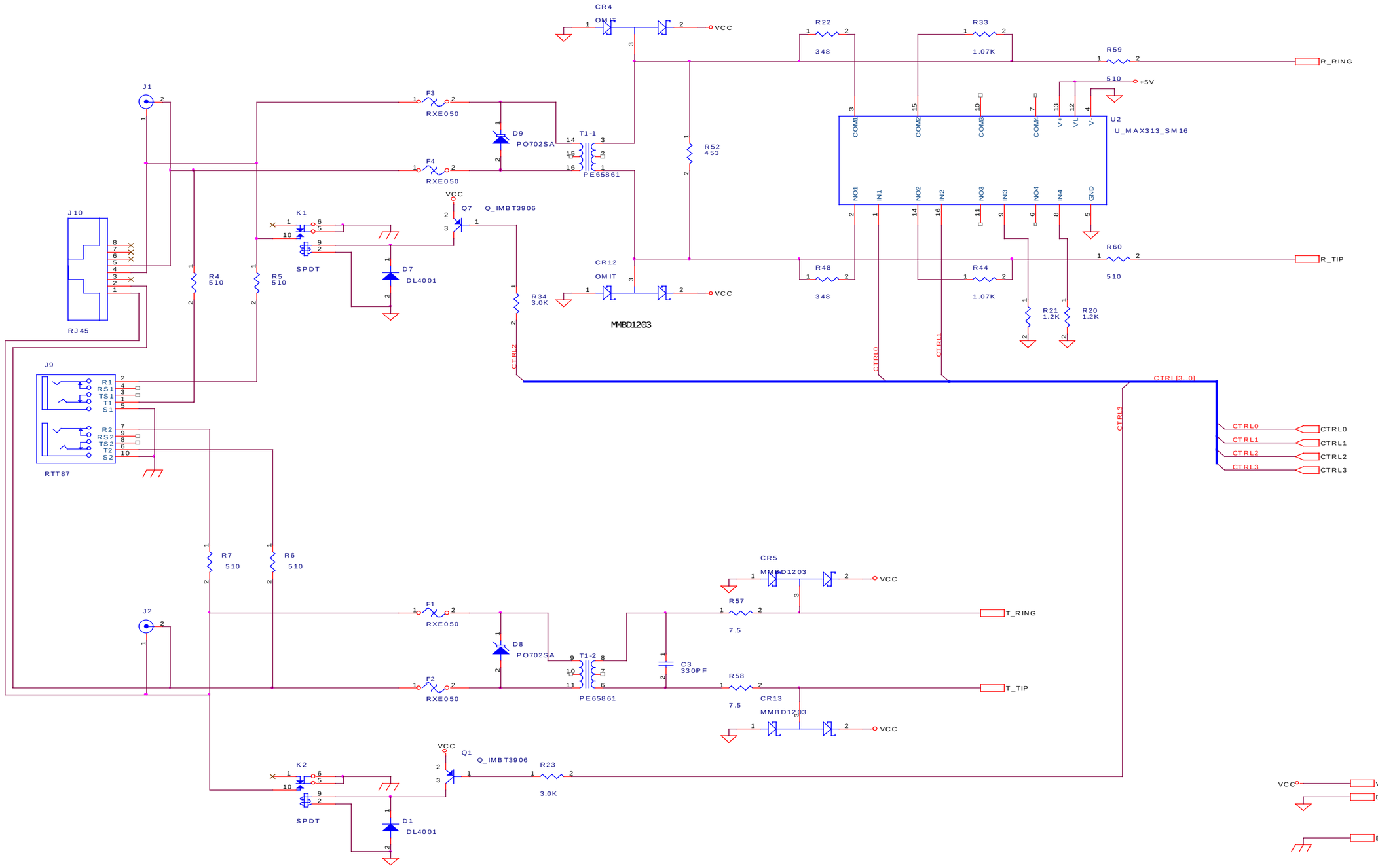
@1997
Title
IOLINK4_TOP BLOCK
Size C
Document Number IOLINK4
Rev B
Date: Monday, February 22, 1999
Sheet 1 of 19



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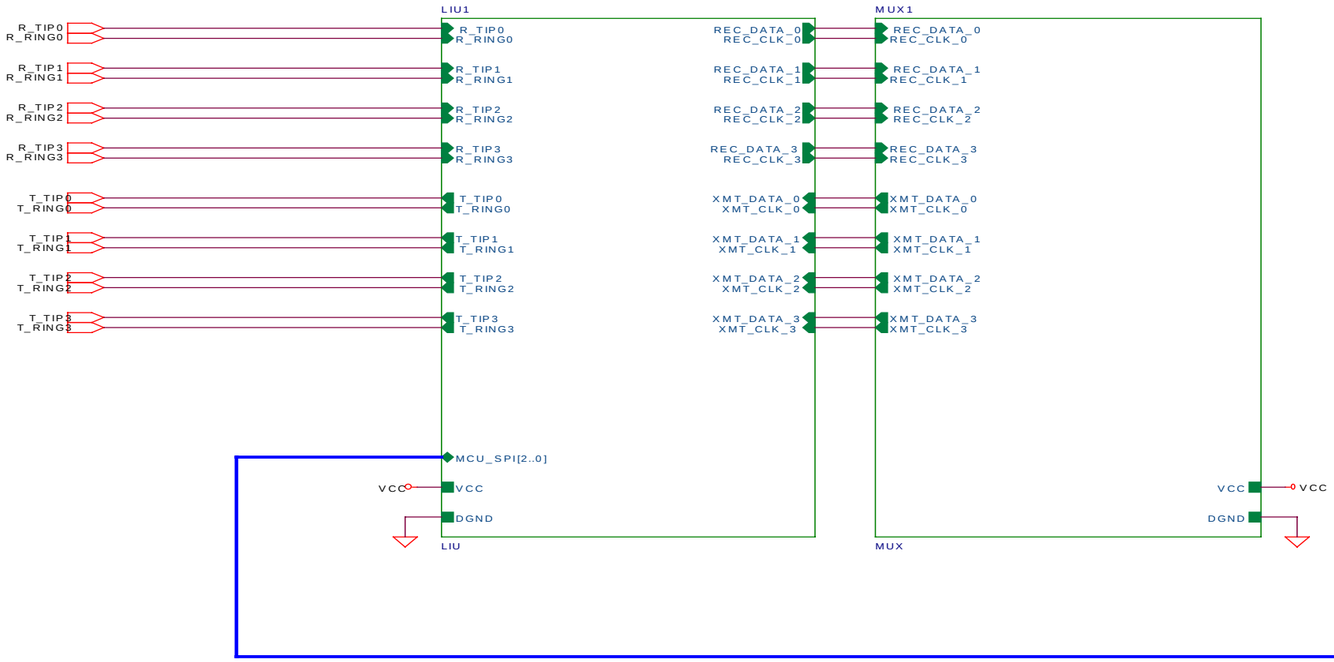
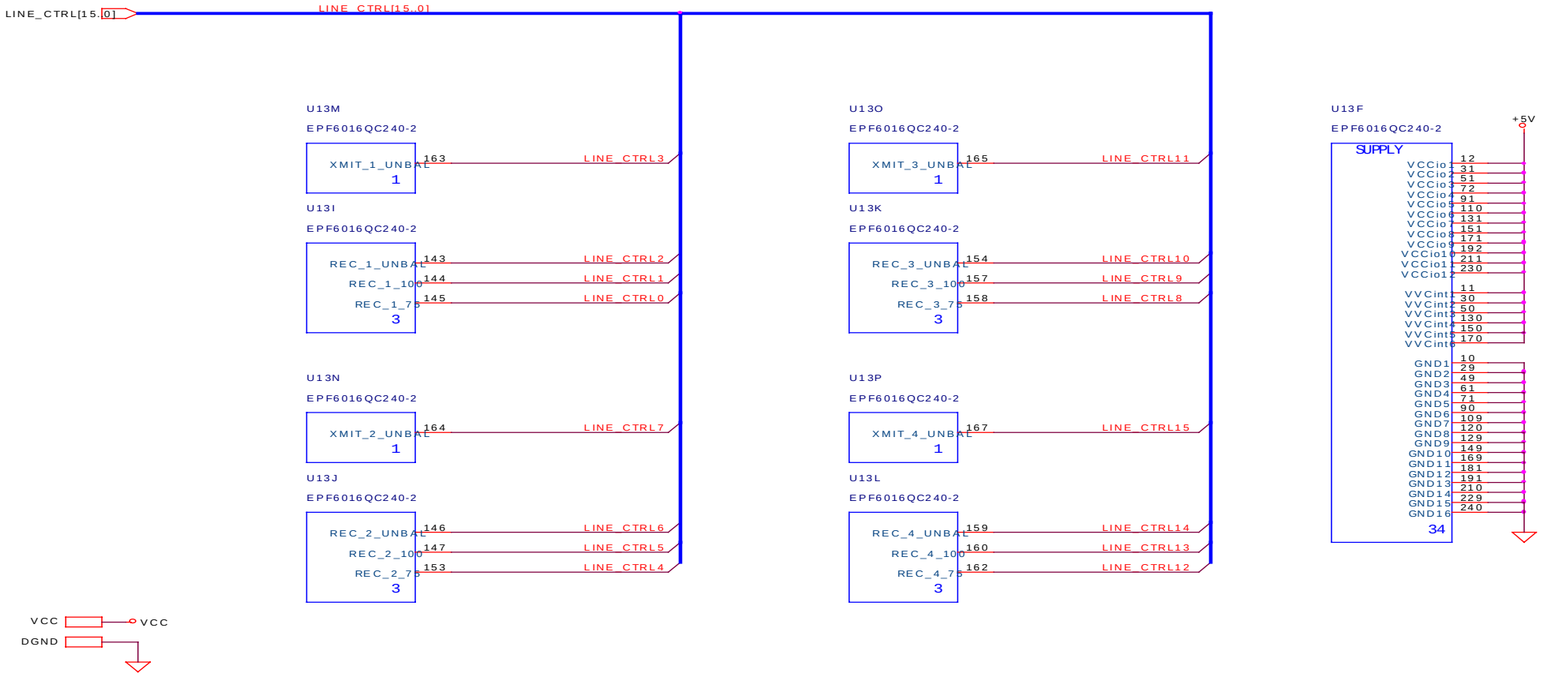
Title: CHANNEL_IO

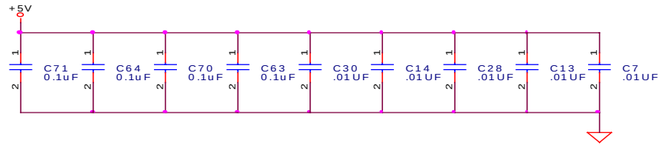
Size: C | Document Number: IOLINK4 | Rev: A



And Then A Miracle Occurs ...

NOTE :
ALTERA EPF6K PART IS SPLIT INTO MULTIPLE HETEROGENOUS PIECES.
SIGNALS LEAVE MUX INTO LCA THEN EXIT TO MCU SECTION.





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Title: LINE_INTERFACE AND MUX

Size C | Document Number IOLINK4 | Rev A

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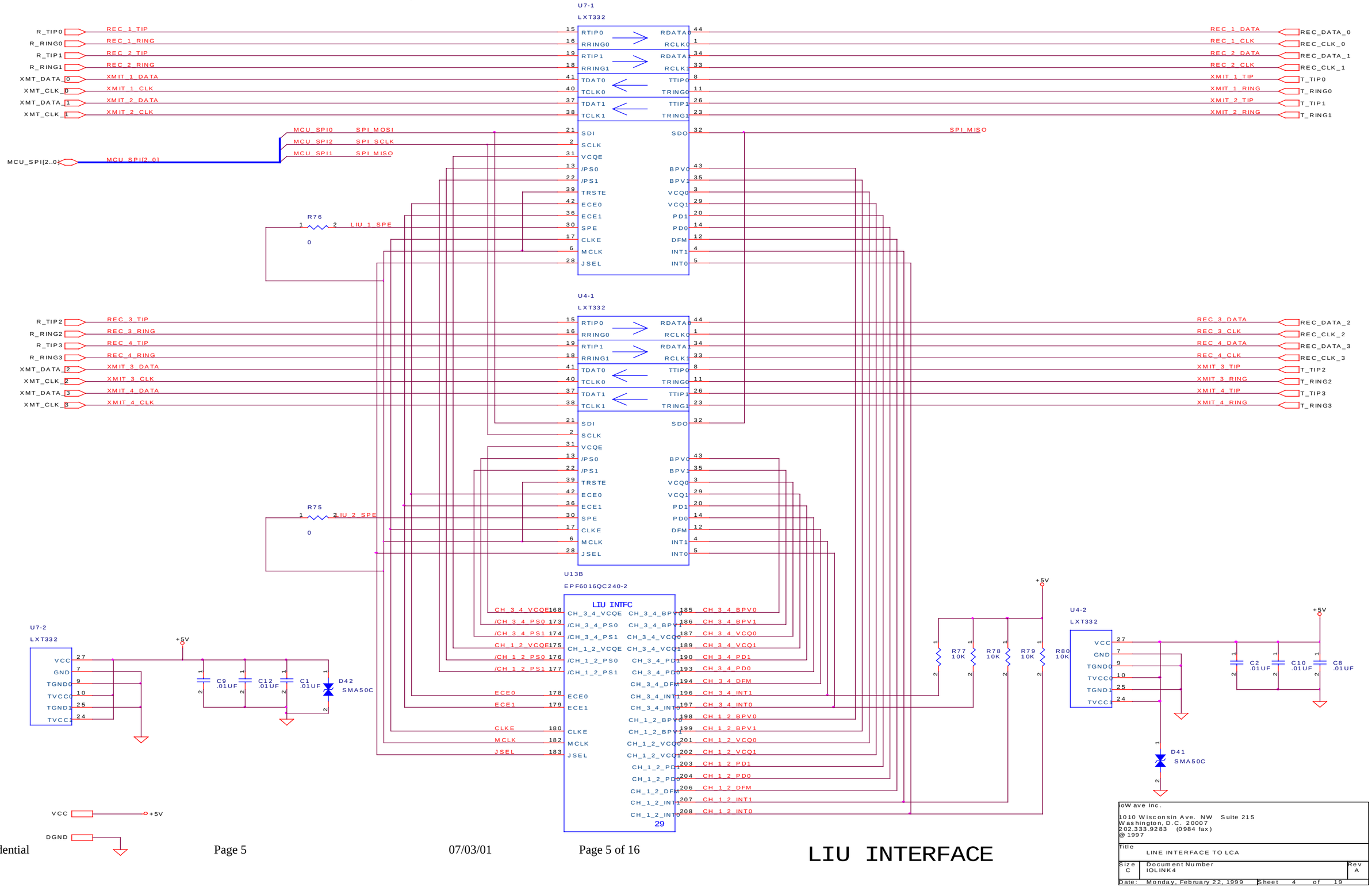

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Title: LINE INTERFACE TO LCA

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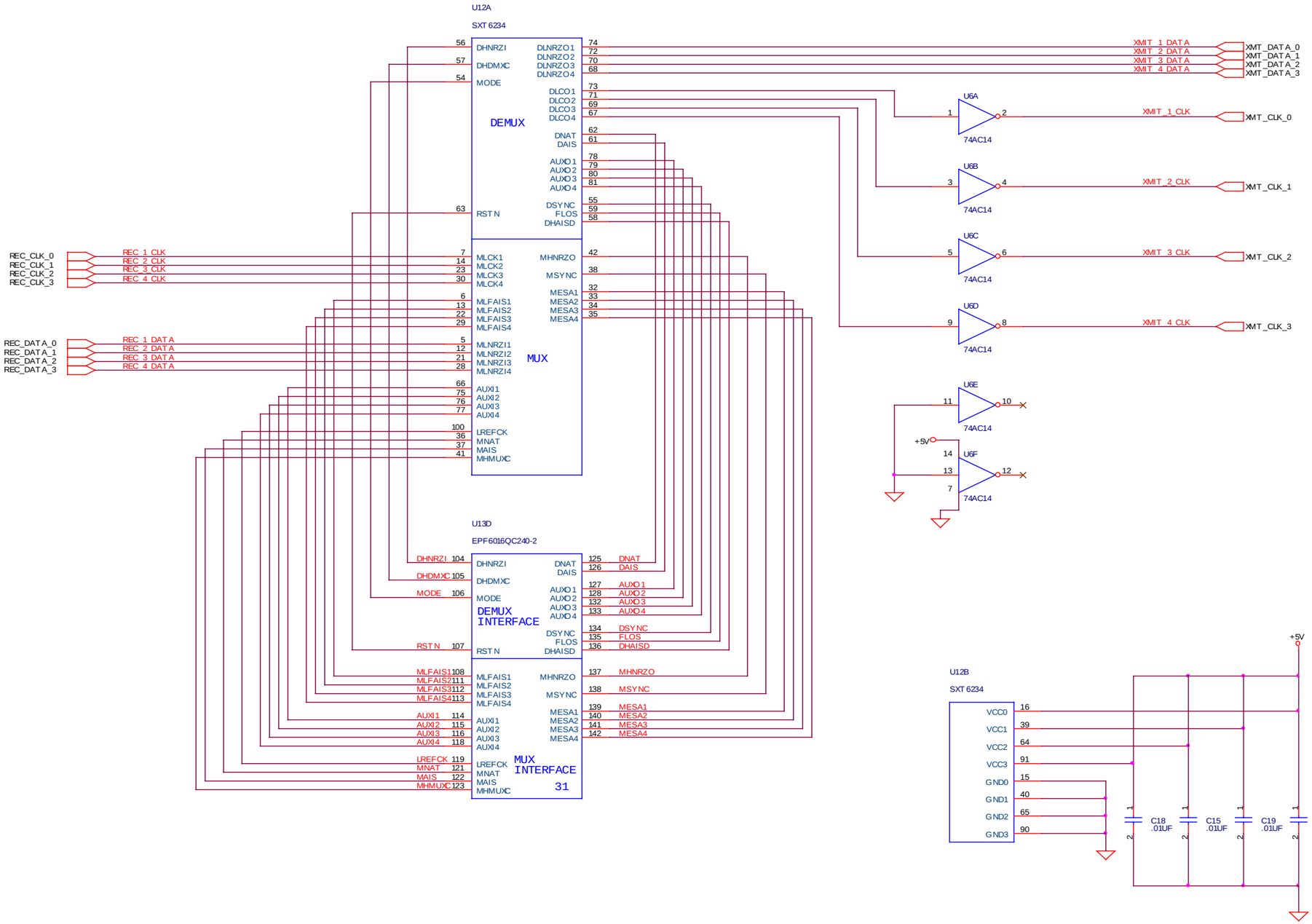
LIU INTERFACE



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Title: 4 TO 1 MULTIPLEXER

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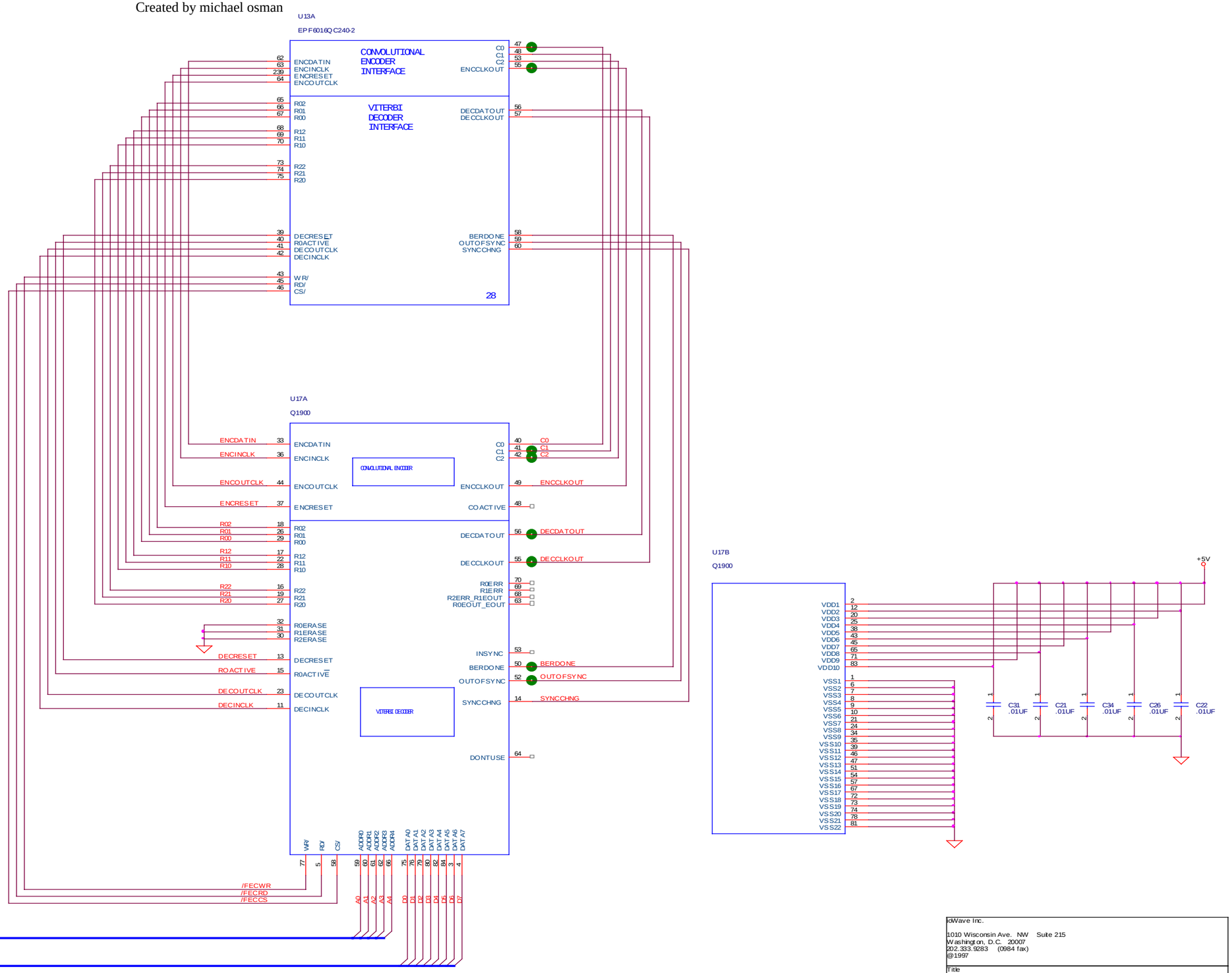

FEC INTERFACE

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Title: FEC INTERFACE

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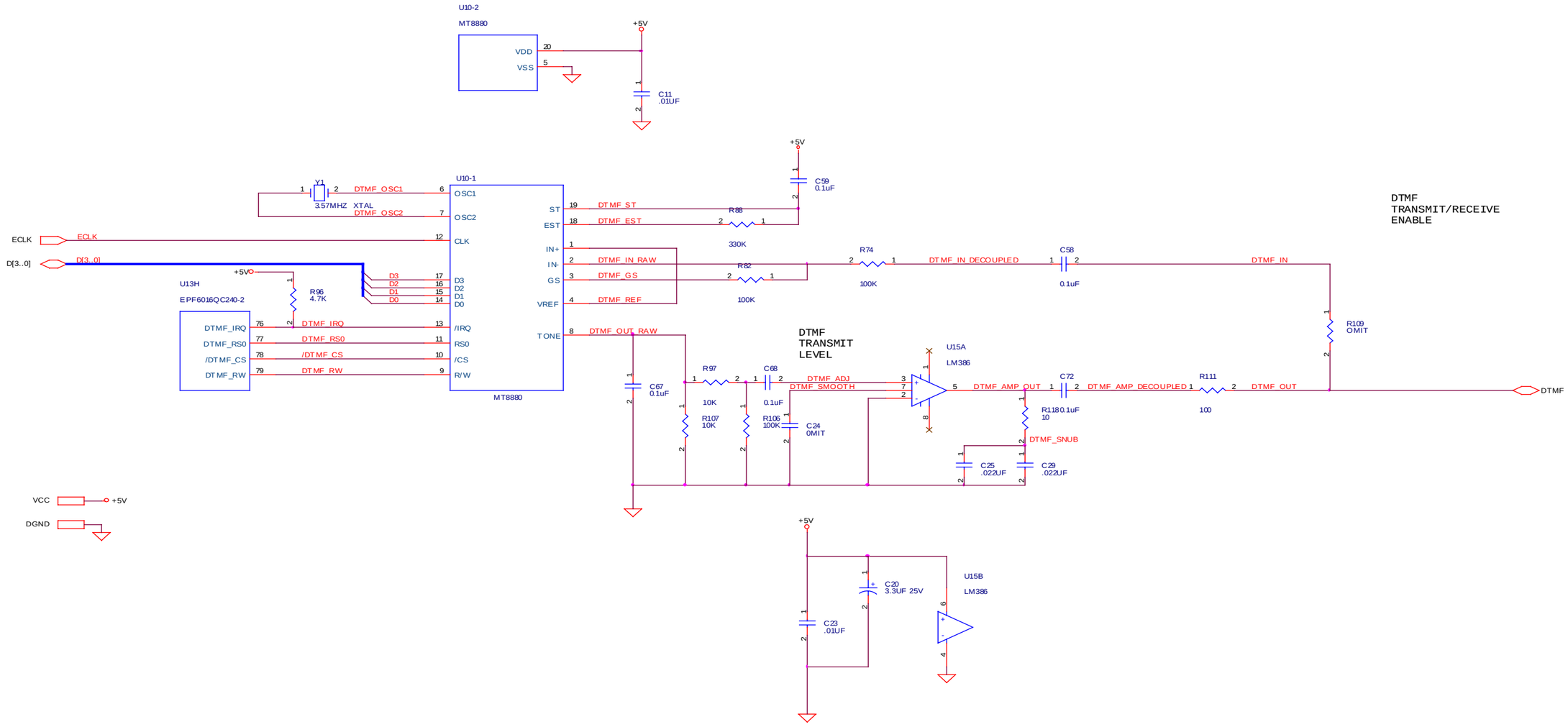

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Title DTMF INTERFACE		
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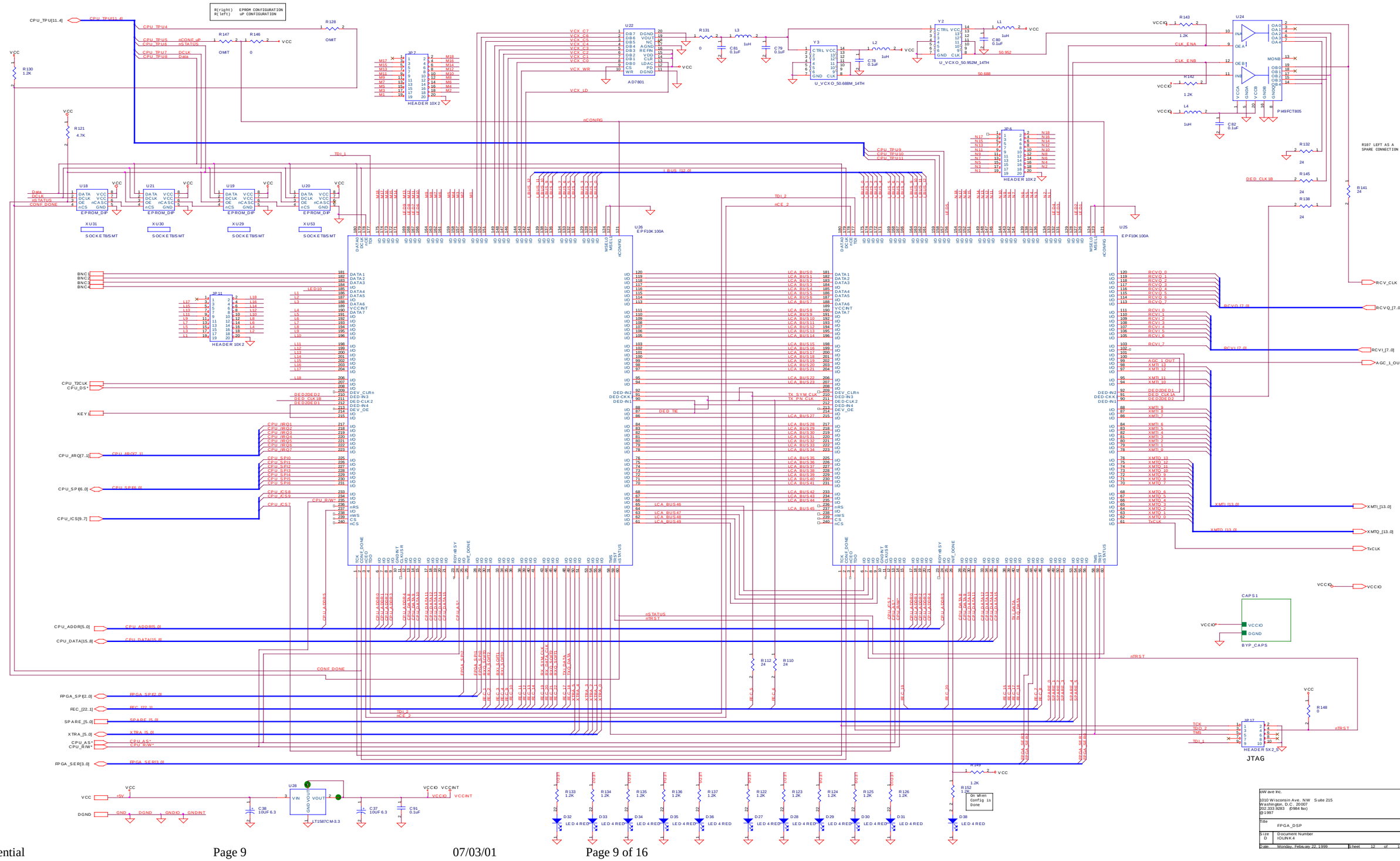
R(right) EPROM CONFIGURATION
R(left) uP CONFIGURATION
CPU_TPU[11..4]
CPU_TPU11..4
CPU_TPU4
CPU_TPU5
CPU_TPU6
CPU_TPU7
CPU_TPU8
nCONF_uP
nSTATUS
DCLK
Data
R128
OMIT
R147
R146
OMIT
0
VCC
R130
1.2K
R121
4.7K
U18
U21
U19
U20
EPROM_DIP
XU31
XU30
XU29
XU53
SOCKETBSMT
Data
DCLK
nSTATUS
CONF_DONE
nCS
nCASC
OE
GND
VCC
U22
AD7801
VCX_C7
VCX_C6
VCX_C5
VCX_C4
VCX_C3
VCX_C2
VCX_C1
VCX_C0
VCX_WR
VCX_LD
R131
L3
C79
0.1uF
C81
0.1uF
C78
0.1uF
L2
Y3
U_VCXO_50.688M_14TH
Y2
U_VCXO_50.952M_14TH
L1
C80
0.1uF
50.952
50.688
JP7
HEADER 10X2
JP6
HEADER 10X2
JP11
HEADER 10X2
nCONFIG
TDI_1
TDI_2
nCE_2
LBUS_12..0
U26
U25
EP F10K 100A
DATA0
DCLK
nCE
nCS
MSEL0
MSEL1
nCONFIG
nSTATUS
CONF_DONE
INIT_DONE
TCK
TDO
TMS
TRST
BNC1
BNC2
BNC3
BNC4
LED10
TCK_2
CPU_TCLK
CPU_DS*
KEY 1
CPU_IRQ[7..1]
CPU_SPI[6..0]
CPU_/CS[9..7]
CPU_R/W*
CPU_ADDR[5..0]
CPU_DATA[15..8]
FPGA_SPI[2..0]
FEC_[22..1]
SPARE_[5..0]
XTRA_[5..0]
CPU_AS*
FPGA_SER[3..0]
LCA_BUS0
LCA_BUS1
LCA_BUS2
LCA_BUS3
LCA_BUS4
LCA_BUS5
LCA_BUS6
LCA_BUS7
LCA_BUS8
LCA_BUS9
LCA_BUS10
LCA_BUS11
LCA_BUS12
LCA_BUS13
LCA_BUS14
LCA_BUS15
LCA_BUS16
LCA_BUS17
LCA_BUS18
LCA_BUS19
LCA_BUS20
LCA_BUS21
LCA_BUS22
LCA_BUS23
LCA_BUS27
LCA_BUS28
LCA_BUS29
LCA_BUS30
LCA_BUS31
LCA_BUS32
LCA_BUS33
LCA_BUS34
LCA_BUS35
LCA_BUS36
LCA_BUS37
LCA_BUS38
LCA_BUS39
LCA_BUS40
LCA_BUS41
LCA_BUS42
LCA_BUS43
LCA_BUS44
LCA_BUS45
LCA_BUS46
LCA_BUS47
LCA_BUS48
LCA_BUS49
TX_SYM_CLK
TX_PN_CLK
DED_TIE
DED-IN2
DED-CKK
DED-IN1
DED-CLK2
DED-IN4
DEV_OE
DEV_CLRn
DED-IN3
DED2DED2
DED_CLK1B
DED2DED1
CPU_/IRQ1
CPU_/IRQ2
CPU_/IRQ3
CPU_/IRQ4
CPU_/IRQ5
CPU_/IRQ6
CPU_/IRQ7
CPU_SPI0
CPU_SPI1
CPU_SPI2
CPU_SPI3
CPU_SPI4
CPU_SPI5
CPU_SPI6
CPU_/CS8
CPU_/CS9
CPU_/CS7
CPU_ADDR0
CPU_ADDR1
CPU_ADDR2
CPU_ADDR3
CPU_ADDR4
CPU_ADDR5
CPU_DATA8
CPU_DATA9
CPU_DATA10
CPU_DATA11
CPU_DATA12
CPU_DATA13
CPU_DATA14
CPU_DATA15
FPGA_SPI0
FPGA_SPI1
FPGA_SPI2
RX1_SOF0
RX1_SOF1
RX1_SOF2
RX1_SOF3
RX_SYM_CLK
RX_PN_DATA
RX1_SOF
TX1_DATA
TX1_SOF
FEC_1
FEC_2
FEC_3
FEC_4
FEC_11
FEC_12
FEC_13
FEC_14
FEC_17
FEC_18
FEC_19
FEC_20
FEC_5
FEC_6
FEC_15
FEC_16
FEC_7
FEC_8
XTRA_0
XTRA_1
XTRA_2
XTRA_3
XTRA_4
XTRA_5
SPARE_0
SPARE_1
SPARE_2
SPARE_3
SPARE_4
SPARE_5
VCCA_SEL0
VCCA_SEL1
VCCB_SEL0
VCCB_SEL1
R112
R110
24
R149
1.2K
VCC
On when Config is Done
D38
LED 4 RED
R133
R134
R135
R136
R137
R122
R123
R124
R125
R126
1.2K
D32
D33
D34
D35
D36
D27
D28
D29
D30
D31
U28
LT1587CM-3.3
VIN
VOUT
GND/VOUT
C38
10UF 6.3
C37
10UF 6.3
C91
0.1uF
VCCIO
VCCINT
+5V
GND
DGND
GNDIO
GNDINT
R143
1.2K
CLK_ENA
CLK_ENB
R142
1.2K
L4
1uH
C82
0.1uF
U24
P H9FCT805
INA
OEA
INB
OEB
OA0
OA1
OA2
OA3
OA4
OB0
OB1
OB2
OB3
OB4
MONB
VCCA
GNDA
VCCB
GNDB
R132
24
R145
24
R138
24
DED_CLK1B
R107 LEFT AS A SPARE CONNECTION
R141
24
RCV_CLK
RCVQ_[7..0]
RCVI_[7..0]
AGC_1_OUT
XMTI_[13..0]
XMTQ_[13..0]
TxCLK
VCCIO
CAPS1
BYP_CAPS
nTRST
R148
0
JP17
HEADER 5X2_S
JTAG
TCK
TDO_2
TMS
TDI_1
iOW ave inc.
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@1997
Title
FPGA_DSP
Size D
Document Number
iOLINK4
Rev A
Date: Monday, Febuary 22, 1999
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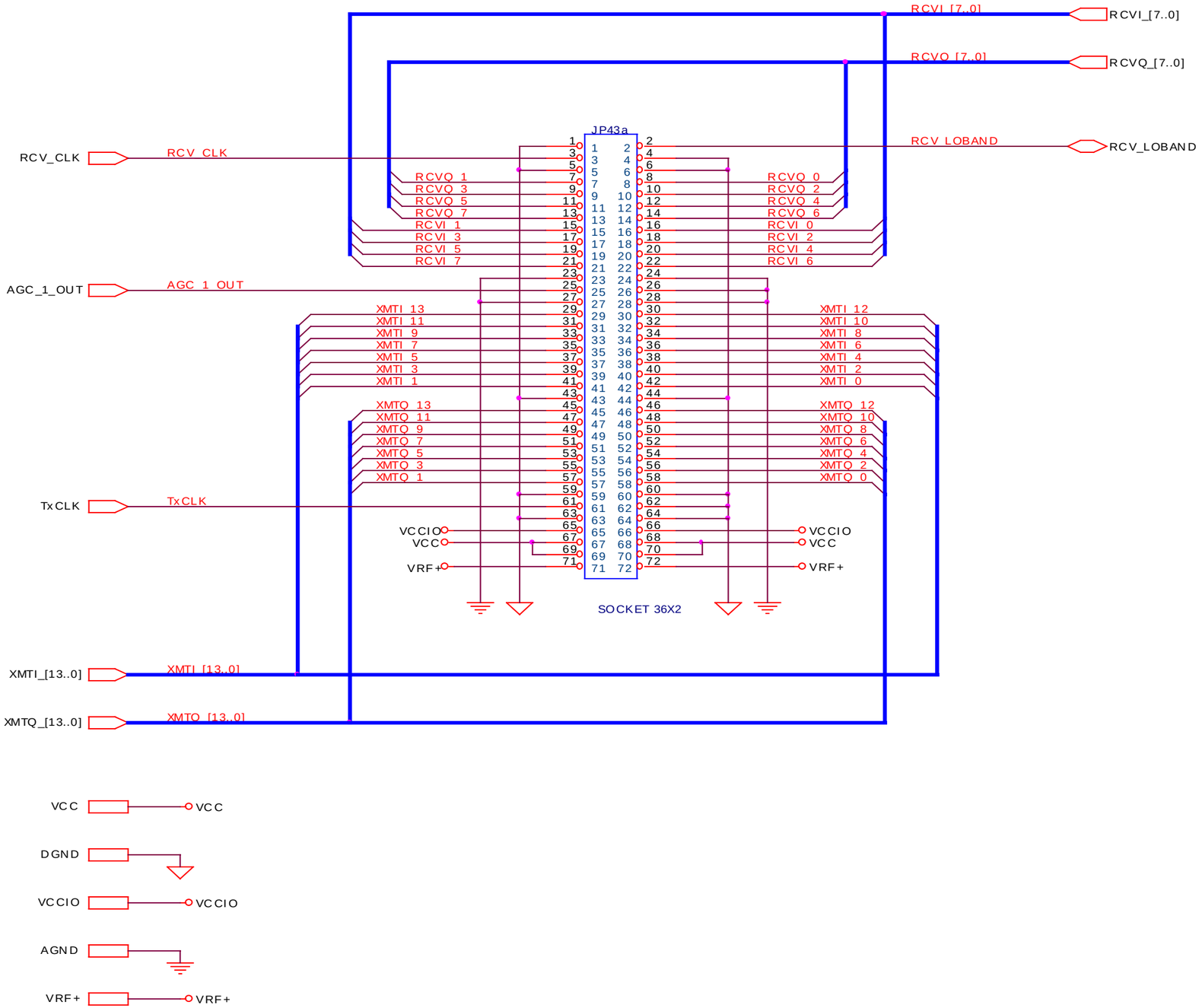

IoWave Inc.	
1010 Wisconsin Ave. NW Suite 215 Washington, D.C. 20007 202.333.9283 (0984 fax) @1997	
Title	IF_CONNECTOR
Size B	Document Number IOLINK4 — Rev A
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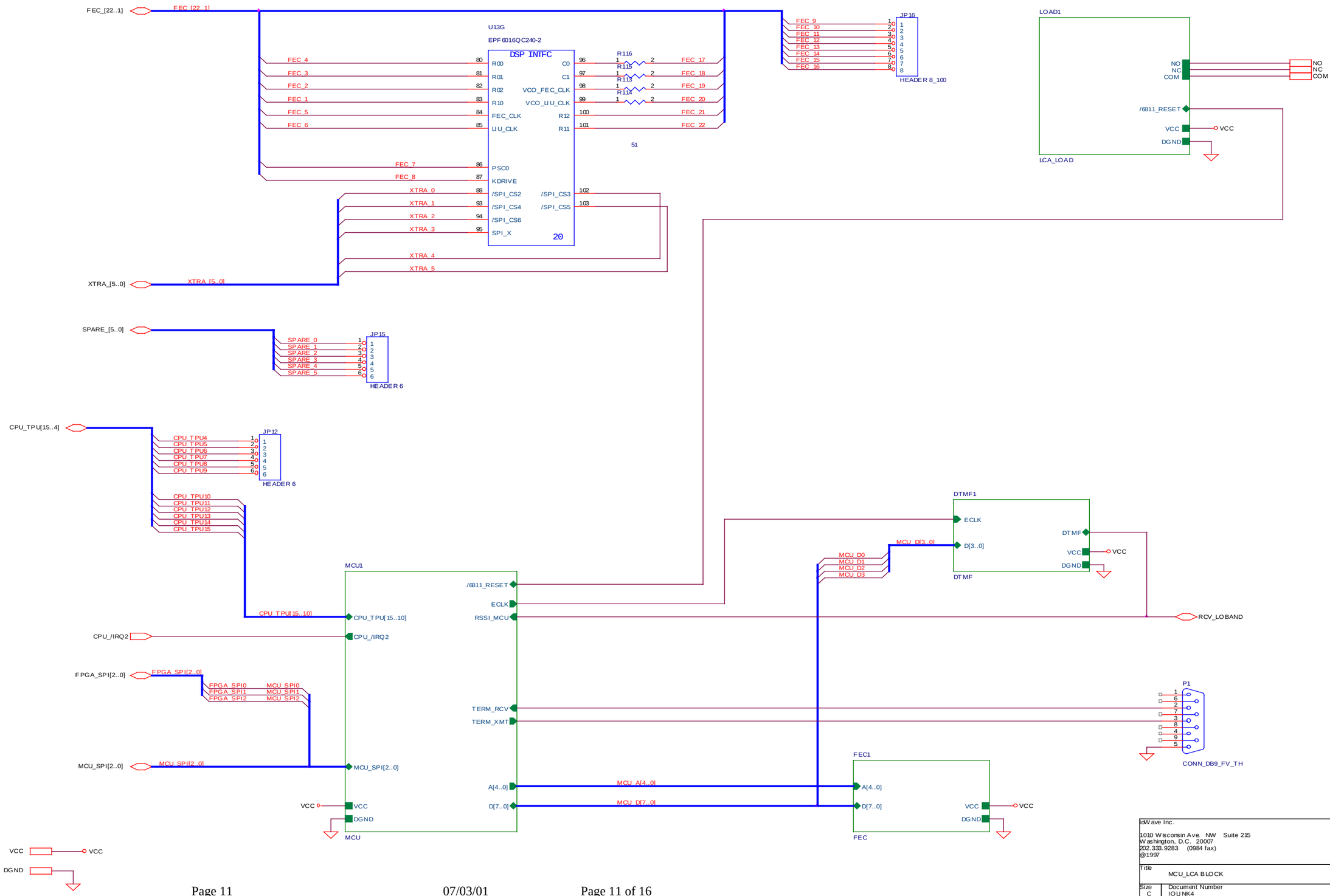

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Washington, D.C. 20007
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@1997

Title: MCU_LCA BLOCK

Size: C | Document Number: IOUNK4 | Rev: A

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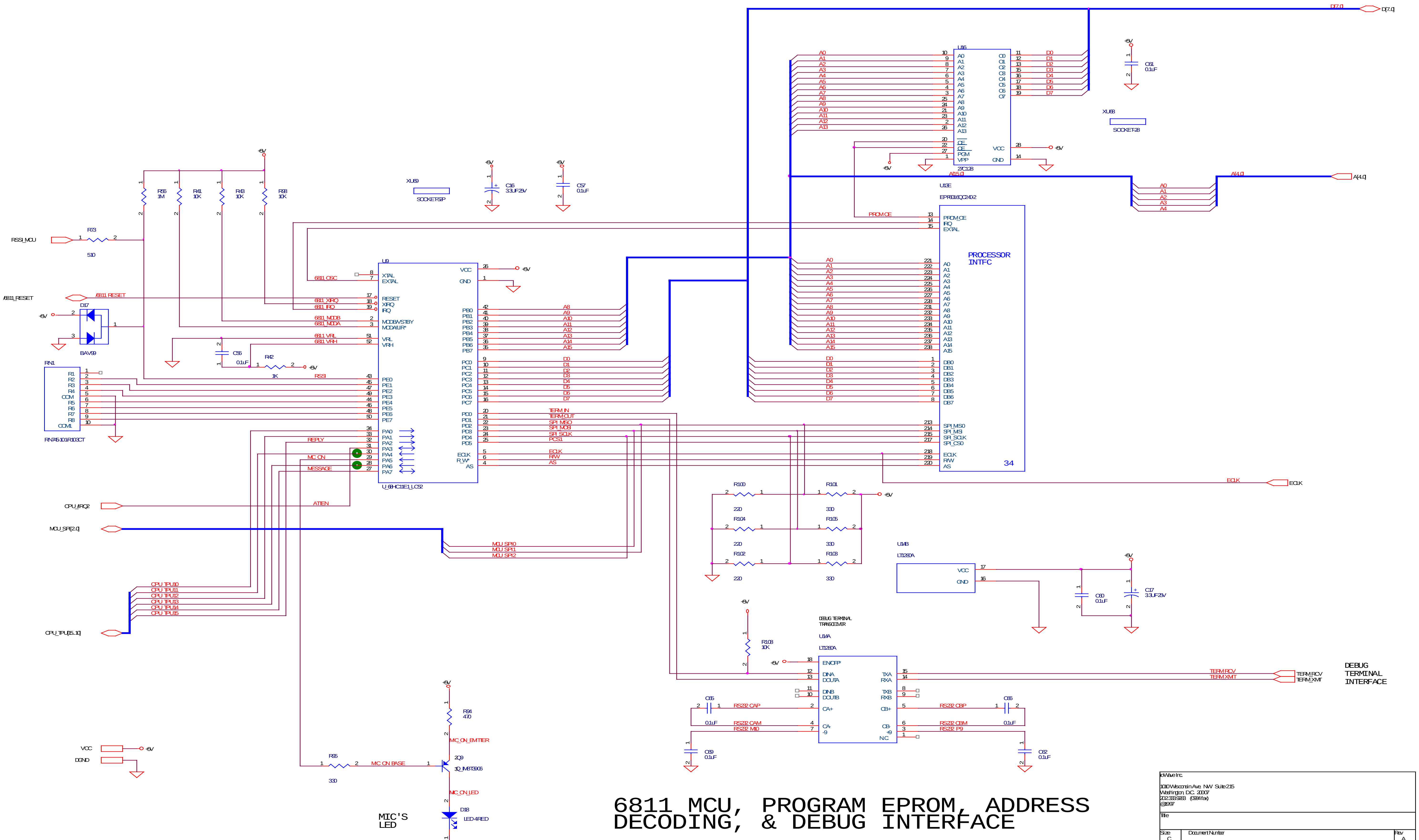
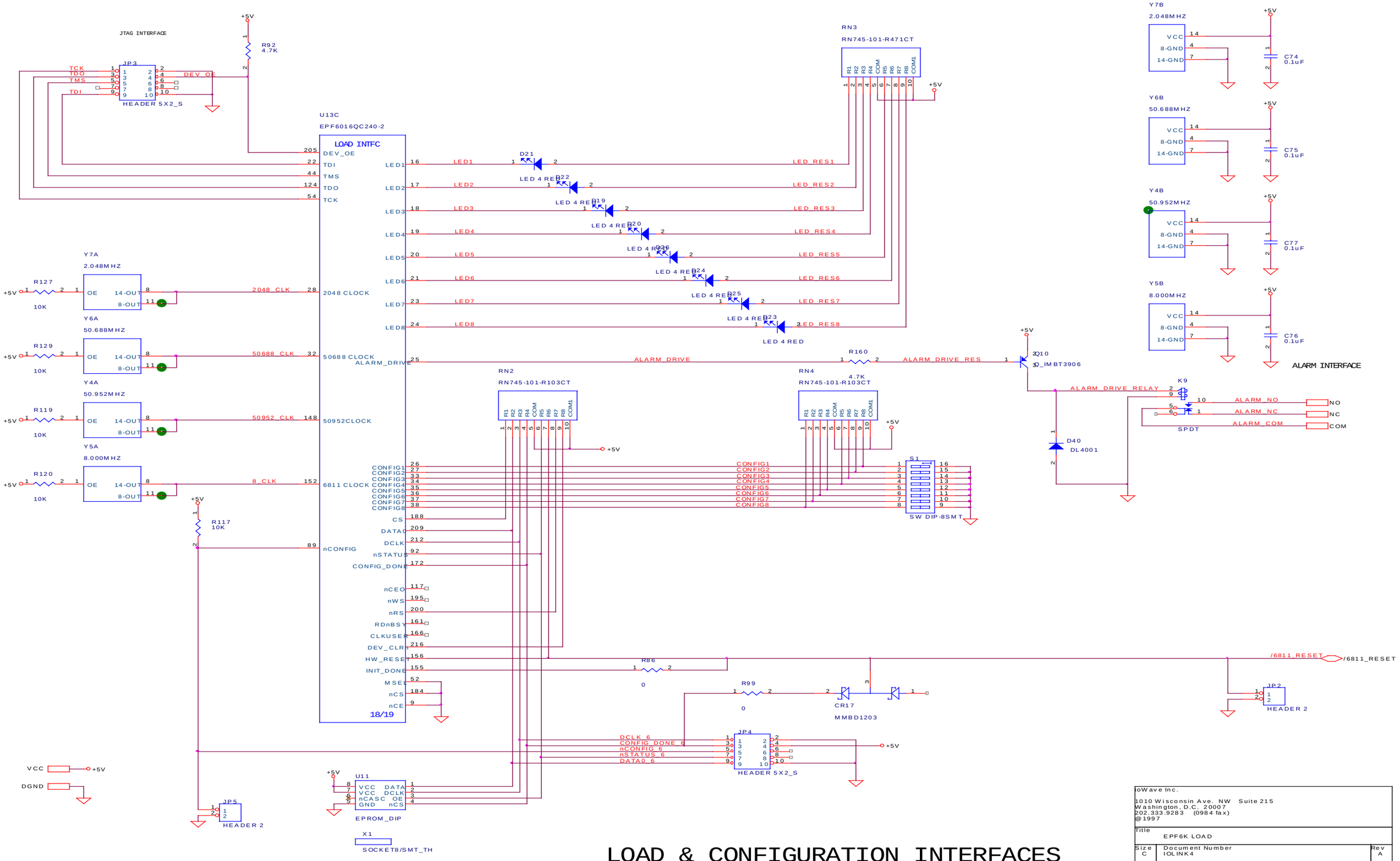

6811 MCU, PROGRAM EPROM, ADDRESS DECODING, & DEBUG INTERFACE
PROCESSOR INTFC
DEBUG TERMINAL INTERFACE
MIC'S LED
IoWave Inc.

LOAD & CONFIGURATION INTERFACES



IoWave Inc.	
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Title	EPF6K LOAD
Size C	Document Number IOLINK4 — Rev A
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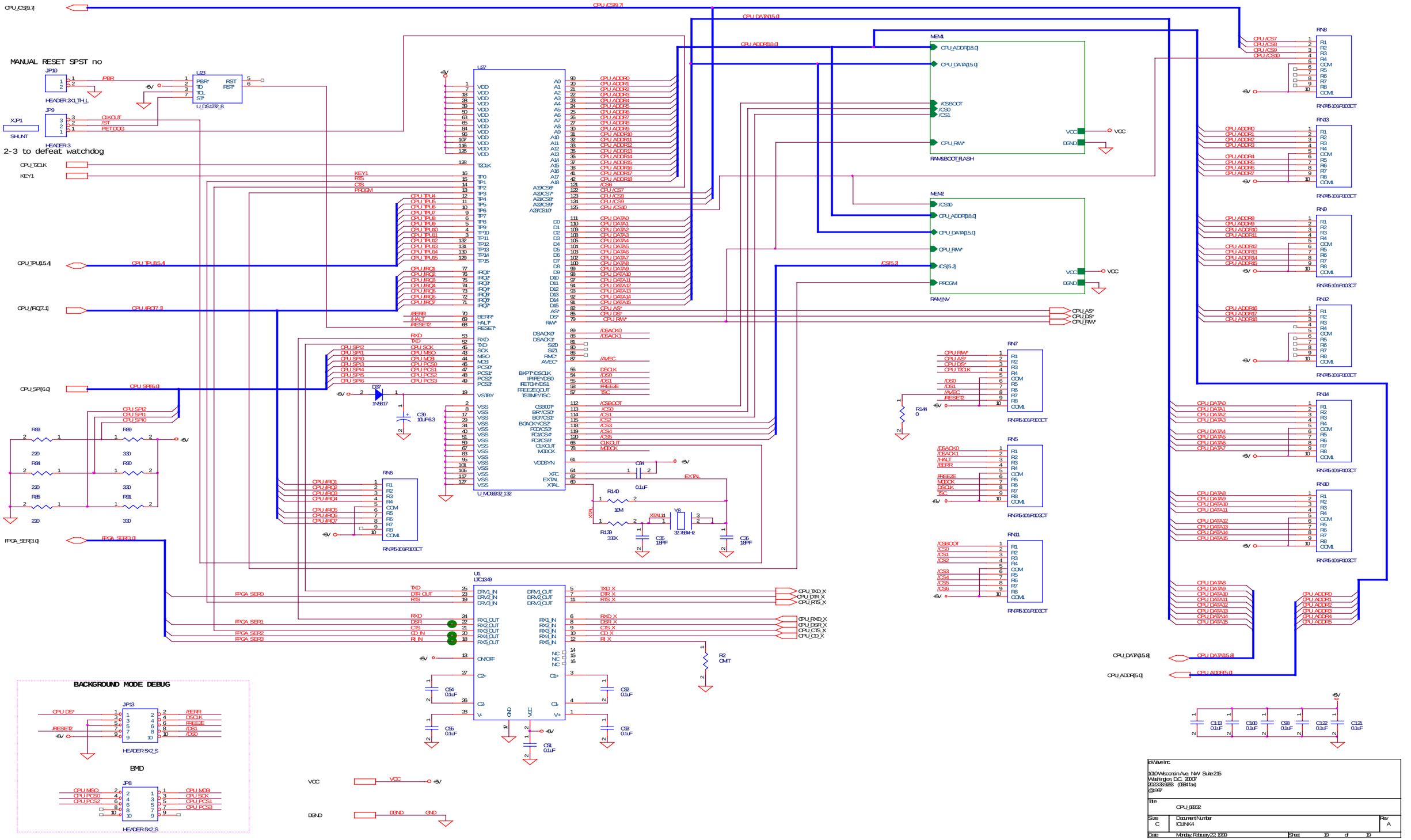
MANUAL RESET SPST no
2-3 to defeat watchdog
HEADER 2X1_THL
HEADER 3
SHUNT
U_DS1232_8
U_MC68332_132
U_LTC1349
RAM&BOOT_FLASH
RAM_NV
RNA7510 1R103CT
HEADER 5X2_S
BACKGROUND MODE DEBUG
BMD
VCC
DGND
ioWave Inc.
1010 Wisconsin Ave. NW Suite 215
Washington, DC 20007
2023338588 (0384fax)
@1997
CPU_6832
Document Number
IOLINK4
Rev
A
Monday, February 22, 1999
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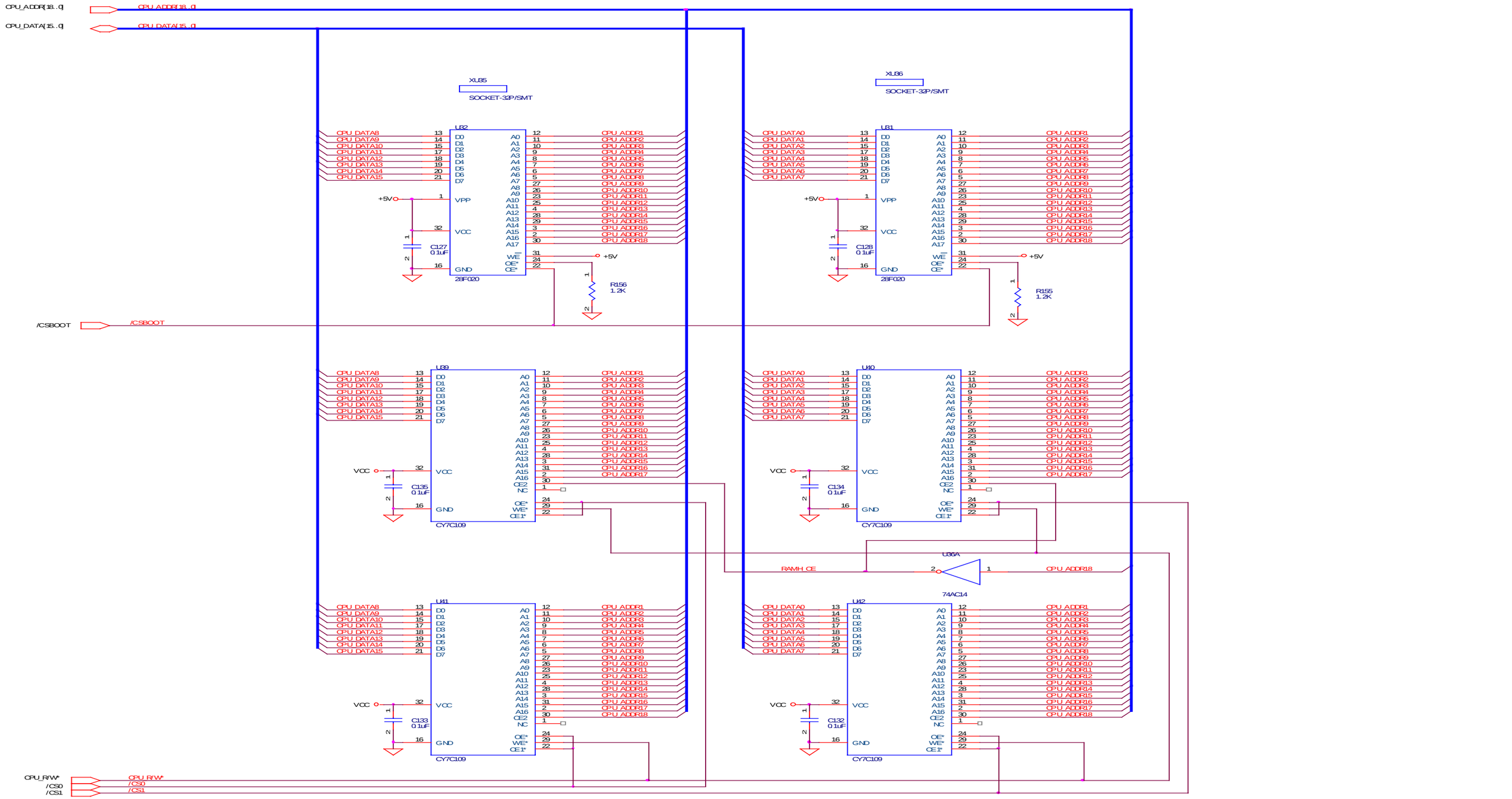

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1010 Wisconsin Ave, NW Suite 215 Washington, D.C. 20007 202.333.9283 (0984 fax) @1997	
Title	CPU_MEM_SYSTEM
Size C	Document Number IOLINK4 — Rev A
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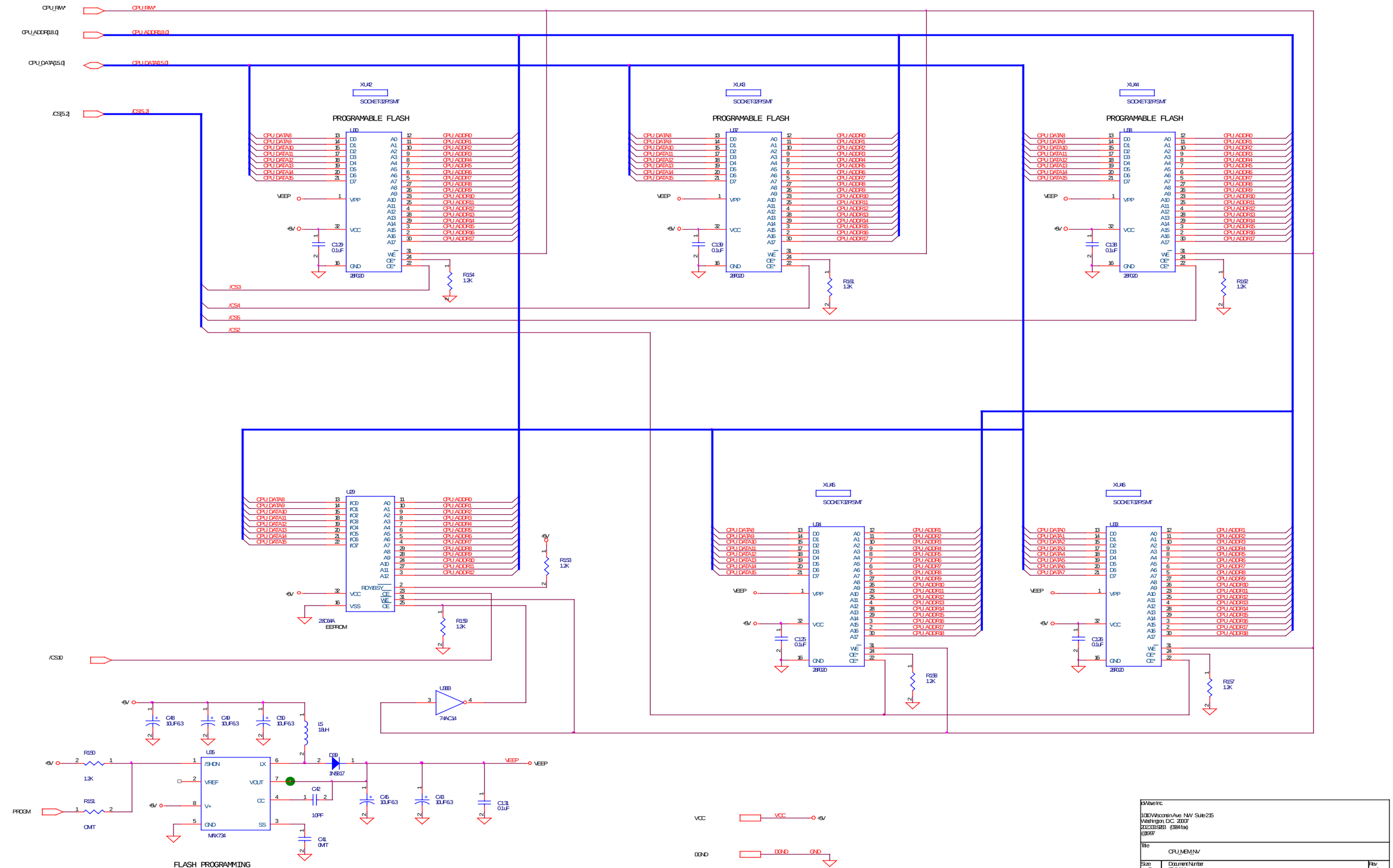
CPU_RW*
CPU_ADDR[18:0]
CPU_DATA[15:0]
/CS[5:2]
XU42
SOCKET32RSMT
PROGRAMABLE FLASH
U80
28F020
XU43
U87
XU44
U88
/CS3
/CS4
/CS5
/CS2
U89
28C64A
EEPROM
/CS10
XU45
U84
XU46
U83
U88B
74AC14
U85
MAX734
FLASH PROGRAMMING
PROGM
VCC
DGND
IoWave Inc
1010 Wisconsin Ave. NW Suite 215
Washington, DC 20007
2023339283 (1984fax)
@ibm
Title
CPU_MEM.NV
Size C
Document Number
IOLINK4
Rev A
Date: Monday, February 22, 1999
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