BB2400 Functional Description

Overview

The BB2400 system consists of a single ISA format PC card and an external antenna/transceiver unit used in a x86 based personal computer and configured as a wireless router. The PC is configured with a version of the Linux operating system combined with a special driver to exercise this system.

To setup a wireless route, two identical sets of hardware are required. By software selection in the PC, one unit becomes a "master" and the second unit becomes a "slave". Communication is established via a wireless Spread Spectrum link in the 2.4GHz ISM band. The master can address more than one slave but in all cases; transmission is only permitted from the slave to the master after the master authorizes the transmission. A slave only listens and talks to a master, but all slaves can listen to a single master simultaneously. In effect, with more than one slave, a master can control a point to multi-point network.

The transmission format is Time Division Duplex (TDD) utilizing a single frequency for communication among all units.

Central to the design, is the use of the Harris HFA3860 Baseband controller and HFA3724 modulator/demodulator, which generates and decodes the spread spectrum signal in a format suitable to meet the requirements of the Spread Spectrum requirements of FCC part 15.247.

System Configuration

As mentioned, the system consists of an ISA card (ISA2400) installed in a standard x86 PC. The PC is also equipped with a standard video adapter and a standard Network Interface Card (NIC) and keyboard. The hardware is the same regardless of the unit's roll as master or slave, only the software switches are different.

The ISA card allows the Linux operating system to send and receive packets much the same as any NIC card would. The card along with its associated driver, emulates the function of a NIC, and converts the serial data stream to byte-wide format and places the data in memory or grabs data from memory depending on the transmit or receive state. The custom driver adds header and trailer information to a standard IP packet and is the interface to the ISA card. This additional information is the destination MAC address of the actual ISA2400 card. The operating system then needs to function only as a router and sends the packet out the NIC if a route is defined for the destination IP address.

Once the data is formatted, the Harris components modulate a signal to yield an IF signal of 280MHz. This signal is sent by coaxial cable to a remote transceiver unit that performs the final frequency translation to/from the 2.4GHz ISM band. An additional cable carries transmit / receive command information as well as synthesizer serial programming commands for the 1st Local Oscillator located in the transceiver.

The remote transceiver is an outdoor unit that includes an integrated 16dBi-gain antenna and special connectors to prevent using the system in an unintentional manner. The gain distribution of the transceiver/antenna combination is such that regardless of cable length, the maximum output power of +36dBm allowed by part 15.247 can never be exceeded.

Detail Description ISA Component of Bitbeam 2400

A block Diagram and circuits schematics are included to understand the operation of the ISA component of this system. This diagram depicts all essential elements of the card and can be described as follows:

ISA Bus Interface This is the circuitry that buffers and decodes the various I/O and memory control signals found on the standard ISA PC Bus. The card occupies 32 I/O locations and 16K memory locations. The decoding of the proper address and subsequent signal routing is performed in this logic. All of the decode logic is compiled into an Field Programmable Gate Array (FPGA).

ISA Address Mapper and Dual Port Memory Controller This circuitry extends the bus interface to allow data to be written into dual port memory asynchronous to the Harris DSP. All of the memory controller logic is compiled into the same FPGA.

Dual Port Memory This memory contains the image of data to be transmitted by the Harris DSP or received from the Harris DSP. This is basically a buffer area that allows the PC to construct or decode a data packet in the background, since the PC cannot guarantee timing. The Harris DSP requires an uninterrupted serial stream of data so this buffer area is used as input or output to a serial framer directly controlled by the DSP. The serial framer is also in the FPGA.

Intel 80C196 Micro Controller The Harris DSP must be programmed via a 3 wire serial bus. Values such as header information, data length and type must be programmed on a near real time basis. Also additional housekeeping values need to be programmed at startup. To accomplish this, an 80C198 embedded controller is used alone, to communicate with the Harris DSP. This allows real time updates not possible with the PC's processor. Communication between the embedded processor and the PC processor is via I/O mapped registers in the FPGA. Firmware for the 80C196 is contained in a 27C256 EPROM.

HFA3860A DSP Central to the system design is the use of the Harris Spread Spectrum Direct Sequence Baseband Processor. This part was selected because the modulated data spectrum meets the requirements of FCC 15.247 and is currently used in many other approved designs. The Harris data sheet is included for completeness. This part essentially takes serial data and attaches various header bytes and to form a Direct Sequence spread signal. Likewise, it provides chip and bit sync to recover received data.

HFA3724 Modulator/Demodulator This chip takes the baseband data generated by the DSP of provides baseband data to the DSP. It consists of an I/Q Modulator/Demodulator that when used with an external frequency source, upconverts of downconverts the Direct Sequence signal to a VHF IF frequency, in this case 280MHz. The external local oscillator (LO) operates a 2 times the

IF or 560MHz. A divider is included in the HFA3724. The Harris data sheet is included for completeness.

560MHz Single Frequency PLL. This is the external signal source for the HFA3724. A single chip PLL synthesizer is programmed by the 80C196 embedded controller and uses the 44MHz reference TCXO also used by the Harris DSP. The PLL is programmed to provide a 560MHz signal to the Up/Down converter. The loop bandwidth is optimized for noise rejection, since the frequency is set at startup and settling time is unimportant. As a failsafe, the frequency is reprogrammed periodically if no signal is received.

TDD IF Amplifier Since this system architecture sends and receives the IF signal along a coaxial cable to the outdoor unit, a bi-directional amplifier is required. Also since the system, by design, is half-duplex, a TX control signal is used to change directions of the amplifier.

Control Output As with the TDD IF amplifier, the outdoor unit is a transceiver as well. The same control signal that controls the TDD amp is also used to switch the outdoor unit to transmit. This unit also contains a PLL that must be programmed by the embedded controller. A differential driver is used to send the data from the card to the outdoor unit. This format is proprietary and uses special connectors so that the outdoor unit can only be used for its intended purpose and only with a companion ISA BB2400 card in a PC.

Detail Description Outdoor Component of Bitbeam 2400

A block Diagram and circuits schematics are included to understand the operation of the Transceiver / Antenna component of this system. This diagram depicts all essential elements of the card and can be described as follows:

Celertik RF to IF Converter This section consists of a GaAs MMICs that takes the 280MHz signal and in transmit mode upconverts to the 2.4GHz ISM band in conjunction with an external local oscillator. Likewise, it can be switched to receive mode in order to downconvert a signal. All switching, mixing, IF amplification and switching functions are contained in this chip.

Dielectric Filters The Up/Down converter image and spectral purity issues are addressed by incorporating high performance filters into the design. The high “Q” low loss nature of dielectric filters make them ideal for this application; that is to filter the desired ISM band signal, both in receive and transmit while all but eliminating the undesired image product. The RF/IF and final amplifier chip when used in conjunction with this filter do provide adequate spectral purity as well as selectivity.

TDD TX / RX Amp A final transmit amplifier is included to boost the transmit signal to a power level of+18dBm. A dielectric filter and a discrete lowpass filer are included at the output to suppress any harmonic energy or spurious products generated in the final amplifier stage. As mentioned before, the gain distribution is such that the maximum effective radiated power allowed by FCC 15.247 can never be exceeded even with 0dB IF cable loss. Also because of the integrated transceiver / antenna combination, very repeatable results are obtained and output power is not subject to variations because of varying cable losses at 2.4GHz.

PLL Synthesizer A single chip PLL synthesizer is programmed by the 80C196 embedded controller and uses a 16.384MHz TCXO as a reference. The PLL is programmed to provide a low side offset frequency to the Up/Down converter. The loop bandwidth again, is optimized for noise rejection, since the frequency is set at startup and settling time is unimportant. As a failsafe, the frequency is reprogrammed periodically if no signal is received.

Level Shifter and EMI Protection The differential control signals are converted to logic levels by the circuit. Since long cable runs between the PC and the outdoor unit can be expected, the antenna incorporate MOV protection against static discharge as well as RF filtering and shielded connectors to eliminate unintentional radiated signals.