APPENDIX 6

ALIGNMENT INSTRUCTIONS

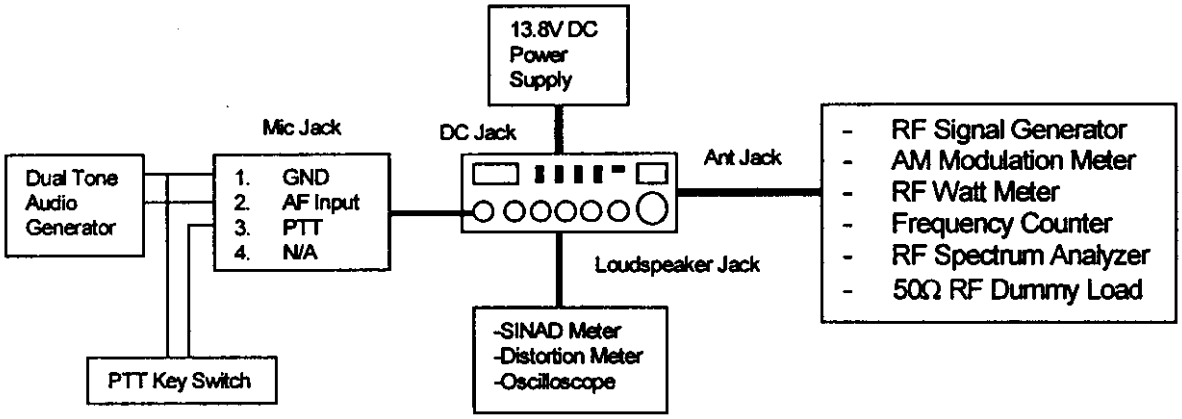
FIVE (5) PAGES OF ALIGNMENT INSTRUCTIONS FOLLOWS THIS SHEET

TRANSMITTER ALIGNMENT

Note: Unless otherwise specified, adjust Mic Gain control on the front panel to fully clockwise position for all following tests.

A. Test Set-Up

Set up test equipment with the NR-150 radio as indicated below:



B. SSB Balanced Modulator Adjustment

1. Set the mode selector to USB, and the channel select to CH 20.
2. Adjust Mic Gain control on the front panel to minimum (fully counterclockwise)
3. Press PTT to transmit on SSB without modulation
4. Adjust **VR7** for minimum RF output.
5. Check RF output on LSB is also minimum
6. Resume Mic Gain control to maximum setting (fully clockwise)

C. RF Power Transistor Bias Current Adjustment

1. Set the mode selector to USB, and the channel select to CH 20.
2. Remove the short link PCB (installed vertically in front of the RF Power transistors)
3. Connect 100mA FS DC current meter to **TP-9** [+] and **TP-8** [–].
4. Adjust **VR11** for 60mA ± 3mA to **TR44**.
5. Connect 200mA FS DC current meter to **TP-9** [+] and **TP-7** [–].
6. Adjust **VR10** to 100mA ± 5mA to **TR43**.
7. Install the short link PCB back to the holder of TP-7, TP-8 & TP-9 upon completion of adjustment.

D. AM RF Power Output Adjustment

1. Set mode selector to AM.
2. Select the channel selector to CH-20.

3. Press PTT to transmit.
4. Adjust VR-13 for 4W RF Power output. (Without modulation)

E. RF Power Amplifier Adjustment

IMPORTANT : VR-12 Bias adjustment, should not be rotated clockwise beyond 2 o'clock position, otherwise the RF transistor may be destroyed.

1. Set the Mode Selector to USB. Compandor OFF.
2. Apply 1KHz 50mV RMS audio signal to Microphone input connector pin 2.
3. Set the Channel Selector to CH-20.
4. Press PTT to transmit.
5. Adjust VR-12 and L-42 for Maximum RF power output as read on the RF Watt Meter.
6. Adjust L-40, L-43, L-44 and L-33 for max. RF power output.
7. Repeat step 4 to 5 until no further improvement is obtained.
8. Adjust L-42 for balanced RF Power output on CH40 & CH1.
9. Switch to AM Mode, disable audio signal generator, press PTT to transmit.
10. Adjust VR-13 for 4W RF Power output on AM Mode with no modulation.
11. Switch back to USB Mode, apply 50mV 1KHz audio, press PTT to transmit.
12. Switch VSWR meter to Peak Detection Mode.
13. Adjust VR-12 for max. 12W SSB Peak Power Output.

F AM Modulation Adjustment

1. Apply 1KHz 50mV rms. AF signal to Microphone input connector pin 2.
2. Activate PTT to transmit in AM Mode. Compandor OFF. Adjust VR-14 for 90% modulation.

G Compandor Functional Test - Transmitter

1. Apply 1KHz 2mV rms. AF signal to Microphone input connector pin 2.
2. Activate PTT to transmit in AM Mode. Compandor OFF.
3. Observe modulation level between 20-80%.
4. Switch Compandor to ON
5. Observe the modulation level increases to around 90%.
6. Increase signal generator level from 2mV to 100mV, Compandor ON.
7. Observe the modulation level remains to be less than 100%.

H. Advanced Test Procedures for Modulation

Following advanced test procedure requires optional/advanced test equipment setup by experienced technical person, and is not normally required in a field repair environment.

i) AM Modulation Monitor

- Apply 1KHz 50mV rms. AF signal to Microphone input connector pin 2 of the radio, and to the Y input (Usually marked as Timebase) of the oscilloscope.
- Monitor RF output waveform with X input (usually marked as CH1) of the oscilloscope.
- Activate PTT to transmit on AM Mode. Compandor OFF.
- Confirm the AM Modulation displayed in the oscilloscope is less than 100% as in Fig iA.

FIG iA - AM Modulation Monitor

Modulation Level = (a-b) x 100% ÷ (a+b)

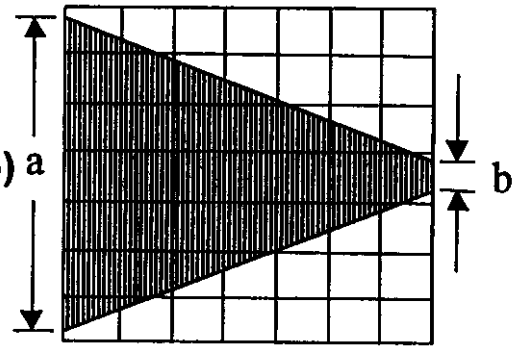


FIG iB - No Modulation

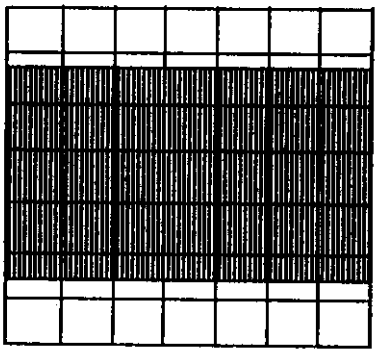


FIG iC - 100% Modulation

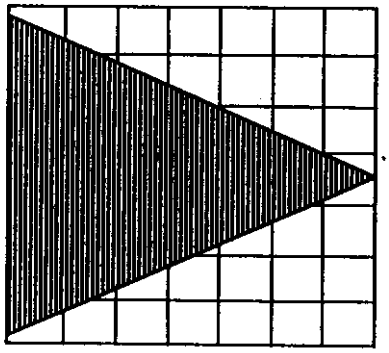
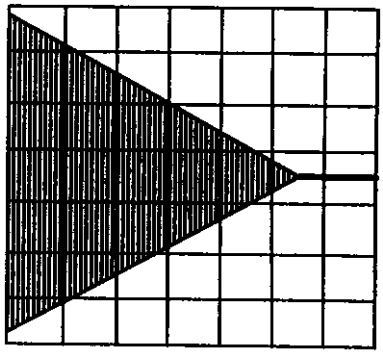


FIG iD - Over Modulation >100%



ii) SSB Modulation Monitor

- Use two AF signal generator connected in a star resistor network to provide a balanced 3 input/output ports with impedance of 600Ω. Compandor OFF.
- Apply 500Hz and 2.4KHz 30mV audio tones signals simultaneously through the resistor network to the Microphone input connector pin 2. Activate PTT to transmit on USB Mode.
- Adjust the output level of the 500Hz AF signal generator to obtain the proper waveform on the oscilloscope as shown in figure iiA. (See Fig C to D for waveforms of improperly set up radios)

Figure iiA PROPERLY ADJUSTED SSB TRANSMITTER

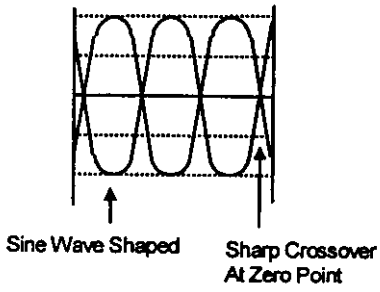


Figure iiB UNBALANCED INPUT TONES

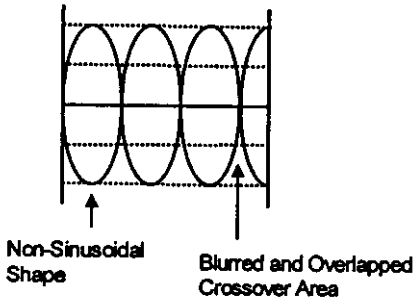


Figure iiC OVER MODULATION

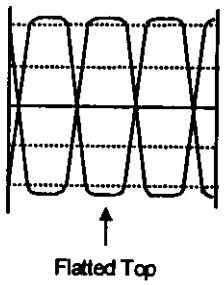
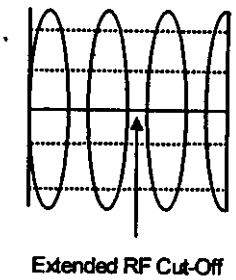


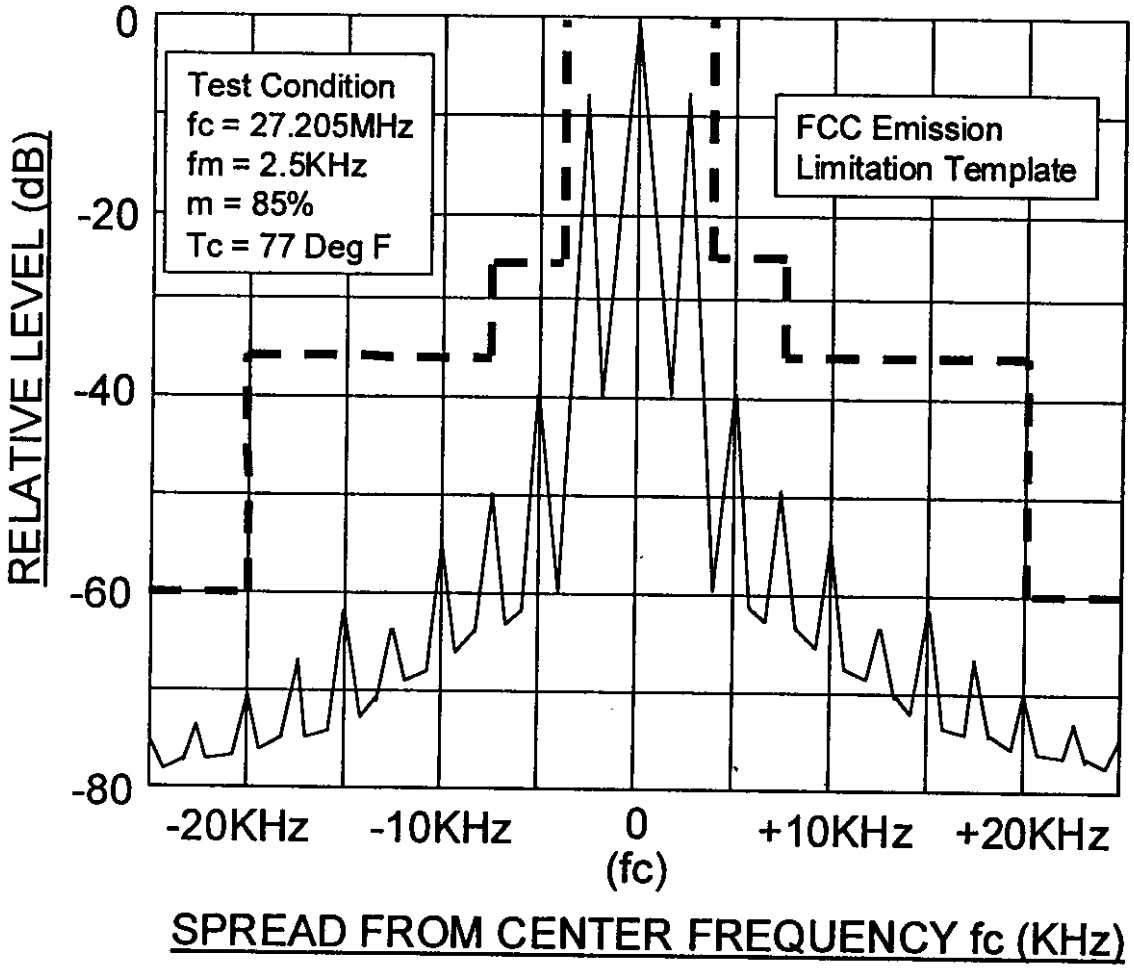
Figure iiD RF POWER TRANSISTORS BIASED INCORRECTLY.



iii) FCC Emission Limitation Check

- Set up equipment as in i) AM Modulation Monitor Test, Compandor OFF.
- Couple the Spectrum Analyzer input to the RF Dummy Load
- Apply 2.5KHz 50mV rms. audio tones signal to the Microphone input connector pin 2.
- Activate PTT to transmit on AM Mode, adjust AM Modulation level to 85% (see Fig iA).
- Observe on the Spectrum Analyzer that the Radio's RF output are within the FCC limits
- Repeat test with Compandor ON.

85% MODULATION SPECTRUM EMISSION LIMITATION TEST



APPENDIX 7

CIRCUITS AND DEVICES TO STABILIZE FREQUENCY

All 40 channels of transmitting, and receiving, frequencies are provided by PLL (Phase Locked Loop) (IC707) circuitry.

The purpose of the PLL is to provide a multiple number of frequencies from a VCO (Voltage Controlled Oscillator) with quartz crystal accuracy and stability locked to crystal oscillator reference frequency.

The reference crystal oscillator frequency is 10.24 MHz.

APPENDIX 8

A. Circuits For Suppression Of Spurious Radiation

The tuning circuit between the output of final amp TR43 and antenna, 4-stage "Phi" network associated with L34, L51, L52 and L31 serves as a spurious radiation suppressor. This network also serves to match the impedance between TX power amp and the antenna.

B. Circuits For Limiting Modulation

Input from the microphone is controlled by the Mic-Gain potentiometer VR505 and amplified by IC4. The amplified signal is used to drive the AM Modulator circuit consists of TR49 & 51.

There are two signals at the base of TR49, the DC voltage controlled by VR13 (RF Power Level Adjust), and the AF level from pin 1 of IC4. The DC bias controls the operating point of the Darlington pair transistors TR50 & 51 to provide power supply to the RF Power transistors TR43 & 44, which controls the RF Carrier Power output of the radio. The AF signal is amplified and superimposed on the DC bias to create high level AM Modulation in TR43 & 44.

The maximum modulation is regulated by the Automatic Level Control (ALC) circuit consists of TR53, TR34 and TR32.

TR53 is a comparator circuit with setpoint adjusted by VR14. When TR53 conducts, the signal is half wave rectified by D83 to drive the current amplifier TR34, which in turn drives TR32 on and shunt down the Mic Audio signal at the input of IC4. The RC circuit (C135, R176 ~ 178) at the base of TR32 ensures the smooth operation of the ALC.

When the modulator overmodulates, AC voltages at emitter of TR53 will increase, and TR53 will conduct more during the negative cycle of the modulation signal, which increases the collector current of TR53 and turn TR43/TR32 on. The audio signal is shunted, input to the modulator decreases until it reaches the Modulation Limit set point of VR14.

C. Circuits For Limiting Power

After being amplified by IC4, audio signals from the microphone is connected to the balanced modulator IC3 (pin 1). Signal from the second offset oscillator is presented to pin 3 of IC3 to produce the double side band suppressed carrier (DSBSC) signal. VR7 is adjusted for minimum carrier output.

C. Circuits For Limiting Power (continued)

The DSBSC signal is routed by the switching diodes to the 10.695 MHz crystal filter, the unwanted sideband is filtered off, and the processed SSB signal is sent to L44/IC9 for mixing with the VCO output (at L43) to obtain the final transmitting frequency.

The high level modulator TR50 & 51 are bypassed by TR52 during SSB opertion. The RF Power amplifiers are biased to class B operation (VR10 ~ 11) to preserve the envelope of the low-level modulated SSB signal. Since the SSB RF output is directly proportional to the level of audio signal driving the balanced modulator, the RF output is sampled by TR47, which provides negative feedback to the audio ALC circuit (TR34 & 53) to limit the maximum SSB power output.

APPENDIX 9

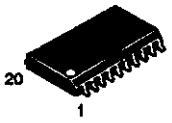
PLL DATA SHEETS

FIVE (5) PAGES FOR MC145106 FOLLOW THIS SHEET

MC145106

PLL Frequency Synthesizer
CMOS

P SUFFIX
PLASTIC DIP
CASE 707



DW SUFFIX
SOG PACKAGE
CASE 751D

ORDERING INFORMATION

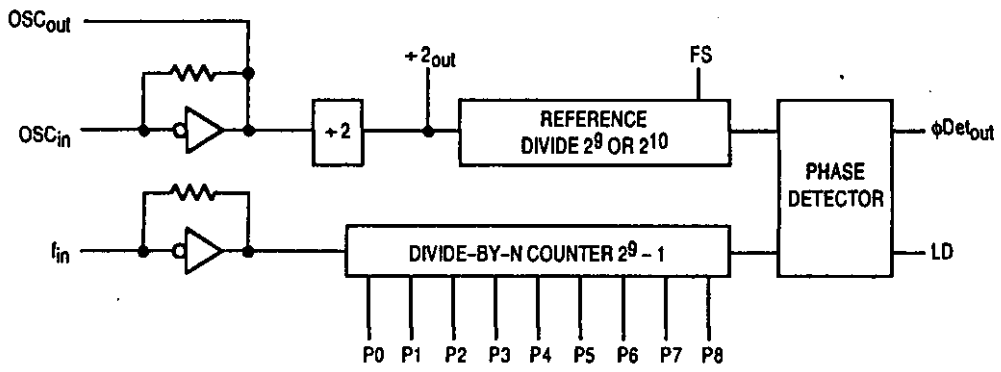
MC145106P	Plastic DIP
MC145106DW	SOG Package

The MC145106 is a phase–locked loop (PLL) frequency synthesizer constructed in CMOS on a single monolithic structure. This synthesizer finds applications in such areas as CB and FM transceivers. The device contains an oscillator/amplifier, a 2^{10} or 2^{11} divider chain for the oscillator signal, a programmable divider chain for the input signal, and a phase detector. The MC145106 has circuitry for a 10.24 MHz oscillator or may operate with an external signal. The circuit provides a 5.12 MHz output signal, which can be used for frequency tripling. A 2^9 programmable divider divides the input signal frequency for channel selection. The inputs to the programmable divider are standard ground–to–supply binary signals. Pull–down resistors on these inputs normally set these inputs to ground enabling these programmable inputs to be controlled from a mechanical switch or electronic circuitry.

The phase detector may control a VCO and yields a high level signal when input frequency is low, and a low level signal when input frequency is high. An out–of–lock signal is provided from the on–chip lock detector with a "0" level for the out–of–lock condition.

- Single Power Supply
- Wide Supply Range: 4.5 to 12 V
- Provision for 10.24 MHz Crystal Oscillator
- 5.12 MHz Output
- Programmable Division Binary Input Selects up to 2^9
- On–Chip Pull–Down Resistors on Programmable Divider Inputs
- Selectable Reference Divider, 2^{10} or 2^{11} (Including ÷ 2)
- Three–State Phase Detector
- See Application Note AN535 and Article Reprint AR254
- Chip Complexity: 880 FETs or 220 Equivalent Gates
- See the MC145151–2 and MC145152–2 for Higher Performance and Added Flexibility

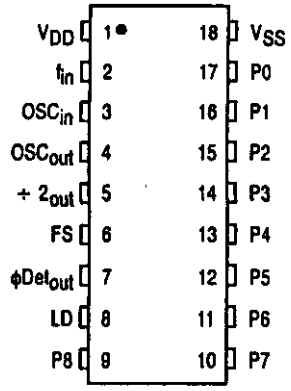
BLOCK DIAGRAM



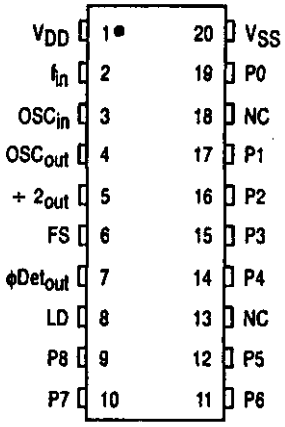
MOTOROLA

PIN ASSIGNMENTS

PLASTIC DIP



SOG PACKAGE



NC = NO CONNECTION

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	− 0.5 to + 12	V
Input Voltage, All Inputs	V_{in}	− 0.5 to V_{DD} + 0.5	V
DC Input Current, per Pin	I	± 10	mA
Operating Temperature Range	T_A	− 40 to + 85	°C
Storage Temperature Range	T_{stg}	− 65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

ELECTRICAL CHARACTERISTICS (T_A = 25°C Unless Otherwise Stated, Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	All Types			Unit
				Min	Typ*	Max	
Power Supply Voltage Range		V_{DD}	—	4.5	—	12	V
Supply Current		I_{DD}	5.0	—	6	10	mA
			10	—	20	35	
			12	—	28	50	
Input Voltage	"0" Level	V_{IL}	5.0	—	—	1.5	V
			10	—	—	3.0	
			12	—	—	3.6	
	"1" Level	V_{IH}	5.0	3.5	—	—	
			10	7.0	—	—	
			12	8.4	—	—	
Input Current	"0" Level	I_{in}	5.0	−5.0	−20	−50	µA
FS, Pull-Up Resistor Source Current)			10	−15	−60	−150	
			12	−20	−80	−200	
(P0 – P8)			5.0	—	—	−0.3	
			10	—	—	−0.3	
			12	—	—	−0.3	
(FS)	"1" Level		5.0	—	—	0.3	
			10	—	—	0.3	
			12	—	—	0.3	
(P0 – P8, Pull-Down Resistor Sink Current)			5.0	7.5	30	75	
			10	22.5	90	225	
			12	30	120	300	
(OSC_{in}, f_{in})	"0" Level		5.0	−2.0	−6.0	−15	
			10	−6.0	−25	−62	
			12	−9.0	−37	−92	
(OSC_{in}, f_{in})	"1" Level		5.0	2.0	6.0	15	
			10	6.0	25	62	
			12	9.0	37	92	
Output Drive Current		I_{OH}					mA
(V_O = 4.5 V)	Source		5.0	−0.7	−1.4	—	
(V_O = 9.5 V)			10	−1.1	−2.2	—	
(V_O = 11.5 V)			12	−1.5	−3.0	—	
(V_O = 0.5 V)	Sink	I_{OL}	5.0	0.9	1.8	—	
(V_O = 0.5 V)			10	1.4	2.8	—	
(V_O = 0.5 V)			12	2.0	4.0	—	
Input Amplitude		—					V p-p
(f_{in} @ 4.0 MHz)			—	1.0	0.2	—	Sine
(OSC_{in} @ 10.24 MHz)			—	1.5	0.3	—	
Input Resistance		R_{in}					MΩ
(OSC_{in}, f_{in})			5.0	—	1.0	—	
			10	—	0.5	—	
			12	—	—	—	
Input Capacitance		C_{in}	—	—	6.0	—	pF
(OSC_{in}, f_{in})							
Three-State Leakage Current		I_{OZ}	5.0	—	—	1.0	µA
(ϕDet_{out})			10	—	—	1.0	
			12	—	—	1.0	
Input Frequency		f_{in}	4.5	0	—	4.0	MHz
(− 40 to + 85°C)			12	0	—	4.0	
Oscillator Frequency		OSC_{in}	4.5	0.1	—	10.24	MHz
(− 40 to + 85°C)			12	0.1	—	10.24	

*Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

TYPICAL CHARACTERISTICS*

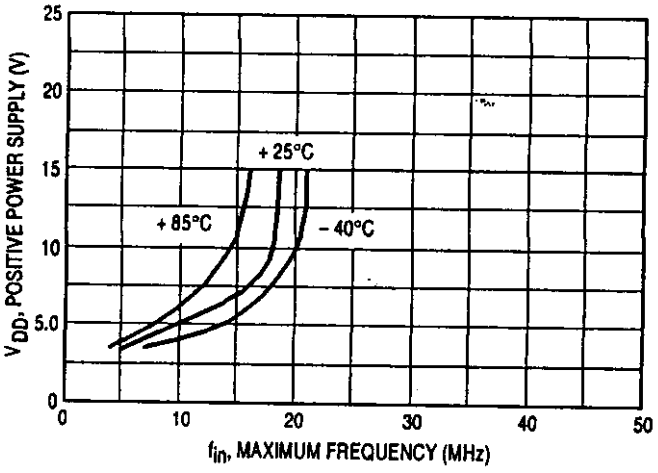


Figure 1. Maximum Divider Input Frequency versus Supply Voltage

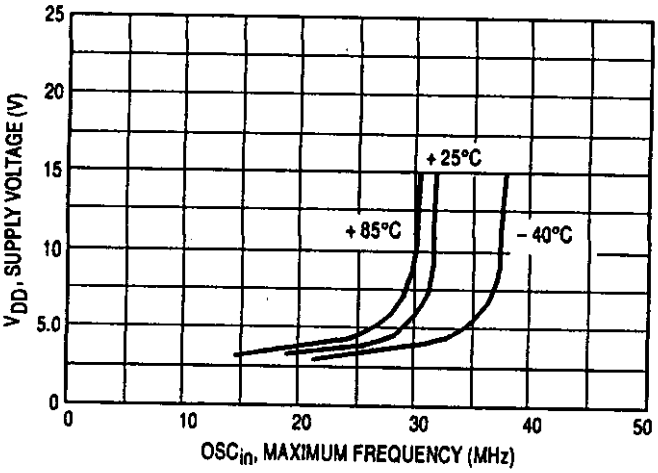


Figure 2. Maximum Oscillator Input Frequency versus Supply Voltage

* Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

TRUTH TABLE

Selection									
P8	P7	P6	P5	P4	P3	P2	P1	P0	Divide by N
0	0	0	0	0	0	0	0	0	2*
0	0	0	0	0	0	0	0	1	3*
0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	1	1	3
0	0	0	0	0	0	1	0	0	4
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	1	255
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	1	511

1: Voltage level = V_{DD}.
0: Voltage level = 0 or open circuit input.
* The binary setting of 00000000 and 00000001 on P8 to P0 results in a 2 and 3 division which is not in the $2^N - 1$ sequence. When pin is not connected the logic signal on that pin can be treated as a "0".

PIN DESCRIPTIONS

P0 – P8
Programmable Inputs (PDIP — Pins 17 – 9; SOG — Pins 19, 17 – 14, 12 – 9)

Programmable divider inputs (binary).

f_{in}
Frequency Input (PDIP, SOG — Pin 2)

Frequency input to programmable divider (derived from VCO).

OSC_{in}, OSC_{out}
Oscillator Input and Oscillator Output (PDIP, SOG — Pins 3, 4)

Oscillator/amplifier input and output terminals.

LD
Lock Detector (PDIP, SOG — Pin 8)

LD is high when loop is locked, pulses low when out–of–lock.

ϕDet_{out} (PDIP, SOG — Pin 7)

Signal for control of external VCO, output high when f_{in}/N is less than the reference frequency; output low when f_{in}/N is greater than the reference frequency. Reference frequency is the divided down oscillator — input frequency typically 5.0 or 10 kHz.

NOTE

Phase Detector Gain = $V_{DD}/4\pi$.

FS
Reference Oscillator Frequency Division Select (PDIP, SOG — Pin 6)

When using 10.24 MHz OSC frequency, this control selects 10 kHz, a "0" selects 5.0 kHz.

$\div 2_{out}$ (PDIP, SOG — Pin 5)

Reference OSC frequency divided by 2 output; when using 10.24 MHz OSC frequency, this output is 5.12 MHz for frequency tripling applications.

V_{DD}
Positive Power Supply (PDIP, SOG — Pin 1)

V_{SS}
Ground (PDIP — Pin 18, SOG — Pin 20)

PLL SYNTHESIZER APPLICATIONS

The MC145106 is well suited for applications in CB radios because of the channelized frequency requirements. A typical 40 channel CB transceiver synthesizer, using a single crystal reference, is shown in Figure 3 for receiver IF values of 10.695 MHz and 455 kHz.

In addition to applications in CB radios, the MC145106 can be used as a synthesizer for several other systems. Various frequency spectrums can be achieved through the use of proper offset, prescaling, and loop programming techniques. In general, 300 – 400 channels can be synthesized using a single loop, with many additional channels available when multiple loop approaches are employed. Figures 4 and 5 are examples of some possibilities.

In the aircraft synthesizer of Figure 5, the VHF loop (top) will provide a 50 kHz, 360 channel system with 10.7 MHz R/T offset when only the 11.0500 MHz (transmit) and 12.1200 MHz (receive) frequencies are provided to mixer #1. When these signals are provided with crystal oscillators, the result is a three crystal 360 channel, 50 kHz step synthesizer. When using the offset loop (bottom) in Figure 5 to provide the indicated injection frequencies for mixer #1 (two for transmit and two for receive) 360 additional channels are possible. This results in a 720–channel, 25 kHz step synthesizer which requires only two crystals and provides R/T offset capability. The receive offset value is determined by the 11.31 MHz crystal frequency and is 10.7 MHz for the example.

The VHF marine synthesizer in Figure 4 depicts a single loop approach for FM transceivers. The VCO operates on frequency during transmit and is offset downward during receive. The offset corresponds to the receive IF (10.7 MHz) for channels having identical receive/transmit frequencies (simplex), and is (10.7 – 4.6 = 6.1) MHz for duplex channels. Carrier modulation is introduced in the loop during transmit.

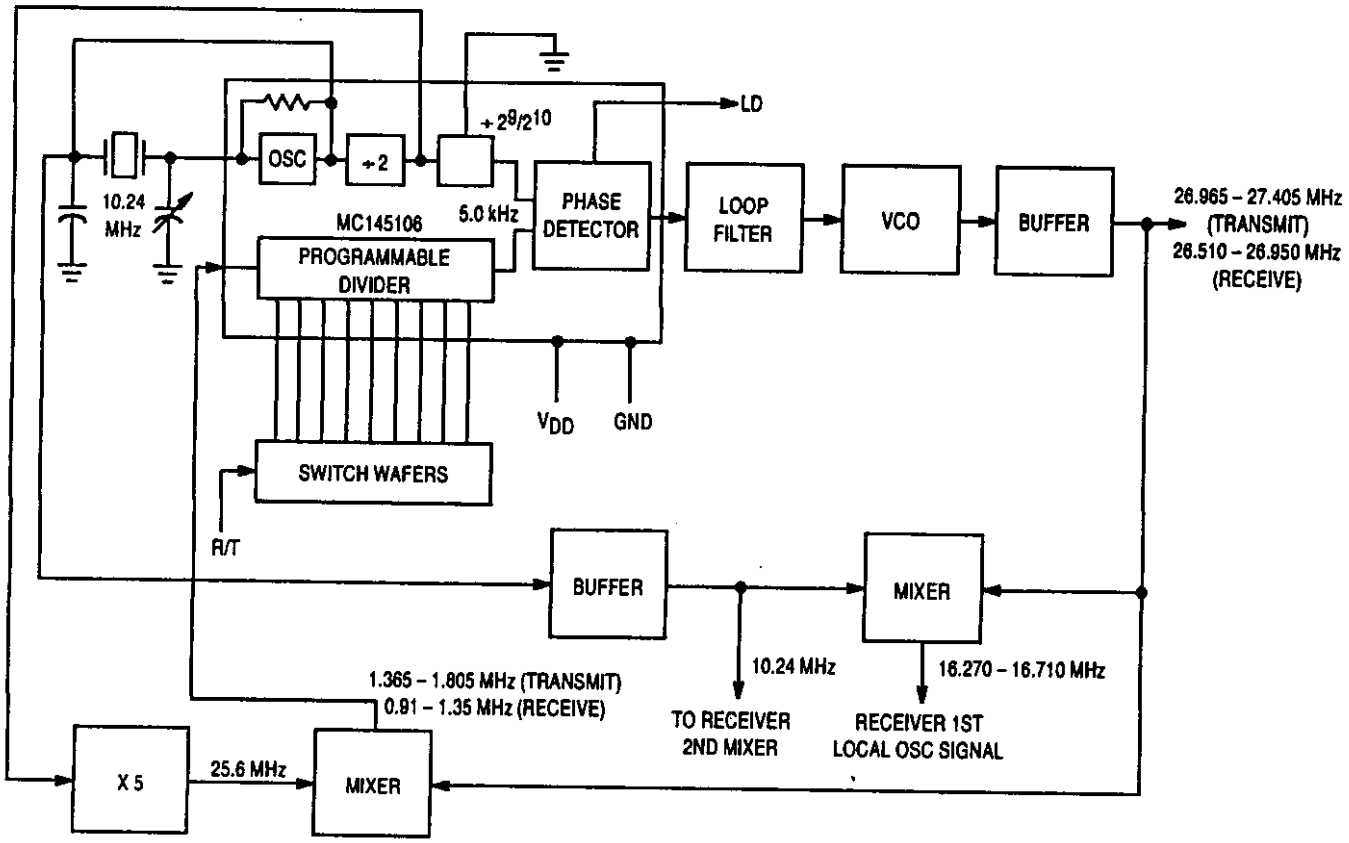


Figure 3. Single Crystal CB Synthesizer Featuring On–Frequency VCO During Transmit

APPENDIX 10

FINAL RF AMPLIFIER DATA SHEETS

THREE (3) PAGES FOR 2SC1969 FOLLOW THIS SHEET

Parts Specification

C.B. Mobile Transceiver

2SC1969 TR-43 NPN EPITAXIAL PLANAR TYPE

DESCRIPTION

2SC1969 is a silicon NPN epitaxial planar type transistor designed for RF power amplifiers on HF band mobile radio applications.

FEATURES

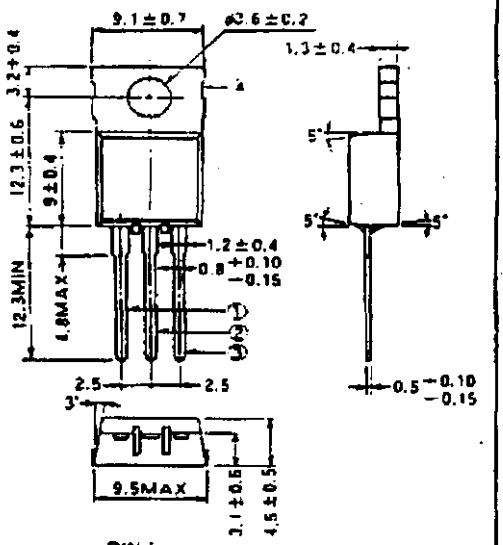
- High power gain: $G_{pe} \geqq 12dB$
  @V_{CC} = 12V, P_O = 16W, f = 27MHz
- Emitter ballasted construction for high reliaiblity and good performances.
- TO-220 package similarly is combinient for mounting.
- Ability of withstanding infinite load VSWR when operated at V_{CC} = 16V, P_O = 20W, f = 27MHz.

APPLICATION

10 to 14 watts output power class AB amplifiers applications in HF band.

OUTLINE DRAWING

Dimensions in mm



PIN :
① BASE
② COLLECTOR (FIN)
③ EMITTER
④ FIN (COLLECTOR)

T-30

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CBO}	Collector to base voltage		60	V
V_{EBO}	Emitter to base voltage		5	V
V_{CEO}	Collector to emitter voltage	R_{BE} = ∞	25	V
I_C	Collector current		6	A
P_C	Collector dissipation	T_A = 25°C	1.7	W
		T_C = 25°C	20	W
T_j	Junction temperature		150	°C
T_{stg}	Storage temperature		−55 to 150	°C
$R_{th\text{-}a}$	Thermal resistance	Junction to ambient	73.5	°C/W
$R_{th\text{-}c}$		Junction to case	6.25	°C/W

Note Above parameters are guaranteed independently

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{(BR)EBO}$	Emitter to base breakdown voltage	I_E = 5mA, I_C = 0	5			V
$V_{(BR)CBO}$	Collector to base breakdown voltage	I_C = 1mA, I_E = 0	60			V
$V_{(BR)CEO}$	Collector to emitter breakdown voltage	I_C = 10mA, R_{BE} = ∞	25			V
I_{CBO}	Collector cutoff current	V_{CB} = 30V, I_E = 0			100	μA
I_{EBO}	Emitter cutoff current	V_{EB} = 4V, I_C = 0			100	μA
h_{FE}	DC forward current gain*	V_{CE} = 12V, I_C = 10mA	10	50	180	—
P_O	Output power	V_{CC} = 12V, P_{in} = 1w, f = 27MHz	16	18		W
η_C	Collector efficiency		60	70		%

Note. * Pulse test: P_W = 150μs, duty = 5%.
Above parameters, ratings, limits and conditions are subject to change

Item	X	A	B	C	D
h_{FE}	10-25	20-45	35-70	55-110	90-180

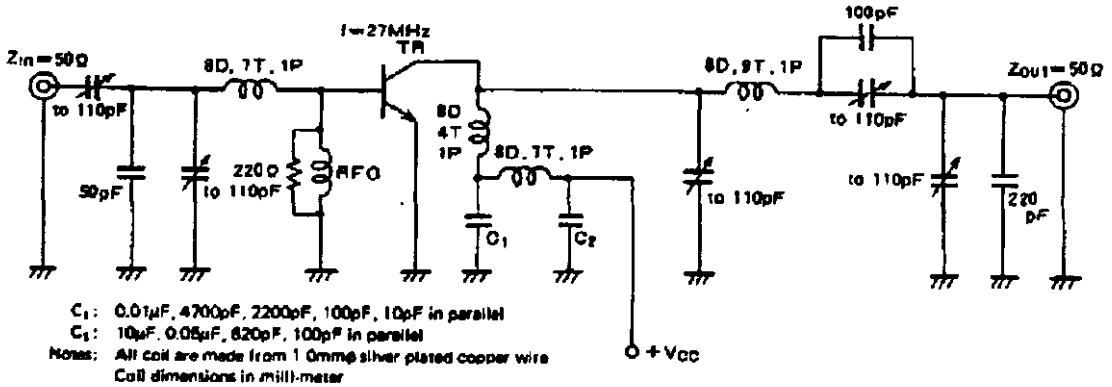
Parts Specification

C.B. Mobile Transceiver

2SC1969

NPN EPITAXIAL PLANAR TYPE

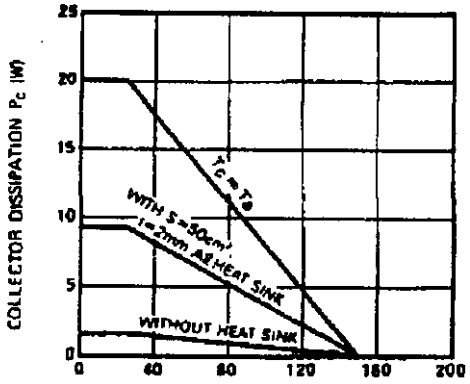
TEST CIRCUIT



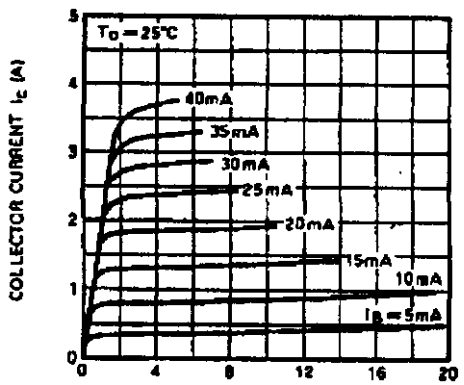
C_1: 0.01μF, 4700pF, 2200pF, 100pF, 10pF in parallel
C_2: 10μF, 0.05μF, 620pF, 100pF in parallel
Notes: All coil are made from 1.0mmφ silver plated copper wire
Coil dimensions in milli-meter
D: Inner diameter of coil
T: Turn number of coil
P: Pitch of coil

TYPICAL PERFORMANCE DATA

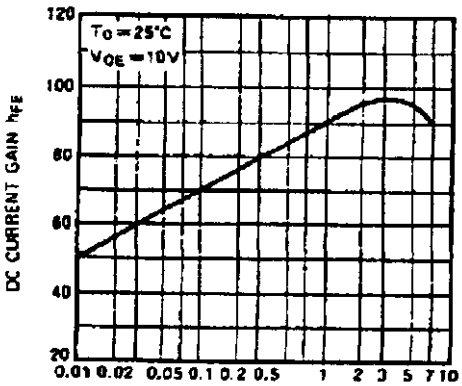
COLLECTOR DISSIPATION VS. AMBIENT TEMPERATURE



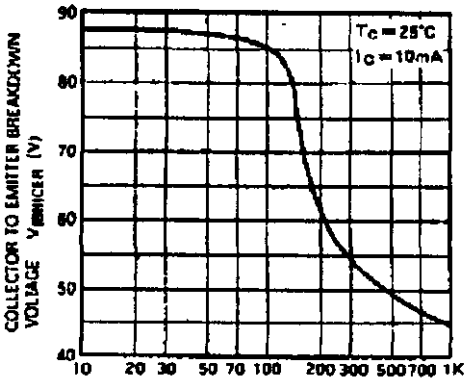
COLLECTOR CURRENT VS. COLLECTOR TO EMITTER VOLTAGE



DC CURRENT GAIN VS. COLLECTOR CURRENT



COLLECTOR TO EMITTER BREAKDOWN VOLTAGE VS. BASE TO EMITTER RESISTANCE



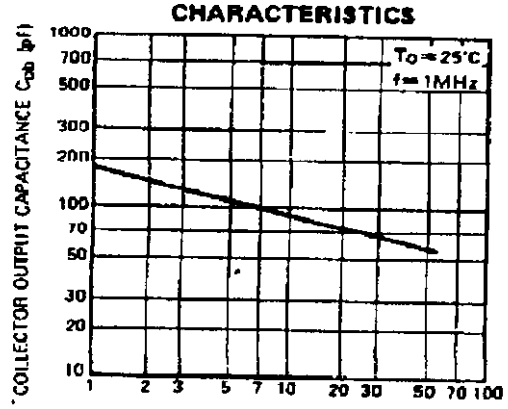
Parts Specification

C.B. Mobile Transceiver

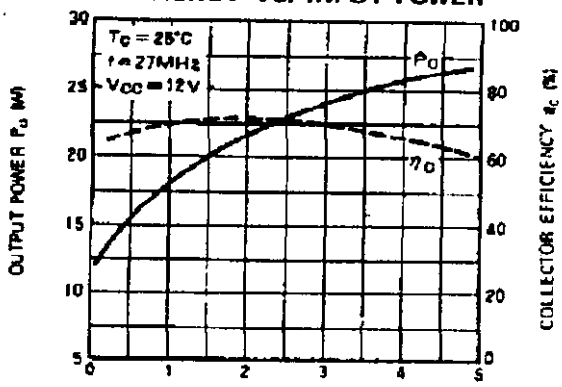
2SC1969

NPN EPITAXIAL PLANAR TYPE

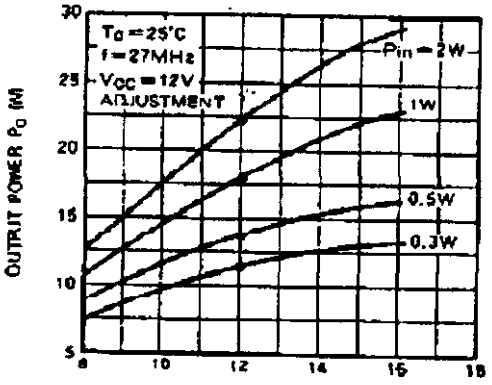
COLLECTOR OUTPUT CAPACITANCE VS. COLLECTOR TO BASE VOLTAGE CHARACTERISTICS



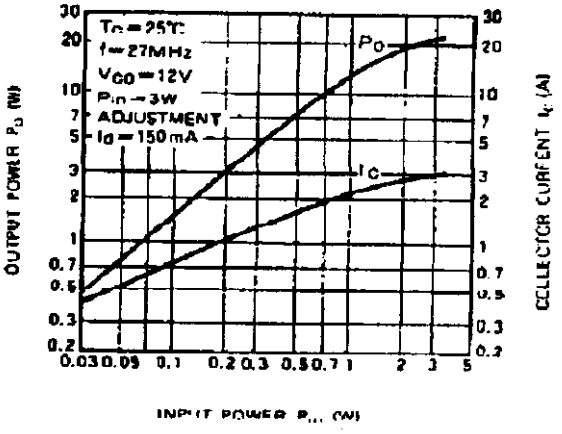
OUTPUT POWER, COLLECTOR EFFICIENCY VS. INPUT POWER



OUTPUT POWER VS. COLLECTOR SUPPLY VOLTAGE



IN CASE AB OPERATING OUTPUT POWER COLLECTOR CURRENT VS. INPUT POWER



THIRD ORDER INTERMODULATION DISTORTION VS. OUTPUT POWER