Transmitter Status (RR1)
(A1=0, A0=1; $\overline{CS}$=0, $\overline{RD}$=0, $\overline{WR}$=1)

This register contains all of the HDLC transmitter bits. It is cleared when $\overline{STANDBY}$=0 or TX/$\overline{RX}$=1.

Bit0 is the Transmit Buffer Full bit. When this bit is set to "1", the Transmit Buffer (WR0) is full, and writing to it again will overwrite its present contents.

Bit1 is the Transmit Character Request bit. This bit is set to "1" when the HDLC Transmitter is requesting either a new data byte or a command to send a new special character. This bit is cleared by writing to the Transmit Buffer (WR0) or the Transmit Control Register (WR1).

Bit2 is the Transmitter Overrun bit. This bit is set to "1" if the Transmit Buffer (WR0) was written to while it was full. This bit is cleared when this register is read.

Bit3 is the Transmitter Underrun bit. This bit is set to "1" if the Transmit Buffer (WR0) was not written to in time while sending a data packet. This error condition results in an ABORT character being sent which effectively terminates the packet. This status bit is cleared when this register is read.

Receive Buffer (RR0)
(A1=0, A0=0; $\overline{CS}$=0, $\overline{RD}$=0, $\overline{WR}$=1)

This register contains the last data byte received. It is cleared when STANDBY=0 or TX/RX=1.

Receiver Status (RR2)
(A1=1, A0=0; $\overline{CS}$=0, $\overline{RD}$=0, $\overline{WR}$=1)

This register contains the receiver status bits for the HDLC controller. These bits are cleared when $\overline{STANDBY}$=0 or TX/$\overline{RX}$=1.

Bit0 is the CRC Result bit. This bit is set to a "0" when a received data packet's CRC is checked and is good. This bit is set to a "1" when the CRC is checked and is invalid.

Bit1 is the CRC Received bit. This bit is set to a "1" when the CRC result is calculated and stored in Bit0. The CRC Received bit is set on a closing FLAG of a data packet in which at least one data byte and two CRC bytes have been read. This bit is cleared when this register is read.

Bit2-Bit4 are the special Character Detection bits. These bits are set whenever a specific special character has been detected and are cleared when this register is read. Bit2 corresponds to an ABORT character, Bit3 corresponds to a FLAG character, and Bit4 corresponds to a WAKEUP character.

Bit5 is the Data Ready bit. This bit is set when a new data word is written into the Receive Buffer (RR0) and is cleared when the Receive Buffer (RR0) or the Receiver Status Register (RR2) is read.

Bit6 is the Receiver Overrun bit. This bit is set when a new received data byte is ready before the previous data byte in the Receive Buffer (RR0) has been read. This is an error condition because a data byte has been lost.

4.2.2 Bus Interface Timing Diagrams

Figure 5 shows the read operation timing diagram. The referenced time constants are:

Symbol	Time		Description
tac	50ns	MIN	Read Set-up
trr	100ns	MIN	Read Pulse Width
tca	50ns	MIN	Read Hold
trd	35ns	MAX	Access Time
tdh	5ns	MIN	Hold Time

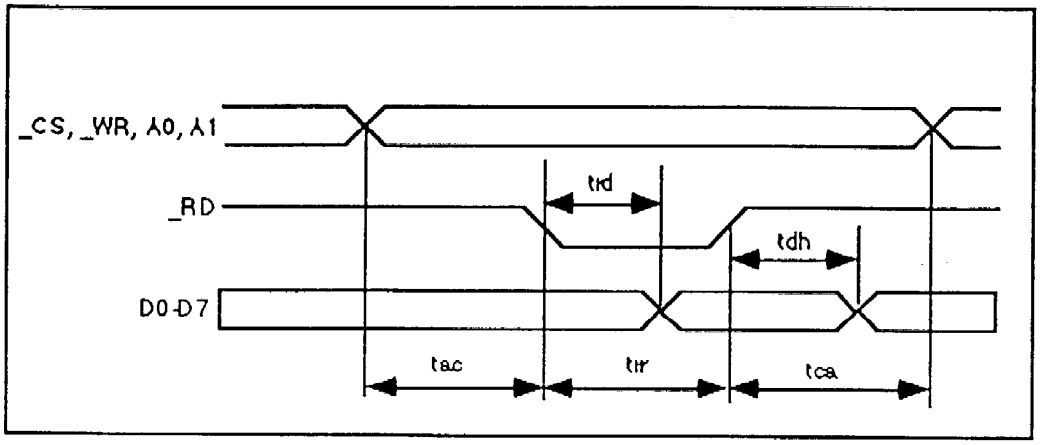

Figure 5 - Read Timing Diagram

Figure 6 shows the write operation timing diagram. Referenced time constants are:

Symbol	Time		Description
tac	50ns	MIN	Write Set-up
trr	100ns	MIN	Write Pulse Width
tca	50ns	MIN	Write Hold

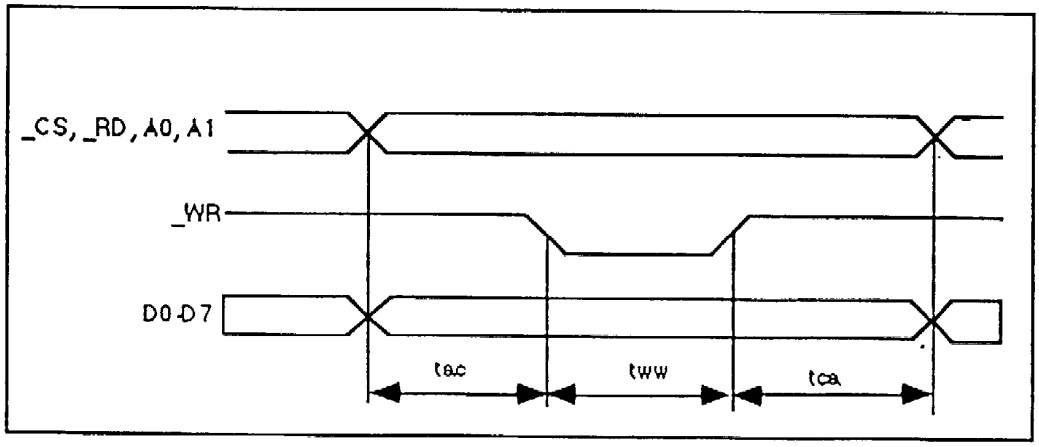

Figure 6 - Write Timing Diagram

4.3 Radio Control

This section describes the process for selecting the radio's mode and channel. The *Frequency Programming* section details how control codes are loaded in the Synthesizer Control Register. The sections *Receive Mode*, *Transmit Mode*, and *Standby Mode* each outline the steps necessary to enter that mode from each of the other modes.

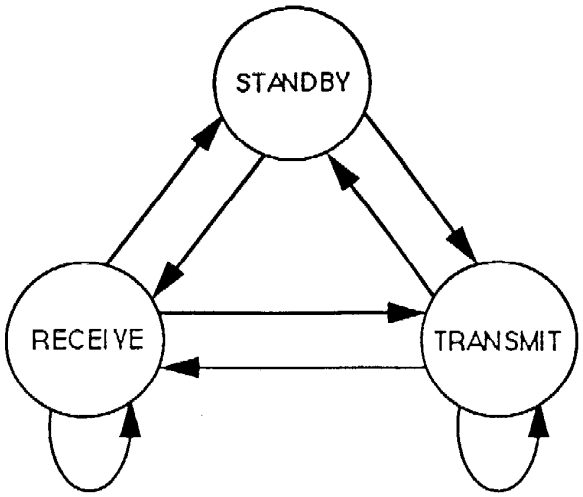

Figure 7 - Radio Modes

4.3.1 Frequency Programming

Before the radio can either transmit or receive, the synthesizer must be set to an operating frequency. Table 1 shows the RDA-100's seven frequency channels and their internal representation by the radio. Its four non-overlapping channels are identified by asterisks. The RDA2's three non-overlapping channels are identified by asterisks in Table 2.

The synthesizer is shared by the transmitter and receiver (see Figure 1) and must be reprogrammed whenever changing mode or switching channel.

As shown in Tables 1 and 2, the programming information for the synthesizer consists of a 16 bit word and a 19 bit word, referred to as the Reference Divider Word and RF Divider Word respectively. Once a word has been input into the shift register, it must be loaded into the Synthesizer Control Register before the next word can be shifted in. The synthesizer uses the control bit (C) to differentiate between the Reference Divider Word(1) and the RF Divider Word(0). Tables 1 and 2 describe the bit pattern corresponding to each transmit and receive frequency available.

The radio's operating frequency is programmed using the three interface bits in the Synthesizer Control Register (WR3): the Synthesizer Clock Bit (Bit0), the Synthesizer Data Bit (Bit1) and the Synthesizer Load Bit (Bit2). To access this register, the address lines A0 and A1 should be set high; $\overline{CS}$ and $\overline{WR}$ should be set low, while $\overline{RD}$ should also be set high. The three bits allow access to the Synthesizer Control Lines over the processor data bus. The data representing the desired frequency is input in a serial fashion, most significant bit first, via the Synthesizer Data Bit. At the positive edge of the Synthesizer Clock Bit, the state of the Synthesizer Data Bit is stored in a shift register. The data is accumulated in the shift register until the Synthesizer Load Bit is set to "1", at which point the data is transferred to a control register. The specific steps for loading a synthesizer frequency word are detailed below and are represented in Figure 8 with a timing diagram. Note that the acronyms (such as T2) refer to the timing diagram in Figure 8.

Channel	Tuned Freq (MHz)	First Bit ..... Last Bit (MSB) .....(LSB)									
		|Ref. Divider Word|		C	|	RF Divider Word				| C
Transmit											
* 1	906	10000000	0101000	1		00001000	11001100	10	0		
2	909	10000000	0101000	1		00001000	11100000	01	0		
* 3	912	10000000	0101000	1		00001000	11100100	00	0		
4	915	10000000	0101000	1		00001000	11100111	11	0		
* 5	918	10000000	0101000	1		00001000	11101011	10	0		
6	921	10000000	0101000	1		00001000	11101111	01	0		
* 7	924	10000000	0101000	1		00001001	00000011	00	0		
	CLOCK	+++++++	+++++++	+		++++++++	++++++++	++	+		
	LOAD			+							+
		|Ref. Divider Word|		C	|	RF Divider Word				| C
Receive											
* 1	906	10000000	0101000	1		00001001	01000011	10	0		
2	909	10000000	0101000	1		00001001	01000111	01	0		
* 3	912	10000000	0101000	1		00001001	01001011	00	0		
4	915	10000000	0101000	1		00001001	01001110	11	0		
* 5	918	10000000	0101000	1		00001001	01100010	10	0		
6	921	10000000	0101000	1		00001001	01100110	01	0		
* 7	924	10000000	0101000	1		00001001	01101010	00	0		
	CLOCK	+++++++	+++++++	+		++++++++	++++++++	++	+		
	LOAD			+							+

* Non-overlapping channels

Table 1- Synthesizer Frequency Words for the RDA

Channel	Tuned Freq (MHz)	First Bit (MSB) ... Last Bit (LSB)								
		|Ref. Divider Word|		C	|	RF Divider Word			|	C
Transmit										
* 1	906	10000000	1010000	1		00001000	11001100	10	0	
2	909	10000000	1010000	1		00001000	11100000	01	0	
3	912	10000000	1010000	1		00001000	11100100	00	0	
* 4	915	10000000	1010000	1		00001000	11100111	11	0	
5	918	10000000	1010000	1		00001000	11101011	10	0	
6	921	10000000	1010000	1		00001000	11101111	01	0	
* 7	924	10000000	1010000	1		00001001	00000011	00	0	
	CLOCK	++++++++	+++++++	+		++++++++	++++++++	++	+	
	LOAD			+						+
		|Ref. Divider Word|		C	|	RF Divider Word			|	C
Receive										
* 1	906	10000000	1010000	1		00001001	01000011	10	0	
2	909	10000000	1010000	1		00001001	01000111	01	0	
3	912	10000000	1010000	1		00001001	01001011	00	0	
* 4	915	10000000	1010000	1		00001001	01001110	11	0	
5	918	10000000	1010000	1		00001001	01100010	10	0	
6	921	10000000	1010000	1		00001001	01100110	01	0	
* 7	924	10000000	1010000	1		00001001	01101010	00	0	
	CLOCK	++++++++	+++++++	+		++++++++	++++++++	++	+	
	LOAD			+						+

* Non-overlapping channels

Table 2 - Synthesizer Frequency Words for the RDA2

The following process must be followed to load either the Reference Divider Word or the RF Divider Word. Because the control bit indicates which word is being loaded, the order in which the words are loaded is unimportant.

- For each bit in the Synthesizer Divider Word, perform the following steps:
  - Set the SYNDATA line to the next bit of the Synthesizer Frequency Word.
  - Wait for the data setup time (T3).
  - Trigger the SYNCLK line for a duration of T4.
  - Hold the data for a period T9.
- Wait for the load setup time (T6).
- Trigger the SYNLD line for a duration of T5.

Note once again that the Synthesizer Control Lines are programmed through the three bits of the Synthesizer Control Register (WR3).

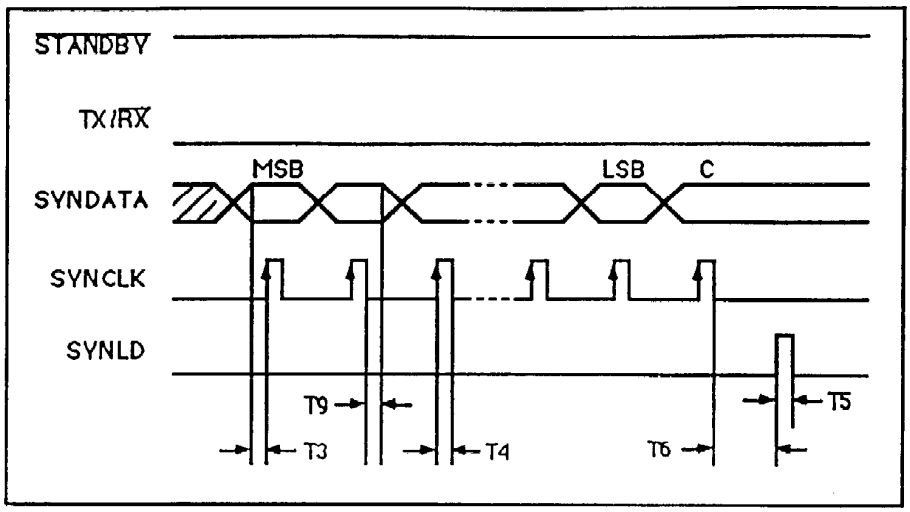

Figure 8 - Serial Data Input Timing

Note that the Reference Divider Word is the same for all transmit and receive frequencies. Therefore, it only needs to be reloaded if the radio is brought out of Standby mode, not when changing between Receive and Transmit modes. Consequently, once the synthesizer has been initialized only the RF Divider Word needs to be loaded during subsequent mode or channel changes.

Also note that the RF Divider Word may be clocked into the shift register at any time. The new RF Divider Word will not affect the radio until the SYNLD line is high and the shift register is loaded into the control register. This allows the radio turn around time to be optimized by loading the RF Divider Word for the next state immediately after raising the SYNLD line for the current state. For example, if the radio is currently in Receive mode and during some idle time the transmit channel was clocked into the shift register, the state could be changed by simply raising the SYNLD line.

4.3.2 Transmit Mode

The following three sections outline the steps necessary to enter the Transmit mode from each of the three modes (including from Transmit mode itself in order to change transmit channels).

4.3.2.1 From Standby Mode

During Standby all the registers in the radio are cleared, therefore, switching to Transmit from Standby requires loading both the Reference Divider Word and the RF Divider Word into the control register. In addition, care must be taken not to supply power to the radio when the transmitter is enabled. The procedure for switching the radio from Standby to Transmit is summarized below.

- Ensure the TX/$\overline{RX}$ line is low so that when power is supplied to the radio, it does not start transmitting at an unknown frequency.
- Raise the $\overline{STANDBY}$ line high.
- Wait for the power supply to stabilize (T2).
- Load the Reference Divider Word into the synthesizer (see section 4.3.1.).
- Load the desired RF Divider Word into the synthesizer (see section 4.3.1.).
- Wait for the synthesizer to stabilize (T7).
- Raise the TX/$\overline{RX}$ line high to activate the transmitter.
- Begin transmitting data (see section 4.4).

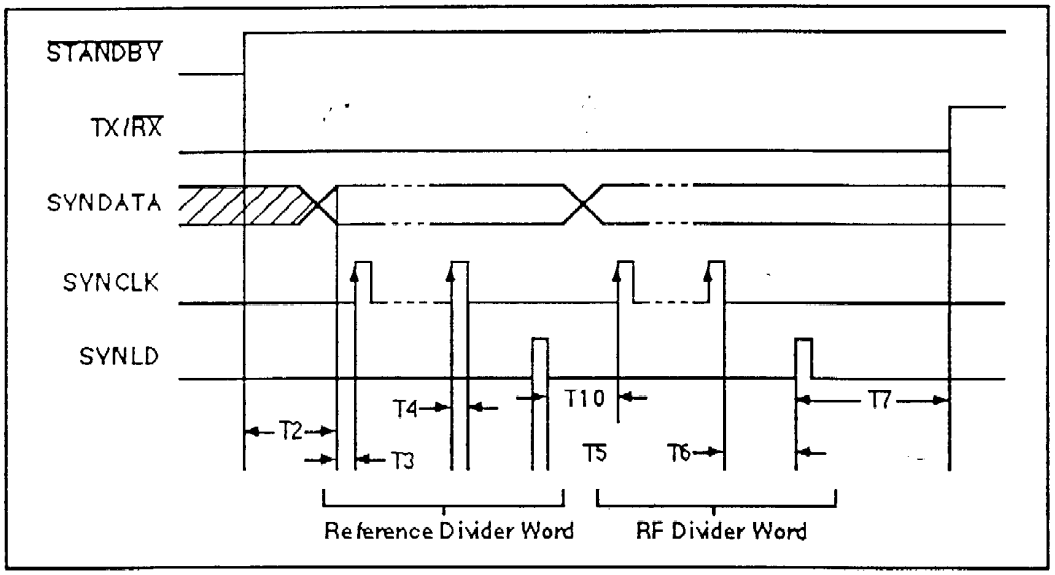

Figure 9 - Standby to Transmit Timing Diagram

For a complete listing of all these timings please see Table 3 in section 4.3.5.

4.3.2.2 From Receive Mode

Switching to Transmit from Receive requires loading the RF Divider Word into the control register. Care must be taken, however, not to set the TX/$\overline{RX}$ line high until the new RF Divider Word has been loaded and the synthesizer has settled. The procedure for switching the radio from Receive to Transmit is summarized below.

- Load the desired RF Divider Word into the synthesizer (see section 4.3.1.).
- Wait for the synthesizer to stabilize (T8).
- Raise the TX/$\overline{RX}$ line high to activate the transmitter.
- Begin transmitting data (see section 4.4).

Note that the RF Divider Word may be shifted into the synthesizer at any time. It will not take effect until the SYNLD line is set high. By shifting in the RF Divider Word early, the time necessary to switch channels may be reduced.

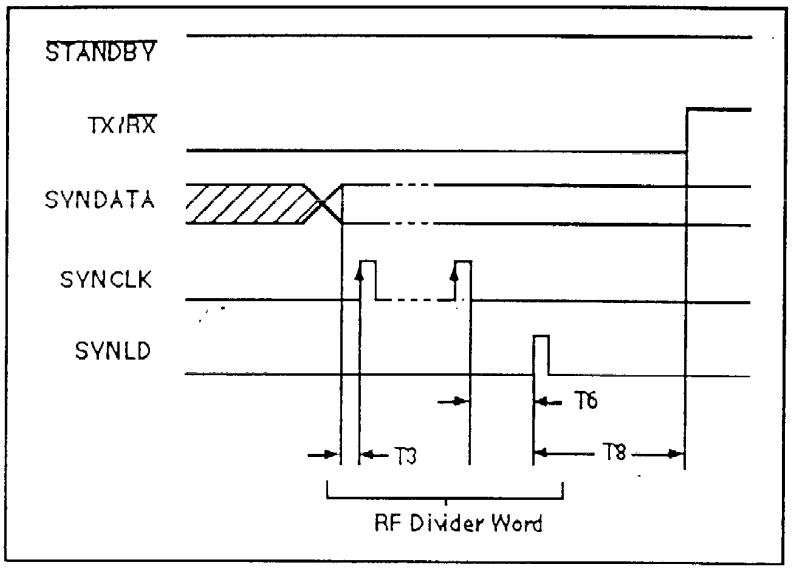

Figure 10 - Receive to Transmit Timing Diagram

For a complete listing of all these timings please see Table 3 in section 4.3.5.

4.3.2.3 From Transmit Mode

Switching to Transmit from Transmit in order to change channels requires that the RF Divider Word be reloaded into the control register. Care must be taken, however, to turn the transmitter off before changing channels. Otherwise, the radio will "splatter" a number of frequencies before reaching the new frequency. The procedure for changing the radio's transmit channel is summarized below.

- Set the TX/$\overline{RX}$ line low to disable the transmitter .
- Shift the new RF Divider Word into the synthesizer (see section 4.3.1.).
- Ensure the transmitter is off (T1).
- Load the new RF Divider Word into the synthesizer, i.e. set SYNLD line high (see section 4.3.1.).
- Wait for the synthesizer to stabilize (T8).
- Raise the TX/$\overline{RX}$ line high to activate the transmitter.
- Begin transmitting data (see section 4.4).

Note that the RF Divider Word word may be shifted into the synthesizer at any time. It will not take effect until the SYNLD line is set high. By shifting in the RF Divider Word early, the time necessary to switch channels may be reduced.

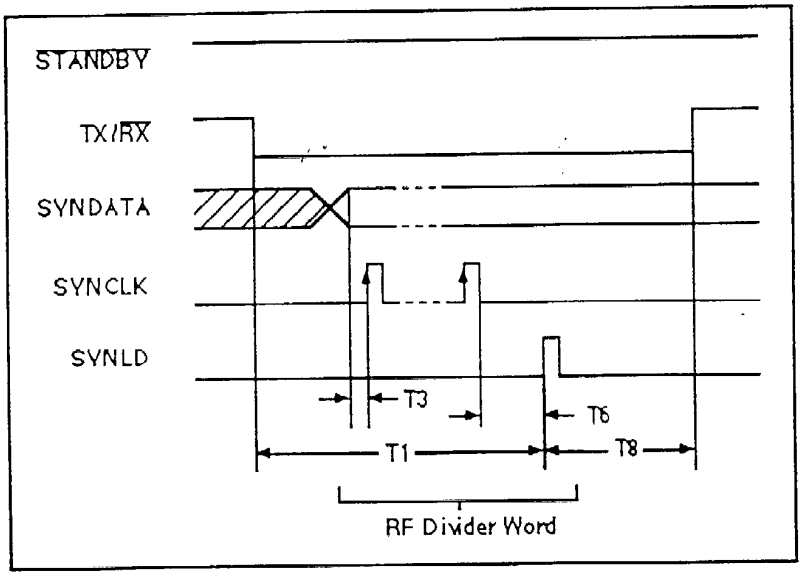

Figure 11 - Changing Transmission Channel Timing Diagram

For a complete listing of all these timings please see Table 3 in section 4.3.5.

4.3.3 Receive Mode

The following three sections outline the steps necessary to enter the Receive mode from each of the three states (including Receive mode itself in order to change receive channels).

4.3.3.1 From Standby Mode

During Standby all the registers in the radio are cleared, therefore,switching to Receive from Standby requires loading both the Reference Divider Word and the RF Divider Word into the control register. In addition, care must be taken not to supply power to the radio without first disabling the transmitter. The procedure for switching the radio from Standby to Receive is summarized below.

- Ensure the TX/$\overline{RX}$ line is low so that when power is supplied to the radio, it does not start transmitting at an unknown frequency.
- Raise the $\overline{STANDBY}$ line high.
- Wait for the power supply to stabilize (T2).
- Load the Reference Divider Word into the synthesizer (see section 4.3.1.).
- Load the desired RF Divider Word into the synthesizer (see section 4.3.1.).
- Wait for synthesizer to stabilize (T7).
- Begin receiving data (see section 4.4).

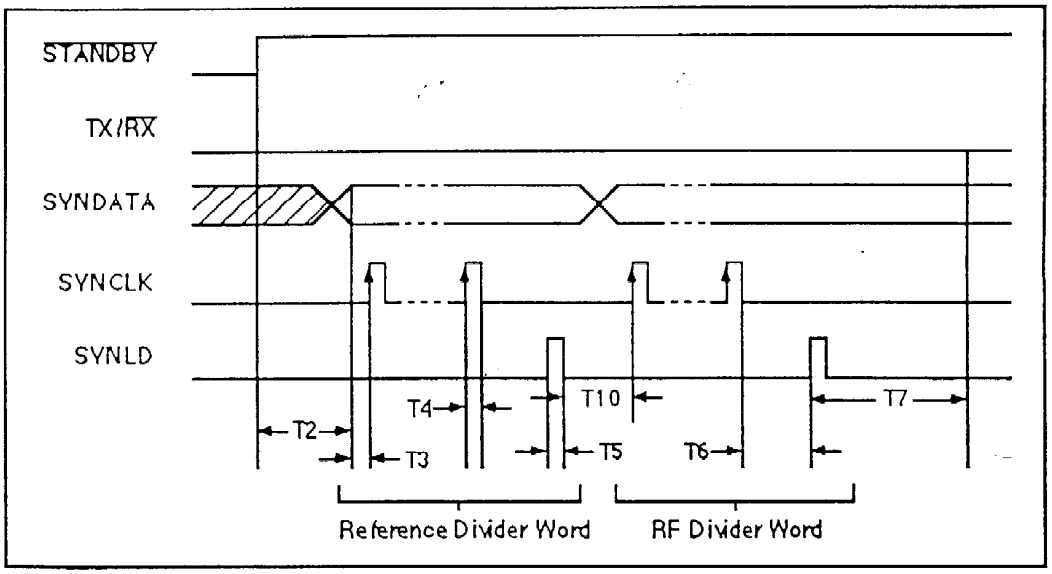

Figure 12 - Standby to Receive Timing Diagram

For a complete listing of all these timings please see Table 3 in section 4.3.5.