The radio's operating frequency is programmed using the three interface bits in the Synthesizer Control Register (WR3): the Synthesizer Clock Bit (Bit0), the Synthesizer Data Bit (Bit1) and the Synthesizer Load Bit (Bit2). To access this register, the address lines A0 and A1 should be set high; $\overline{CS}$ and $\overline{WR}$ should be set low, while $\overline{RD}$ should also be set high. The three bits allow access to the Synthesizer Control Lines over the processor data bus. The data representing the desired frequency is input in a serial fashion, most significant bit first, via the Synthesizer Data Bit. At the positive edge of the Synthesizer Clock Bit, the state of the Synthesizer Data Bit is stored in a shift register. The data is accumulated in the shift register until the Synthesizer Load Bit is set to "1", at which point the data is transferred to a control register. The specific steps for loading a synthesizer frequency word are detailed below and are represented in Figure 8 with a timing diagram. Note that the acronyms (such as T2) refer to the timing diagram in Figure 8.

Channel	Tuned Freq (MHz)	First Bit (MSB) ... Ref. Divider Word	C	RF Divider Word ... Last Bit (LSB)	C
Transmit					
* 1	906	10000000 0101000	1	00001000 11001100 10	0
2	909	10000000 0101000	1	00001000 11100000 01	0
* 3	912	10000000 0101000	1	00001000 11100100 00	0
4	915	10000000 0101000	1	00001000 11100111 11	0
* 5	918	10000000 0101000	1	00001000 11101011 10	0
6	921	10000000 0101000	1	00001000 11101111 01	0
* 7	924	10000000 0101000	1	00001001 00000011 00	0
	CLOCK	++++++++ +++++++	+	++++++++ ++++++++ ++	+
	LOAD		+		+
Receive		Ref. Divider Word	C	RF Divider Word	C
* 1	906	10000000 0101000	1	00001001 01000011 10	0
2	909	10000000 0101000	1	00001001 01000111 01	0
* 3	912	10000000 0101000	1	00001001 01001011 00	0
4	915	10000000 0101000	1	00001001 01001110 11	0
* 5	918	10000000 0101000	1	00001001 01100010 10	0
6	921	10000000 0101000	1	00001001 01100110 01	0
* 7	924	10000000 0101000	1	00001001 01101010 00	0
	CLOCK	++++++++ +++++++	+	++++++++ ++++++++ ++	+
	LOAD		+		+

* Non-overlapping channels

Table 1- Synthesizer Frequency Words for the RDA

Channel	Tuned Freq (MHz)	First Bit (MSB) .... |Ref. Divider Word|	C	| RF Divider Word .... Last Bit (LSB)	| C
Transmit					
* 1	906	10000000 1010000	1	00001000 11001100 10	0
2	909	10000000 1010000	1	00001000 11100000 01	0
3	912	10000000 1010000	1	00001000 11100100 00	0
* 4	915	10000000 1010000	1	00001000 11100111 11	0
5	918	10000000 1010000	1	00001000 11101011 10	0
6	921	10000000 1010000	1	00001000 11101111 01	0
* 7	924	10000000 1010000	1	00001001 00000011 00	0
	CLOCK	++++++++ +++++++	+	++++++++ ++++++++ ++	+
	LOAD		+		+
		|Ref. Divider Word|	C	| RF Divider Word	| C
Receive					
* 1	906	10000000 1010000	1	00001001 01000011 10	0
2	909	10000000 1010000	1	00001001 01000111 01	0
3	912	10000000 1010000	1	00001001 01001011 00	0
* 4	915	10000000 1010000	1	00001001 01001110 11	0
5	918	10000000 1010000	1	00001001 01100010 10	0
6	921	10000000 1010000	1	00001001 01100110 01	0
* 7	924	10000000 1010000	1	00001001 01101010 00	0
	CLOCK	++++++++ +++++++	+	++++++++ ++++++++ ++	+
	LOAD		+		+

* Non-overlapping channels

Table 2 - Synthesizer Frequency Words for the RDA2

The following process must be followed to load either the Reference Divider Word or the RF Divider Word. Because the control bit indicates which word is being loaded, the order in which the words are loaded is unimportant.

- For each bit in the Synthesizer Divider Word, perform the following steps:
  - Set the SYNDATA line to the next bit of the Synthesizer Frequency Word.
  - Wait for the data setup time (T3).
  - Trigger the SYNCLK line for a duration of T4.
  - Hold the data for a period T9.
- Wait for the load setup time (T6).
- Trigger the SYNLD line for a duration of T5.

Note once again that the Synthesizer Control Lines are programmed through the three bits of the Synthesizer Control Register (WR3).

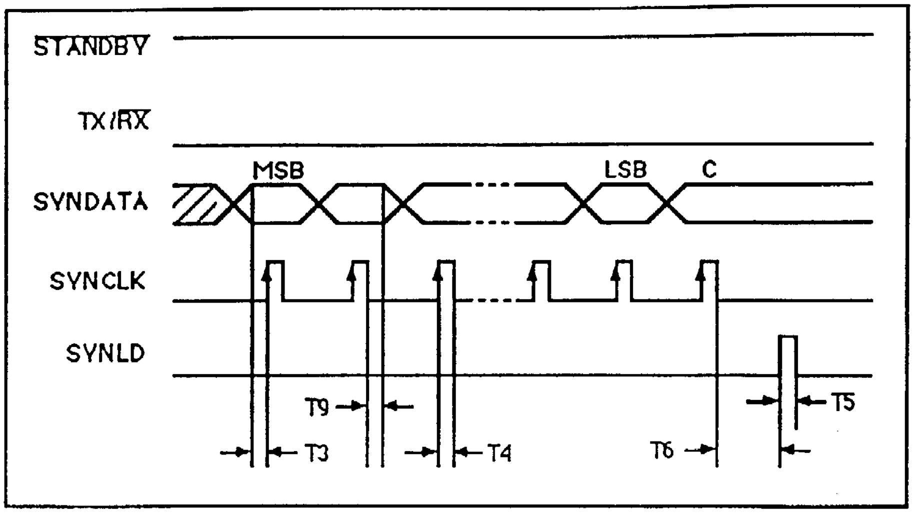


Figure 8 - Serial Data Input Timing

Note that the Reference Divider Word is the same for all transmit and receive frequencies. Therefore, it only needs to be reloaded if the radio is brought out of Standby mode, not when changing between Receive and Transmit modes. Consequently, once the synthesizer has been initialized only the RF Divider Word needs to be loaded during subsequent mode or channel changes.

Also note that the RF Divider Word may be clocked into the shift register at any time. The new RF Divider Word will not affect the radio until the SYNLD line is high and the shift register is loaded into the control register. This allows the radio turn around time to be optimized by loading the RF Divider Word for the next state immediately after raising the SYNLD line for the current state. For example, if the radio is currently in Receive mode and during some idle time the transmit channel was clocked into the shift register, the state could be changed by simply raising the SYNLD line.

4.3.2 Transmit Mode

The following three sections outline the steps necessary to enter the Transmit mode from each of the three modes (including from Transmit mode itself in order to change transmit channels).

4.3.2.1 From Standby Mode

During Standby all the registers in the radio are cleared, therefore, switching to Transmit from Standby requires loading both the Reference Divider Word and the RF Divider Word into the control register. In addition, care must be taken not to supply power to the radio when the transmitter is enabled. The procedure for switching the radio from Standby to Transmit is summarized below.

- Ensure the TX/$\overline{RX}$ line is low so that when power is supplied to the radio, it does not start transmitting at an unknown frequency.
- Raise the $\overline{STANDBY}$ line high.
- Wait for the power supply to stabilize (T2).
- Load the Reference Divider Word into the synthesizer (see section 4.3.1.).
- Load the desired RF Divider Word into the synthesizer (see section 4.3.1.).
- Wait for the synthesizer to stabilize (T7).
- Raise the TX/$\overline{RX}$ line high to activate the transmitter.
- Begin transmitting data (see section 4.4).

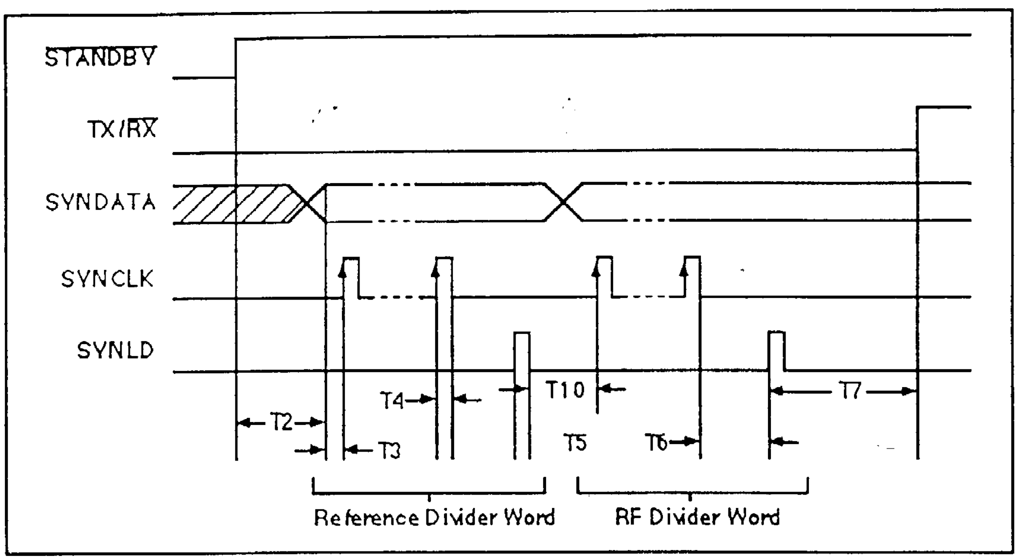


Figure 9 - Standby to Transmit Timing Diagram

For a complete listing of all these timings please see Table 3 in section 4.3.5.

4.3.2.2 From Receive Mode

Switching to Transmit from Receive requires loading the RF Divider Word into the control register. Care must be taken, however, not to set the TX/RX line high until the new RF Divider Word has been loaded and the synthesizer has settled. The procedure for switching the radio from Receive to Transmit is summarized below.

- Load the desired RF Divider Word into the synthesizer (see section 4.3.1.).
- Wait for the synthesizer to stabilize (T8).
- Raise the TX/RX line high to activate the transmitter.
- Begin transmitting data (see section 4.4).

Note that the RF Divider Word may be shifted into the synthesizer at any time. It will not take effect until the SYNLD line is set high. By shifting in the RF Divider Word early, the time necessary to switch channels may be reduced.

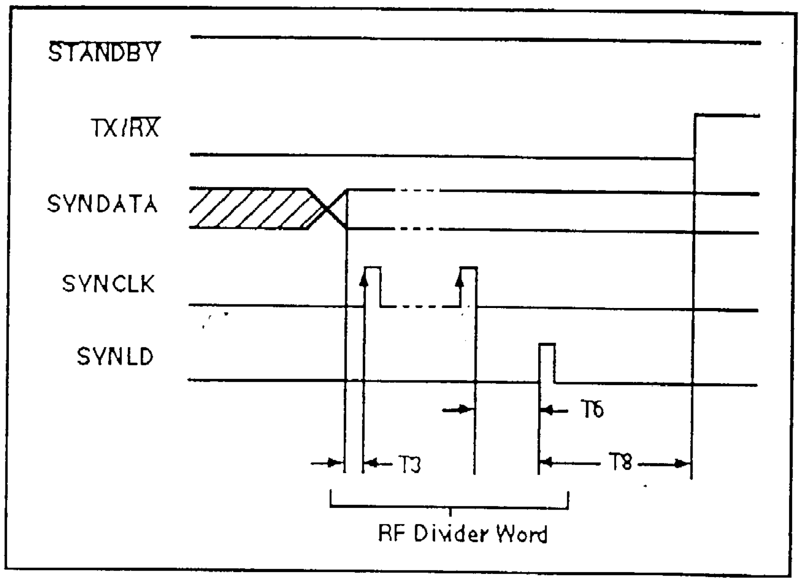


Figure 10 - Receive to Transmit Timing Diagram

For a complete listing of all these timings please see Table 3 in section 4.3.5.

4.3.2.3 From Transmit Mode

Switching to Transmit from Transmit in order to change channels requires that the RF Divider Word be reloaded into the control register. Care must be taken, however, to turn the transmitter off before changing channels. Otherwise, the radio will "splatter" a number of frequencies before reaching the new frequency. The procedure for changing the radio's transmit channel is summarized below.

- Set the TX/$\overline{RX}$ line low to disable the transmitter .
- Shift the new RF Divider Word into the synthesizer (see section 4.3.1.).
- Ensure the transmitter is off (T1).
- Load the new RF Divider Word into the synthesizer, i.e. set SYNLD line high (see section 4.3.1.).
- Wait for the synthesizer to stabilize (T8).
- Raise the TX/$\overline{RX}$ line high to activate the transmitter.
- Begin transmitting data (see section 4.4).

Note that the RF Divider Word word may be shifted into the synthesizer at any time. It will not take effect until the SYNLD line is set high. By shifting in the RF Divider Word early, the time necessary to switch channels may be reduced.

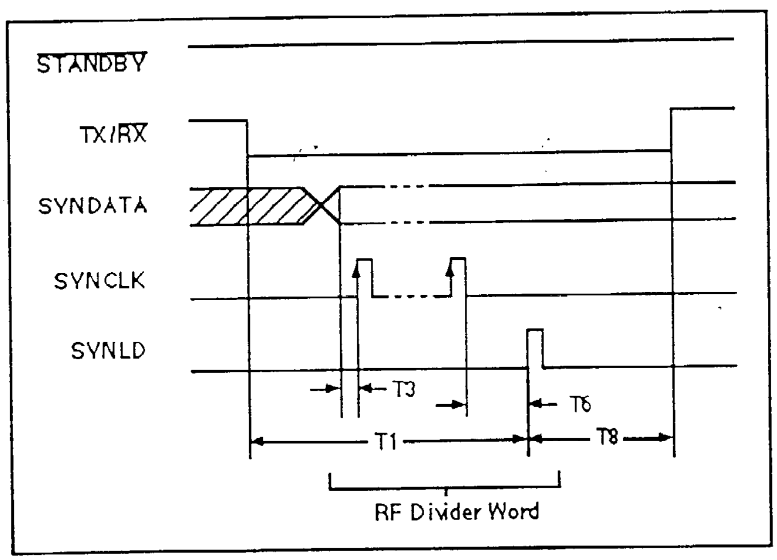


Figure 11 - Changing Transmission Channel Timing Diagram

For a complete listing of all these timings please see Table 3 in section 4.3.5.

4.3.3 Receive Mode

The following three sections outline the steps necessary to enter the Receive mode from each of the three states (including Receive mode itself in order to change receive channels).

4.3.3.1 From Standby Mode

During Standby all the registers in the radio are cleared, therefore,switching to Receive from Standby requires loading both the Reference Divider Word and the RF Divider Word into the control register. In addition, care must be taken not to supply power to the radio without first disabling the transmitter. The procedure for switching the radio from Standby to Receive is summarized below.

- Ensure the TX/RX line is low so that when power is supplied to the radio, it does not start transmitting at an unknown frequency.
- Raise the STANDBY line high.
- Wait for the power supply to stabilize (T2).
- Load the Reference Divider Word into the synthesizer (see section 4.3.1.).
- Load the desired RF Divider Word into the synthesizer (see section 4.3.1.).
- Wait for synthesizer to stabilize (T7).
- Begin receiving data (see section 4.4).

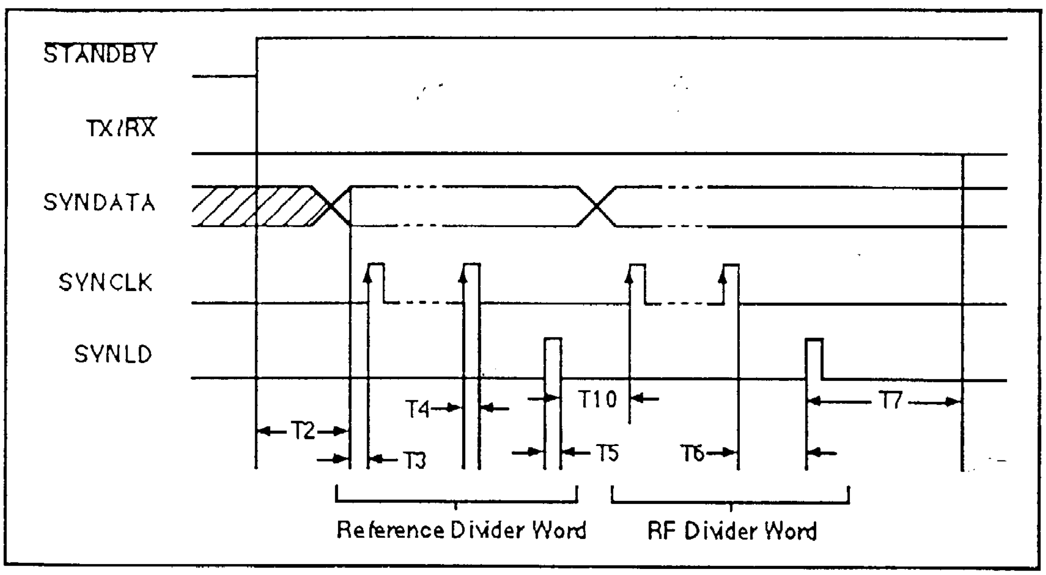


Figure 12 - Standby to Receive Timing Diagram

For a complete listing of all these timings please see Table 3 in section 4.3.5.

4.3.3.2 From Transmit Mode

Switching to Receive from Transmit requires loading the RF Divider Word into the control register. Care must be taken, however, to set the TX/$\overline{RX}$ line low before setting the new frequency. Otherwise, the radio transmitter will "splatter" a number of frequencies before switching into Receive mode. The procedure for switching the radio from Transmit to Receive is summarized below.

- Set the TX/$\overline{RX}$ line low to disable the transmitter.
- Shift the new RF Divider Word into the synthesizer (see section 4.3.1).
- Ensure the transmitter is totally off (T1).
- Load the new RF Divider Word into the synthesizer, i.e. set SYNLD line high (see section 4.3.1).
- Wait for the synthesizer to stabilize (T8).
- Begin receiving data (see section 4.4).

Note that the RF Divider Word word may be shifted into the synthesizer at any time. It will not take effect until the SYNLD line is set high. By shifting in the RF Divider Word early, the time necessary to switch channels may be reduced.

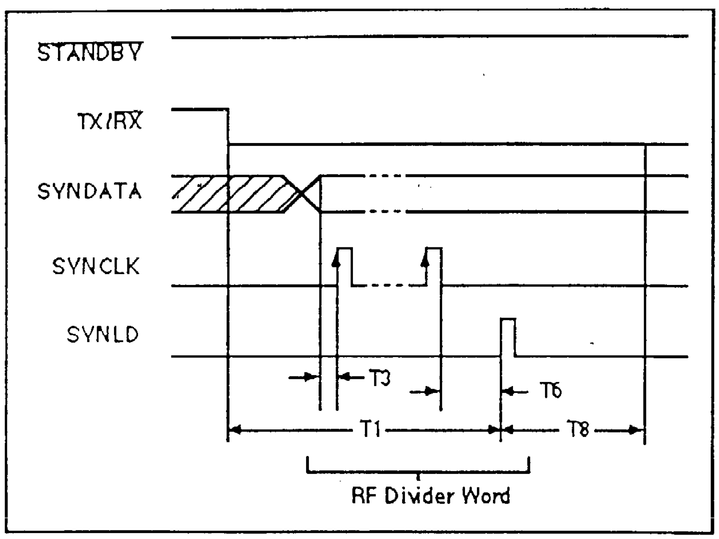


Figure 13 - Transmit to Receive Timing Diagram

For a complete listing of all these timings please see Table 3 in section 4.3.5.

4.3.3.3 From Receive Mode

Going to Receive from Receive in order to change channels requires that the RF Divider Word be reloaded into the control register. The procedure for changing the receive channel is summarized below.

- Load the new RF Divider Word into the synthesizer (see section 4.3.1.).
- Wait for the synthesizer to stabilize (T8).
- Begin receiving data (see section 4.4).

Note that the RF Divider Word word may be shifted into the synthesizer at any time. It will not take effect until the SYNLD line is set high. By shifting in the RF Divider Word early, the time necessary to switch channels may be reduced.

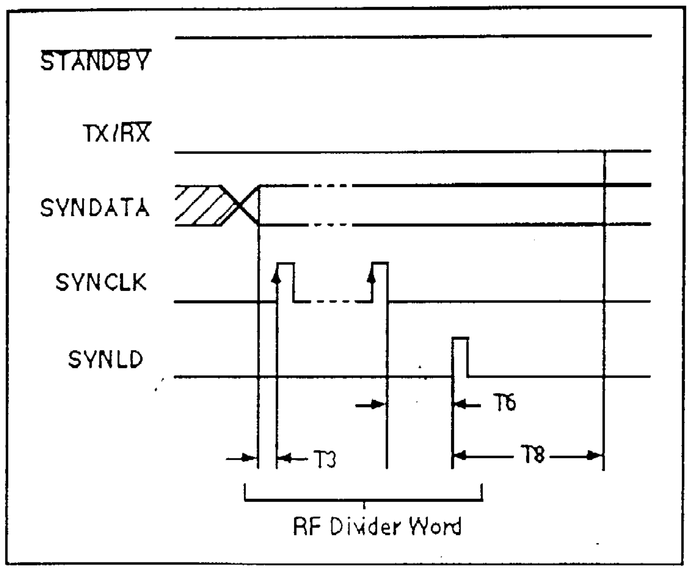


Figure 14 - Receive Channel Change Timing Diagram

For a complete listing of all these timings please see Table 3 in section 4.3.5.

4.3.4 Standby Mode

The following two sections detail the necessary steps to put the radio into Standby mode from either Transmit or Receive mode.

4.3.4.1 From Transmit Mode

When switching the radio into Standby mode, the transmitter must be turned off before enabling the STANDBY line. Otherwise, the radio will "splatter" a number of frequencies before powering down. The procedure for entering Standby mode from Transmit mode is summarized below.

- Set the TX/RX line low.
- Wait for the transmitter to turn-off (T1).
- Set the STANDBY line low.

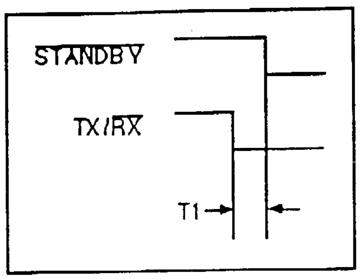


Figure 15 - Transmit to Standby Timing Diagram

For a complete listing of all these timings please see Table 3 in section 4.3.5.

4.3.4.2 From Receive Mode

When switching the radio into Standby mode, the transmitter must be off before enabling the STANDBY line. Because the TX/RX line is already low in Receive mode, all that is necessary to switch the radio into Standby is to set the STANDBY line low.

4.3.5 Radio Timing Chart

The following chart (Table 3) gives the timing values for the timing diagrams presented in sections 4.3.1-4.3.4.

Symbol	Min. Time	Description
T1	50 µs	Transmitter Turn-off
T2	150 µs	Synthesizer Power-up
T3	1 µs	Synthesizer Data Set-up
T4	1 µs	Synthesizer Clock Pulse Width
T5	1 µs	Synthesizer Load Pulse Width
T6	1 µs	Synthesizer Load Set-up
T7	2.5 ms	Synthesizer Settling from Standby (RDA-100/2)
	4.5 ms	Synthesizer Settling from Standby (RDA-100)
T8	800 µs	Synthesizer Settling
T9	1 µs	Synthesizer Data Hold
T10	1 µs	Synthesizer Load Hold

Table 3 - Radio Timing Chart

4.4 Data Interface Timing

This section describes the procedures to be followed to transmit and receive data. The timing diagram in Figure 16 depicts the relationship between the transmitter and receiver during the course of a transmission. The times denoted in the diagram and the relationships suggested will be referred to throughout this section. The timing diagrams and discussion that follows refer to measurements made with two radios communicating between each other.

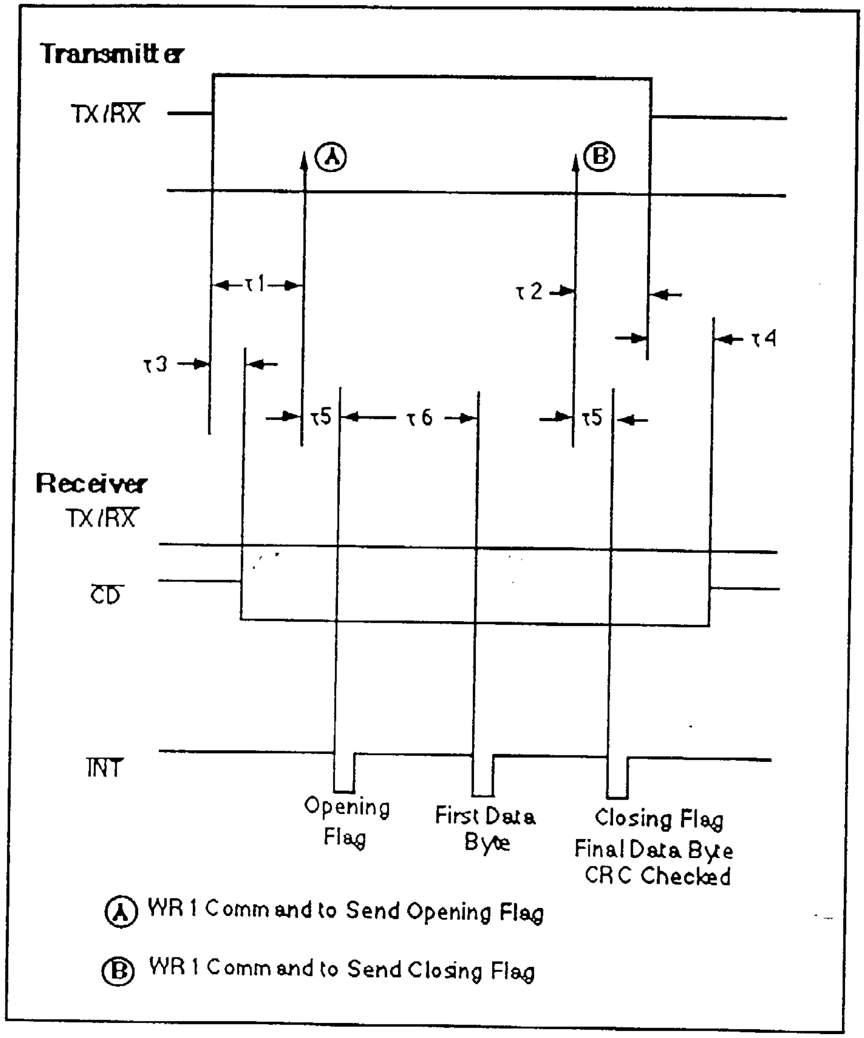


Figure 16 - Data Interface Timing Diagram

The list below enumerates each step the transmitter follows during a data transfer:

- Program the Synthesizer
  Before turning on the transmitter the synthesizer must be programmed to the appropriate frequency (see section 4.3.1). If the synthesizer is not set prior to supplying power to the transmitter, the radio may transmit at the wrong frequency.
- Set TX/$\overline{RX}$ High
  After the synthesizer has settled (see Table 3 in section 4.3.5), the transmit line may be set high. This will turn on the transmitter and start the transmission of the ABORT control character.
- Wait for the Receiver to Detect Carrier
  The transmitter must wait a time $\tau1$ before beginning to send an HDLC packet. This allows the receiver to lock-up to the transmitter.
- Transmit Actual Data
  Transmit a data packet or packets using the parallel interface described in section 4.2.
- Hold Transmitter High
  After the last byte of data or special character has been written, the transmitter must be left on for a time $\tau2$ to allow the data to propagate through the transmitter circuitry.
- Set TX/$\overline{RX}$ Low
  Once the data packet has been transmitted, the transmitter may be turned off. It is important to note that data is still transmitted while the TX/$\overline{RX}$ line is making its transition, and it is advisable to send an ABORT or FLAG character. This will be discussed further from the receiver's perspective.

The list below enumerates each step the receiver follows during a data transfer:

- Program the Synthesizer
  Before receiving data, the receiver must be programmed to the same channel as the transmitter (see section 4.4).
- Wait for Carrier Detect
  $\tau3$ seconds after the transmitter is turned on, the receiver will recognize the RF signal. In order to recognize a signal, it must be on the programmed channel and must maintain the correct spread spectrum signature over a period of time $\tau1$. Once the signature has been established the $\overline{CD}$ line goes low. Because $\overline{CD}$ gates the data, the first several bits of data will be lost while the receiver locks-up. For this reason, the transmitter is required to wait time $\tau1$ before sending actual data.
- Receive Data Packet
  Receive a data packet or packets using the parallel interface described in section 4.2. A data packet consists of an opening FLAG, a series of data bytes, a two-byte CRC and a closing FLAG.

The following table gives the interface clock timings discussed throughout section 4.4.

Symbol	Minimum	Maximum	Description
$\tau 1$	330 µs		Transmitter setup time
			Scrambler flush time
$\tau 2$	170 µs		Transmitter hold time
$\tau 3$	300 µs		$\overline{CD}$ lock-up time
$\tau 4$	70 µs	120 µs	$\overline{CD}$ release time
$\tau 5$	165 µs	248 µs	Data propagation delay
$\tau 6$	247 µs	322 µs	Delay for first data byte

Table 4 - Data Interface Clock Timings for the RDA

Symbol	Minimum	Maximum	Description
$\tau 1$	250 µs		Transmitter setup time
			Scrambler flush time
$\tau 2$	85 µs		Transmitter hold time
$\tau 3$		235 µs	CD lock-up time
$\tau 4$	35 µs	60 µs	CD release time
$\tau 5$	82 µs	124 µs	Data propagation delay
$\tau 6$	124 µs	161 µs	Delay for first data byte

Table 5 - Data Interface Clock Timings for the RDA2

5 Performance Verification Testing

This section contains information needed to verify the radio's performance. Included are the test equipment requirements, a test setup diagram, and a step by step procedure for all the pertinent performance tests. Refer to Figure 17 throughout this section for test setup criteria. The configuration of the measurement instruments will be described when appropriate; familiarity with the equipment is assumed.

To perform these tests, it is necessary to use the radio in serial mode. Note that the channels for the RDA and the RDA2 are programmed differently, so a different test set-up must be used with each of these data rate configurations.

5.1 Equipment List

Table 6 details the test equipment recommended for the Performance Verification Tests. This list identifies the type of equipment required and a possible model. Other vendors and models may be used.

Description	Vendor	Model #
Digital Volt Meter	Fluke	87
Digital Volt Meter	Fluke	75
Power Meter	Hewlett-Packard	437B
Power Splitter	Mini-Circuits	ZFSCJ-2-4
Power Sensor	Hewlett-Packard	8481H
Synthesized Signal Generator	Hewlett-Packard	8660C
Modulator Section	Hewlett-Packard	86632B
RF Section (1-2600MHz)	Hewlett-Packard	86603A
Pulse Generator	Hewlett-Packard	8012B
Pattern Generator / Error Detector	Hewlett-Packard	3780A
Attenuator (110 dB)	JFW Industries Inc.	50BR-009
Coax fixed attenuator 10dB	Solitron Microwave	929-6200-10
Power Supply (1.0 Amps)	Leader	LPS-152
Oscilloscope (100MHz)	Tektronix	2245A
Spectrum Analyzer	Tektronix	494P

Table 6 - Test Equipment Requirements

5.2 Equipment Setup

The Bit Error Rate Tester (BERT) model HP3780A is used as the data source as well as the data receiver. When testing receiver functions, the data source is clocked by the REF Radio's TXCLK line and drives the REF Radio's TXDATA line. The DUT's RXDATA and RXCLK lines connect to the BERT's received data and clock inputs. It should be noted that since the BERT's input impedance is 75 ohms, the radio's HCMOS outputs cannot directly drive the BERT's input lines. A series 500Ω resistor should be added to each the radio's TXCLK, RXCLK and RXDATA lines before going into the BERT.

The DUT output can be connected to a power meter for output power measurements or to a power splitter. The splitter serves two purposes. First, it allows the spectrum analyzer to monitor the DUT output when transmitter measurements such as modulation BW are made. The splitter also monitors the DUT input when testing its receiver functions. In this mode, the spectrum analyzer serves as a reference as it sees exactly the same signal the receiver sees.

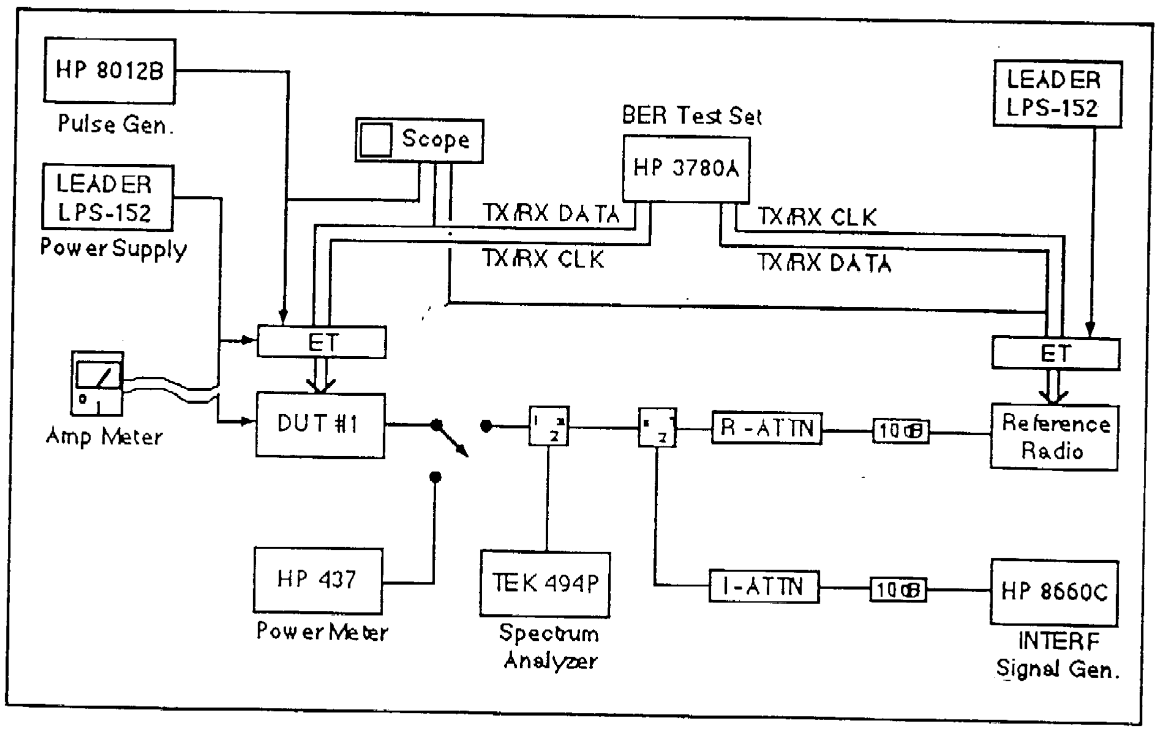


Figure 17 - Test System Setup

NOTE: It is recommended that a fixed 10dB attenuator always be used in series with the INTERF Radio and the REF Radio to keep from accidentally over-driving the DUT's input.

A second power splitter allows the injection of an interfering signal from the Interference Signal Generator. This is used when testing some of the DUT's receiver characteristics such as adjacent channel rejection, interference rejection and image rejection. The step attenuator in series with the Interference Signal Generator (ISG) is used to set the relative level of the interfering signal. In order to make the ISG simulate another RDA family radio, its internal FM modulation (1 KHz) is enabled. Setting the deviation to 1.3 MHz peak-to-peak produces an interfering signal with characteristics very similar to an RDA series radio, occupying approximately the same channel bandwidth.

Finally, an oscilloscope monitors the RX/TX Data lines of both radios, as well as the TX/$\overline{RX}$ line of the DUT to derive timing relationships. Power supply currents are measured with an Amp Meter in series with the 5v supply line. A Digital Volt Meter is also used to monitor DC voltages at several test points within the radio.

5.3 Main Performance Tests

5.3.1 Power Output

After correctly zeroing and calibrating the power meter, connect it directly to the output of the DUT. Place the radio in transmit mode, select the desired frequency and measure the power. Power should be measured within 1 sec of placing radio in transmit mode.

5.3.2 Bit Error Rate (BER)

After selecting the desired operating frequency place the REF Radio in transmit mode. Connect the REF Radio TXDATA and TXCLK lines to the BERT's transmit data output and transmit clock input respectively. Place the DUT in receive mode and connect its receive lines to the BERT. Connect the input of the DUT to the power splitter. Set up the BERT as follows: PRBS n=9, Frequency=Ext, BER=10^6, Measurement= Binary, CK=Ext and Data Threshold=200 mv.

This basic setup will be used throughout the remaining performance tests. The radio is defined to be functioning properly if its BER is less than 1E-5 under the conditions being tested. These conditions are defined in the following sections.

5.3.3 Sensitivity

Setup for a BER measurement. Set I-attenuator to maximum (make sure the Interference Signal Generator is off). Set R-attenuator so that the received signal level as measured with the spectrum analyzer is -40 dBm (1 MHz resolution BW should be used whenever making power measurements with the spectrum analyzer). Increase attenuation by 40 dB. The signal into the DUT should be -80 dBm. Make a BER measurement. Increase attenuation by 1 dB and repeat the measurement until the BER is above 1E-5.

NOTE: Whenever making a sensitivity measurement, the REF Radio and associated ET Board should be isolated from the DUT to keep radiation from the REF Radio from skewing the sensitivity measurement. This may happen when radiated emissions arrive at the DUT at higher levels than the cabled transmission. Isolation can be accomplished by enclosing the REF Radio in a shielded box (metal). Ferrite beads should be used on all lines coming into or out of the box. Equivalent isolation can be achieved by separating the REF Radio from the DUT by a distance of 30 feet or more. Again, ferrite beads should be used on all lines coming from the REF Radio.

5.3.4 Dynamic Range

Setup for a BER measurement. Set R-attenuator so that the received signal level as measured with the spectrum analyzer is -40 dBm. Remove attenuation until the measured BER increases above 1E-5 or all attenuation has been removed. At this point measure received signal power level on spectrum analyzer. The difference between this measurement and the sensitivity measurement performed previously, is the Dynamic Range of the radio.

5.3.5 Carrier Frequency

Set the DUT to Transmit mode. Select DUT's desired operating frequency and set the spectrum analyzer's center frequency to the same value. Measure the radio's frequency by activating the analyzer's built-in frequency counter.

5.3.6 Modulation BW

Set the DUT to Transmit mode. Set the spectrum analyzer to 2dB/div, a 500 KHz/div span, a 100 KHz resolution BW (this is the only measurement in which the spectrum analyzer's resolution BW is not 1 MHz). Set its center frequency to the DUT's frequency. Adjust the spectrum analyzer's reference level to bring the peak of the modulation spectrum to the top of the screen. Measure the bandwidth 3 divisions down this point.

5.3.7 Processing Gain

Processing Gain can be defined as the modulation BW divided by the information rate (data clock rate in our case). This number can be converted to decibels using the following formula: PG = 10 x LOG (BW / R).

5.3.8 Data Clock Rate

Guaranteed by design.

5.3.9 Emissions outside [902-928] MHz band

5.3.9.1 Harmonic Distortion

Set the DUT to Transmit mode. Tune the spectrum analyzer to the DUT frequency and measure the peak power level (remember to use 1MHz resolution BW). Now tune the spectrum analyzer to twice the radio frequency and measure the peak power level again. The difference between these two measurements is the relative emission level of the second harmonic in dBc. Repeat this process for the third harmonic.

5.3.9.2 L.O. Leakage

Set the DUT to receive mode. Tune the spectrum analyzer to the DUT's frequency plus 44 MHz and adjust the spectrum analyzer's reference level until the L.O. leakage is clearly distinguishable above the noise floor. Measure the peak power level in dBm.

5.3.10 Power Consumption

Power consumption for the DUT is measured with an Amp Meter in series with the +5V supply. Measure the power consumption on the 5V line in Transmit, Receive and Standby modes. The measurements are made by setting the DUT to the desired mode and measuring the current with an amp meter on the desired line.

5.4 Supplementary Characteristics Test

5.4.1 Undesired Signal Rejection

Undesired signal rejection is a measure of how large an undesired signal the radio can tolerate while maintaining a BER of less than 1E-5. These measurements should be performed at received signal level of -75 dBm.

Setup the DUT for a BER measurement. Select the desired frequency of operation. Set the R-attenuator until the received signal level measured at the spectrum analyzer is -45 dBm. Set the Interference Signal Generator (ISG) to the desired frequency (this frequency will vary depending on whether interference, image or adjacent channel rejection is being measured).

Set the I-attenuator to 75 dB and adjust the ISG level until the spectrum analyzer measures the same interference level as that of the DUT. Add 30 dB of attenuation to both the R- attenuator and the ISG. The desired and interfering signal levels should now be -75 dBm. Set the ISG to internal frequency modulation at 1 KHz and 1.3 MHz of deviation. Take out I-attenuation until the BER increases above 1E-5. Subtract the I-attenuation value from 75. The result is the interference, image or adjacent channel rejection figure in dBc. Each of these three measurements will cover specific interfering frequencies which are described in the following sections.

5.4.1.1 Adjacent Channel Rejection

Set the ISG's frequency to the adjacent channel to be measured (i.e. one of 906,912,918 or 924 MHz) and proceed to measure rejection as described above.

5.4.1.2 Interference Rejection

Set the ISG's frequency the same as the DUT and proceed to measure rejection as described above. Note that in this case I-attenuation will most likely have to "increase" by 1 to 4 dB reflecting a negative rejection figure. Also, make sure the DUT level and the ISG level are as close to -75 dBm as possible. It is a good idea to recheck the levels with the spectrum analyzer after the 30 dB of additional attenuation are added.

5.4.1.3 Image Rejection

Set the ISG's frequency to the image frequency; that is 88 MHz above the DUT's frequency. Proceed to measure rejection as described above.

5.4.2 Receiver Turn-on Time

Setup for a receiver sensitivity test. Set the attenuation for a received signal strength of -75 dBm. Drive the DUT TX/$\overline{RX}$ line with a pulse generator. The pulse generator should be set to output an HCMOS level pulse of 20 msec period and 50% duty cycle. With the oscilloscope monitor the DUT's TX/$\overline{RX}$ line and its RXDATA line. Set the pattern generator to an all "0" pattern.

Triggering the oscilloscope on the TX/$\overline{RX}$ line's negative edge, measure the time it takes the RXDATA line to settle to the all "0" state. This is the receiver's turn-on time (note that while in transmit mode, the radio sets the RXDATA line to its high state).

5.4.3 Transmitter Turn-on Time

Setup for a transmitter measurement test. Set the attenuation for a received signal strength of -20 dBm. Drive the DUT TX/$\overline{RX}$ line with a pulse generator. The pulse generator should be set as it was for the receiver turn-on time test. With the oscilloscope, monitor the DUT's TX/$\overline{RX}$ line and the REF Radio's RXDATA line. Once again, set the pattern generator to an all "0" pattern.

Triggering the oscilloscope on the DUT's TX/$\overline{RX}$ line's positive edge, measure the time it takes the RXDATA line to settle to the all "0" state. This is the transmitter's turn-on time.

5.4.4 Transmitter Turn-off Time

With the same setup used in transmitter turn-on time, now trigger the oscilloscope on the DUT's TX/$\overline{RX}$ line's negative edge. You will observe that the REF Radio's RXDATA line will still be receiving zeros for a time after the transmitter is instructed to turn off. Once the transmitter is completely off, the REF Radio will be receiving noise only and the RXDATA line will begin to jump. The time elapsed between the transition on the TX/$\overline{RX}$ and the first jump on the RXDATA line is the transmitter turn-off time.

5.4.5 Receiver Turn-on Time

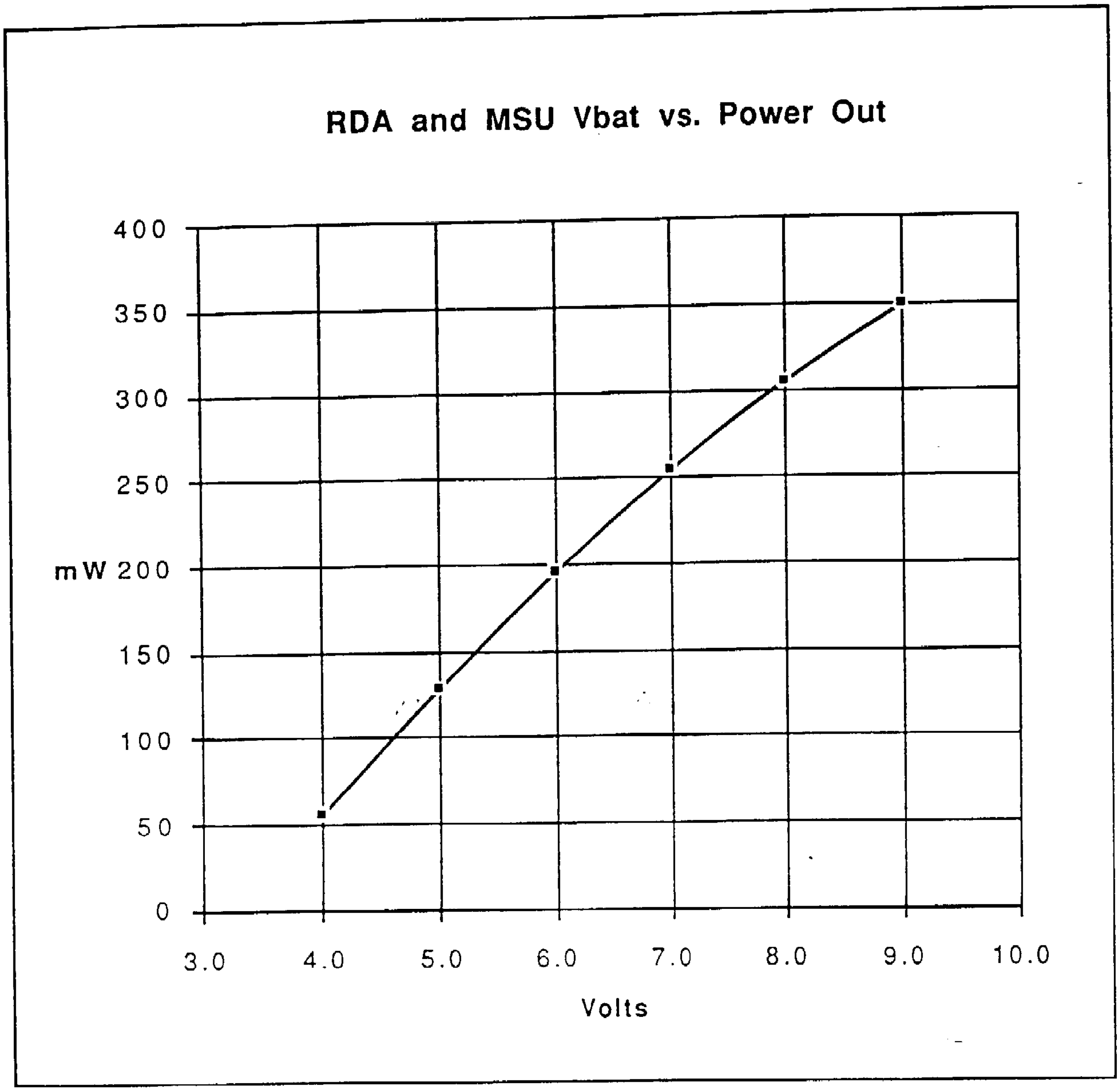
Setup for a receiver sensitivity test. Set the attenuation for a received signal strength of -75 dBm. Drive the DUT $\overline{STANDBY}$ line with a pulse generator with a 20 msec period and 50% duty cycle. With the oscilloscope monitor the DUT's $\overline{STANDBY}$ line and its RXDATA line. Set the pattern generator to an all "0" pattern.

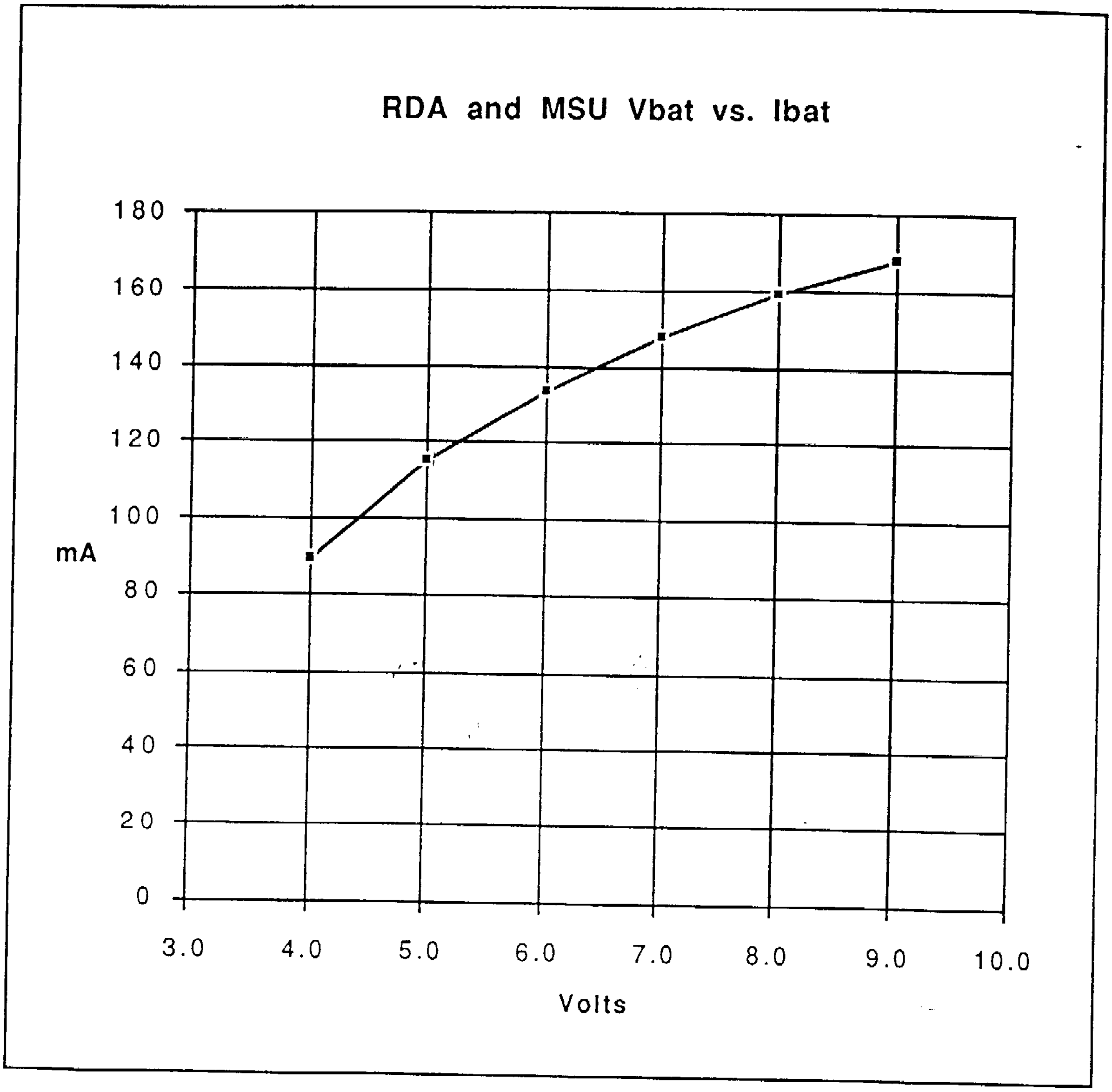
Triggering the oscilloscope on the $\overline{STANDBY}$ line's positive edge, measure the time it takes the RXDATA line to settle to the all "0" state. This is the receiver's turn-on time.

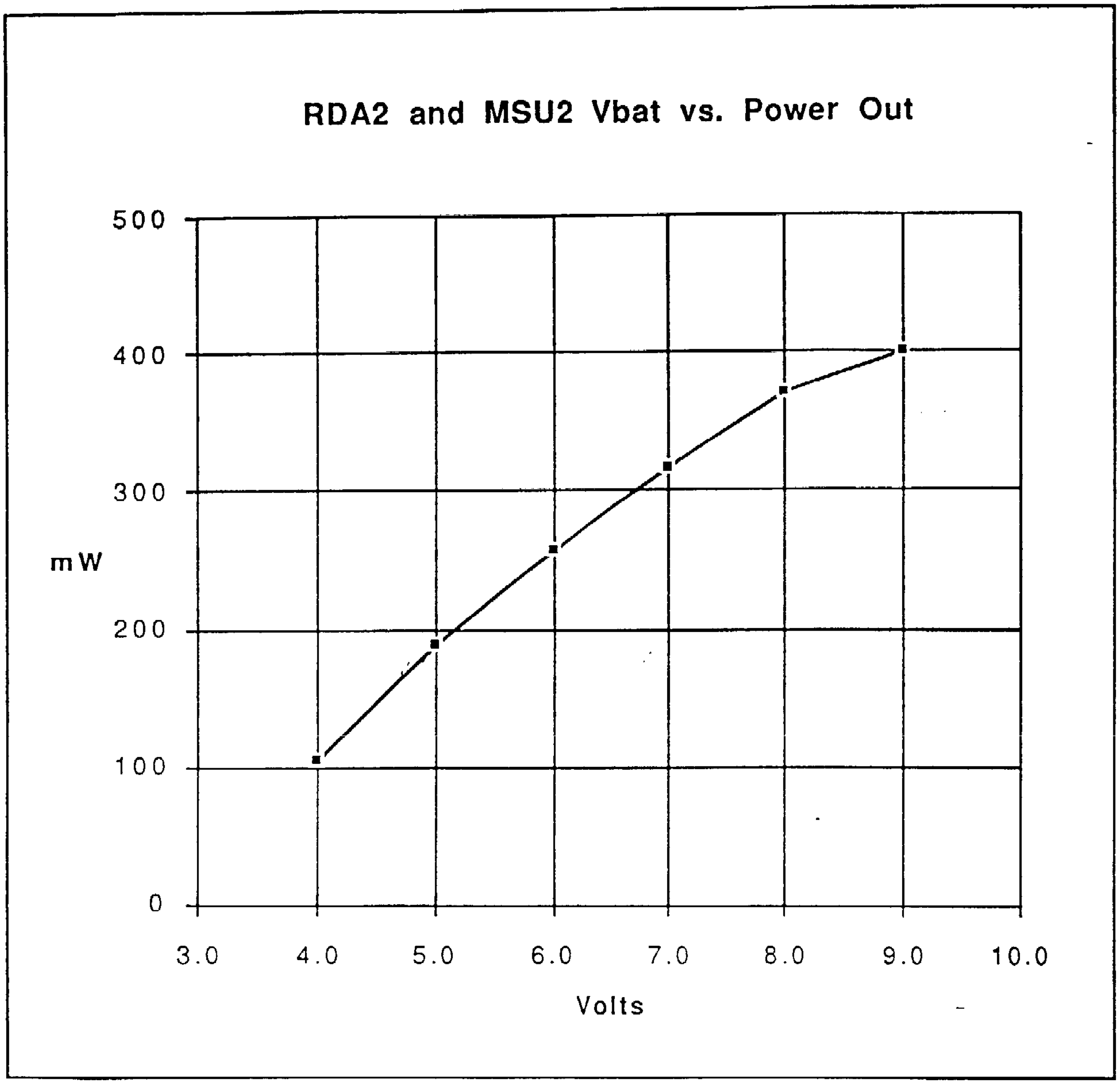
5.4.6 RSSI

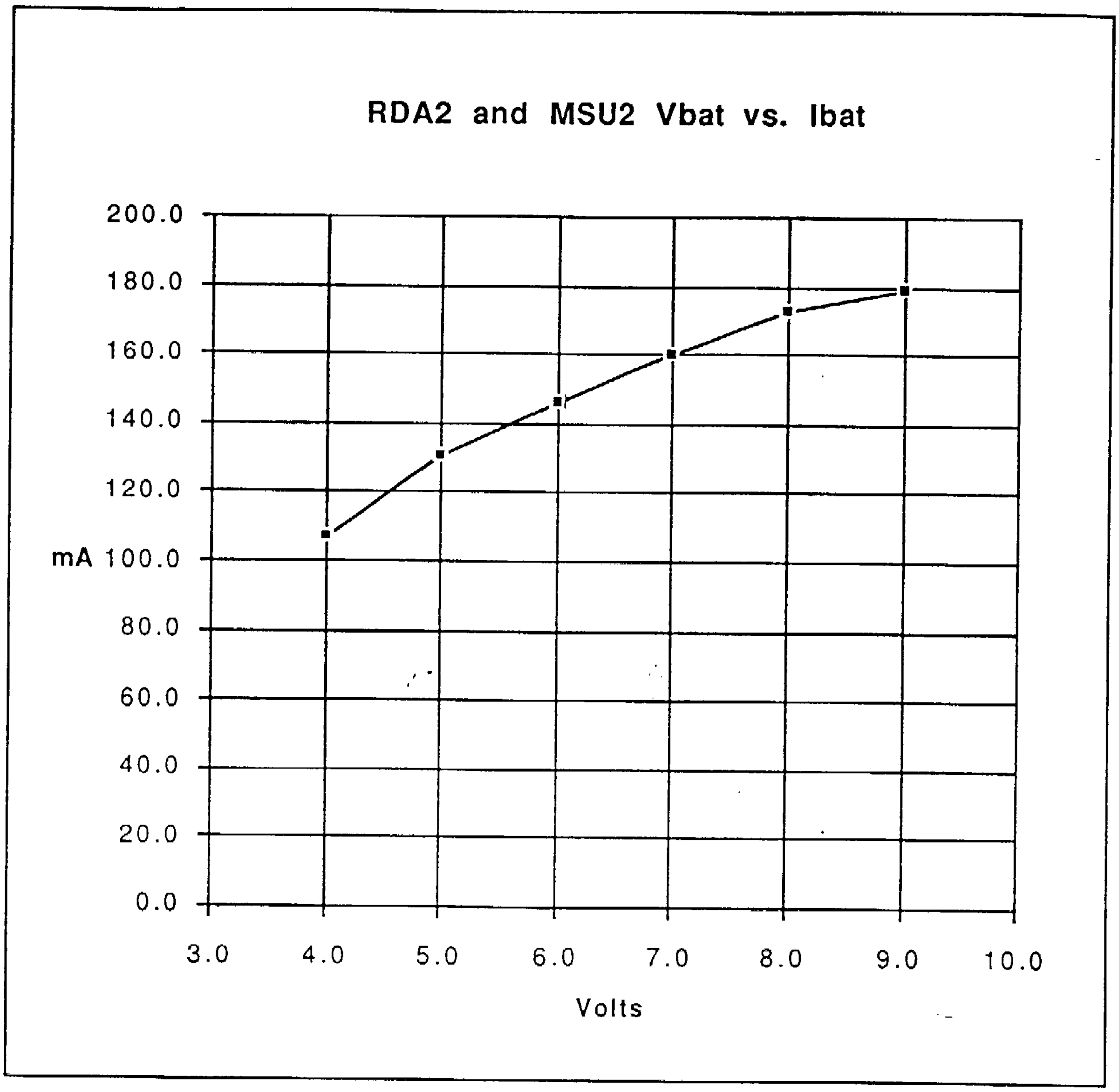
Received Signal Strength Indicator voltage varies monotonically between about 1V and 4V for input signal level variations between -100 dBm and -30 dBm. To measure the characteristics of this curve first setup for a receiver measurement test. Then adjust attenuation until received signal level is -30 dBm as indicated by the spectrum analyzer. With a DVM measure the DC voltage at the test point labeled RSSI. Repeat this measurement for all desired levels of input signal.

Addendum A-Vbat vs. Power Out and Ibat Graphs




RDA and MSU Vbat vs. Ibat
180
160
140
120
100
mA
80
60
40
20
0
3.0
4.0
5.0
6.0
7.0
8.0
9.0
10.0
Volts


RDA2 and MSU2 Vbat vs. Power Out
500
400
300
200
100
0
mW
3.0
4.0
5.0
6.0
7.0
8.0
9.0
10.0
Volts


RDA2 and MSU2 Vbat vs. Ibat
200.0
180.0
160.0
140.0
120.0
mA 100.0
80.0
60.0
40.0
20.0
0.0
3.0
4.0
5.0
6.0
7.0
8.0
9.0
10.0
Volts