# Z-Card 210
# Theory of operation 1.0
# December 22,1999

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## 1.0 Purpose

The purpose of this document is to provide a detailed description of the circuitry that makes up Z SQUARE'S product

## 2.0 Introduction

Appendix A presents the block diagram of Z SQUARE'S radio.

The radio transceiver provides full-duplex operation with a transmitter architecture employing vector modulation of an offset loop oscillator and a receiver utilizing a dual-conversion, heterodyne architecture. The radio is designed to meet the CDPD specifications and comply with FCC regulations. The radio is controlled by the Ruby II. Communication Processor. It also passes signals to and from the Topaz radio interface IC, and transmits and receives radio signals between the MDBS over the airlink interface.

The Z SQUARE'S Radio provides vector controlled modulation. The radio interface has a radio On/Off Control which is controlled by the Topaz CDPD Radio Interface Chip Port registers. It will control the power to the receiver chain and transmitter chain independently. The radio TX Power is controlled by the Topaz CDPD Radio Interface Chip TX Power D/A. The Ruby II Serial Controller is used to control the radio channel select synthesizers with configuration and synthesizer commands.

## 3.0 Radio Theory of Operation

## 3.1 Receiver Operation

The receiver architecture of the radio is a typical double conversion super-heterodyne receiver. The block diagram of the receiver architecture is presented in Appendix A. It is also beneficial to relate the following information to the schematic diagram presented in appendix A.

The power supply to the receiver chain is controlled with the PWRON line. A high voltage(>3.0V) enables the RF front end, the IF down converter /demodulator IC, the dual PLL IC, the TCXO, both the 1st LO and 2nd LO (128.16 MHz discrete design), and the voltage regulator which maintains voltage stability to the oscillators. A low voltage(<0.5V) to the PWRON line disables the power supply to the circuitry mentioned above.

In the receive path an antenna is connected to the duplexer which filters out the receive band between 869 and 894 MHz. The duplexer provides 50 dB isolation between the transmit and receive frequencies. The duplexer is followed by a low noise amplifier and a mixer IC. Between the LNA and mixer is an image reject filter.

The 1st LO ranges in frequency from 952.20-977.13 MHz in 30KHz steps and is used to drive the mixer that downconverts the received signal to a first . IF frequency of 83.16 MHz(IF1,). The input level to the mixer is at -9 dBm $\pm 3$ dB. This LO is generated by phase locking a voltage controlled oscillator to a temperature compensated crystal oscillator with the dual PLL IC. This ensures the accuracy of the down converted signal to be within $\pm 2.5$ PPM (over temperature and voltage variation )of the 1st LO frequency. The inaccuracy of the second LO is insignificant since it is oscillating at a much lower frequency. The accuracy of the 1st LO is important with respect to the transmitted signal since this same LO is used to generate the transmit signal also.

Following the 83.16 MHz IF filter is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, a quadrature detector, a logarithmic received signal strength indicator(RSSI) with fast rise and fall time, and a voltage regulator receives the 83.16 MHz signal, down converts it to 455 KHz, amplifies it into limiting to strip off any AM components and then demodulates the remaining FM signal . The signal is taken off chip for two stages of IF filtering by two 455 KHz CERAMIC FILTERS WITH 30 KHz of bandwidth. U2 also generates the RSSI voltage.

The demodulated output can be used as either a single ended or differential signal depending on assembly procedures. In the single ended mode the demodulated signal is
present on RXPOS and the OFFDAC signal is looped back on the RXNEG connector pin so that the OFFDAC signal is used as the comparator voltage for the received data. In the differential mode the received data is present on both the RXPOS and RXNEG connector pins $180^{o}$ out of phase. In this configuration the OFFDAC line is used to control the center frequency of the demodulator tank circuit so that voltage offsets between the differential receive signals can be eliminated.

## 3.2 Transmitter Operation

The transmitted signal from the radio is generated by mixing a low frequency vector modulated signal($2^{nd}$ LO)at 128.16 MHz with the $1^{ST}$ LO. The $1^{st}$ LO is the same one described in the receiver discussion above. The $1^{ST}$ LO has it's power divided in two so that 1/2 the power can

be used to generate the transmitted signal. Both the 128.16 MHz signal and the 1ST LO are phase locked to the TCXO(U6). A copy of the data sheet for the TCXO can be found in appendix A. Phase locking to the TCXO ensures that the output frequencies of the two PLL's are accurate to within ± 2.5 ppm of their respective frequencies and hence the transmitted signal is within ±2.5 pm of its intended frequency over both temperature and voltage variations. The block diagram of the transmitter chain is presented in Appendix A.

**(The 128.16 MHz 2nd LO is derived from a VCO circuit locked by 15.36MHz TCXO. It drives the Quadrature Modulator (U8). Inside the Modulator, the 2nd LO is first multiplied by 2 to get 256.32MHz, then divided by 2 to obtain 0° and 90° orthogonal quaternary signals. Hese signals are modulated by I & Q signals respectively as shown in figure. The I & Q are 19.2Kbps signals generated by D/A converter according to MSK characteristics and GMSK filter (BT=0.5). The modulation index is 0.5. The peak frequency deviation is 4.8KHz.**

**After modulation, the IF signal will pass a 128MHz SAW bandpass filter to reject spurious noise and mix with RFLO to RF band. The Tx signal is offset 45MHz with Rx band.)**

The output of the transmitter is controlled by two different methods. The TXON line controls power supply to the transmitter chain . A high voltage(>3.0V) enables the quadrature modulator and upconverter(U8), and amplifier(U9,U10,U11). A low voltage(<0.5V) to the TXON line disables the power supply to the circuitry mentioned above. By disabling this circuitry there is no RF input to the power amplifier, therefore, there is no transmitted signal power .

The 2nd LO is a 128.16 MHz VCO that is phase locked to the 15.36 MHz TCXO. This is used to drive a quadrature modulator. The carrier input to is quadrature modulated by differential I & Q signals IPOS/INEG and QPOS/QNEG. The modulating signal is a GMSK at 19.2 KBPS±50 ppm with BT=0.5 and H=0.5±5%. These modulation characteristics which are generated by the TOPAZ baseband solution ensure that the adjacent and alternate channel emissions spectrums will be well within the emission specifications set forth by FCC regulation. A bit value of lis represented by an instantaneous frequency which is greater than the carrier center frequency and a bit value of 0 is represented by a frequency that is less than the carrier center frequency. The peak carrier deviation as a result of this modulation is 4.8 KHz.

The output of the 128.16 MHz modulator is filtered by a low pass filter to eliminate harmonics before the signal reaches the upconverter. This filter substantially reduces the level of spurious signals that reach the power amplifier. The 128.16 MHz signal is then upconverted in U8 with the resulting output offset 45 MHz below the received frequency. The output of the mixer is amplified, filtered and routed to the Power amp. A data sheet for the filter is presented in

appendix A. The filter performs two functions. It is used to filter out the 1 ST AND 2nd LOs MxN mixing products generated in the upconverter and it also filters out the phase noise of the transmitted signal that falls in the receive band. It is necessary to filler the phase noise or it will desensitize the receive signal during transmission.

The filtered signal is then amplified to 1.2 W max by a high gain/high efficiency power amplifier Two stage power amplifier. A copy supply input and typically draws 750 mA, when the PLC line sets the power output to maximum. When the PLC line is set to transmit at the lowest power level(+8dBm). the power amplifier typically draws 155 mA. The level control control circuit maintains the RF power at a specific level controlled by the PLC input voltage. The PLC signal accurately controls the output power levels that correspond to the CDPD class III output levels by controlling the bias voltages of the two stages of amplification with the power amplifier. By controlling the bias voltages of each stage the current is controlled. After passing through the duplexer to the antenna, the remaining power is .6 W max. The duplexer attenuates the hamonics of the transmitted signal and it also increases the attenuation of the transmitted signals phase noise in the receive band.