

Circuit Description for 841.829 (Grand Phone)

This is a 900MHz Band cordless telephone for domestic use. Radio transmitter with FM technology provides greater mobility to the user within approximately 200 meters radius around the base.

Following paragraphs describe the detail of major building blocks.

1. Ringer Detection

a. Base

Incoming ringer signal is first attenuated by C39,Z2,Z6,R10 and Q14. The signal is then feed to micro-controller (MCU) U2 for generating response signal according to the setting of inputs and sends digitally coded information to handset via RF link.

b. Handsets

When digitally coded information is received from the base it will be decoded at MCU U1. Then necessary ringer is generated and applied to Q11, which drive the Buzzer BZ1.

2. Surge protection

The surge absorber V1 is mounted in the Base unit. It designed to operate when voltage over 330V. In general it is common to have induced surges in the telephone line due to lightening. If it allow entering the unit damage to the unit is imminent. The line interface, fuse and ringer detected circuit is most venerable to high voltage surges and V1 surge absorber can prevent it.

3. Line control

When the unit is operated by remote handset, line control is done by MCU. It turns on transistor Q11,Q10. Then telephone line power feeds to line interface circuit (Q8,Q9), turn on the telephone line and internal voice path, and around component.

4. Power Control

a. Base unit

The main power is come from AC/DC adaptor, which provide 9V DC to

the unit. Radio part, MCU and line interface related circuit is supplied with non-backup regulated 5V voltage..

b. Handset

Three cells of battery(3.6V) provided necessary power to the handset. In order to keep power consumption to minimum, the radio receiver is turn on and off periodically by MCU and Q1. The MCU is supplied with regulated 3.6V by U3.

c. Charger

Power is provided by an external 9V adaptor. There is 1 socket for charging. When the handset is placed on the cradle, the charging terminals of the base and handset units contact each other. And then it can start to charge the battery.

5. Security Code

The security code contains 16 bits of data, which makes of 65535 combinations. Security code is changed (randomly) once only when the handset is on cradle after the base first power up. Unless the base is cold-boot again, which means the base loss power to around 2.9V and then insert power again, the security code of handset and base remain no change.

6. Radio Module

a. RF general

Both handset and base use 900MHz analogue radio that transmits and receive signal in full duplex mode. Audio and data signal is FM modulated before transmitting from the module. The radio module is fully cover with shield plate in order to minimize interference to other equipment.

The RF module consists of transmit and receive paths. The transmit path uses direct modulation architecture such that the audio signal directly modulates on the VCO. The receiver side uses super heterodyne architecture such that the RF signal is down-converted to IF frequency 10.7MHz and then demodulated to audio signal by FM discriminator.

The whole RF system is composed of one antenna, one antenna supporting PCB, and one RF module integrated together by soldering. Antenna is immovable, and made of the white copper wire with 0.8mm diameter.

b. Transmitter

The audio signal from telephone line is firstly compressed by compander and the compressed signal is then amplified and pre-emphasized in Baseband.

As the amplitude of the signal determines the FM frequency derivation, the amplitude is controlled by the potential divider before modulating the Tx VCO in PLL IC and VCO circuit. If channel 20 is selected, the Tx VCO is locked at Base:903.75MHz/ Handset:926.25MHz Once the signal enters the Tx VCO, Tx VCO frequency derivatives with the analog signal giving FM modulation. The FM signal is transmitted out to Antenna through the amplifier and filter.

c. Receiver:

The transmitted signal from the Handset is received at the receiver in RF module.

If channel 20 is used, the received signal is at Base926.25MHz/

Handset:903.75MHz while the Rx VCO inside the transceiver is locked at

Base:936.95MHz/ Handset:893.05MHz the two frequencies are then mixed by the mixer inside the transceiver giving 10.7MHz IF. To increase adjacent channel rejection, two IF filters are used to filter the 10.7MHz signal. This filtered 10.7MHz IF is then further down-converted to 455kHz by the mixer inside the FM detector IC. Finally the audio signal can be discriminated out from the 455kHz signal by the FM detector.

Lastly, the demodulated audio signal is de-emphasized and decompressed in baseband.

900MHz FREQUENCY TABLE (WIDE BAND)

| CH | HAND | | | BASE | | |
|----|--------|--------|--------|--------|--------|--------|
| | TX | RX | LOCAL | TX | RX | LOCAL |
| 1 | 925.30 | 902.80 | 892.10 | 902.80 | 925.30 | 936.00 |
| 2 | 925.35 | 902.85 | 892.15 | 902.85 | 925.35 | 936.05 |
| 3 | 925.40 | 902.90 | 892.20 | 902.90 | 925.40 | 936.10 |
| 4 | 925.45 | 902.95 | 892.25 | 902.95 | 925.45 | 936.15 |
| 5 | 925.50 | 903.00 | 892.30 | 903.00 | 925.50 | 936.20 |
| 6 | 925.55 | 903.05 | 892.35 | 903.05 | 925.55 | 936.25 |
| 7 | 925.60 | 903.10 | 892.40 | 903.10 | 925.60 | 936.30 |
| 8 | 925.65 | 903.15 | 892.45 | 903.15 | 925.65 | 936.35 |
| 9 | 925.70 | 903.20 | 892.50 | 903.20 | 925.70 | 936.40 |
| 10 | 925.75 | 903.25 | 892.55 | 903.25 | 925.75 | 936.45 |
| 11 | 925.80 | 903.30 | 892.60 | 903.30 | 925.80 | 936.50 |
| 12 | 925.85 | 903.35 | 892.65 | 903.35 | 925.85 | 936.55 |
| 13 | 925.90 | 903.40 | 892.70 | 903.40 | 925.90 | 936.60 |
| 14 | 925.95 | 903.45 | 892.75 | 903.45 | 925.95 | 936.65 |
| 15 | 926.00 | 903.50 | 892.80 | 903.50 | 926.00 | 936.70 |
| 16 | 926.05 | 903.55 | 892.85 | 903.55 | 926.05 | 936.75 |
| 17 | 926.10 | 903.60 | 892.90 | 903.60 | 926.10 | 936.80 |
| 18 | 926.15 | 903.65 | 892.95 | 903.65 | 926.15 | 936.85 |
| 19 | 926.20 | 903.70 | 893.00 | 903.70 | 926.20 | 936.90 |
| 20 | 926.25 | 903.75 | 893.05 | 903.75 | 926.25 | 936.95 |
| 21 | 926.30 | 903.80 | 893.10 | 903.80 | 926.30 | 937.00 |
| 22 | 926.35 | 903.85 | 893.15 | 903.85 | 926.35 | 937.05 |
| 23 | 926.40 | 903.90 | 893.20 | 903.90 | 926.40 | 937.10 |
| 24 | 926.45 | 903.95 | 893.25 | 903.95 | 926.45 | 937.15 |
| 25 | 926.50 | 904.00 | 893.30 | 904.00 | 926.50 | 937.20 |
| 26 | 926.55 | 904.05 | 893.35 | 904.05 | 926.55 | 937.25 |
| 27 | 926.60 | 904.10 | 893.40 | 904.10 | 926.60 | 937.30 |
| 28 | 926.65 | 904.15 | 893.45 | 904.15 | 926.65 | 937.35 |
| 29 | 926.70 | 904.20 | 893.50 | 904.20 | 926.70 | 937.40 |
| 30 | 926.75 | 904.25 | 893.55 | 904.25 | 926.75 | 937.45 |
| 31 | 926.80 | 904.30 | 893.60 | 904.30 | 926.80 | 937.50 |
| 32 | 926.85 | 904.35 | 893.65 | 904.35 | 926.85 | 937.55 |
| 33 | 926.90 | 904.40 | 893.70 | 904.40 | 926.90 | 937.60 |
| 34 | 926.95 | 904.45 | 893.75 | 904.45 | 926.95 | 937.65 |
| 35 | 927.00 | 904.50 | 893.80 | 904.50 | 927.00 | 937.70 |
| 36 | 927.05 | 904.55 | 893.85 | 904.55 | 927.05 | 937.75 |
| 37 | 927.10 | 904.60 | 893.90 | 904.60 | 927.10 | 937.80 |
| 38 | 927.15 | 904.65 | 893.95 | 904.65 | 927.15 | 937.85 |
| 39 | 927.20 | 904.70 | 894.00 | 904.70 | 927.20 | 937.90 |
| 40 | 927.25 | 904.75 | 894.05 | 904.75 | 927.25 | 937.95 |

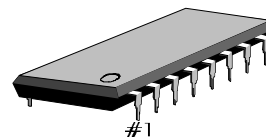
INTRODUCTION

The S1T3361D is designed for use in FM dual conversion communication. It contains a complete narrow band FM demodulation system operable to less than 2.5V supply voltage. This low-power narrow-band FM IF system provides the second converter, second IF, demodulator. Filter Amp and squelch circuitry for communications and scanning receivers.

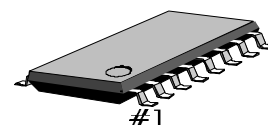
FEATURES

- Low power consumption (4.0mA typ. at $V_{CC} = 4.0V$)
- Excellent input sensitivity (-3dB limiting, $2.0\mu V_{rms}$ typ.)
- Minimum number of external components required.
- Operating Voltage: 2.5 to 7.0V

16-DIP-300A



16-SOP-225A



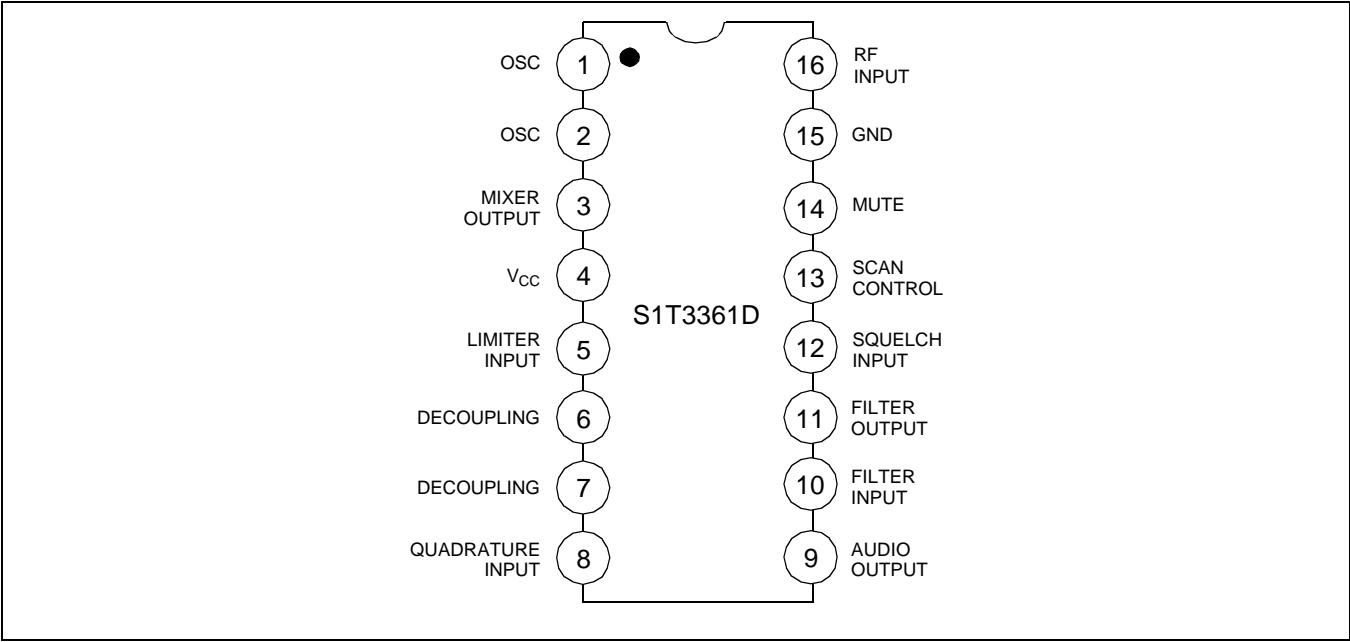
APPLICATIONS

- Cordless phone (for home usage)
- FM dual conversion communications equipment

ORDERING INFORMATION

| Device | Package | Operating Temperature |
|-----------------|-------------|-----------------------|
| S1T3361D01-D0B0 | 16-DIP-300A | - 20°C to +70°C |
| S1T3361D01-S0B0 | 16-SOP-225A | |

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

| Characteristic | Symbol | Value | Unit |
|---|-----------------------|----------------|-------------------|
| Max. Supply Voltage | V _{CC (MAX)} | 10 | V |
| Supply Voltage Range | V _{CC} | 2.5 to 7.0 | V |
| Detector Input Voltage | V _{I (DET)} | 1.0 | V _{P-P} |
| RF Input Voltage (V _{CC} ≥ 4.0V) | V _{I (RF)} | 1.0 | V _{rms} |
| Mute Function | V _{MUTE} | – 0.5 to + 0.5 | V _{peak} |
| Operating Temperature | T _{OPR} | – 20 to + 70 | °C |
| Storage Temperature | T _{STG} | – 65 to + 150 | °C |

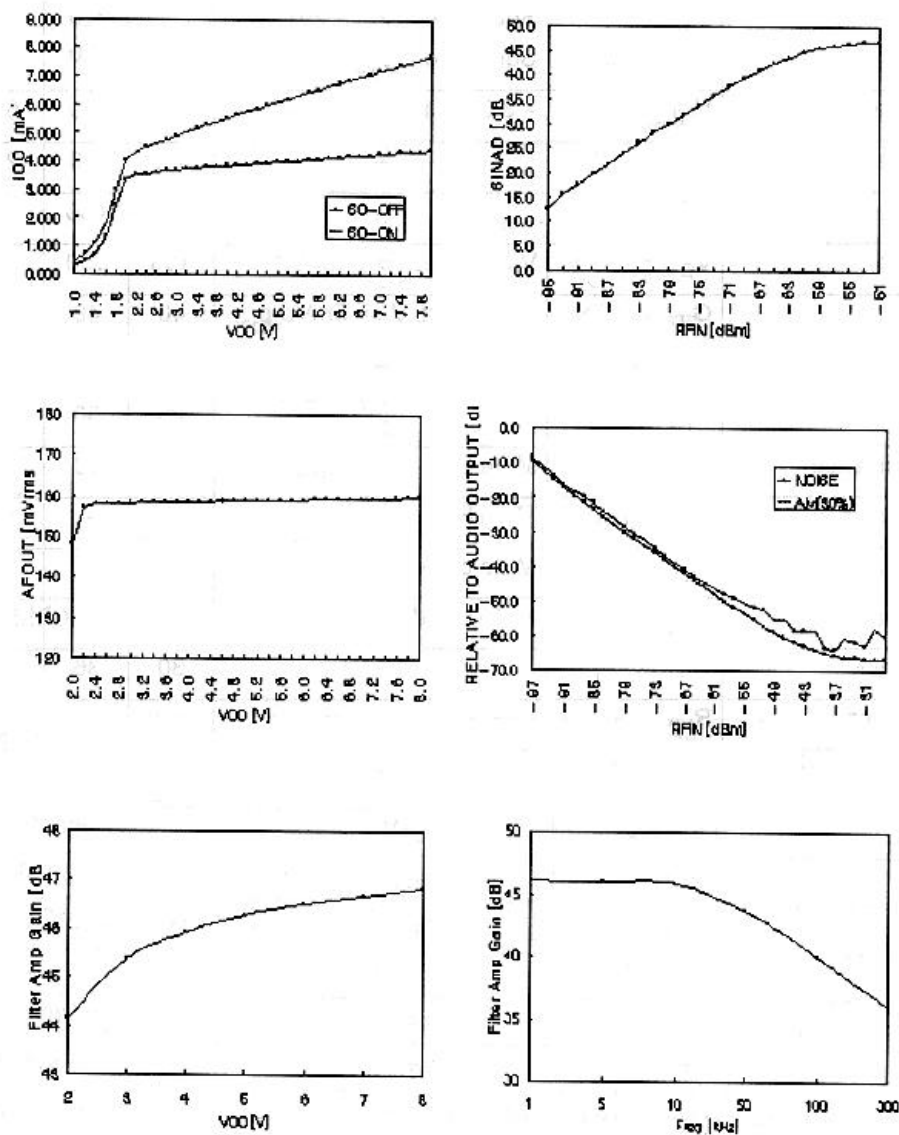
NOTE:
Absolute maximum ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{CC} = 4.0V$, $f_o = 10.7MHz$, $\Delta f = \pm 3kHz$, $f_{MOD} = 1kHz$, $T_a = 25^\circ C$, unless otherwise specified)

| Characteristic | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------------------------|-----------------|-------------------------------|------|------|------|------------|
| Operating Current | I_{CC} | Squelch off ($V_{12} = 2V$) | 2.0 | 4.0 | 8.0 | mA |
| | | Squelch on ($V_{12} = GND$) | 3.0 | 6.0 | 10 | mA |
| Input Limiting Voltage | $V_{I(LIM)}$ | -3.0dB limiting | — | 2.0 | 6.0 | μV |
| Detector Output Voltage | $V_O(DET)$ | — | — | 2.0 | — | V_{dc} |
| Detector Output Impedance | $Z_O(DET)$ | — | — | 400 | — | W |
| Recoverd audio output voltage | V_O | $V_{in} = 10mV$ | 134 | 150 | 168 | mV_{rms} |
| Filter Gain | G_V | $f = 10kHz$, $V_{in} = 5mV$ | 40 | 48 | 52 | dB |
| Filter Output DC Voltage | $V_O(DC)$ | — | 1.0 | 1.5 | 2.0 | V_{dc} |
| Trigger Hysteresis of Filter | V_{TH} | — | — | 50 | — | mV |
| Mute Switch-on Resistance | $R_{ON(MUTE)}$ | Mute Low | — | 10 | 40 | Ω |
| Mute Switch-off Resistance | $R_{OFF(MUTE)}$ | Mute High | 1 | - | 10 | $M\Omega$ |
| Scan Control Low Output | $V_L(SCAN)$ | Mute off ($V_{12} = 2V$) | — | — | 0.5 | V_{dc} |
| Scan Control High Output | $V_H(SCAN)$ | Mute on ($V_{12} = GND$) | 3.0 | — | — | V_{dc} |
| Mixer Conversion Gain | $G_V(MIXER)$ | — | 30 | 36 | — | dB |
| Mixer Input Resistance | $R_I(MIXER)$ | — | — | 3.3 | — | $k\Omega$ |
| Mixer Input Capacitance | $C_I(MIXER)$ | — | — | 2.2 | — | pF |

CHARACTERISTIC GRAPH



NOTES

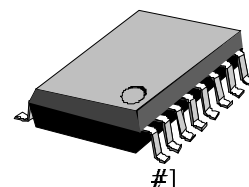
INTRODUCTION

The S1T8825 is a high performance dual frequency synthesizer with two integrated high frequency pre-scalers for RF operation up to 1.1 GHz.

The S1T8825 is composed of modulus pre-scalers providing 64 and 66, no dead-zone PFD, selectable charge pump current, selectable power down mode circuits, lock detector output, and loop filter's time constant switch.

It is fabricated using the ASP5HB Bi-CMOS process and is available 16-TSSOP with surface mount plastic packaging. Serial data is transferred into the S1T8825 via three-wire interface (CK, DATA, EN).

16-TSSOP-0044



FEATURES

- Two systems for receiver and transmitter
- Very low operating current consumption: $I_{cc} = \text{Typ. } 5.5\text{mA @ } 3.0\text{V}$
- Low operating power supply voltage : 2.2 ~ 5.5V (200MHz ~ 550MHz Operating)
2.7 ~ 3.6V (550MHz ~ 1.1GHz Operating)
- Modulus pre-scaler: 64 / 66
- No dead-zone PFD
- Colpitts type local oscillation
- Selectable charge pump current
- Selectable power down mode
- TSSOP 16-pin package (0.65 mm pitch)

ORDERING INFORMATION

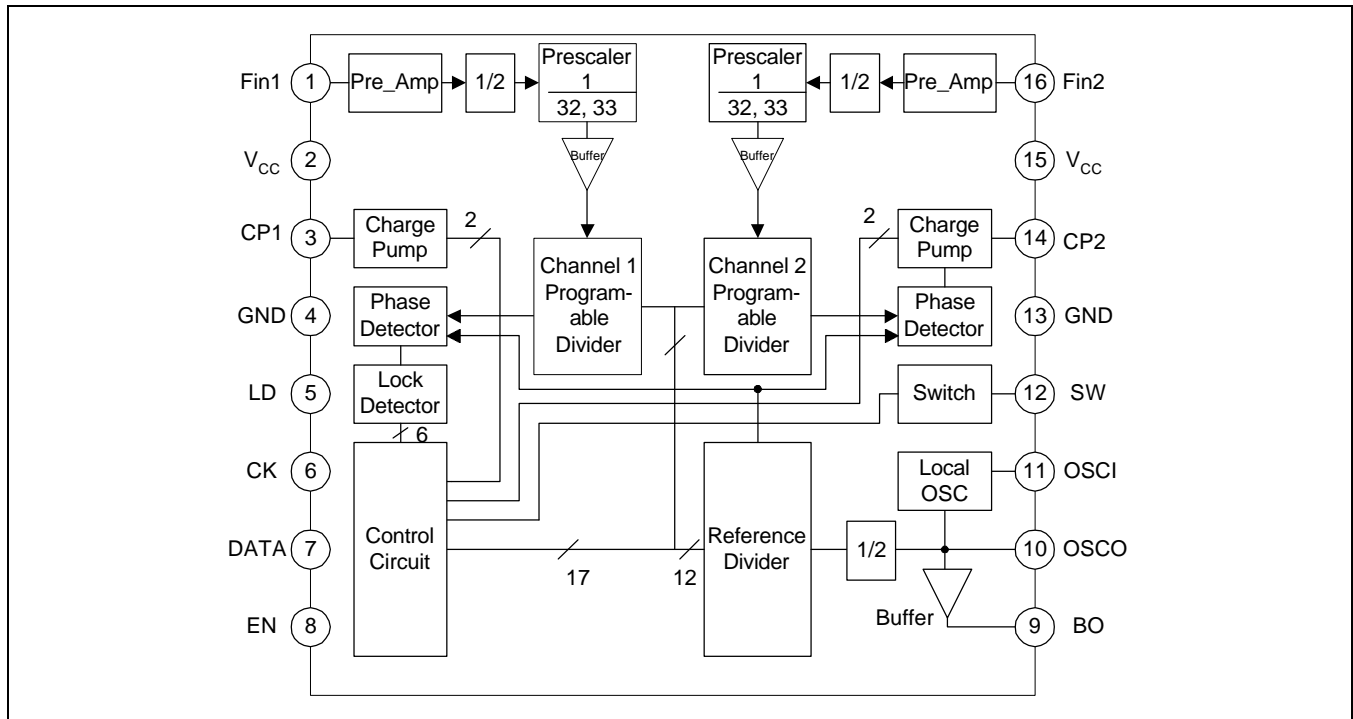
| Device | Package | Operating Temperature |
|------------------|---------------|-----------------------|
| +S1T8825X01-R0B0 | 16-TSSOP-0044 | -30 °C to + 85 °C |

+: New Product

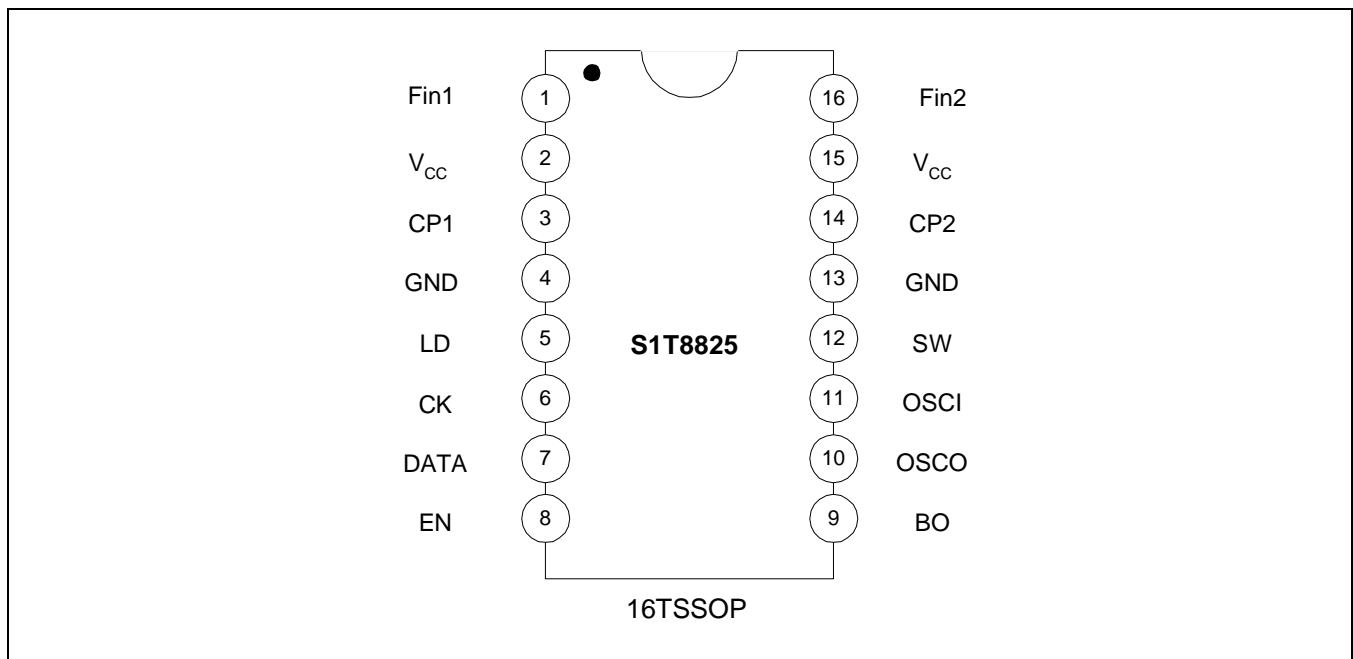
APPLICATIONS

- Cordless telephone systems
- Portable wireless communications (PCS)
- Wireless Local Area Networks (WLANs)
- Other wireless communication systems

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

| Pin No. | Symbol | I/O | Description |
|---------|--------|-----|--|
| 1 | Fin1 | I | Input terminal of channel 1 RF signal. |
| 2, 15 | Vcc | – | Power supply voltage input. PIN2 and PIN15 are connected together. |
| 3 | CP1 | O | Output terminal of channel 1 charge pump. Charge pump is constant current output circuit, and output current is selected by input serial data. |
| 4, 13 | GND | – | Terminal of GND. PIN4 and PIN13 are connected together. |
| 5 | LD | O | Output terminal of lock detection. It is the open drain output. |
| 6 | CK | I | Input terminal of clock. |
| 7 | DATA | I | Input terminal of data. |
| 8 | EN | I | Input terminal of enable signal. |
| 9 | BO | O | Output terminal of buffer amplifier. The signal of local oscillation is output through the buffer amplifier. |
| 10 | OSCO | O | Output terminal of local oscillation signal. |
| 11 | OSCI | I | Input terminal of local oscillation signal. In case of external input, connecting it to this terminal. |
| 12 | SW | O | Switch-over terminal for the time constant of loop filter. It is an open drain output. If you don't switch the time constant of loop filter, general output is available. |
| 14 | CP2 | O | Output terminal of channel 2 charge pump. Charge pump is a constant current output circuit, and the output current is selected by input serial data. |
| 16 | Fin2 | I | Input terminal of channel 2 RF signal. |

ABSOLUTE MAXIMUM RATINGS

| Characteristic | Symbol | Value | Unit |
|-----------------------|------------------|-----------|------|
| Power Supply Voltage | V _{CC} | 6 | V |
| Power Dissipation | P _D | 600 | mW |
| Operating temperature | T _{OPR} | –30 — +85 | °C |
| Storage temperature | T _{STG} | –55 — +50 | °C |



Take care ! ESD sensitive device

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 3V, unless otherwise specified)

| Characteristic | Symbol | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|------------------|--|------------------------|-----------------------|-------|------|------|
| Operating power supply voltage | V _{CC} | Fin1=Fin2= 200MHz ~ 550MHz | | 2.2 | 3.0 | 5.5 | V |
| | | Fin1=Fin2= 550MHz ~ 1.1GHz | | 2.7 | 3.0 | 3.6 | V |
| Operating current consumption | I _{CC} | Fin1=Fin2=1.1GHz/ -5dBm input | | 3.5 | 5.5 | 7.5 | mA |
| Standby current | I _{SB} | Standby mode | | – | 0 | 10 | μA |
| Fin operating frequency | Fin | Fin1 = Fin2 = – 5dBm | | 200 | – | 1100 | MHz |
| Fin input sensitivity | Fin | Fin1 = Fin2 = 200MHz | V _{CC} =2.2V | – 15 | – | 0 | dBm |
| | | | V _{CC} =3.0V | – 15 | – | 0 | |
| | | | V _{CC} =5.5V | – 10 | – | 0 | |
| | | Fin1 = Fin2 = 550MHz | V _{CC} =2.2V | –15 | – | 0 | |
| | | | V _{CC} =3.0V | –15 | – | 0 | |
| | | | V _{CC} =5.5V | – 10 | – | 0 | |
| | | Fin1 = Fin2 = 1.1GHz | V _{CC} =2.7V | – 10 | – | 0 | |
| | | | V _{CC} =3.0V | – 10 | – | 0 | |
| | | | V _{CC} =3.6V | – 10 | – | 0 | |
| OSCI operating frequency | F _{osc} | V _{Fin} = 0dBm, sinewave | | 5 | - | 25 | MHz |
| OSCI input voltage | V _{osc} | f _{osc} = 10MHz | V _{CC} = 2.2V | – 10 | 0 | 5 | dBm |
| | | | V _{CC} = 3.0V | – 10 | 0 | 5 | |
| | | | V _{CC} = 5.5V | 0 | - | 5 | |
| | | f _{osc} = 20MHz | V _{CC} = 2.2V | – 10 | 0 | 5 | |
| | | | V _{CC} = 3.0V | – 10 | 0 | 5 | |
| | | | V _{CC} = 5.5V | – 5 | 0 | 5 | |
| Serial data input high voltage (CK, DATA, EN) | V _{IH} | V _{CC} = 2.2 to 5.5V | | V _{CC} – 0.4 | – | - | V |
| Serial data input low voltage (CK, DATA, EN) | V _{IL} | V _{CC} = 2.2 to 5.5V | | – | – | 0.4 | V |
| Charge pump output current | I _{CP1} | CP1 = 0, CP2 = 0 V _{CP} = 1.5 V | | – | ± 100 | – | μA |
| | I _{CP2} | CP1 = 1, CP2 = 0 V _{CP} = 1.5V | | – | ± 200 | – | μA |
| | I _{CP3} | CP1 = 0, CP2 = 1 V _{CP} = 1.5V | | – | ± 400 | – | μA |
| | I _{CP4} | CP1 = 1, CP2 = 1 V _{CP} = 1.5V | | – | ± 800 | – | μA |
| Charge pump leakage | I _{CPL} | Standby mode, V _{cp} = 1.5V | | –1 | – | +1 | μA |

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT AND TIMING

CK (Pin6), DATA (Pin7), EN (Pin8) terminals in S1T8825 are used for MCU serial data interface (MSB: 1st input data; LSB: Last input data). Serial data controls the programmable reference divider, programmable divider (CH1), programmable divider (CH2), and control latch separately by means of group code. Binary serial data is entered via the DATA pin.

One bit of data is shifted into the internal shift register on the rising edge of the clock. When EN pin is high, stored data is latched. The three terminals, CK, DATA, and EN, contain Schmitt trigger circuits to keep the data from errors caused by noise, etc.

< Notice >

1. When power supply of S1T8825 is disconnected, CLK, DATA, EN port from MCU should be pulled low.
2. When power goes up first, R counter data should be entered earlier than N1 and N2 counter data.
3. When power goes up first, control data should be entered earlier than N1 and N2 counter data.

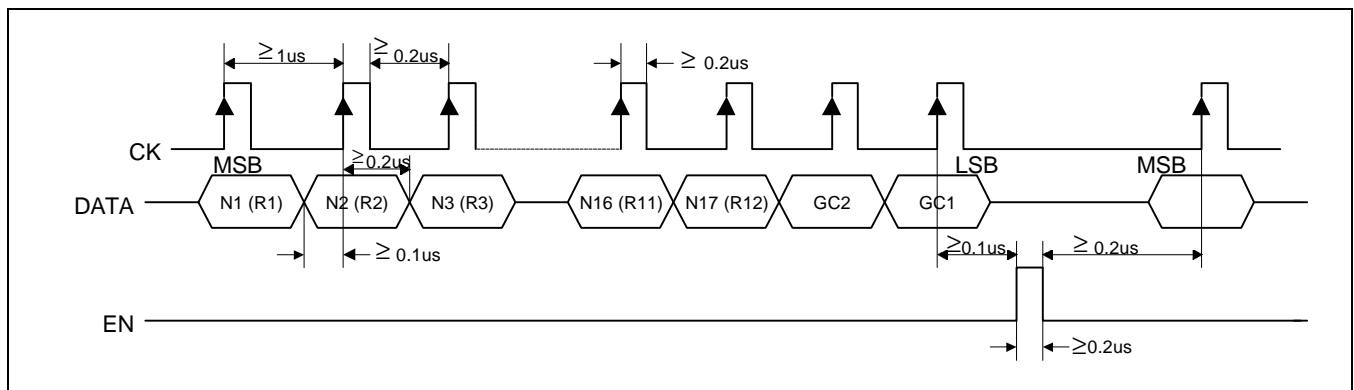


Figure 1.

NOTE: Start data input with MSB first

SERIAL DATA GROUP AND GROUP CODE

The S1T8825 can be controlled through 4 kinds of group selection. Each group is identified by selective a 2-bit group code given below.

| Serial Bits | | Group Location |
|-------------|-------------|----------------|
| GC1 (LSB) | GC2 (LSB-1) | |
| 0 | 0 | Control Latch |
| 0 | 1 | Ch 1 N Latch |
| 1 | 0 | Ch 2 N Latch |
| 1 | 1 | OSC R Latch |

CONTROL LATCH

The control register executes the following functions:

- Mode selection (H: test mode, L: normal mode)
- Charge pump's polarity and output current selection for each channel.
- Output state selection for Lock Detector.
- Standby control of each channel and reference divider.
- ON / OFF control in filter switch.

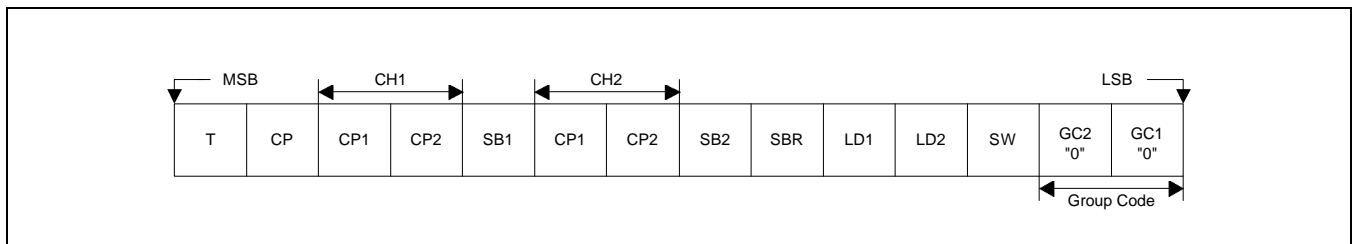


Figure 2.

| Bit | Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7 |
|-------------|-----------|-----------------------------|--------------------------------------|--------------------------------------|-------------------|--------------------------------------|--------------------------------------|
| Name | T | CP | CP1 | CP2 | SB1 | CP1 | CP2 |
| Description | test mode | charge pump output polarity | channel 1 charge pump output current | channel 1 charge pump output current | channel 1 standby | channel 2 charge pump output current | channel 2 charge pump output current |

| Bit | Bit 8 | Bit 9 | Bit 10 | Bit 11 | Bit 12 | Bit 13 | Bit 14 |
|-------------|-------------------|---------------------------|-------------------------|-------------------------|---------------|----------------|----------------|
| Name | SB2 | SBR | LD1 | LD2 | SW | GC2 | GC1 |
| Description | channel 2 standby | reference divider standby | lock detector control 1 | lock detector control 2 | filter switch | group code "0" | group code "0" |

CHARGE PUMP OUTPUT POLARITY (CP)

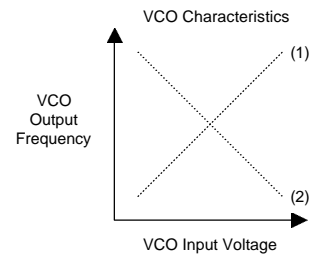
In normal operation, the CP should be “0”.

In reverse operation, the CP should be “1”.

Depending upon VCO characteristics, CP should be set accordingly;

When VCO characteristics are like (1), CP should be set to low

When VCO characteristics are like (2), CP should be set to high.

**CHARGE PUMP OUTPUT CURRENT (CP1, CP2)**

The S1T8825 includes a constant current output type charge pump circuit.

Output current is varied according to control bit “CP1” and “CP2”.

In order to get high speed lock-up, select the best charge pump output current.

| Control Bit | | Charge Pump Output Current |
|-------------|-----|----------------------------|
| CP1 | CP2 | |
| 0 | 0 | $\pm 100 \mu\text{A}$ |
| 0 | 1 | $\pm 200 \mu\text{A}$ |
| 1 | 0 | $\pm 400 \mu\text{A}$ |
| 1 | 1 | $\pm 800 \mu\text{A}$ |

TEST MODE AND LOCK DETECTOR OUTPUT (T, LD1, LD2)

When T is normal "0", LD (Pin5) state is varied by controlling "SB1", "SB2", "LD1" and "LD2".

When T is high "1", LD (Pin5) state is changed to be useful for test

| T | SB1 | SB2 | LD1 | LD2 | LD Output State |
|---|-----|-----|-----|-----|-------------------------|
| 0 | 0 | 0 | 0 | 0 | low |
| | | | 0 | 1 | channel2 |
| | | | 1 | 0 | channel1 |
| | | | 1 | 1 | channel1. AND. channel2 |
| | | 1 | 0 | 0 | low |
| | | | 0 | 1 | high |
| | | | 1 | 0 | channel1 |
| | | | 1 | 1 | channel1 |
| | 1 | 0 | 0 | 0 | low |
| | | | 0 | 1 | channel2 |
| | | | 1 | 0 | high |
| | | | 1 | 1 | channel2 |
| | | 1 | 0 | 0 | low |
| | | | 0 | 1 | high |
| | | | 1 | 0 | high |
| | | | 1 | 1 | high |
| 1 | 1 | 0 | 0 | 0 | low |
| | | | 0 | 1 | pres2 |
| | | | 1 | 0 | fpll2 |
| | | | 1 | 1 | fref |
| | 0 | 1 | 0 | 0 | div4 |
| | | | 0 | 1 | pres1 |
| | | | 1 | 0 | fpll1 |
| | | | 1 | 1 | fosc/2 |
| | 1 | 1 | × | × | low |
| | 0 | 0 | × | × | low |

LOCK DETECTOR OUTPUT

When the phase comparator detects a phase difference, LD (Pin5) outputs “L”.
When the phase comparator locks, LD outputs “H”. On standby, it outputs “H”.
When T is less than $2/f_{osc}$ ($T < 2/f_{osc}$) for more than three cycles of reference divider output as in the figure below, the lock detector outputs “H”.

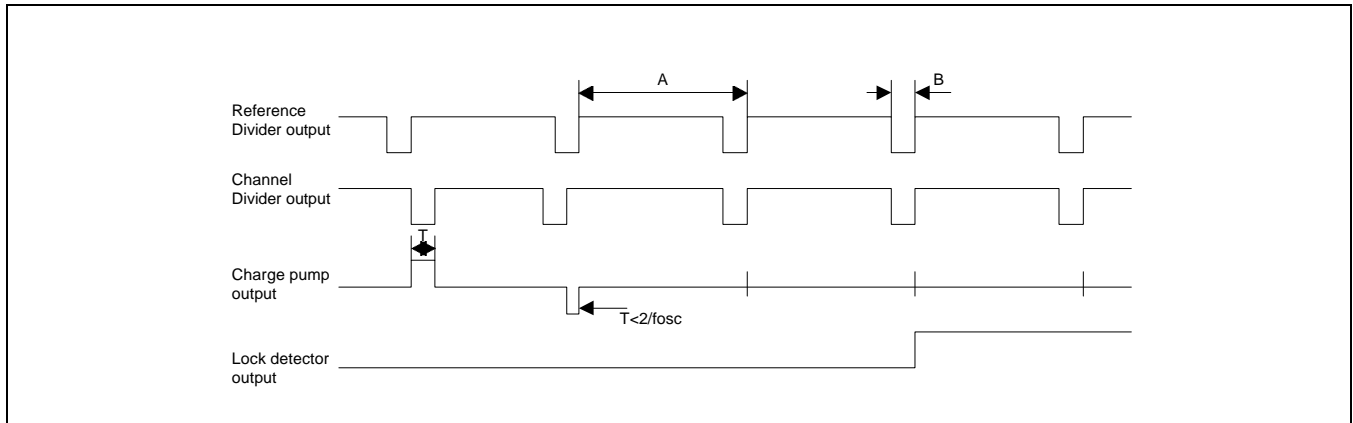


Figure 3. Lock Detector Output

f_{osc} : OSCI operating frequency (LOCAL OSC).

T: time difference of the pulse between reference divider output and channel divider output.

$$A = \frac{\text{Number of divisions by reference divider}}{f_{osc}} \quad (\text{s})$$

$$B = \frac{2}{f_{osc}} \quad (\text{s})$$

PROGRAMMABLE STANDBY MODE (SB1, SB2, SBR)

Standby mode can be controlled by 3-control bits such as SB1, SB2 and SBR. SB1 and SB2 can control the standby mode of channel 1 and channel2. The “SBR” bit can do ON / OFF control of reference divider.

| Control Bit | | | Standby Mode State | | | |
|-------------|-----|-----|--------------------|-----|-----|--------------------|
| SB1 | SB2 | SBR | CH1 | CH2 | REF | Mode Status |
| 0 | 0 | × | ON | ON | ON | Inter locking Mode |
| 0 | 1 | × | ON | OFF | ON | CH1 Locking Mode |
| 1 | 0 | × | OFF | ON | ON | CH2 Locking Mode |
| 1 | 1 | 0 | OFF | OFF | ON | REF On Mode |
| 1 | 1 | 1 | OFF | OFF | OFF | Standby Mode |

FILTER SWITCH CONTROL (SW)

The operation mode of the SW terminal is set by bit "SW".

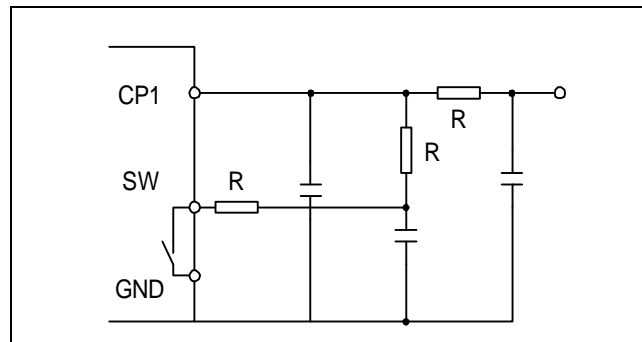
SW control is useful for switching the time constant of the loop filter.

Output type of this terminal is an open drain output. High lock mode or normal lock mode can be used, taking advantage of filter switch control (SW) with the charge pump output current.

When fast lock function can't be used, normal lock mode is available.

| Control Bits | | | Operation Mode |
|--------------|-----|-----|------------------|
| SW | CP1 | CP2 | |
| 0 | 0 | 0 | Normal Lock Mode |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | High Lock Mode |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

(SW and LPF example) The third order LPF



CRYSTAL OSCILLATOR CIRCUIT (OSCI, OSCO) AND BUFFER OUT (BO)

External capacitors C1, C2, C3, and C4 are required to set the proper crystal's load capacitance and oscillation frequency as shown in figure 4. The value of the capacitors is dependent on the crystal chosen.

The BO (Pin9) outputs local oscillation signal with buffer amplifier.

This terminal (Pin9) can be applied to the 2nd mixer input

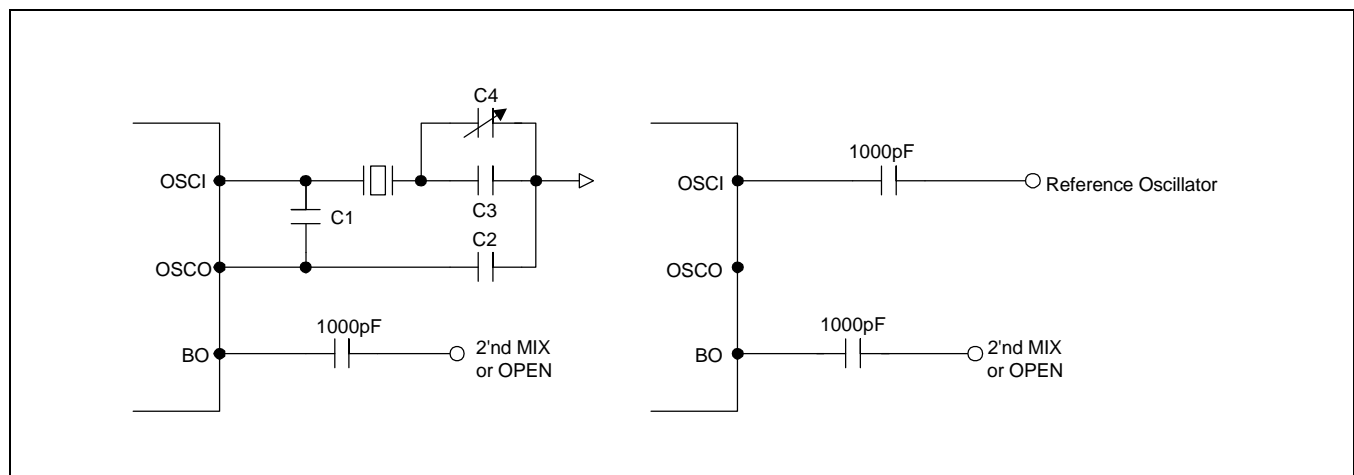


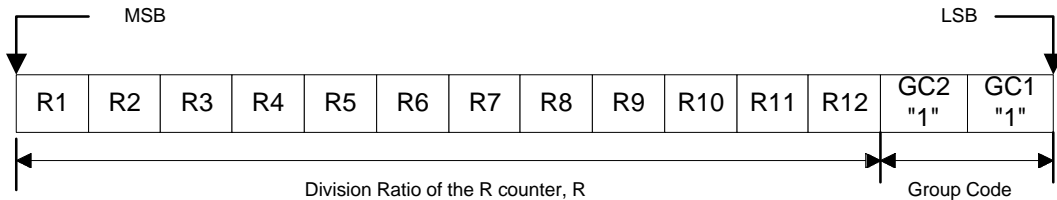
Figure 4.

PROGRAMMABLE REFERENCE COUNTER

This block generates the reference frequency for the PLL.

The reference divider is composed of 12-bit reference divider and a half fixed divider

Sending certain data to the reference divider allows the setting of any of 6 to 8190 divisions (multiple of two).



$$R = R1 \times 2^0 + R2 \times 2^1 + \dots + R12 \times 2^{11}$$

$$\text{Division ratio: } 2 \times R = 2 \times (3 \sim 4095) = 6 \sim 8190$$

Data is shifted in MSB first.

| Division Ratio | R12 | R11 | R10 | R9 | R8 | R7 | R6 | R5 | R4 | R3 | R2 | R1 |
|----------------|-----|-----|-----|----|----|----|----|----|----|----|----|----|
| 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| • | • | • | • | • | • | • | • | • | • | • | • | • |
| 4095 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Example) A 21.25MHz X-tal oscillator is connected, and divided into 25kHz steps.
(Reference frequency is 12.5kHz)

$$21.25 \text{ MHz} \div 12.5 \text{ kHz} = 1700$$

$$1700 = 2 \times R$$

$$R = (850)_{10} = (1101010010)_2$$

| | | | | | | | | | | | | | |
|-----|---|---|---|---|---|---|---|---|---|---|---|---|-----|
| MSB | | | | | | | | | | | | | LSB |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

CHANNEL 1, CHANNEL 2 PROGRAMMABLE N COUNTER

These programmable dividers are composed of a 5-bit swallow counter (5-bit programmable divider), 12-bit programmable main counter, and two-modulus prescalers providing 64 and 66 divisions. Sending certain data to the swallow counter and the 12-bit programmable main counter allows the setting of any of 2048 to 262142 divisions (multiple of two). The 12-bit programmable divider and swallow counter are set by each channel; each channel is identified by a group code.

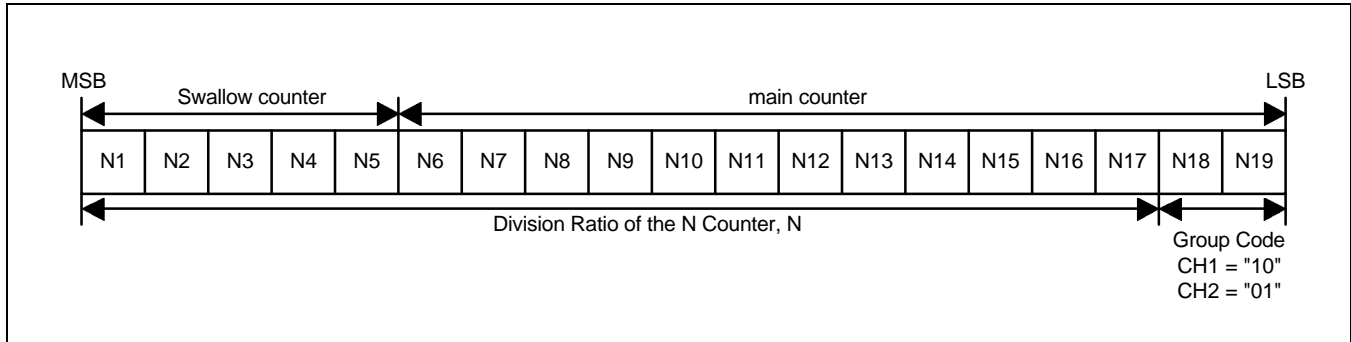


Figure 5.

5-BIT SWALLOW COUNTER DIVISION RATIO (A COUNTER)

$$A = N1 \times 2^0 + N2 \times 2^1 \dots N5 \times 2^4$$

Division ratio: 0 to 31, $B \geq A$

| Division Ratio (A) | N5 | N4 | N3 | N2 | N1 |
|--------------------|----|----|----|----|----|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| • | • | • | • | • | • |
| 31 | 1 | 1 | 1 | 1 | 1 |

12-BIT MAIN COUNTER DIVISION RATIO (B COUNTER)

$$B = N6 \times 2^0 + N7 \times 2^1 + N8 \times 2^2 \dots N17 \times 2^{11}$$

Division ratio: 3 to 4095

Data is shifted in MSB first

| Division Ratio (B) | N17 | N16 | N15 | N14 | N13 | N12 | N11 | N10 | N9 | N8 | N7 | N6 |
|--------------------|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|
| 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| • | • | • | • | • | • | • | • | • | • | • | • | • |
| 4095 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Channel1 and 2 Programmable Counter Division Ratio, N

$$N = 2 \times (32 \times B + A), B \geq A$$

Division ratio: 192 ~ 262142

Example) A Signal of 453 MHz is entered into Fin1, and divided into 25 kHz steps.

(Reference frequency is 12.5 kHz)

$$453 \text{ MHz} \div 12.5 \text{ kHz} = 36240$$

$$36240 = 2 \times (32 \times B + A)$$

$$\therefore B = (1132)_{10} = (10001101100)_2, A = (16)_{10} = (10000)_2$$

| | | | | | | | | | | | | | | | | | | |
|-----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----|---|
| MSB | | | | | | | | | | | | | | | | | LSB | |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

Example) A Signal of 462.9 MHz is entered into Fin2, and divided into 25 kHz step.

(Reference frequency is 12.5 kHz)

$$462.9 \text{ MHz} \div 12.5 \text{ kHz} = 37032$$

$$37032 = 2 \times (32 \times B + A)$$

$$\therefore B = (1157)_{10} = (10010000101)_2, A = (8)_{10} = (01000)_2$$

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| MSB | | | | | | | | | | | | | | | | | LSB | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | | | | | | | | | | | | | | | |

PHASE DETECTOR AND CHARGE PUMP CHARACTERISTICS

Phase difference detection Range: $-2\pi \sim +2\pi$

When SW = Low

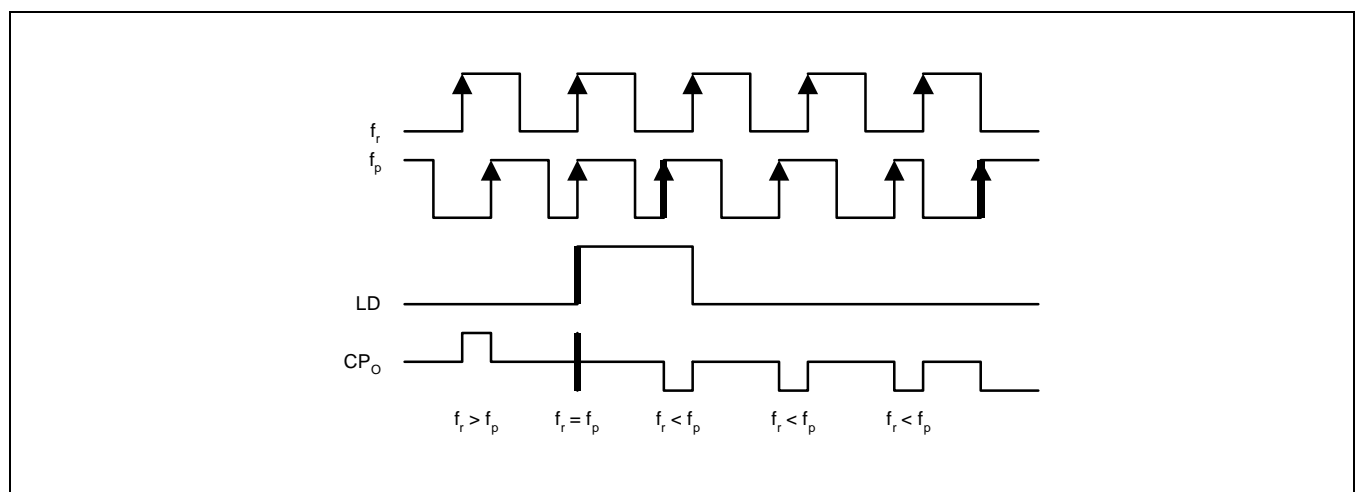
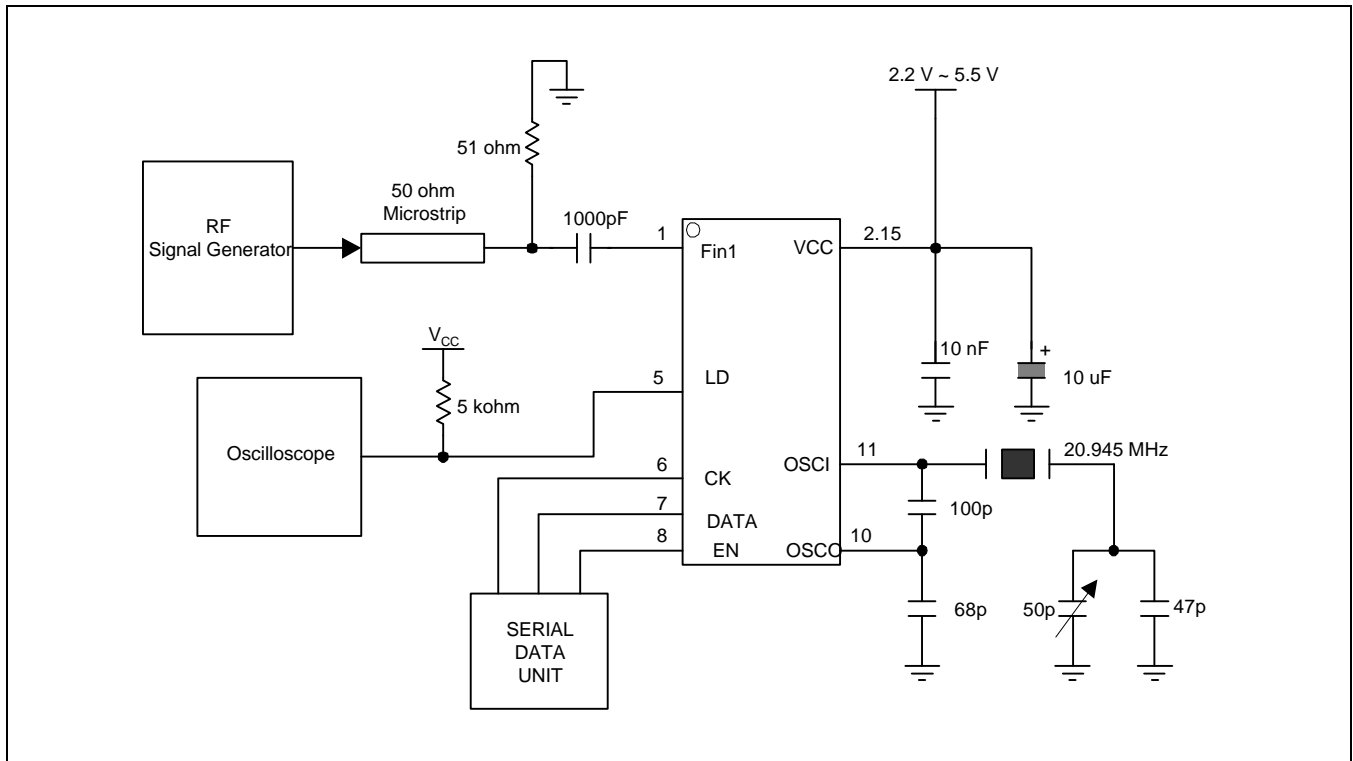
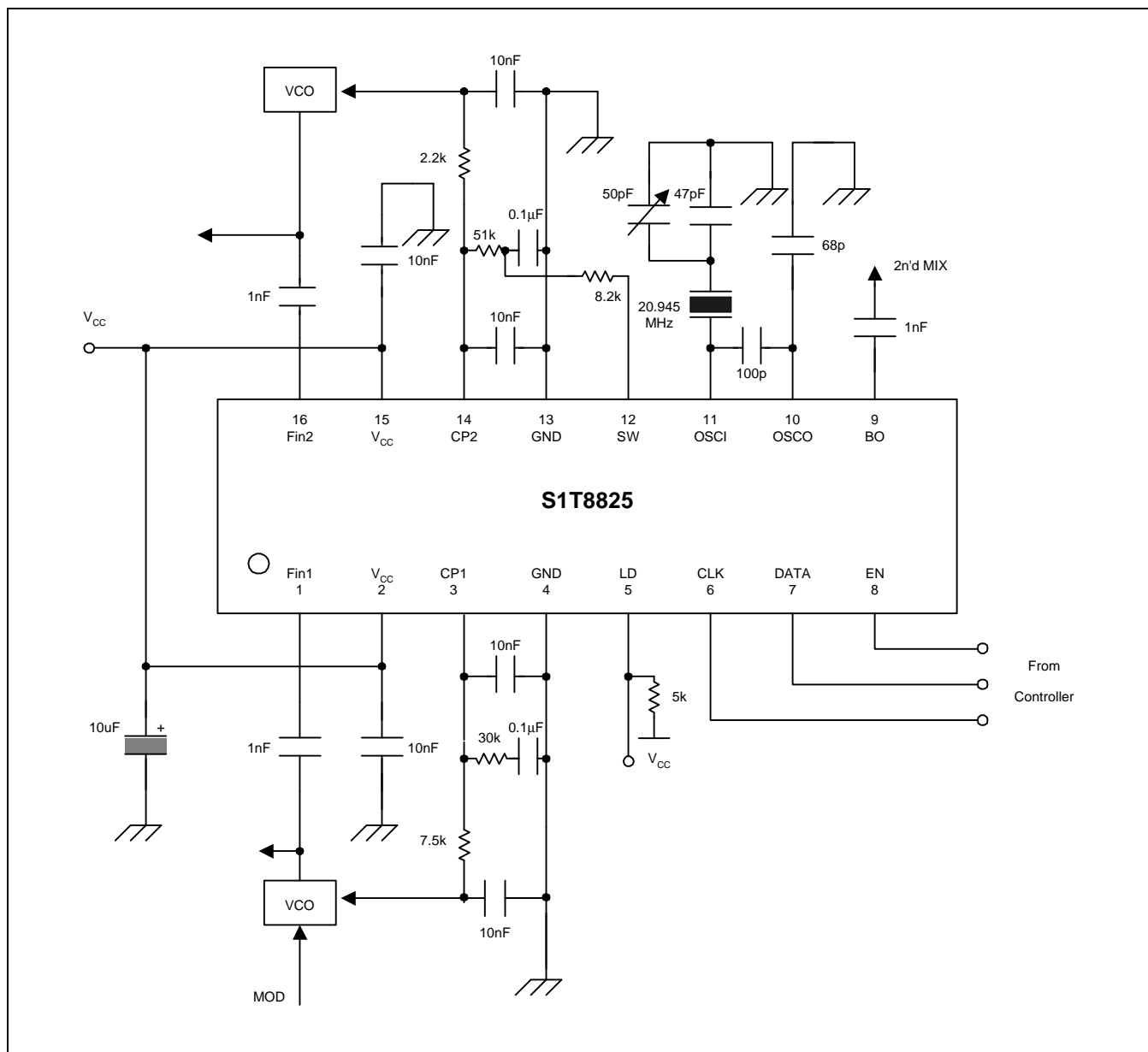


Figure 6.

SENSITIVITY TEST CIRCUIT



TYPICAL APPLICATION CIRCUIT



NOTES