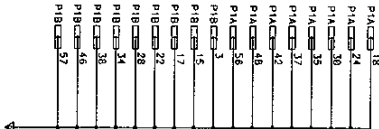
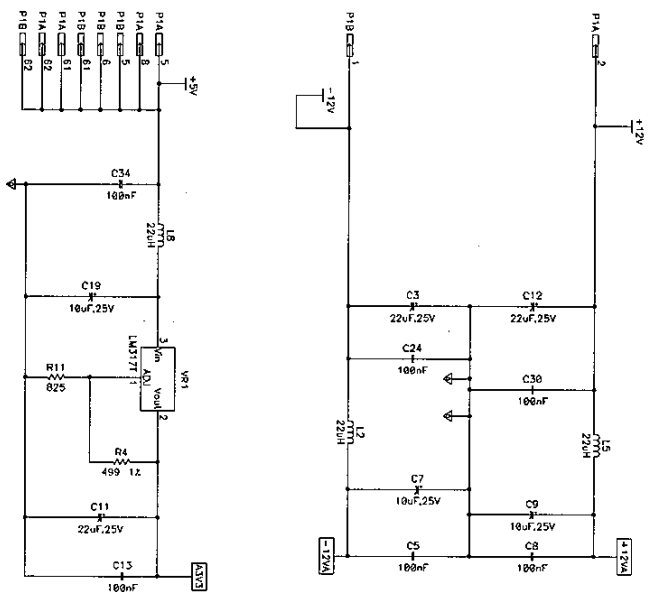


EXHIBIT D

Circuit Diagram

REV	DESCRIPTION	DATE	APPROVED
1			

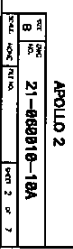


2. ALL CAPACITANCE ARE IN UF +/- 20%, 50V
1. ALL RESISTANCE ARE IN OHM, 1%.

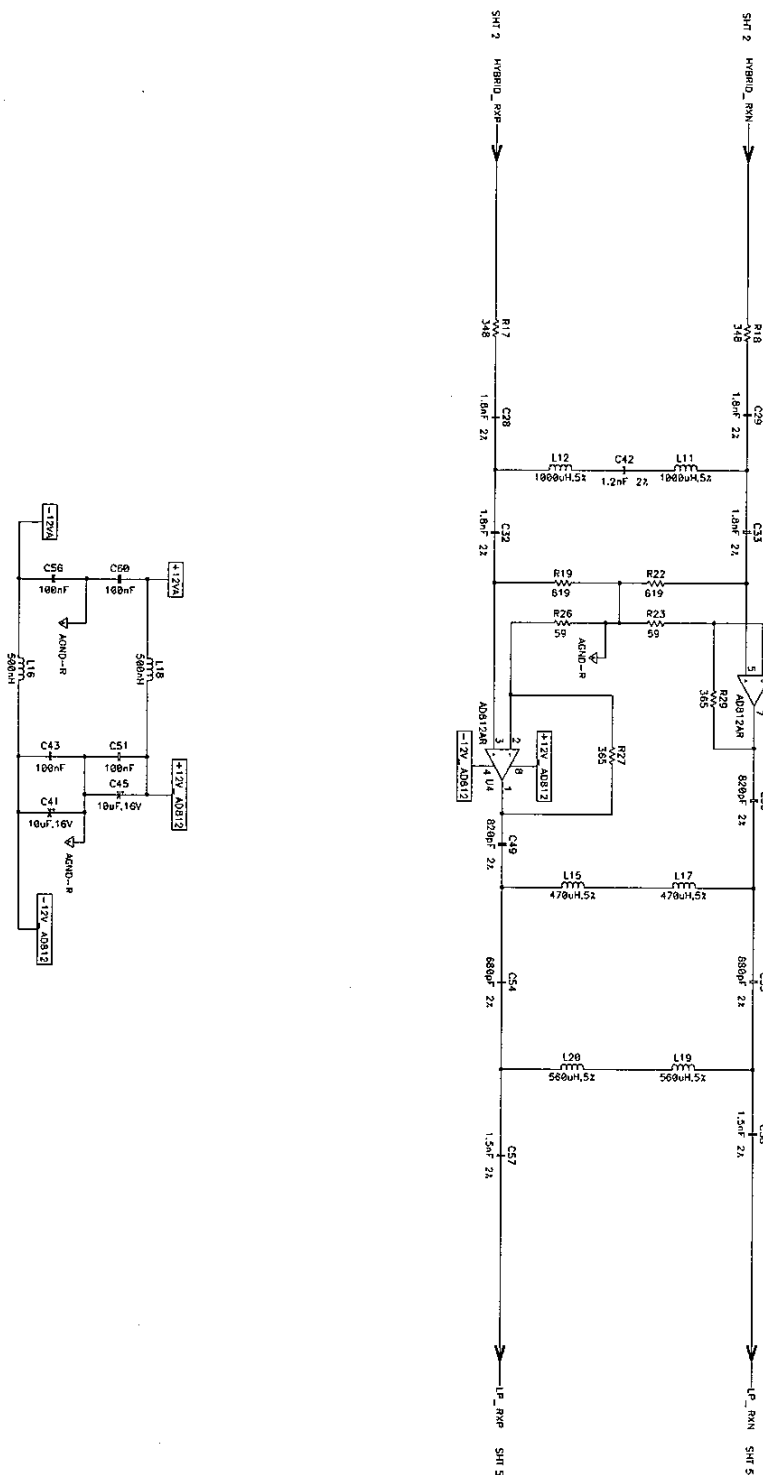
NOTES: UNLESS OTHERWISE SPECIFIED

REV	DATE	DESCRIPTION	APPROVED	DATE	DESCRIPTION
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3	10/10/80	REVISION 2			
4	10/10/80	REVISION 3			
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2		1	
REV	DESCRIPTION	DATE	APPROVED



RECEIVE PATH

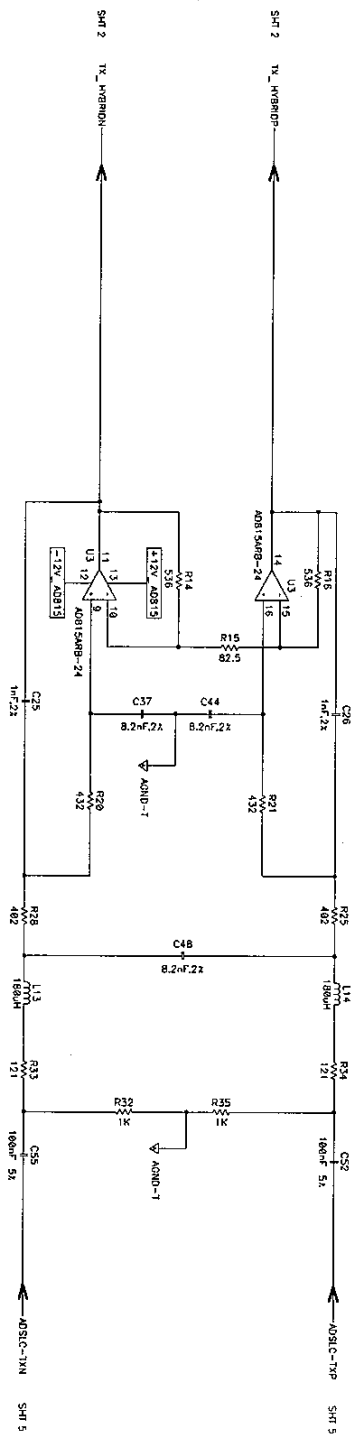


APOLLO 2

21-066010-10A

REV 3 OF 7

TRANSMIT PATH



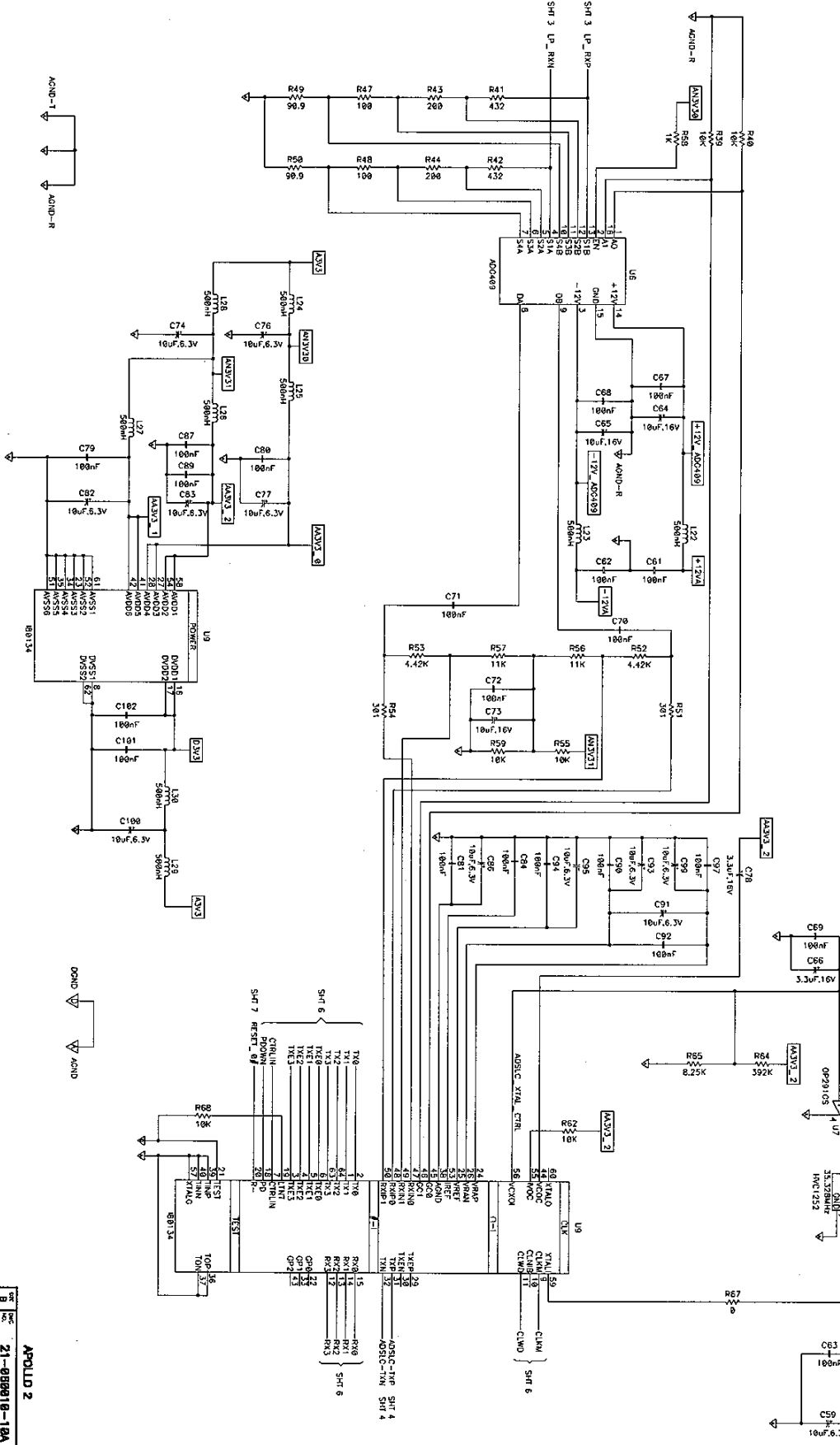
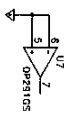
NOTE:
FOR UT (A0813), PM 5.6.26.17.18.19.20
MUST BE TIED TO +12V
ACCORDING TO THE SPECIFICATION.

APOLLO 2

21-059018-10A

REV	DATE	BY	CHKD	APP'D
1	1968	100		

ADSL ANALOG FRONT END



ADSL DIGITAL

