VX-4500 / 4600 Circuit Description

1. Circuit Configuration by Frequency

The receiver is a double-conversion superheterodyne with a first intermediate frequency (IF) of 50.85 MHz and a second IF of 450 kHz. Incoming signal from the antenna is mixed with the local signal from the VCO/PLL to produce the first IF of 50.85MHz. This is then mixed with the 50.45 MHz second local oscillator output to produce the 450 kHz second IF. This is detected to give the demodulated signal. The transmit signal frequencies generated by the PLL VCO and modulated by the signal from the microphone. It is then amplified and sent to the antenna.

2. Receiver System

2-1. Front-end RF amplifier

Incoming RF signal from the antenna is delivered to the RF Unit and passes through Low-pass filer, and removed undesired frequencies by varactor diode tuned band-pass filer consisting of diodes D1013, D1015, D1005, D1022 and Coils L1012 and L1013, capacitors C1090, C1095, C1105, C1107 andC1116,C1117.The passed signal is amplified in Q1021 and moreover cuts animage frequency with the band path filter consisting of Coils L1012, L1015 and L1018,L1033,and capacitors C1130C,1135, C1151, C1156 and C1173,C1181,C1182,C1197 and C1205,C1212,C1217,C1213. and comes into the 1st mixer.

2-2. First Mixer

The 1st mixer consists of the Q1040. Buffered output from the VCO is amplified by Q1026 to provide a pure first local signal between 184.85 and 224.85 MHz for injection to the first mixer. The output IF signal is enters from the mixer to the crystal filter. The IF signal then passes through monolithic crystal filters XF1001 (±5.5 kHz BW) to strip away all but the desired signal.

2-3. IF Amplifier

The first IF signal is amplified by Q1049. The amplified first IF signal is applied to FM IF subsystem IC Q1054which contains the second mixer second local oscillator limiter amplifier noise amplifier and S-meter amplifier. The signal from reference oscillator X1002 becomes 3 times of frequencies in Q1054, it is mixed with the IF signal and becomes 450 kHz. The second IF then passes through the ceramic filter CF1002 (for wide channels) CF1001,CF1003 (for narrow channels) to strip away unwanted mixer products which removes amplitude variations in the 450 kHz IF before detection of the speech by the ceramic discriminator CD1001.

2-4. Audio amplifier

Detected signal from Q1054 is inputted to Q1010 and is output through the band path filter inside Q1010 pin28. When the optional unit is installed the Q1010 is made "OFF" and the AF signal from Q1010 pin21 goes the optional unit. When the optional unit is not installed, Q1010 is made "ON" and the signal goes through Q1010 pin21. The signal then goes through AF mute Q1010 de-emphasis part .amplified with AF power amplifier Q1003 after passing AF volume Q1010. The output of Q1003 (TDA1519CTH) drives a speaker (it chooses the external SP or internal SP in J1001).

2-5. Squelch Circuit

There are 15 levels of squelch setting from 0 to 14. The level 0 means open the squelch. The level 1 means the threshold setting Level and level 14 means tight squelch. From 2 to 13 is established in the middle of threshold and tight. The bigger figure is nearer the tight setting. The level 15 becomes setting of carrier squelch.

2-5-1. Noise Squelch
Noise squelch circuit is composed of the band path filter of Q1054 noise amplifier Q1060 and noise detector D1048, D1052. When a carrier isn't received, the noise ingredient which goes out of the demodulator Q1054 is amplified in Q1060 through the band path filter Q1054 is detected to DC voltage with D1048, D1052 and is inputted to 15 pin the A/D port of the Q1041 CPU. When a carrier is received the DC voltage becomes "LOW" because the noise is compressed. When the detected voltage to CPU is "HIGH," the CPU stops AF output with Q1010 "OFF" by making the 80pin "L"level. When the detection voltage is low the CPU makes Q1010"ON" with making 80pin "H" and the AF signal is output.

2-5-2. Carrier Squelch
The pin 14 (A/D port) of Q1048 CPU detect RSSI voltage output from pin 12 of Q1054, and controls AF output. The RSSI output voltage changes according to the signal strength of carrier. The stronger signal makes the RSSI voltage to be higher voltage. The process of the AF signal control is same as Noise Squelch. The shipping data is adjusted 3dB higher than squelch tight sensitivity.

3. Transmitter System

3-1. MIC Amplifier
The AF signal from microphone jack J2001 (8ch) or J3001 is amplified with microphone amplifier Q1010 is amplified after microphone selection switch Q1010 and passes microphone gain volume Q1010. The control from the CPU it passes output and it passes a pre-emphasis circuit. Q1010 becomes "OFF" when an option unit is attached and the AF signal from Q1010 pin38 goes via the option unit. When an option unit isn't attached Q1010 becomes "ON," the signal passes Q1010 pin 35,34 is input to Q1040 pre-emphasis circuit. The signal passed limiter and splatter filer of Q1010 is adjusted by maximum deviation adjustment volume. The adjusted low frequency signal ingredient is amplified by Q1047 added modulation terminal of TCXO (X1002) the FM modulation is made by reference oscillator.
The high frequency signal ingredient is amplified, and adjusted the level by volume Q1010 to make frequency balance between low frequency. After that it is made FM modulation to transmit carrier by the modulator D1026 of VCO.

3-2. Drive and Final amplifier The modulated signal from the VCO Q1017 is buffered by Q1026 and amplified by Q1023 . The low-level transmit signal is then applied to the Power Module Q1013 for final amplification up to 50 watts output power. The transmit signal then passes low-pass filtered to suppress away harmonic spurious radiation before delivery to the antenna.

3-3. Automatic Transmit Power Control
The output power of Power Module is detected by CM coupler, it is detected by D1005 and D1008 and is input to comparator Q1048. The comparator
compares two different voltages and makes output power stable by controlling the bias voltage of Power Module. There are 3 levels of output power (Hi, Mid and Lo) it is switched by the Voltage of Q1010 pin44.

3-4. PLL Frequency Synthesizer
The frequency synthesizer consists of PLL IC Q1043 VCO, TCXO (X1002) and buffer amplifier. The output frequency from TCXO is 16.8 MHz and the tolerance is ±2.5 ppm (in the temperature range -30 to +60 degrees).

3-4-1. VCO

While the radio is receiving, the RX oscillator Q1034 in VCO generates a programmed frequency between 184.85 and 224.85 MHz as 1st local signal. While the radio is transmitting the TX oscillator Q1031 (2SC3356) in VCO generates a frequency between 134 and 174 MHz. The output from oscillator is amplified by buffer amplifier Q1029 and becomes output of VCO. The output from VCO is divided one is amplified by Q1039 and feed back to pin17 of the PLL IC Q1043. The other is amplified in Q1026 and in case of the reception it is put into the mixer as the 1st local signal through D1020 in transmission it is amplified in Q1029 and more amplified in Q1026 through D1020 and it is put the input terminal of the Power Module Q1013.

3-4-2. VCV CNTL

Tuning voltage (VCV) of VCO is expanding the lock range of VCO by controlling the of varactor diode at the voltage and the control voltage from PLL IC Q1043. Control voltage is added to the varactor diode after converted to D/A converter Q1010 pin45.

3-4-3. PLL

The PLL IC Q1054 consists of reference divider, main divider, phase detector, charge pumps and delta-fractional accumulator. The reference frequency from TCXO is inputted to pin 8 of PLL IC Q1054 (TRF3750IP) and is divided by reference divider. This IC is decimal point dividing PLL IC Q1054 (TRF3750IP) and the dividing ratio becomes 1/8 of usual PLL frequency step. Therefore, the output of reference divider is 8 times of frequencies of the channel step. For example when the channel stepping is 5 kHz, the output of reference divider becomes 40 kHz. The other hand, inputted feed back signal to pin 6 of PLL IC Q1054 (TRF3750IP) from VCO is divided with the dividing ratio which becomes same frequency as the output of reference divider. These two signals are compared by phase detector, the phase difference pulse is generated. The phase difference pulse and the pulse from fractional accumulator pass through the charge pumps and LPF. It becomes the DC voltage (VCV) to control the VCO. The oscillation frequency of VCO is locked by the control of this DC voltage. The PLL serial data from CPU Q1065 (CPU: LC87F5CC8A) is sent with three lines of SDO (pin 12), SCK (pin 11) and PSTB (pin 13). The lock condition of PLL is output from the UL (pin 14) terminal and UL becomes “H” at the time of the lock condition and becomes “L” at the time of the unlocked condition. The CPU Q1065 (CPU: LC87F5CC8A) always watches over the UL condition, and when it becomes “ L ” unlocked condition, the CPU Q1065 (CPU:LC87F5CC8A) prohibits transmitting and receiving.