Circuit Description of the CST801VI Transmitter
The CST801VI is broken down into 4 sections.

Audio - audio amplifier, pre-emphasis, audio deviation adjustment, and agc limiting.

Txco/Pll - phase lock loop, loop filter, Reference Oscillator, VCO, and VCO Buffer

OOL - out of lock detection, pre-amplifier, and RF final amplifier.

DC - DC - dc to dc converter

Audio Section:

The transmitter audio is amplified by U7A, the resistors (R45 and R48) and capacitors (C55 and C56) create the 6 Dbm/Octive pre-emphasis curve from 300 – 3000 Hz. The out put of the Op Amp U7 is ac coupled to a diode rectifier (D1) this voltage is filtered by C52 which drives the audio limiting FET (Q5). The drain to source impedance shorts some of the audio to ground to prevent over modulation. (R35) adjusts the amount of transmitted audio deviation.

Txco/Pll Section:

The 12.8 Mhz reference Oscillator (Y2) provides the 5 ppm Transmitter Temperature Stability over the range of -30 to +60 degree C. The TX frequency adjustment is controlled by (R11).
The Phase Lock Loop (U6) contains 3 programmable counters which are loaded by a serial data stream from the microprocessor (U3). The frequency is loaded into the B and A counters and the step size is loaded into the R counter.
The Voltage controlled oscillator (Q6) is connected to a VCO/Buffer (U2), the 2 outputs from the buffer connect to the pre-amplifier and the other is applied to the phase detector of the PLL (U6). The output of the phase detector pin 2 of (U6) is filtered into a dc voltage by the loop filter (C46,C47,R34,R16). This voltage is applied to the VCO varactor (D2) which changes capacitance with voltage moving the VCO frequency.

Out of Lock
RF amplifier Section:

When the VCO frequency is locked to the programmed transmitter frequency a logic level high from pin 14 of the PLL (U6) is applied to the N channel FET (Q3) which turns on the P channel FET (Q1) applying a dc bias voltage to the pre-amplifier (Q4) and the RF final Amplifier (Q2).

The output from the VCO/Buffer (U2) is amplified by the pre-amp (Q4), its output level is +10 dBm. The collector of (Q4) is loaded into the final amplifier by the LC network of (C3,C58,L1). (Q2) the RF final amplifier has ~ 13 dBm of gain from 150 – 174 Mhz. The drain of the final amplifier is match into 50 ohms through the LC network of (L8,C38,C39) an additional low pass filter (C40,L9,C70) is added to provide more harmonic attenuation.

DC – DC Converter :

U1 on the dc – dc pcb converters the pager 1.5 volts to 3.0 volts through the switching mode converter. The 3.0 volts is applied to the TX pcb and is regulated down to 2.85 volts to supply all the digital components on the transmitter. The 3.0 volts from the dc-dc converter is only applied to the RF Final transistor (Q2).