Exhibit C

Measurement Report

NATIONAL DATACOMM

CORPORATION

FCC ID.:IOU0610S01

Wireless LAN PC Card

FCC Part 15
EMI TEST REPORT

of

E.U.T. : Wireless LAN PC Card

MODEL : NW610

FCC ID. : IOU0610S01

for

APPLICANT : NATIONAL DATACOMM CORPORATION

ADDRESS : 2F, No. 28, Industry East 9th Road, Science Park, Hsin-Chu, Taiwan, R.O.C.

Test Performed by

ELECTRONICS TESTING CENTER, TAIWAN
NO. 8 LANE 29, WENMIMG ROAD,
LOSHAN TSUN, KWEISHAN HSIANG,
TAOYUAN, TAIWAN, R.O.C.

Tel:(03)3280026-32
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Report Number : ET87R-02-081
Issued Date : APR. 03, 1998

TEST REPORT CERTITIFICATION

Applicant	: NATIONAL DATACOMM CORPORATION 2F, No. 28, Industry East 9th Road, Science Park, Hsin-Chu, Taiwan, R.O.C.
Manufacturer	: NATIONAL DATACOMM CORPORATION 2F, No. 28, Industry East 9th Road, Science Park, Hsin-Chu, Taiwan, R.O.C.
Description of EUT	:
a) Type of EUT	: Wireless LAN PC Card
b) Trade Name	: InstantWave
c) Model No.	: NW610
d) Power Supply	: DC 5V
Regulation Applied	: FCC Rules and Regulations Part 15 Subpart B & C(1993)

I HEREBY CERTIFY THAT: The data shown in this report were made in accordance with the procedures given in ANSI C63.4, and the energy emitted by the device was founded to be within the limits applicable. I assume full responsibility for accuracy and completeness of these data.

Note: 1. The result of the testing report relate only to the item tested.
2. The testing report shall not be reproduced expect in full, without the written approval of ETC.

Test Date : MAR. 10, 1998

Test Engineer : Chin Cheng Yeh.
(Chin Cheng Yeh)

Approve & Authorized Signer : Will Yauo
Will Yauo, Supervisor
EMI Test Site of ELECTRONICS
TESTING CENTER, TAIWAN

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1 GENERAL INFORMATION

1.1 Product Description

a) Type of EUT : Wireless LAN PC Card

b) Trade Name : InstantWave

c) Model No. : NW610

d) Power Supply : DC 5V

1.2 Characteristics of Device

The Wireless LAN PC Card comply with the IEEE 802.11 wireless standard (Frequency-Hopping). The adaptor provide a physical interface with the wireless medium.

1.3 Test Methodology

For Wireless LAN PC Card, both conducted and radiated emissions were performed according to the procedures illustrated in ANSI C63.4(1992) and for processing gain measurement is according to FCC Public Notice. Other required measurements were illustrated in separate sections of this test report for details.

1.4 Test Facility

The open area test site and conducted measurement facility used to collect the radiated data is located on the roof top of Building at No.34, 5 Lirn, Din Fu Tsun, Lin Kou, Taipei, Taiwan, R.O.C.

This site has been fully described in a report submitted to your office, and accepted in a letter dated Feb. 10 , 1997.

2 PROVISIONS APPLICABLE

2.1 Definition

Unintentional radiator:
A device that intentionally generates and radio frequency energy for use within the device, or that sends radio frequency signals by conduction to associated equipment via connecting wiring, but which is not intended to emit RF energy by radiation or induction.

Class A Digital Device:
A digital device which is marketed for use in commercial or business environment; exclusive of a device which is market for use by the general public, or which is intended to be used in the home.

Class B Digital Device :
A digital device which is marketed for use in a residential environment notwithstanding use in a commercial, business of industrial environment. Example of such devices that are marketed for the general public.

Note : A manufacturer may also qualify a device intended to be marketed in a commercial, business, or industrial environment as a Class B digital device, and in fact is encouraged to do so, provided the device complies with the technical specifications for a Class B Digital Device. In the event that a particular type of device has been found to repeatedly cause harmful interference to radio communications, the Commission may classify such a digital device as a Class B Digital Device, Regardless of its intended use.

Intentional radiator:
A device that intentionally generates and emits radio frequency energy by radiation or induction.

2.2 Requirement for Compliance

(1) Conducted Emission Requirement

For unintentional device, according to § 15.107(a) Line Conducted Emission Limits is as following:

Frequency MHz	Emissions μV	Emissions dBμV
0.45 - 30.0	250	48.0

For intentional device, according to § 15.207(a) Line Conducted Emission Limits is same as above table.

(2) Radiated Emission Requirement

For unintentional device, according to § 15.109(a), except for Class A digital devices, the field strength of radiated emissions from unintentional radiators at a distance of 3 meters shall not exceed the following values:

Frequency MHz	Distance Meters	Radiated dBμV/m	Radiated μV/m
30 - 88	3	40.0	100
88 - 216	3	43.5	150
216 - 960	3	46.0	200
above 960	3	54.0	500

For intentional device, according to § 15.209(a), the general requirement of field strength of radiated emissions from intentional radiators at a distance of 3 meters shall not exceed the above table.

(3) Antenna Requirement

For intentional device, according to § 15.203, an intentional radiator shall be designed to ensure that no antenna other than that furnished by the responsible party shall be used with the device.

(4) Channel Separation

According to 15.247(a)(1), frequency hopping system shall have, hopping channel carrier frequencies separated by a minimum of 25 kHz or the 20 dB bandwidth of the hopping channel.

(5) Hopping Frequencies Requirement

According to 15.247(a)(1)(ii), for hopping system operating in the 2400-2483.5 MHz and 5725-5850 MHz bands shall use at least 75 hopping frequencies.

(6) Bandwidth Requirement

According to 15.247(a)(1)(ii), for hopping system operating in the 2400-2483.5 MHz and 5725-5850 MHz bands, the maximum 20dB bandwidth is 1 MHz. And the average time of occupancy on any frequency shall not be greater than 0.4 seconds with a 30 second period.

(7) Output Power Requirement

For direct sequence system and hopping system, according to 15.247(b), the maximum peak output power of the transmitter shall not exceed 1 Watt. If transmitting antennas of directional gain greater than 6 dBi are used, the power shall be reduced by the amount in dB that the directional gain of the antenna exceeds 6 dBi.

(8) 100 kHz Bandwidth of Frequency Band Edges Requirement

According to 15.247(c), if any 100 kHz bandwidth outside these frequency bands, the radio frequency power that is produced by the modulation products of the spreading sequence, the information sequence and the carrier frequency shall be either at least 20 dB below that in any 100 kHz bandwidth within the band that contains the highest level of the desired power or shall not exceed the general levels specified in § 15.209(a), whichever results in the lesser attenuation.

2.3 Restricted Bands of Operation

Only spurious emissions are permitted in any of the frequency bands listed below :

MHz	MHz	MHz	GHz
0.090 - 0.110	16.42-16.423	399.9-410	4.5-5.25
0.495 - 0.505 **	16.69475 - 16.69525	608-614	5.35-5.46
2.1735 - 2.1905	16.80425 - 16.80475	960-1240	7.25-7.75
4.125-4.128	25.5-25.67	1300-1427	8.025-8.5
4.17725-4.17775	37.5-38.25	1435-1626.5	9.0-9.2
4.20725-4.20775	73-74.6	1645.5-1646.5	9.3-9.5
6.215-6.218	74.8-75.2	1660-1710	10.6-12.7
6.26775-6.26825	108-121.94	1718.8-1722.2	13.25-13.4
6.31175-6.31225	123-138	2200-2300	14.47-14.5
8.291-8.294	149.9-150.05	2310-2390	15.35-16.2
8.362-8.366	156.52475 - 156.52525	2483.5-2500	17.7-21.4
8.37625-8.38675	156.7-156.9	2655-2900	22.01-23.12
8.41425-8.41475	162.0125-167.17	3260-3267	23.6-24.0
12.29-12.293	167.72-173.2	3332-3339	31.2-31.8
12.51975-12.52025	240-285	3345.8-3358	36.43-36.5
12.57675-12.57725	322-335.4	3360-4400	Above 38.6
13.36-13.41			

** : Until February 1, 1999, this restricted band shall be 0.490-0.510 MHz

2.4 Labeling Requirement

The device shall bear the following statement in a conspicuous location on the device :

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions : (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

2.5 User Information

The users manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

For a Class B digital device or peripheral, the instructions furnished the user shall include the following or similar statement, placed in a prominent location in the text of the manual.

The Federal Communications Commission Radio Frequency Interference Statement includes the following paragraph.

This equipment has been tested and found to comply with the limits for a Class B Digital Device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction may cause harmful interference to radio communication. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-- Reorient or relocate the receiving antenna.

-- Increase the separation between the equipment and receiver.

-- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-- Consult the dealer or an experienced radio / TV technician for help.

3. SYSTEM TEST CONFIGURATION

3.1 Justification

For both radiated and conducted emissions below 1 GHz, the system was configured for testing in a typical fashion as a customer would normally use it. The peripherals other than EUT were connected in normally standing by situation. Measurement was performed under the condition that a computer program was exercised to simulate data communication of EUT, and the transmission rate was set to maximum allowed by EUT. Three highest emissions were verified with varying placement of cables to maximize the emission from EUT.

For conducted emissions, only measured on TX and RX operation, for the digital circuits portion also function normally whenever TX or RX is operated.

Measurement of radiated emissions from digital circuits is performed with system in hopping mode. And for emissions from RF portion, in order to make a accuracy measurement, transmitting frequencies was set to stable situation by software control, and not in frequency hopping mode.

3.2 Devices for Tested System

Device	Manufacture	Model / FCC ID.	Description
Wireless LAN PC Card *	NATIONAL DATACOMM CORPORATION	NW610 IOU0610S01	----
Monitor	IBM Co.	8512-001 C5F7NF13CM14	1.8m Unshielded
Notebook	Digital	A09-97ZNOTE	1.8m Unshielded with One Ferrite Core
Keyboard	Microsoft	E03786URETI CIGE03786	1.8m Shielded
Modem	SmarTeam	1200AT EF56A51200AT	1.5m Shielded Cable 1.9m Adapter Cord
Mouse	Hewlett-Packard	M-S34 DZL211029	1.8m Shielded

Remark "*" means equipment under test.

4 RADIATED EMISSION MEASUREMENT

4.1 Applicable Standard

For unintentional radiator, the radiated emission shall comply with § 15.109(a).

For intentional radiators, according to § 15.247 (a), operation under this provision is limited to frequency hopping and direct sequence spread spectrum, and the out band emission shall be comply with § 15.247 (c)

4.2 Measurement Procedure

1. Setup the configuration per figure 1 and 2 for frequencies measured below and above 1 GHz respectively.
2. For emission frequencies measured below 1 GHz, a pre-scan is performed in a shielded chamber to determine the accurate frequencies of higher emissions will be checked on a open test site. As the same purpose, for emission frequencies measured above 1 GHz, a pre-scan also be performed with a 1 meter measuring distance before final test.
3. For emission frequencies measured below and above 1 GHz, set the spectrum analyzer on a 100 kHz and 1 MHz resolution bandwidth respectively for each frequency measured in step 2.
4. The search antenna is to be raised and lowered over a range from 1 to 4 meters in horizontally polarized orientation. Position the highness when the highest value is indicated on spectrum analyzer, then change the orientation of EUT on test table over a range from 0 ° to 360 ° with a speed as slow as possible, and keep the azimuth that highest emission is indicated on the spectrum analyzer. Vary the antenna position again and record the highest value as a final reading. A RF test receiver is also used to confirm emissions measured.

   Note : A high pass filter was used to avoid pre-amplifier saturated when measure TX operation mode in frequency band above 1 GHz.
5. Repeat step 4 until all frequencies need to be measured were complete.
6. Repeat step 5 with search antenna in vertical polarized orientations.
7. Check the three frequencies of highest emission with varying the placement of cables associated with EUT to obtain the worse case and record the result.

Figure 1 : Frequencies measured below 1 GHz configuration

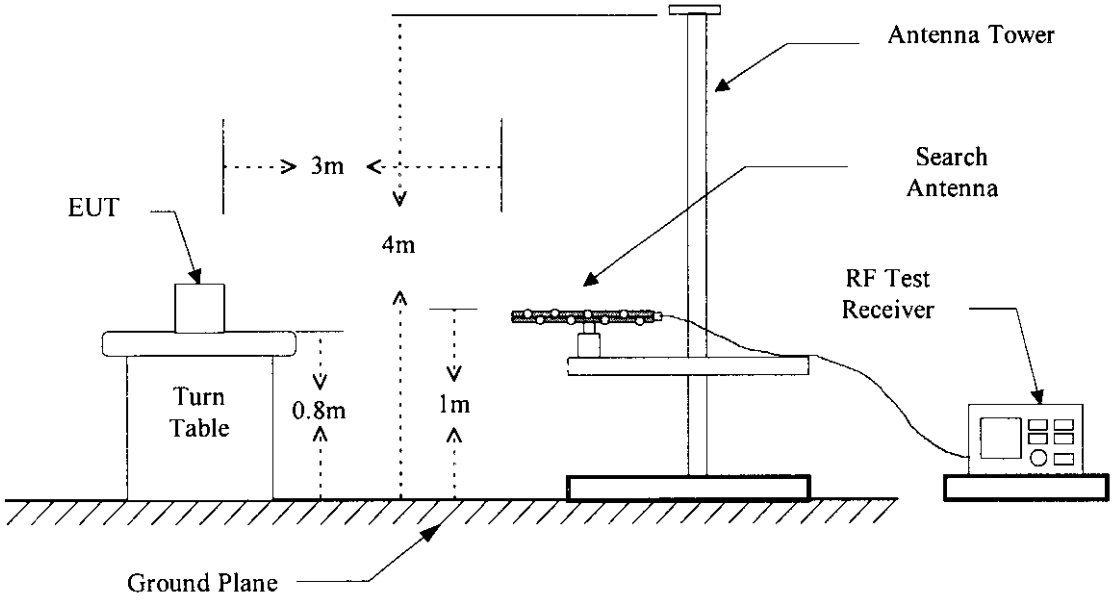
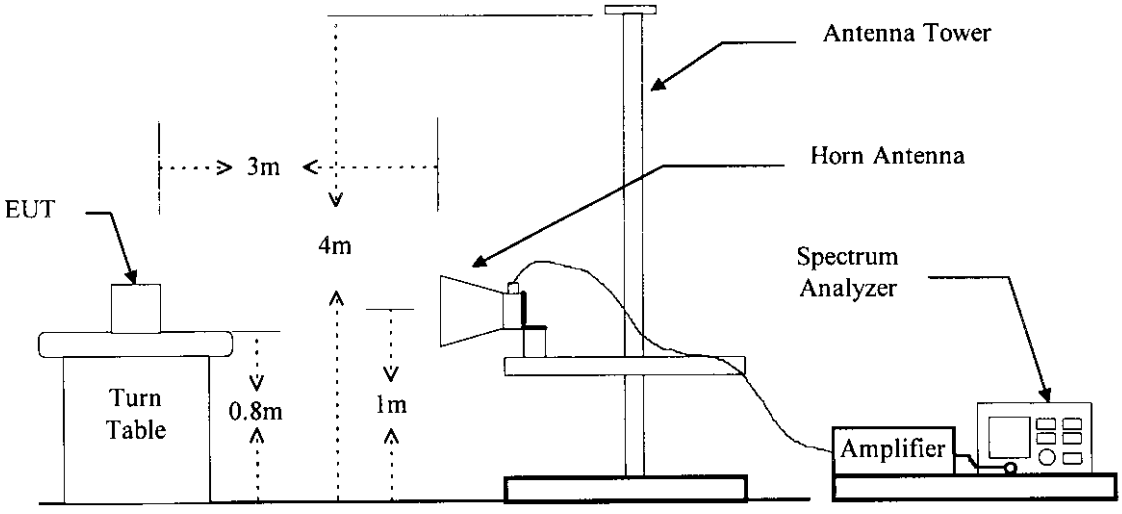


Figure 2 : Frequencies measured above 1 GHz configuration



4.3 Measuring Instrument

The following instrument are used for radiated emissions measurement :

Equipment	Manufacturer	Model No.	Next Cal. Date
Spectrum Analyzer	Hewlett-Packard	8568B	OCT. 16, 1998
Pre-selector	Hewlett-Packard	85685A	OCT. 16, 1998
Quasi Peak Detector	Hewlett-Packard	85650A	OCT. 07, 1998
Spectrum Analyzer	Hewlett-Packard	8563A	NOV. 16, 1998
RF Test Receiver	Hewlett-Packard	8546A	FEB. 11, 1998
RF Test Receiver	Rohde & Schwarz	ESVS 30	DEC. 19, 1998
Horn Antenna	EMCO	3115	AUG. 05, 1998
Double Ridge Guide Horn Antenna	EMCO	3116	MAY 08, 1998
Log periodic Antenna	EMCO	3146	DEC. 10, 1999
Biconical Antenna	EMCO	3110B	AUG. 05, 1998
Preamplifier	Hewlett-Packard	8449B	MAY 08, 1998
Preamplifier	Hewlett-Packard	8447D	DEC. 23, 1998

Measuring instrument setup in measured frequency band when specified detector function is used :

Frequency Band (MHz)	Instrument	Function	Resolution bandwidth	Video Bandwidth
30 to 1000	RF Test Receiver	Quasi-Peak	120 kHz	N/A
	Spectrum Analyzer	Peak	100 kHz	100 kHz
Above 1000	Spectrum Analyzer	Peak	1 MHz	1 MHz
	Spectrum Analyzer	Average	1 MHz	300 Hz

4.4 Radiated Emission Data

4.4.1 RF Emissions

a) Channel 2

Operation Mode : Tx / Rx

Local Frequency : 1081 MHz

Fundamental Frequency : 2401.993 MHz

Test Date : MAR. 10, 1998 Temperature : 25 ℃ Humidity : 55%

Frequency	Meter Reading @3m Peak (dBuV)		Corrected Factor	Result (dBuV/m)		Limit @3m	Margin
(MHz)	H	V	(dB)	H	V	(dBuV/m)	(dB)
4804.007	44.3	42.4	2.5	46.8	44.9	54.0	-7.2
7206.000	38.8	42.5	5.2	44.0	47.7	54.0	-6.3
9607.993	--	--	6.9	--	--	54.0	--
12009.965	--	--	9.2	--	--	54.0	--
14411.958	--	--	11.5	--	--	54.0	--
16813.951	--	--	11.8	--	--	54.0	--
19215.944	--	--	8.9	--	--	54.0	--
21617.937	--	--	9.7	--	--	54.0	--
24019.930	--	--	10.3	--	--	54.0	--

Note :

1. Remark "--" means that the emission level is too low to be measured.
2. Measuring data showed on above table was derived with peak detector function.

b) Channel 40

Operation Mode : Tx / Rx

Local Frequency : 1100 MHz

Fundamental Frequency : 2439.937 MHz

Test Date : MAR. 10, 1998 Temperature : 25 ℃ Humidity : 55%

Frequency (MHz)	Meter Reading @3m (dBuV)		Corrected Factor (dB)	Result (dBuV/m)		Limit @3m (dBuV/m)	Margin (dB)
	H	V		H	V		
4879.895	46.8	47.9	2.5	49.3	50.4	54.0	-3.6
7319.832	36.3	38.5	5.4	41.7	43.9	54.0	-10.1
9759.760	--	--	7.2	--	--	54.0	--
12199.685	--	--	9.3	--	--	54.0	--
14639.622	--	--	11.6	--	--	54.0	--
17079.559	--	--	13.3	--	--	54.0	--
19519.496	--	--	8.5	--	--	54.0	--
21959.433	--	--	9.9	--	--	54.0	--
24399.370	--	--	10.7	--	--	54.0	--

Note :

1. Remark "--" means that the emission level is too low to be measured.
2. Measuring data showed on above table was derived with peak detector function.

c) Channel 80

Operation Mode : Tx / Rx

Local Frequency : 1120 MHz

Fundamental Frequency : 2480.020 MHz

Test Date : MAR. 10, 1998 Temperature : 25 ℃ Humidity : 55%

Frequency	Meter Reading @3m (dBuV)		Corrected Factor	Result (dBuV/m)		Limit @3m	Margin
(MHz)	H	V	(dB)	H	V	(dBuV/m)	(dB)
4960.060	49.5	50.0	3.0	52.5	53.0	54.0	-1.0
7440.080	38.4	41.4	5.8	44.2	47.2	54.0	-6.8
9920.100	--	--	7.2	--	--	54.0	--
12400.100	--	--	9.4	--	--	54.0	--
14880.120	--	--	11.5	--	--	54.0	--
17360.140	--	--	15.2	--	--	54.0	--
19840.160	--	--	8.6	--	--	54.0	--
22320.180	--	--	10.2	--	--	54.0	--
24800.200	--	--	11.0	--	--	54.0	--

Note :

1. Remark "--" means that the emission level is too low to be measured.
2. Measuring data showed on above table was derived with peak detector function.

4.4.2 Other Emissions

a) Emission frequencies below 1 GHz

Operation Mode : Tx / Rx

Test Date : MAR. 10, 1998 Temperature : 25 ℃ Humidity : 55%

Frequency	Meter Reading @3m (dBuV)		Corrected Factor	Result (dBuV/m)		Limit @3m	Margin
(MHz)	H	V	(dB)	H	V	(dBuV/m)	(dB)
38.179	32.6	47.2	-12.2	20.4	35.0	40.0	-5.0
69.633	41.0	47.8	-16.4	24.6	31.4	40.0	-8.6
140.279	48.0	42.0	-11.2	36.8	30.8	43.5	-6.7
149.629	47.2	49.2	-10.4	36.8	38.8	43.5	-4.7
199.900	38.4	39.0	-8.8	29.6	30.2	43.5	-13.3
548.879	40.9	40.7	-3.3	37.6	37.4	46.0	-8.4

4.5 Field Strength Calculation

The field strength is calculated by adding the Antenna Factor, High Pass Filter Loss(if used) and Cable Loss, and subtracting the Amplifier Gain (if any) from the measured reading. The basic equation calculation is as follows:

Result = Reading + Corrected Factor

where Corrected Factor

= Antenna FACTOR + Cable Loss + High Pass Filter Loss - Amplifier Gain

5 CONDUCTED EMISSION MEASUREMENT

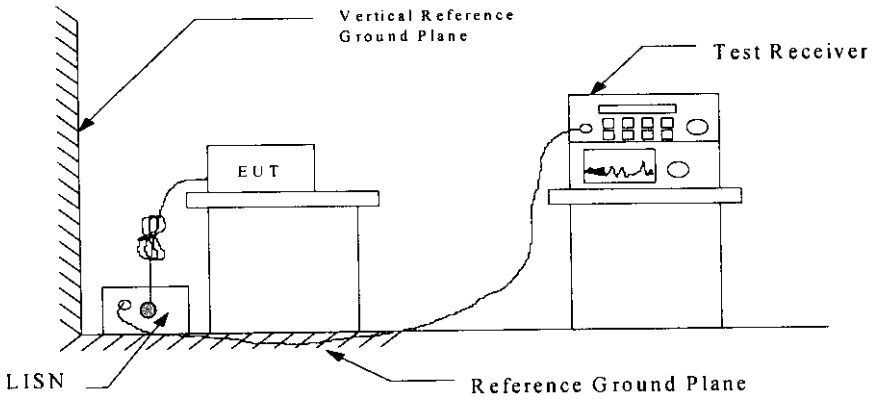
5.1 Standard Applicable

For unintentional and intentional device, Line Conducted Emission Limits are in accordance to § 15.107(a) and § 15.207(a) respectively. Both Limits are identical specification.

5.2 Measurement Procedure

1. Setup the configuration per figure 3.
2. A preliminary scan with a spectrum monitor is performed to identify the frequency of emission that has the highest amplitude relative to the limit by operating the EUT in selected modes of operation, typical cable positions, and with a typical system configuration.
3. Record the 6 or 8 highest emissions relative to the limit.
4. Measure each frequency obtained from step 3 by a test receiver set on quasi peak detector function, and then record the accuracy frequency and emission level. If all emissions measured in the specified band are attenuated more than 20 dB from the limit, this step would be ignored, and the peak detector function would be used.
5. Confirm the highest three emissions with variation of the EUT cable configuration and record the final data.
6. Repeat all above procedures on measuring each operation mode of EUT.

Figure 3 : Conducted emissions measurement configuration



5.3 Conducted Emission Data

a) Channel 2

Operation Mode : Tx ./ Rx
Test Date : MAR. 10, 1998 Temperature : 25 ℃ Humidity: 60%

Frequency (MHz)	Reading (dBuV)		Factor (dB)	Result (dBuV)		Limit (dBuV)	Margin (dB)
	Va	Vb		Va	Vb		
0.5759	38.6	37.4	0.3	38.9	37.7	48.0	-9.1
1.2801	31.4	28.2	0.3	31.7	28.5	48.0	-16.3
1.6889	39.3	38.6	0.3	39.6	38.9	48.0	-8.4
1.9489	36.4	34.2	0.3	36.7	34.5	48.0	-11.3
5.7072	35.8	32.4	0.4	36.2	32.8	48.0	-11.8
6.9544	33.3	31.8	0.4	33.7	32.2	48.0	-14.3

b) Channel 40

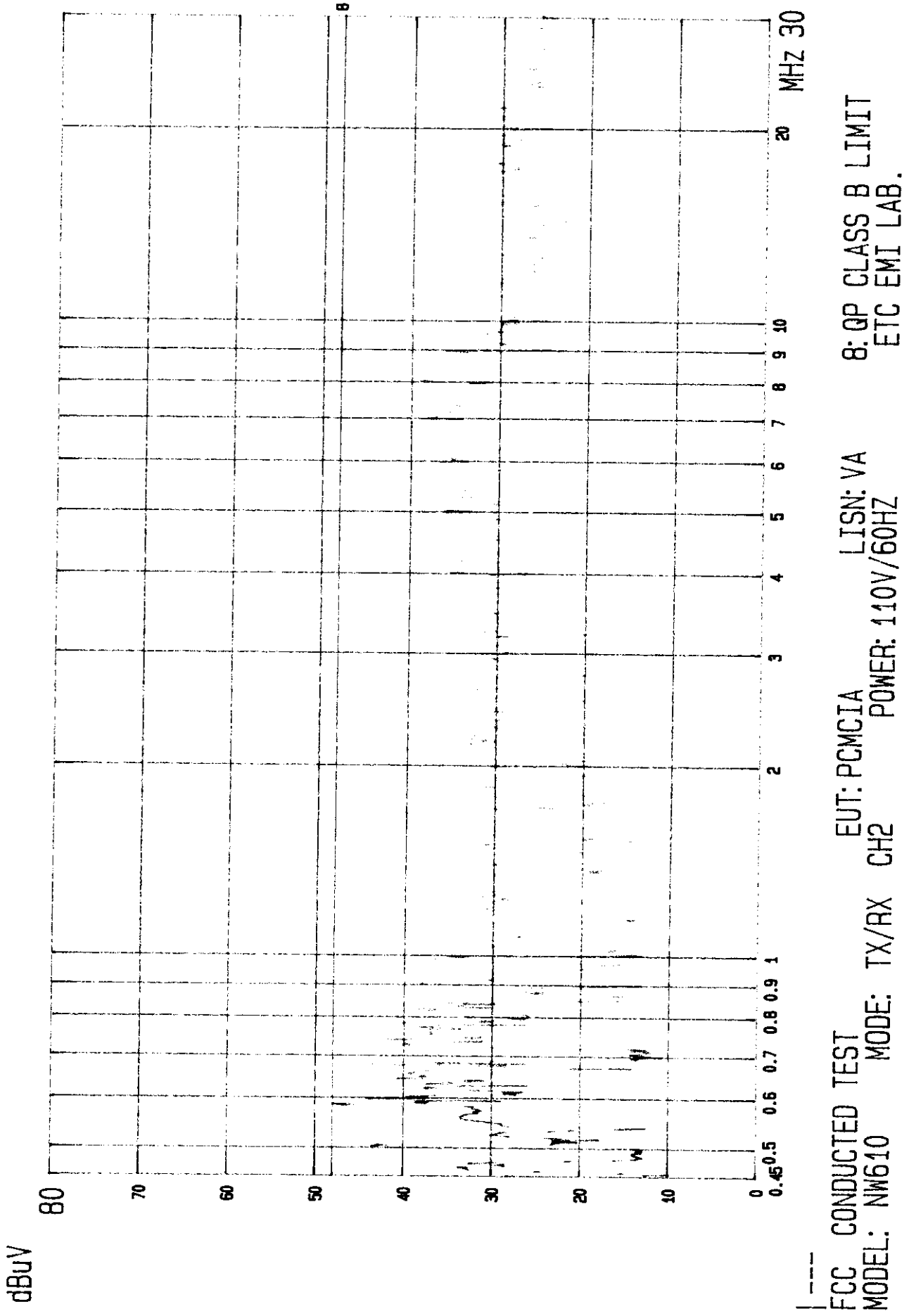
Operation Mode : Tx / Rx
Test Date : MAR. 10, 1998 Temperature : 25 ℃ Humidity: 60%

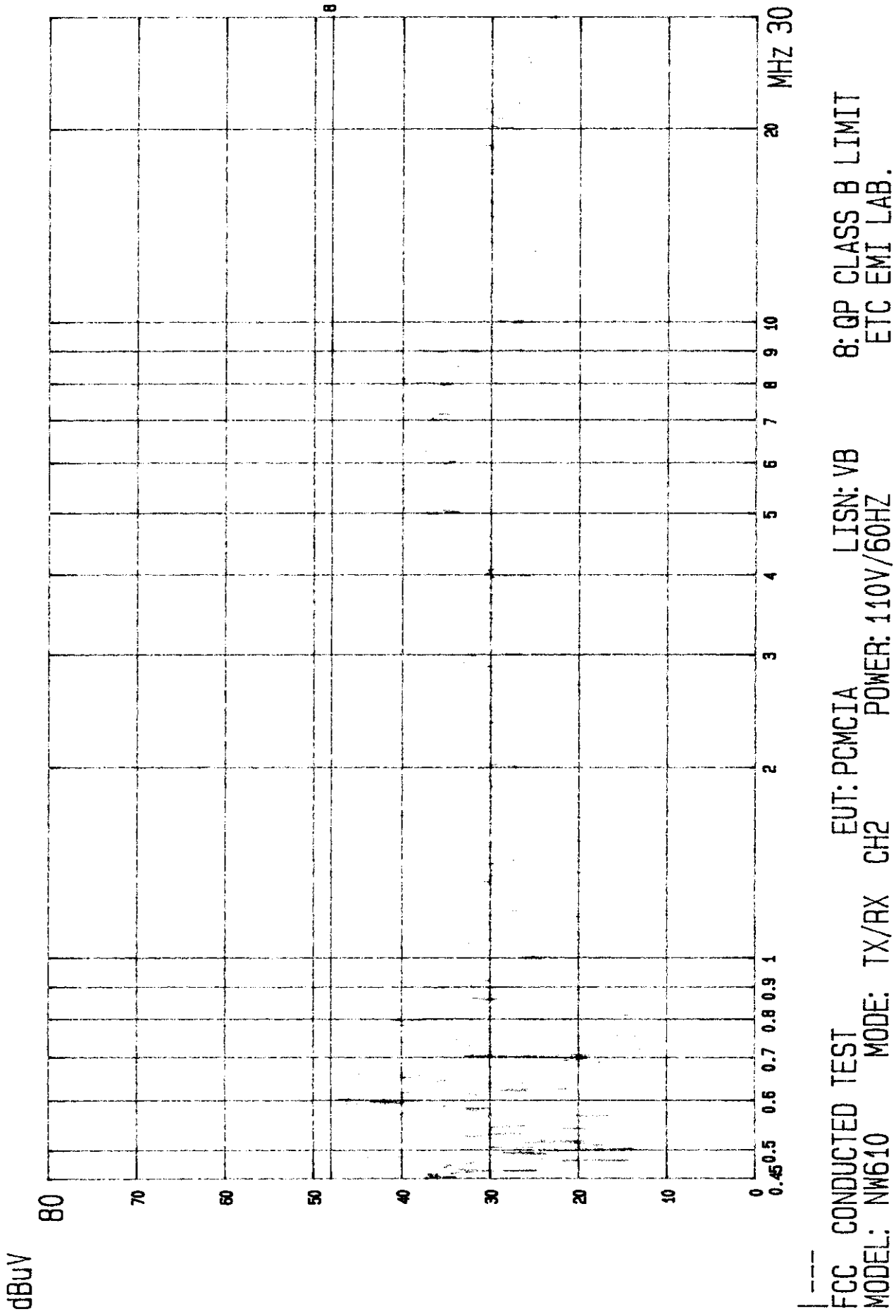
Frequency (MHz)	Reading (dBuV)		Factor (dB)	Result (dBuV)		Limit (dBuV)	Margin (dB)
	Va	Vb		Va	Vb		
0.4525	39.8	38.6	0.3	40.1	38.9	48.0	-7.9
0.9148	33.4	32.4	0.3	33.7	32.7	48.0	-14.3
1.6896	39.4	34.7	0.3	39.7	35.0	48.0	-8.3
1.9506	38.4	37.4	0.3	38.7	37.7	48.0	-9.3
2.0187	32.3	30.9	0.3	32.6	31.2	48.0	-15.4
5.3009	28.4	27.1	0.3	28.7	27.4	48.0	-19.3
6.4078	34.8	33.4	0.3	35.1	33.7	48.0	-12.9
6.9446	35.1	34.6	0.4	35.5	35.0	48.0	-12.5

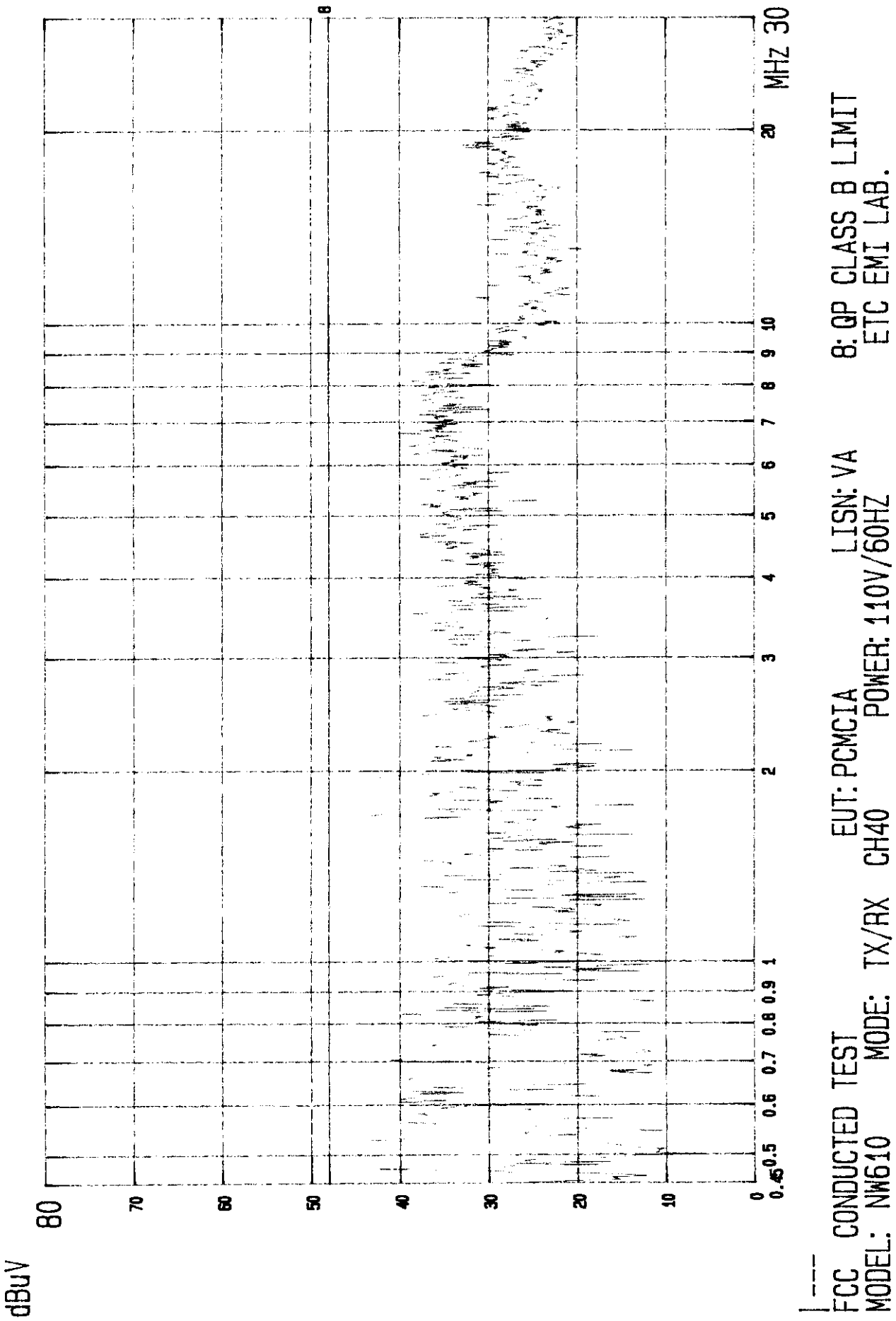
c) Channel 80

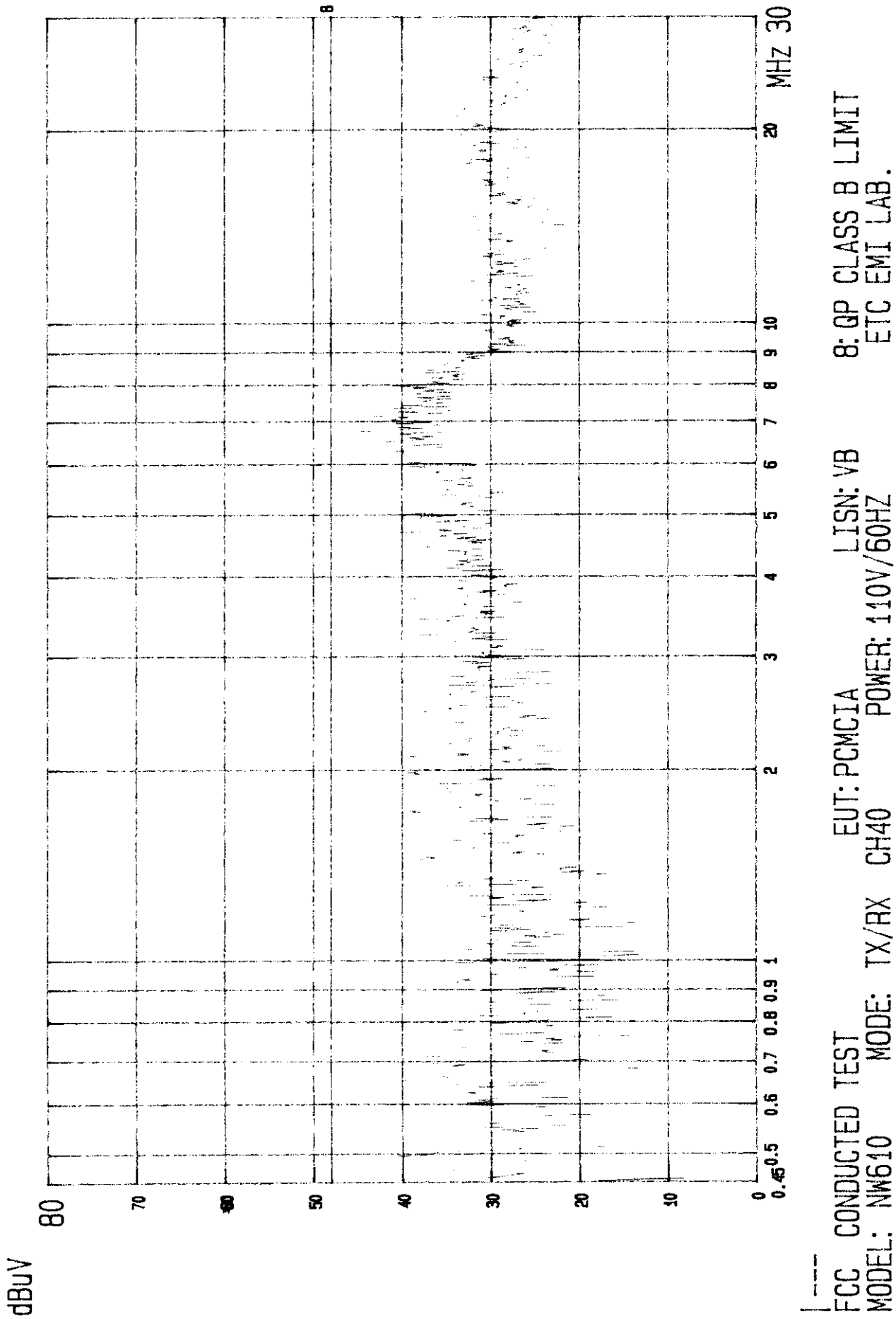
Operation Mode : Tx / Rx
Test Date : MAR. 10, 1998 Temperature : 25 ℃ Humidity: 60%

Frequency (MHz)	Reading (dBuV)		Factor (dB)	Result (dBuV)		Limit (dBuV)	Margin (dB)
	Va	Vb		Va	Vb		
0.4817	36.4	40.3	0.3	36.7	40.6	48.0	-7.4
0.6558	34.6	36.9	0.3	34.9	37.2	48.0	-10.8
1.4367	36.2	34.2	0.3	36.5	34.5	48.0	-11.5
1.6926	39.8	38.6	0.3	40.1	38.9	48.0	-7.9
4.7786	34.2	33.6	0.3	34.5	33.9	48.0	-13.5
6.6193	33.4	34.8	0.4	33.8	35.2	48.0	-12.8


FCC CONDUCTED TEST
MODEL: NW610 MODE: TX/RX CH2
EUT: PCMCIA LISN: VA
POWER: 110V/60HZ
8: QP CLASS B LIMIT
ETC EMI LAB.
dBuV
80
70
60
50
40
30
20
10
0
0.45
0.5
0.6
0.7
0.8
0.9
1
2
3
4
5
6
7
8
9
10
20
MHz 30


FCC CONDUCTED TEST
MODEL: NW610 MODE: TX/RX CH2
EUT: PCMCIA LISN: VB
POWER: 110V/60HZ
8: QP CLASS B LIMIT
ETC EMI LAB.
dBuV
80
70
60
50
40
30
20
10
0
0.45
0.5
0.6
0.7
0.8
0.9
1
2
3
4
5
6
7
8
9
10
20
MHz 30


dBuV
80
70
60
50
40
30
20
10
0
0.45
0.5
0.6
0.7
0.8
0.9
1
2
3
4
5
6
7
8
9
10
20
MHz 30
FCC CONDUCTED TEST
MODEL: NW610 MODE: TX/RX CH40
EUT: PCMCIA LISN: VA
POWER: 110V/60HZ
8: QP CLASS B LIMIT
ETC EMI LAB.


FCC CONDUCTED TEST
MODEL: NW610
MODE: TX/RX CH40
EUT: PCMCIA
LISN: VB
POWER: 110V/60HZ
8: QP CLASS B LIMIT
ETC EMI LAB.
dBuV
80
70
60
50
40
30
20
10
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0.45
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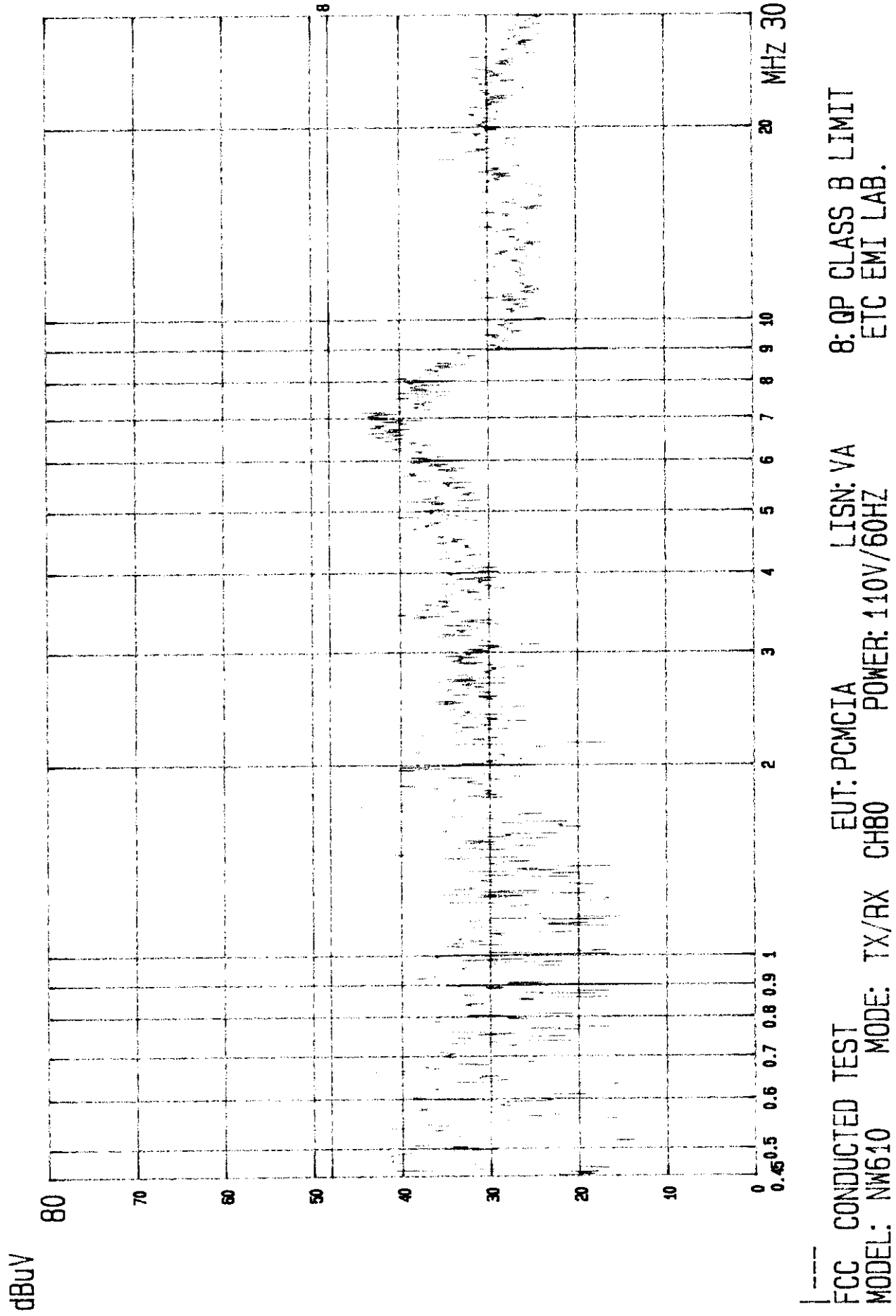
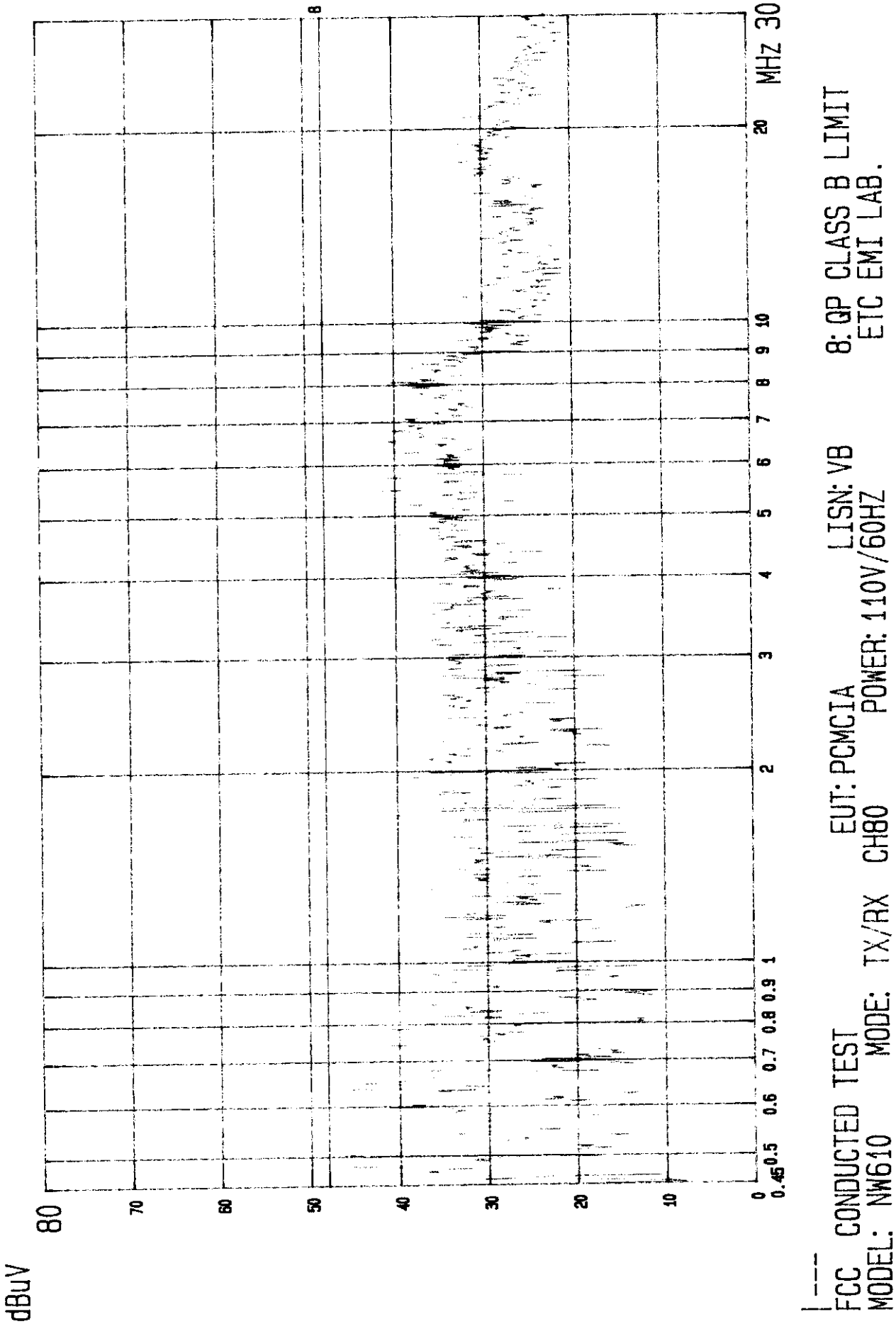
20
MHz 30


dBuV
80
70
60
50
40
30
20
10
0
0.45
0.5
0.6
0.7
0.8
0.9
1
2
3
4
5
6
7
8
9
10
20
MHz 30
FCC CONDUCTED TEST
MODEL: NW610
MODE: TX/RX CH80
EUT: PCMCIA
POWER: 110V/60HZ
LISN: VA
8: QP CLASS B LIMIT
ETC EMI LAB.


dBuV
80
70
60
50
40
30
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10
0
0.45
0.5
0.6
0.7
0.8
0.9
1
2
3
4
5
6
7
8
9
10
20
MHz 30
FCC CONDUCTED TEST
MODEL: NW610
MODE: TX/RX CH80
EUT: PCMCIA
POWER: 110V/60HZ
LISN: VB
8: QP CLASS B LIMIT
ETC EMI LAB.

5.4 Result Data Calculation

The result data is calculated by adding the LISN Factor to the measured reading. The basic equation with a sample calculation is as follows:

RESULT = READING + LISN FACTOR

Assume a receiver reading of 22.5 dB μ V is obtained, and LISN Factor is 0.1 dB, then the total of disturbance voltage is 22.6 dB μ V.

RESULT = 22.5 + 0.1 = 22.6 dB μ V

Level in μ V = Common Antilogarithm[(22.6 dB μ V)/20]

= 13.48 μ V

5.5 Conducted Measurement Equipment

The following test equipment are used during the conducted test .

Equipment	Manufacturer	Model No.	Next Cal. Date
RF Test Receiver	Rohde and Schwarz	ESH3	JAN. 04, 1999
Spectrum Monitor	Rohde and Schwarz	EZM	N.C.R.
Line Impedance Stabilization network	Kyoritsu	KNW-407	DEC. 01, 1998
Plotter	Hewlett-Packard	7440A	N/A
Shielded Room	Riken	----	N.C.R.

6 ANTENNA REQUIREMENT

6.1 Standard Applicable

For intentional device, according to § 15.203, an intentional radiator shall be designed to ensure that no antenna other than that furnished by the responsible party shall be used with the device.

And according to § 15.247 (b), if transmitting antennas of directional gain greater than 6 dBi are used, the power shall be reduced by the amount in dB that the directional gain of the antenna exceeds 6 dBi.

6.2 Antenna Gain

The antenna is permanently mounted on RF box, no consideration of replacement.

The directional gain of antenna used for transmitting is 2dBi, Please see Appendix I for details

7 EMISSION BANDWIDTH MEASUREMENT

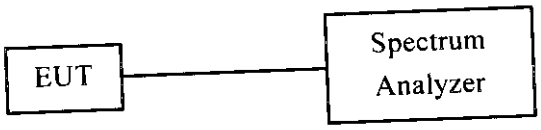
7.1 Standard Applicable

According to 15.247(a)(1)(ii), for hopping system operating in the 2400-2483.5 MHz and 5725-5850 MHz bands, the maximum 20dB bandwidth is 1 MHz. And the average time of occupancy on any frequency shall not be greater than 0.4 seconds with a 30 second period

7.2 Measurement Procedure

1. Check the calibration of the measuring instrument using either an internal calibrator or a known signal from an external generator.
2. Position the EUT as shown in figure 4 without connection to measurement instrument. Turn on the EUT and connect it to measurement instrument . Then set it to any one convenient frequency within its operating range. Set a reference level on the measuring instrument equal to the highest peak value.
3. Measure the frequency difference of two frequencies. Record the frequency difference as the emission bandwidth.
4. Repeat above procedures until all frequencies measured were complete.

Figure 4 : Emission bandwidth measurement configuration.

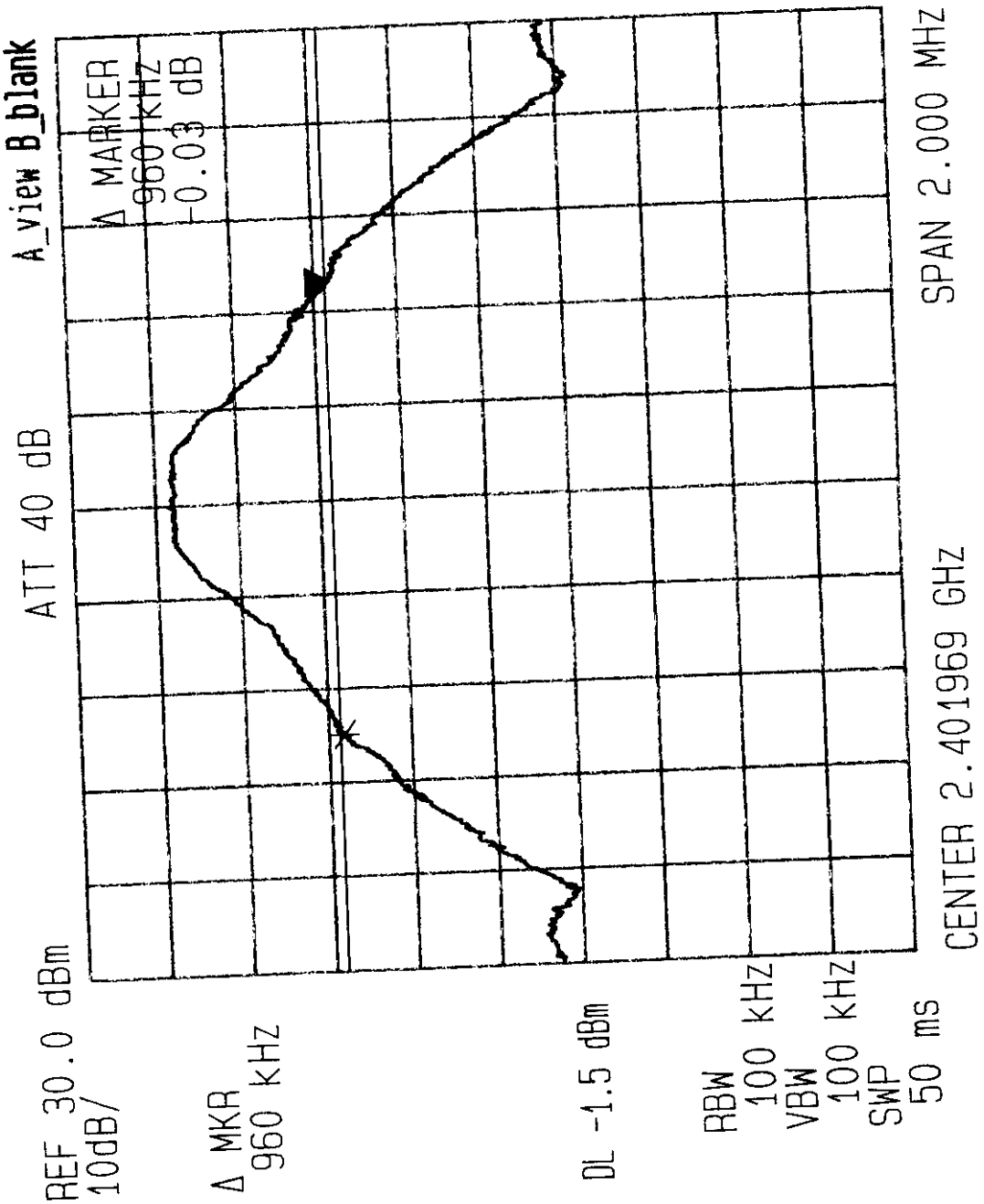


7.3 Measurement Equipment

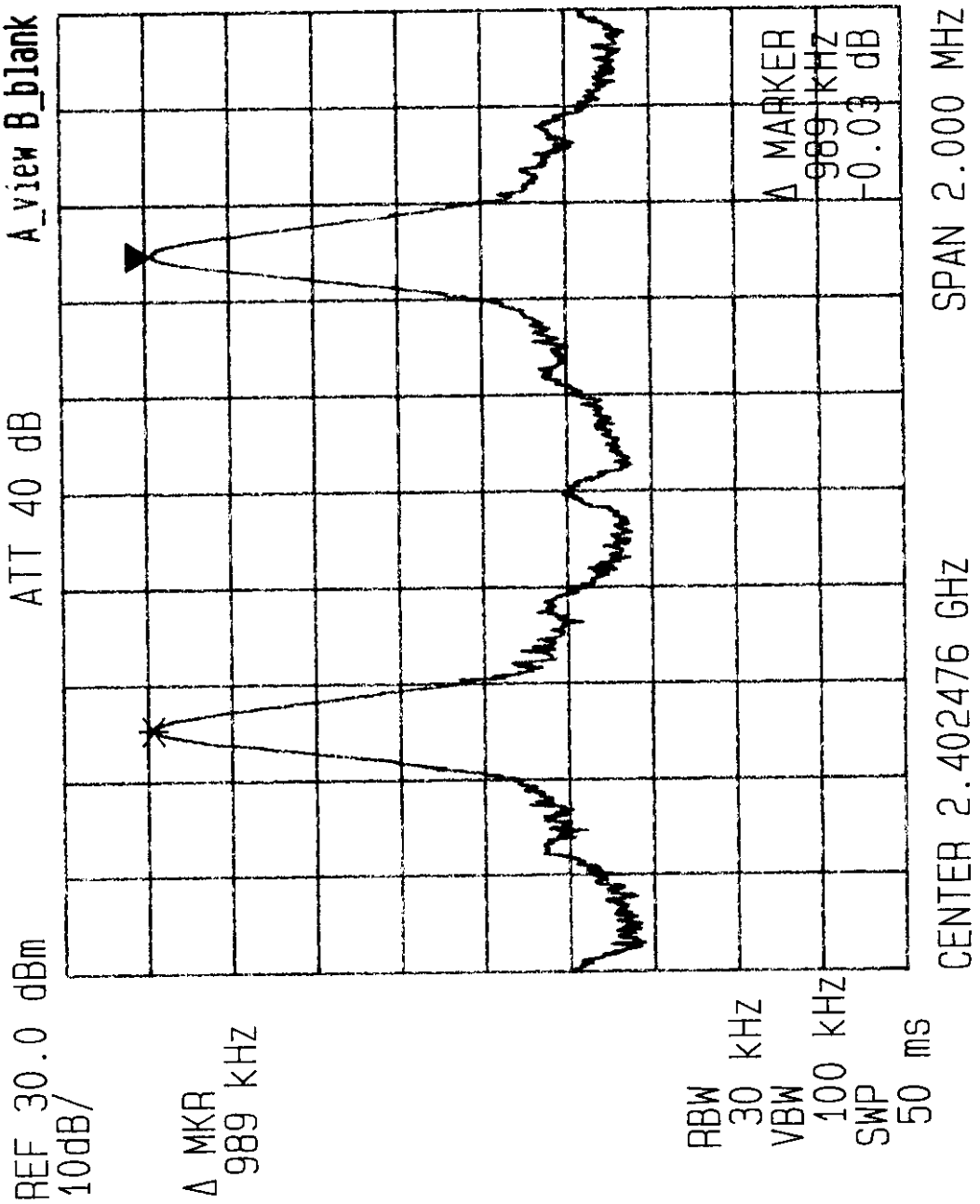
Equipment	Manufacturer	Model No.	Next Cal. Date
Spectrum Analyzer	Hewlett-Packard	8546A	FEB. 11, 1998
Plotter	Hewlett-Packard	7440A	N/A

7.4 Measurement Data

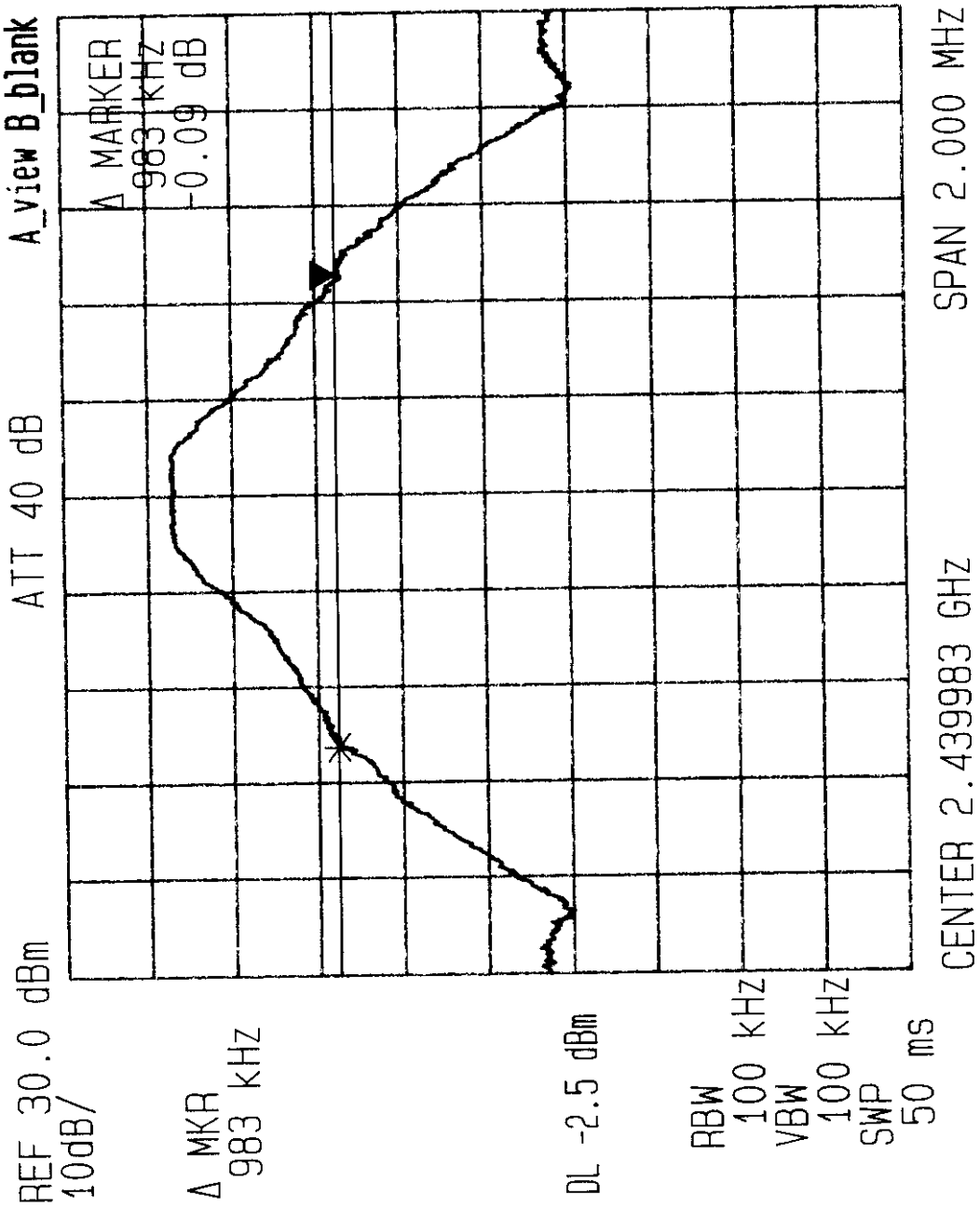
a1) Channel 2 : 20dB emission bandwidth



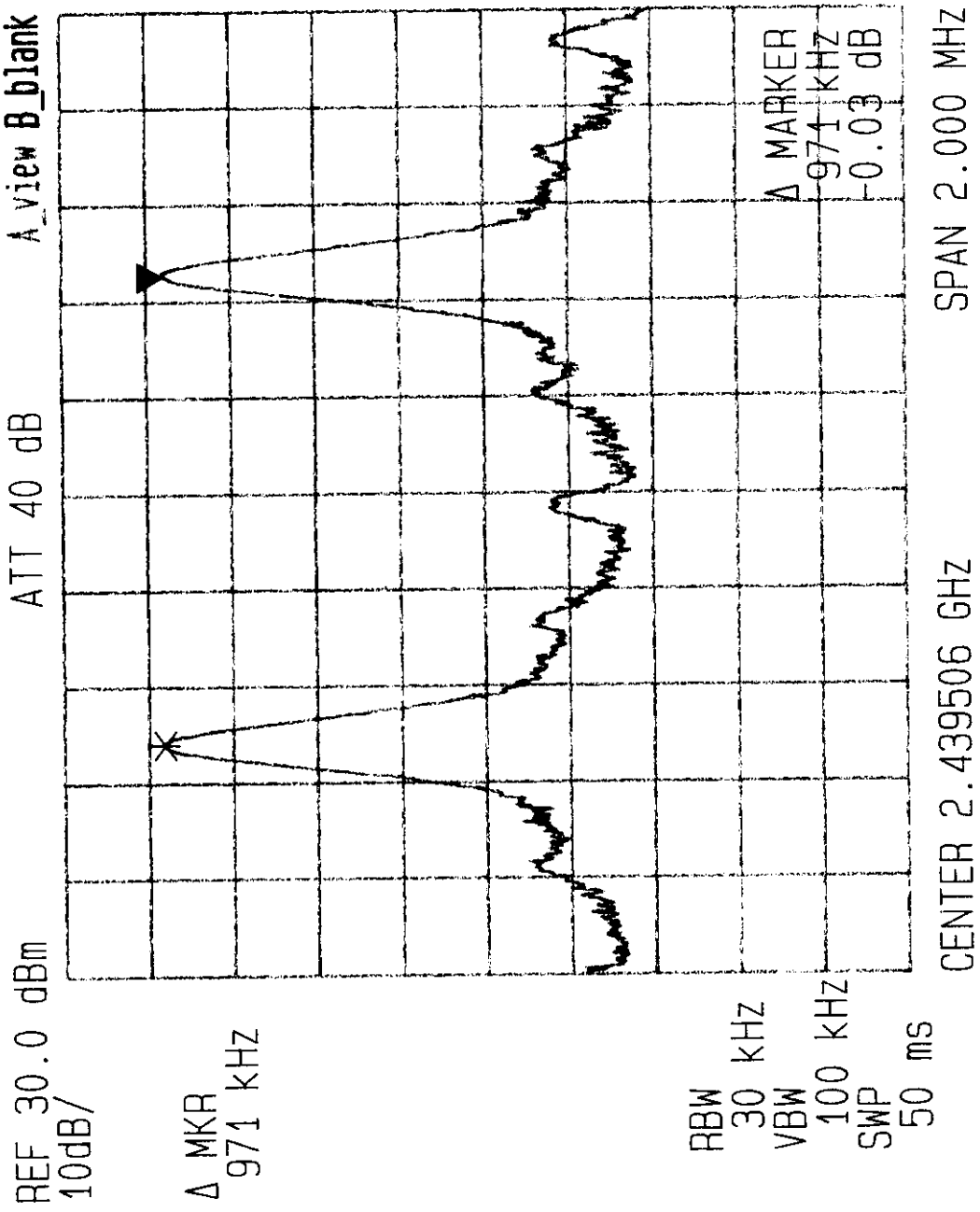
a2) Separation of adjacent channels



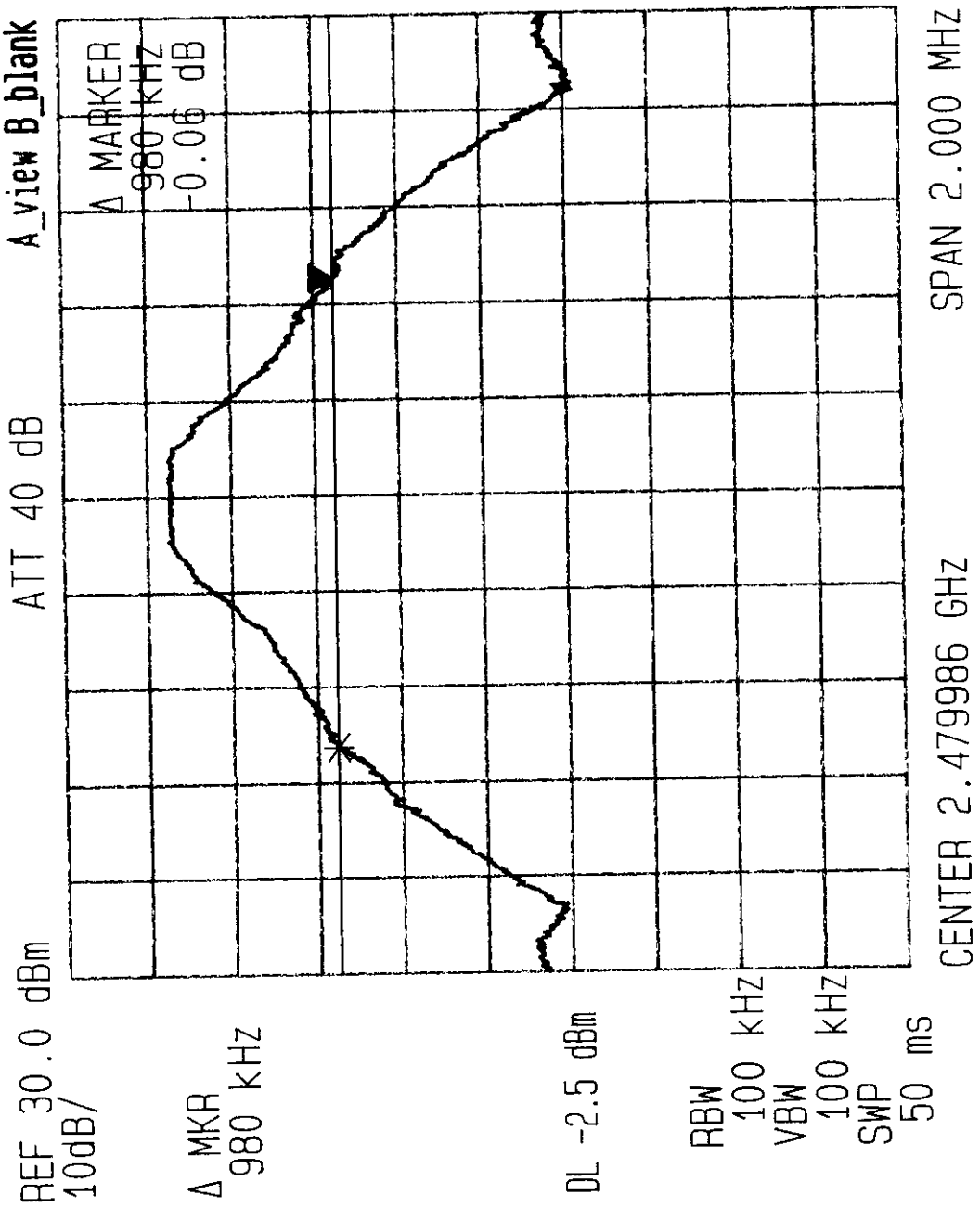
b1) Channel 40 : 20dB emission bandwidth



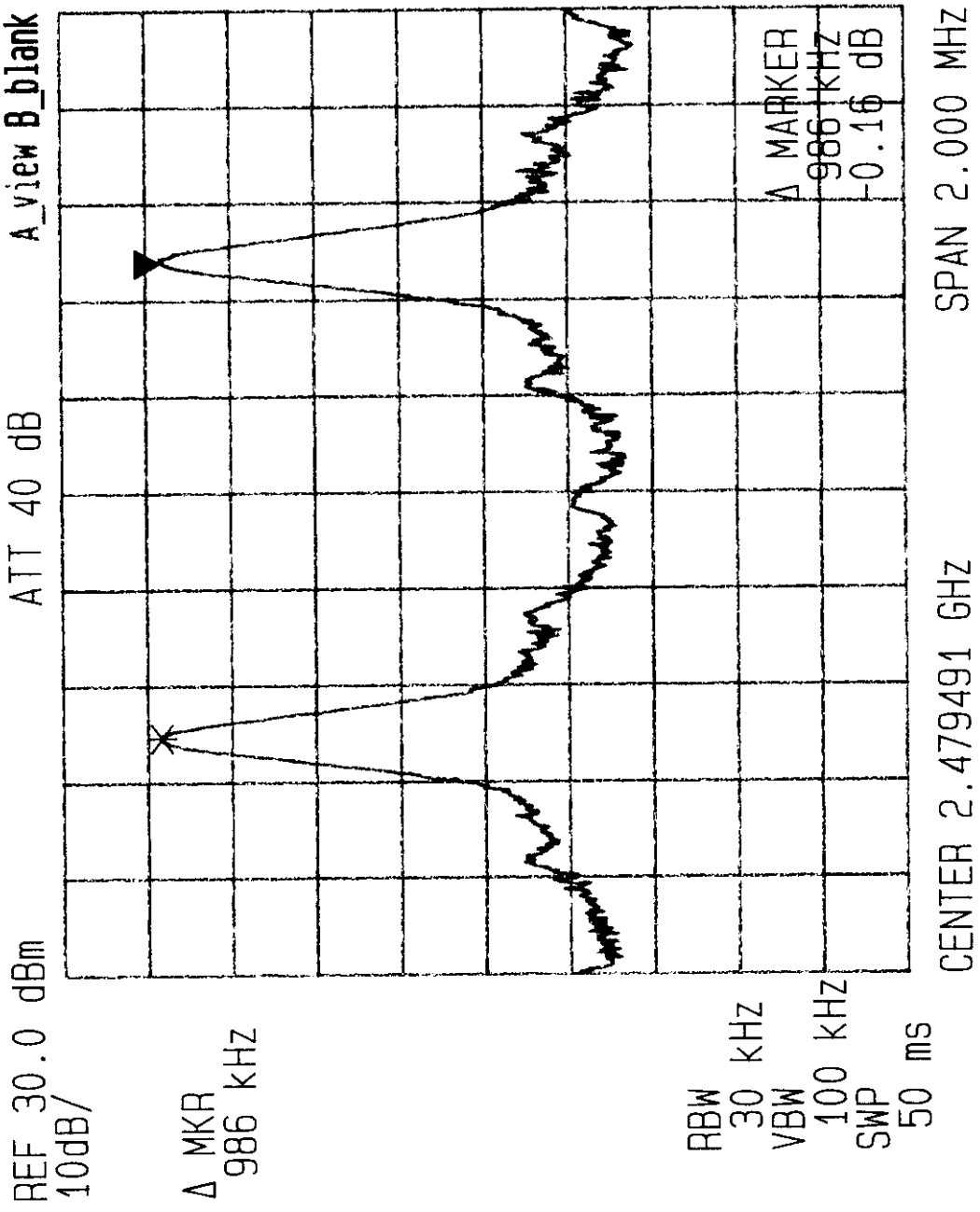
b2) Separation of adjacent channels



c1) Channel 80 : 20dB emission bandwidth



c2) Separation of adjacent channels



8 AVERAGE TIME OF OCCUPANCY ON HOPPING FREQUENCY

8.1 Standard Applicable

According to 15.247(a)(1)(ii), for hopping system operating in the 2400-2483.5 MHz and 5725-5850 MHz bands, the average time of occupancy on any frequency shall not be greater than 0.4 seconds with a 30 second period

8.2 Measurement Procedure

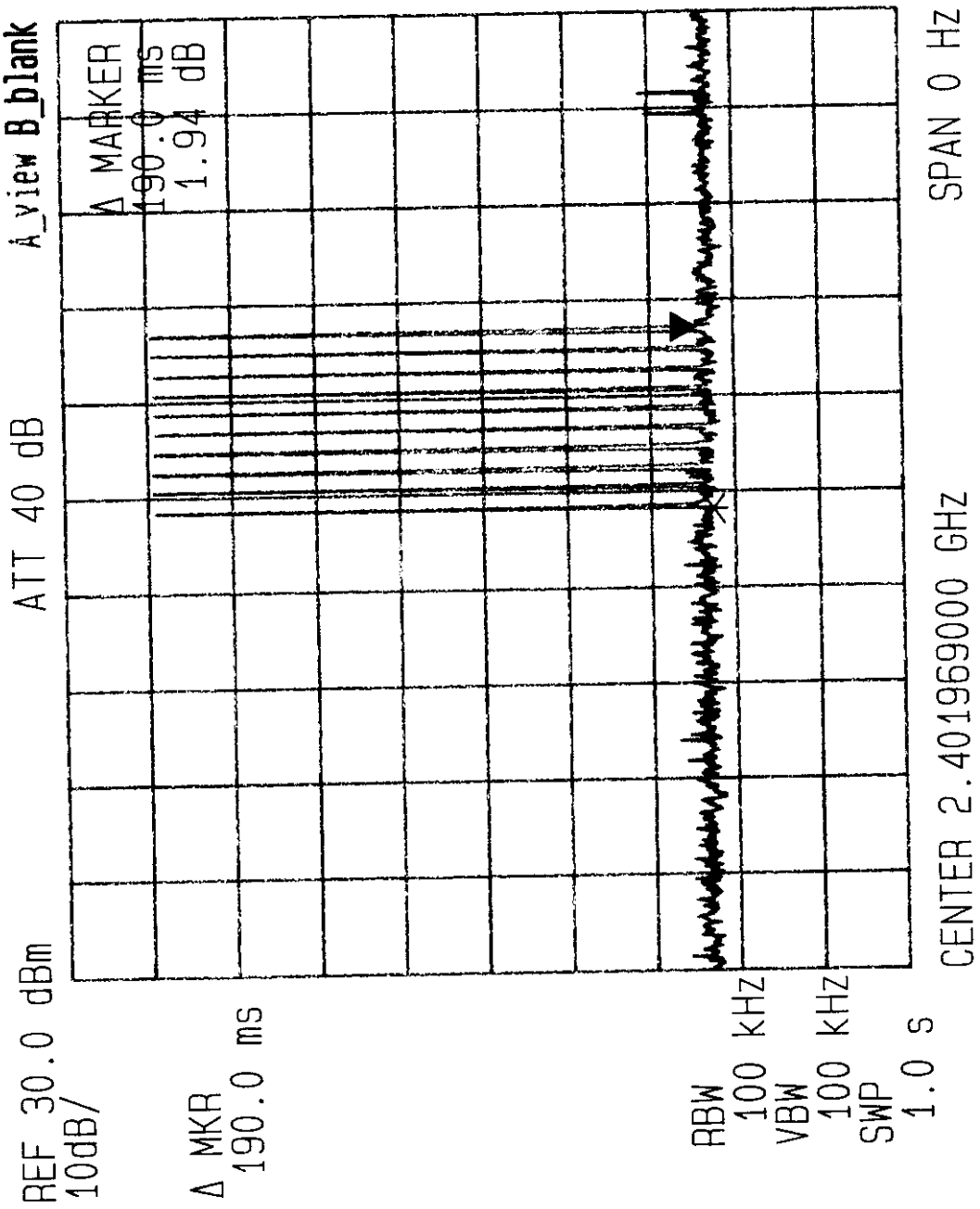
1. Check the calibration of the measuring instrument using either an internal calibrator or a known signal from an external generator.
2. Position the EUT as shown in figure 4 without connection to measurement instrument. Turn on the EUT and connect it to measurement instrument . Then set the center frequency on any frequency would be measured and set the frequency span to zero span. And then set the sweep time to 1 second.
3. Set the spectrum analyzer on a 100 kHz resolution bandwidth and 100 kHz video bandwidth as well as on max. hold function.
4. Keep spectrum analyzer in sweeping until the measured frequencies were recorded on display and then set the view function of spectrum analyzer and plot the result.

Explanation:

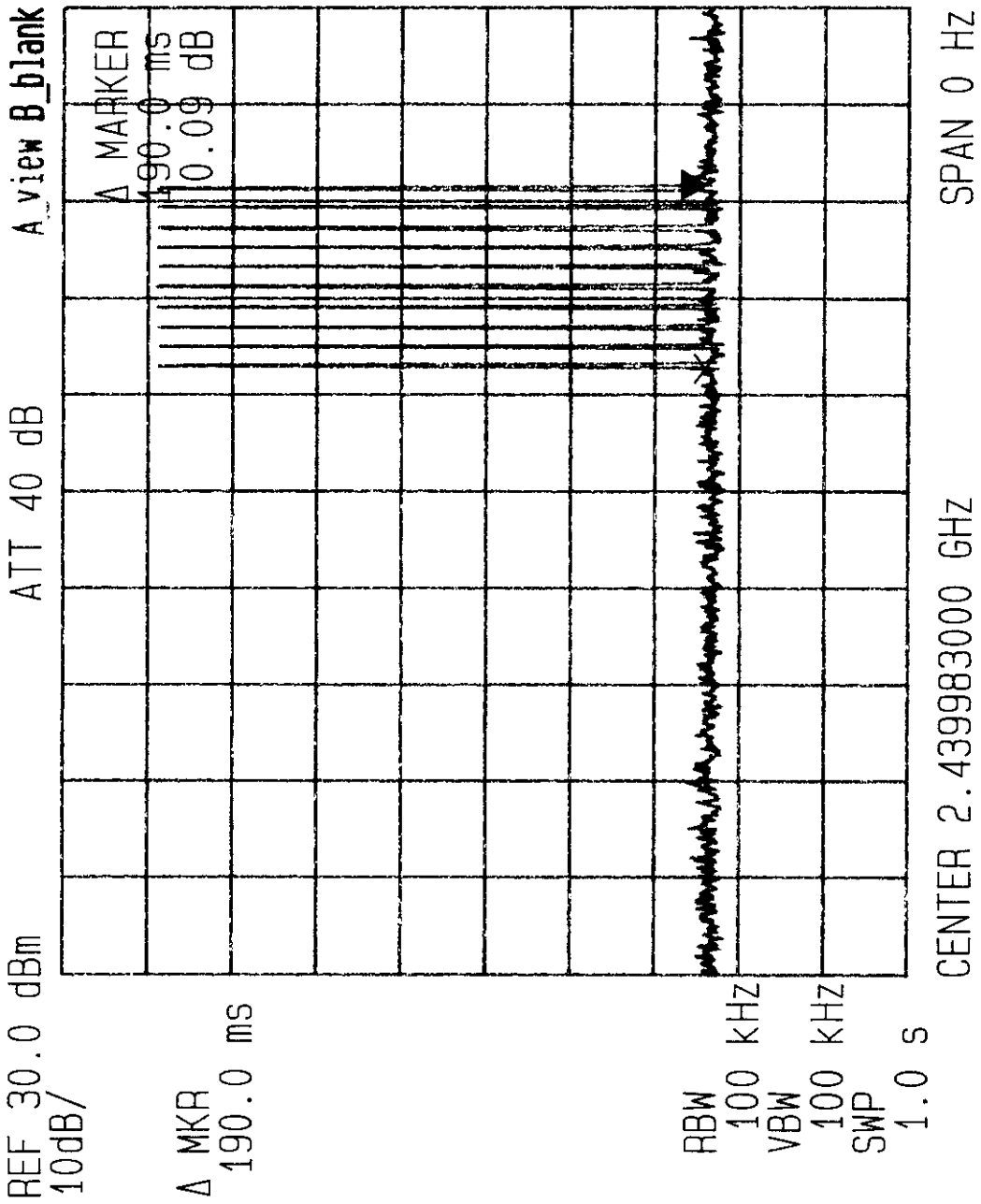
This dwell time is measured at a sweep time of 1 second, the result is 190 ms. And for there is a empty cycle time of 10 ms, the total hopping time in one turn is 200 $\times$ 79 = 15.8 seconds. Therefore, the maximum dwell time is a 30-second period for each channel is 190 $\times$2 = 380 ms.

8.3 Measurement Data

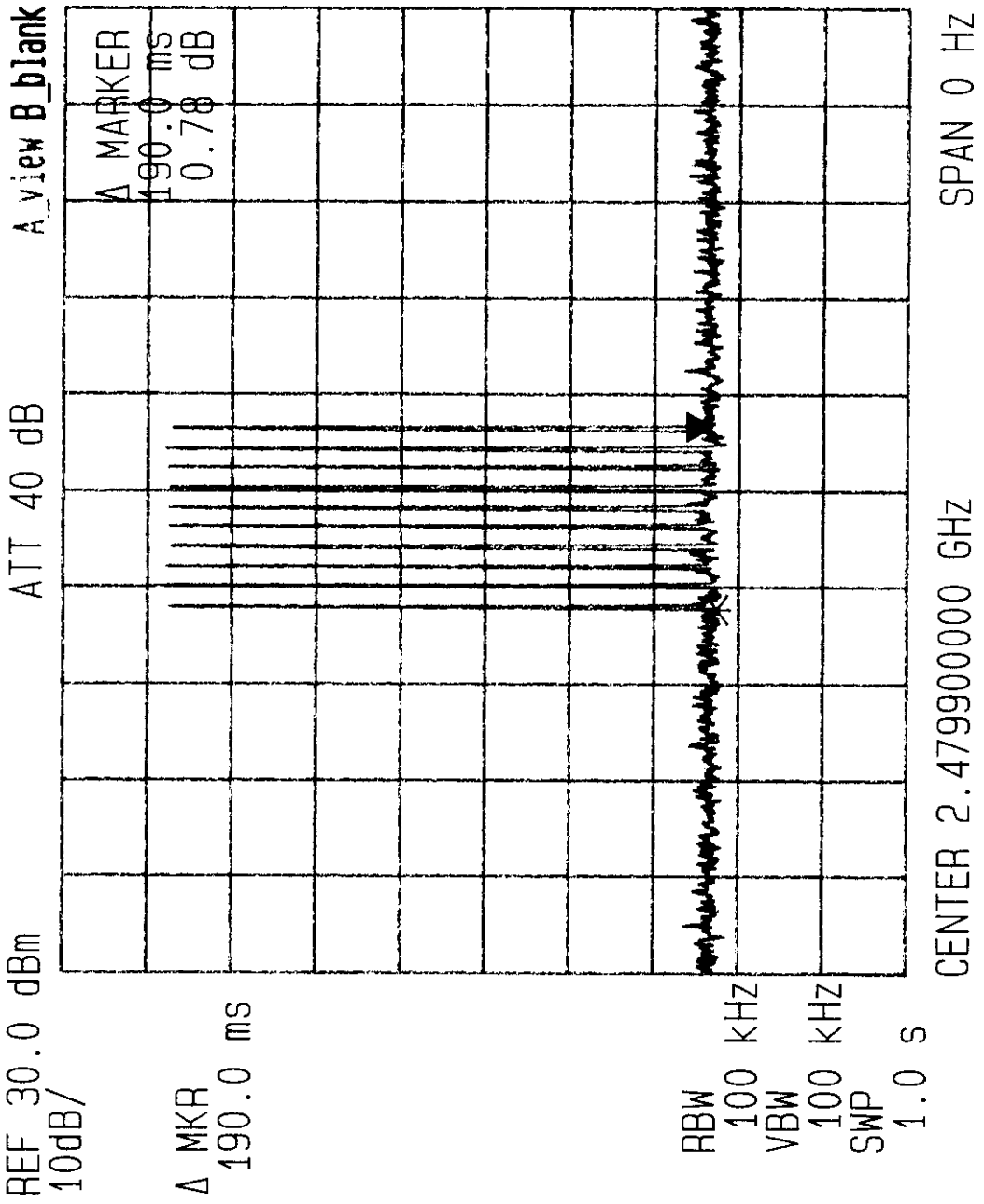
a) Channel 2 : the dwell time is 0.1900 second



b) Channel 40 : the dwell time is 0.1900 second



c) Channel 80 : the dwell time is 0.1900 second



9 OUTPUT POWER MEASUREMENT

9.1 Standard Applicable

For direct sequence system, according to 15.247(b), the maximum peak output power of the transmitter shall not exceed 1 Watt. If transmitting antennas of directional gain greater than 6 dBi are used, the power shall be reduced by the amount in dB that the directional gain of the antenna exceeds 6 dBi.

9.2 Measurement Procedure

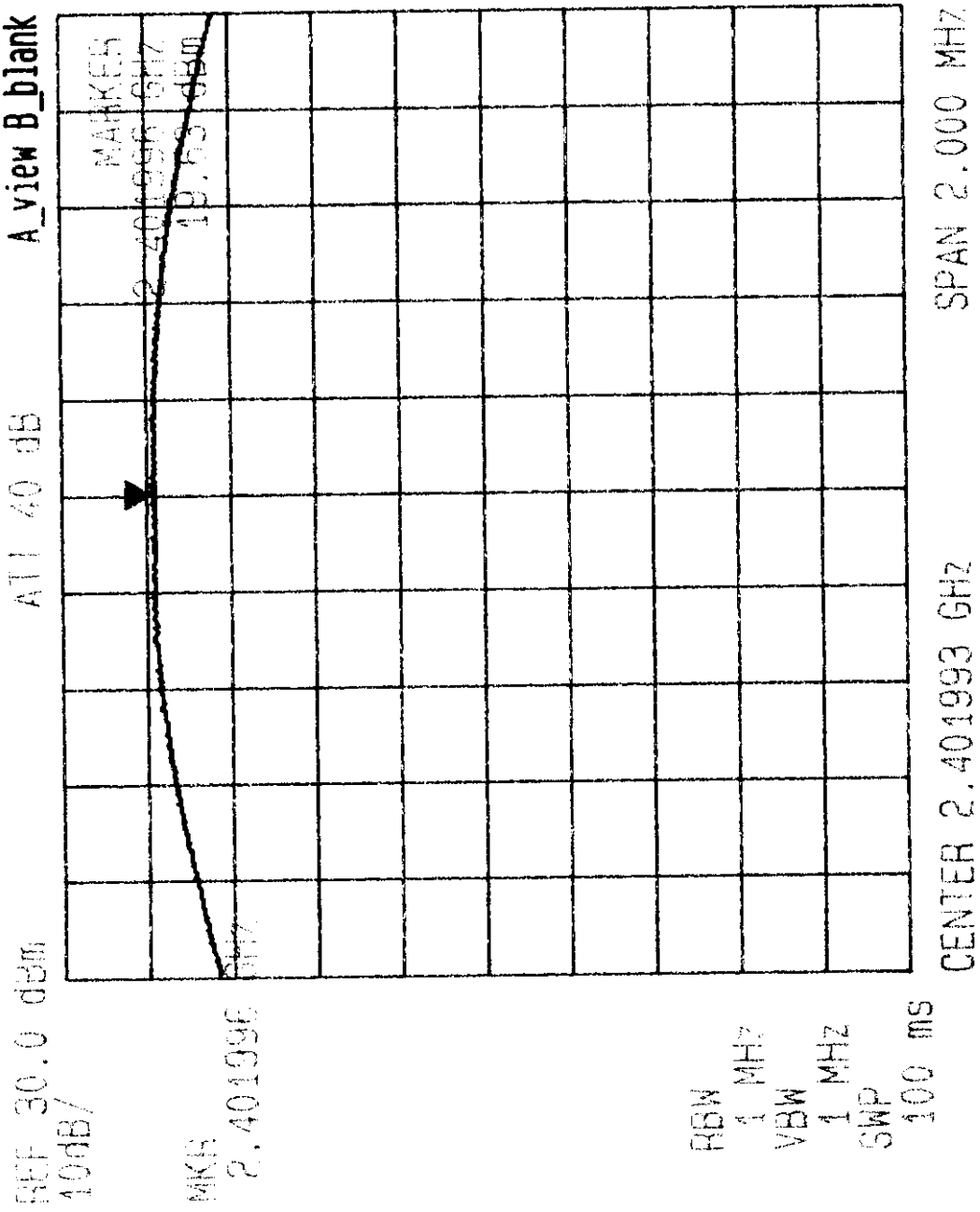
1. Check the calibration of the measuring instrument using either an internal calibrator or a known signal from an external generator.
2. Position the EUT as shown in figure 4 without connection to measurement instrument. Turn on the EUT and connect its antenna terminal to measurement instrument via a low loss cable. Then set it to any one measured frequency within its operating range and make sure the instrument is operated in its linear range.
3. Set RBW of spectrum analyzer to 1 MHz and VBW to 1 MHz.
4. Measure the highest amplitude appearing on spectral display and record the level to calculate result data.
5. Repeat above procedures until all frequencies measured were complete.

9.3 Measurement Equipment

Equipment	Manufacturer	Model No.	Next Cal. Date
Spectrum Analyzer	Hewlett-Packard	8546A	FEB. 11, 1999

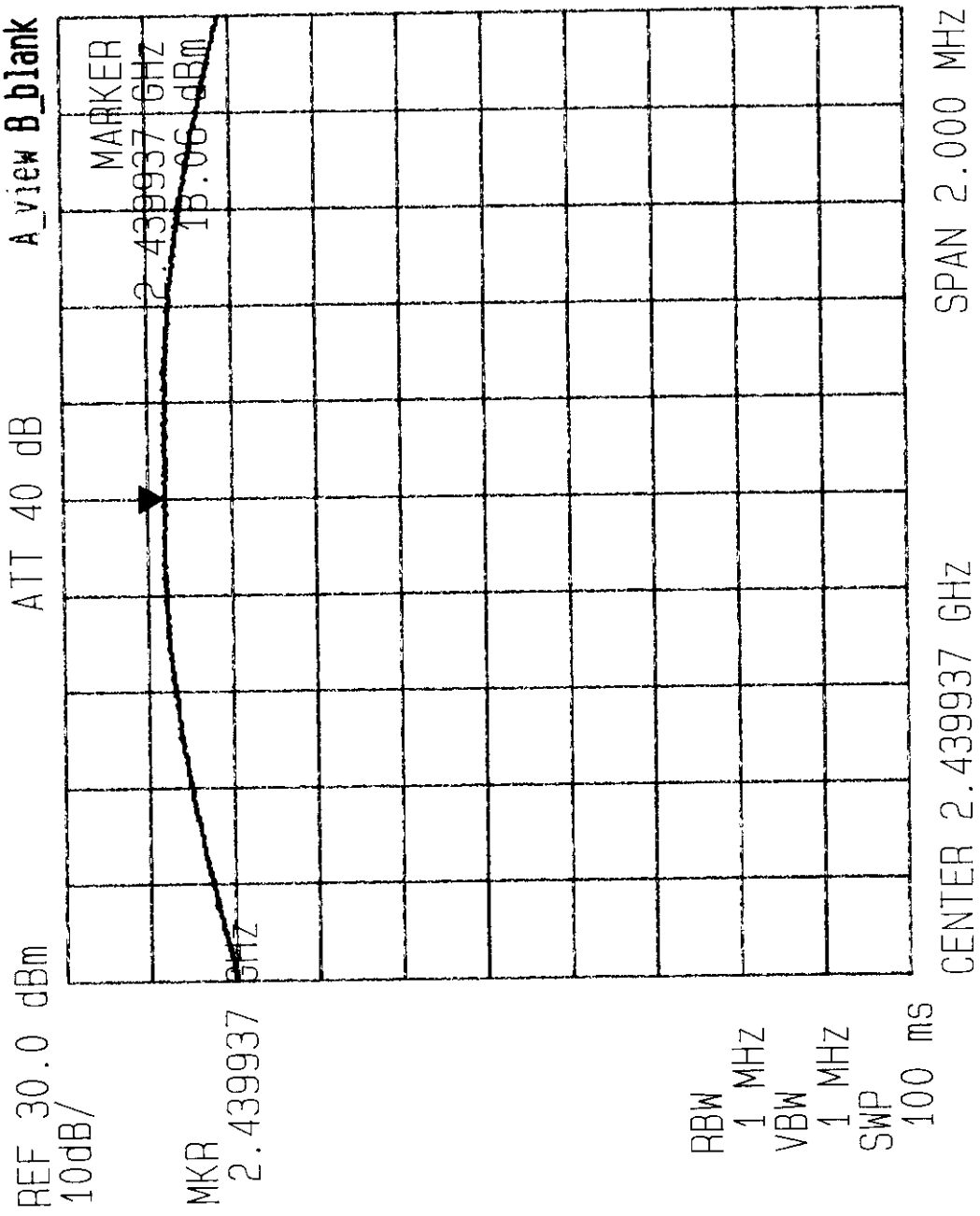
9.4 Measurement Data

a) Channel 2, 2.401969 GHz
19.63 dBm, or 91.830mW



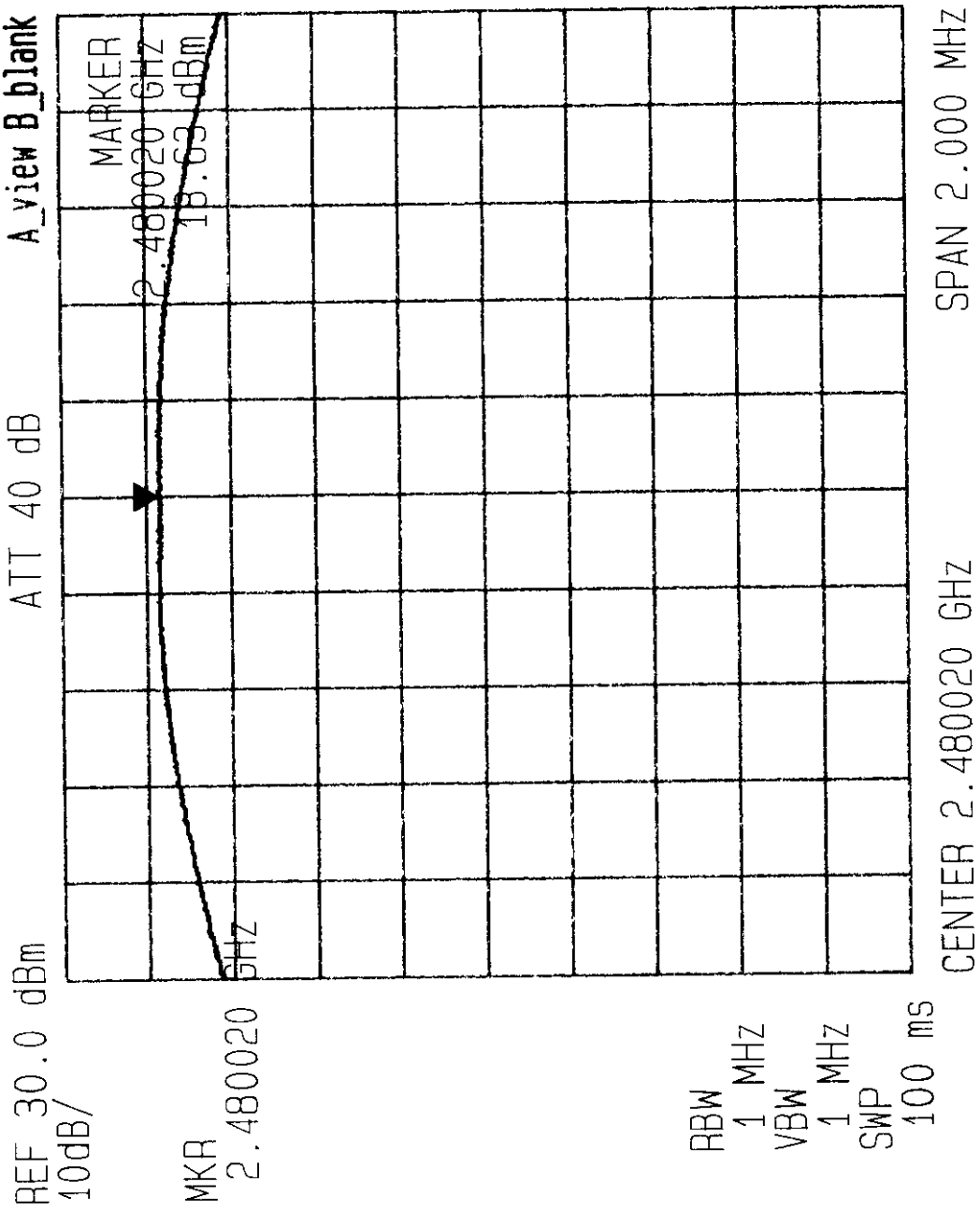
b) Channel 40, 2.439983 GHz

18.06 dBm, or 63.973 mW



c) Channel 80, 2.479986 GHz

18.63 dBm, or 72.945 mW



10 100 kHz BANDWIDTH OF BAND EDGES MEASUREMENT

10.1 Standard Applicable

According to 15.247(c), if any 100 kHz bandwidth outside these frequency bands, the radio frequency power that is produced by the modulation products of the spreading sequence, the information sequence and the carrier frequency shall be either at least 20 dB below that in any 100 kHz bandwidth within the band that contains the highest level of the desired power or shall not exceed the general levels specified in § 15.209(a), whichever results in the lesser attenuation.

10.2 Measurement Procedure

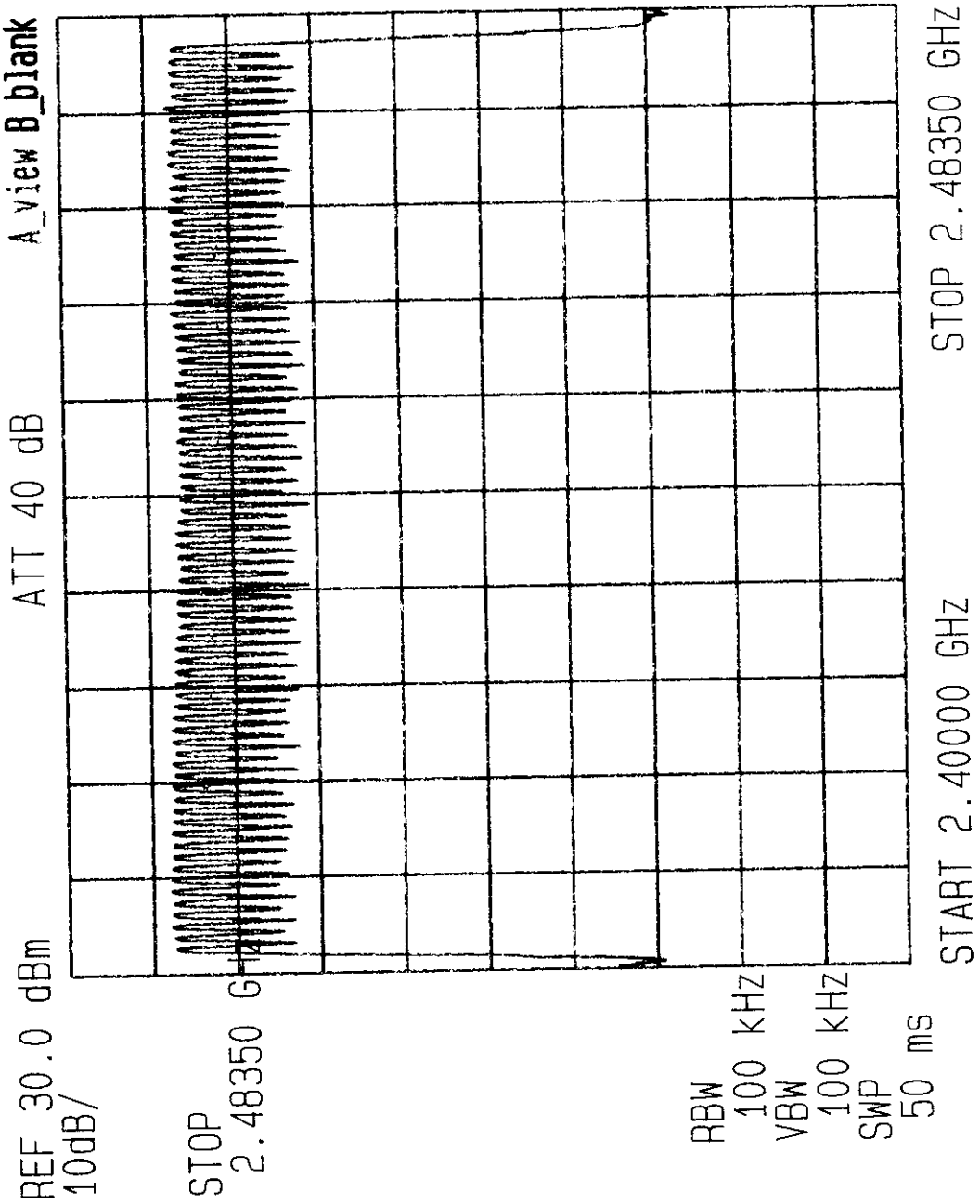
1. Check the calibration of the measuring instrument using either an internal calibrator or a known signal from an external generator.
2. Position the EUT as shown in figure 4 without connection to measurement instrument. Turn on the EUT and connect its antenna terminal to measurement instrument via a low loss cable. Then set it to any one measured frequency within its operating range and make sure the instrument is operated in its linear range.
3. Set both RBW and VBW of spectrum analyzer to 100 kHz with a convenient frequency span including 100kHz bandwidth from band edge.
4. Measure the highest amplitude appearing on spectral display and set it as a reference level. Plot the graph with marking the highest point and edge frequency.
5. Repeat above procedures until all measured frequencies were complete.

10.3 Measurement Equipment

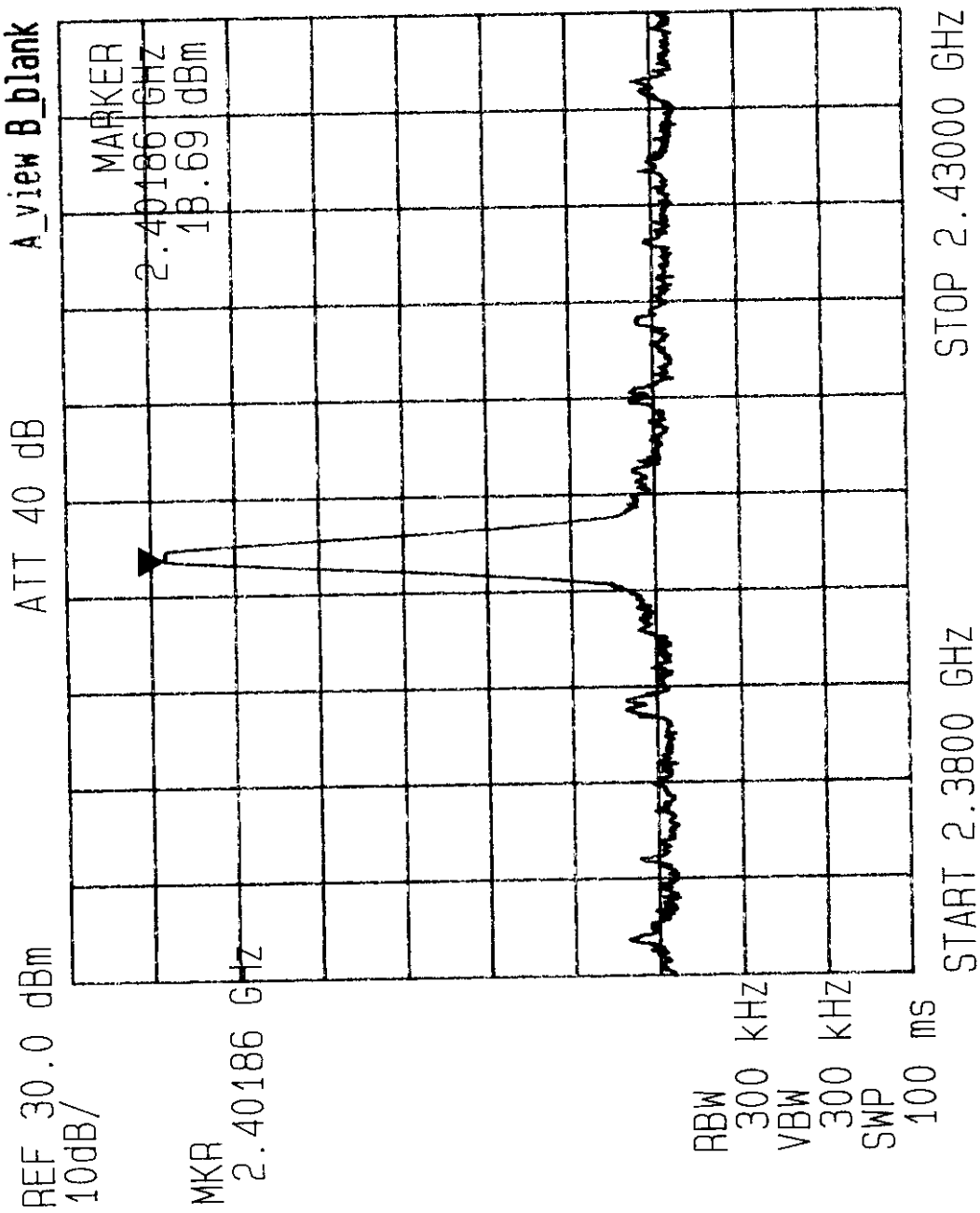
Equipment	Manufacturer	Model No.	Next Cal. Date
Spectrum Analyzer	Hewlett-Packard	8546A	FEB. 11, 1999
Plotter	Hewlett-Packard	7440A	N/A

10.4 Measurement Data

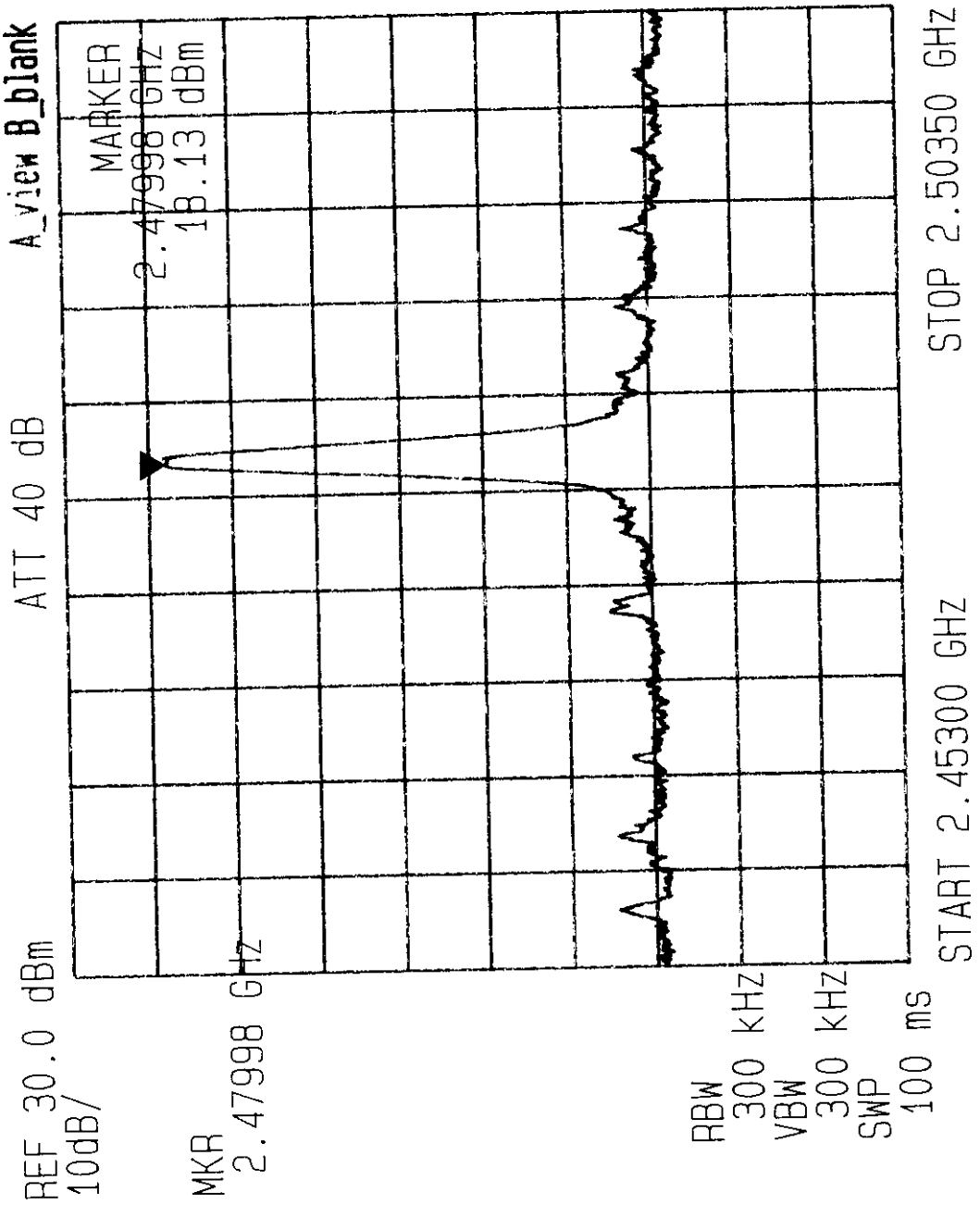
a) Total occupied bandwidth of all channels



b) 100 kHz bandwidth from lower band edge



c) 100 kHz bandwidth from upper band edge



11 HOPPING FREQUENCIES

11.1 Standard Applicable

According to 15.247(a)(1)(ii), for hopping system operating in the 2400-2483.5 MHz and 5725-5850 MHz bands shall use at least 75 hopping frequencies.

11.2 Measurement Procedure

1. Check the calibration of the measuring instrument using either an internal calibrator or a known signal from an external generator.
2. Position the EUT as shown in figure 4 without connection to measurement instrument. Turn on the EUT and connect its antenna terminal to measurement instrument via a low loss cable. Then set EUT to any one measured frequency within its operating range and make sure the instrument is operated in its linear range.
3. Adjust the frequency span of spectrum analyzer from 2.4 GHz to 2.4835 GHz
4. Set the spectrum analyzer on a 100 kHz resolution bandwidth and 100 kHz video bandwidth as well as on max. hold function.
5. Keep spectrum analyzer in sweeping until all hopping frequencies were recorded on display.

11.3 Measurement Equipment

Equipment	Manufacturer	Model No.	Next Cal. Date
Spectrum Analyzer	Hewlett-Packard	8546A	FEB. 11, 1999
Plotter	Hewlett-Packard	7440A	N/A

11.4 Measuring Data

Please see 10.4 (a) total occupied bandwidth of al channels

NDC Wireless PC card for personal computer

Declaration :

NDC wireless PC card for personal computer is implemented by applying Frequency Hopping Spread Spectrum techniques and following the Draft Standard for Wireless LAN specified by IEEE802.11.

The implementation of the frequency hopping sequence completely follows the rule of set 1 specified on IEEE 802.11 14.6.8 Hop Sequence. By following the Hop Sequence defined by set 1, not only the channel overlapping can be prevented, but also the equal usage of the channel can be achieved.

The equal usage of each frequency channel is proved by the data shown on Fig 2, Fig3. The Total dwell time for each respective channel is defined as 200 mini-seconds. The total channel number for the hopping frequency is 79. For one particular channel it will hop every 15.8 seconds shown on Fig 3. This is proved by setting the 30 seconds sweet time at the spectrum analyzer. The measured hopping channel can only appear twice in the whole the sweet time. The data shown on Fig 2 ,Fig 3 proves NDC wireless LAN ISA adapter complies with FCC 15.247(a)(1). The other energy peaks shown on the Fig 2,Fig 3 are the leakage from the adjacent channel.

Parameters setting:

Continuous test signal dwell time = 190ms ; shown on ETC Report No.:ET87R-02-081 sheet 36 of 47 sheets ,sheet 37 of 47 sheets, sheet 38 of 47 sheets.
Empty cycle=10ms ; idle time interval between the end of previous hopping and the begin of the next hopping.
Total dwell time = Continuous test signal dwell time +Empty cycle
= 190ms+10ms
= 200ms

Description :

The block diagram of NDC wireless PC adapter is attached as Figure 1. According to circuit diagram, both the transmitter and the receiver share the common circuitry in many area such as

- the 1st LO (Local Oscillation) Synthesizer
- 2nd LO(Local Oscillation) Synthesizer
- IF filter
- RF filter

With the same circuitry for both transmission and receiving signal paths, it will guaranteed the same bandwidth for both the transmitter and the receiver. Moreover, by following the hop sequence specified by IEEE 802.11, the channel synchronization between the transmitter and receiver is also achieved.

It complies with all the radio specifications defined by IEEE 802.11. All the radio operation

Answer to Pseudo -random hopping pattern :

According to TableB-1 Hopping set 1

1. There are 79 hopping channel in North America band.
2. There are 26 hopping sequences (first row on Table B-1) can be selected the users. The first 13 hopping sequences are listed on page 308 and page 309. The second 13 hopping sequence are listed on page 310 and page 311.
3. Once a hopping sequence is specified. The channel will hop vertically across the columns on table B-1 which is pseudo random. For example; if the sequence 0 is selected, the hopping will follow the sequence 2, 25, 64, 10, ……,32,48.
4. In order to make it clear, the sequence 0 is hopping based on the following table.

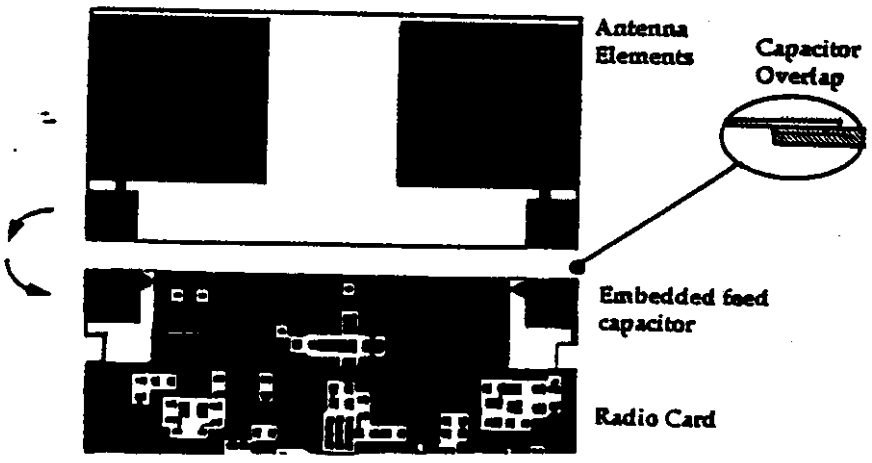
Index	0 - Hopping sequence
1.	2
2.	25
3.	64
4.	10
5.	45
6.	18
7.	73
8.	49
9.	21
10.	63
11.	78
12.	31
13.	61
14.	24
15.	54
16.	65
17.	28
18.	79
19.	33
20.	4
21.	20
22.	13
23.	38
24.	74
25.	56
26.	71
27.	23
28.	5
29.	39
30.	12
31.	36
32.	68
33.	9
34.	70
35.	77
36.	6
37.	62
38.	29

Index	0 - Hopping sequence
39.	14
40.	27
41.	16
42.	59
43.	43
44.	76
45.	34
46.	72
47.	11
48.	60
49.	80
50.	47
51.	22
52.	75
53.	66
54.	41
55.	15
56.	35
57.	67
58.	52
59.	58
60.	44
61.	50
62.	17
63.	7
64.	19
65.	8
66.	69
67.	51
68.	42
69.	3
70.	30
71.	57
72.	37
73.	55
74.	26
75.	46
76.	53
77.	40
78.	32
79.	48

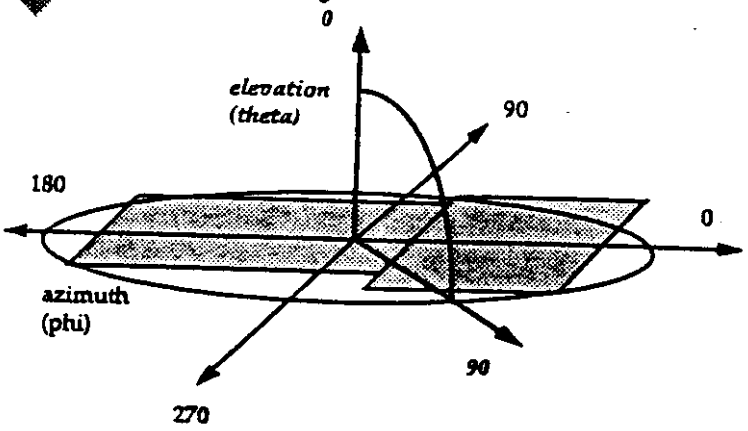
PC Card Antenna
Electrical Performance Summary

- Gain Level
  - aim to be as omni-directional as possible
  - dependant on host, expect 0 to 2 dBi peak
- Input return loss better than 10 dB across ISM Band in Typical host
- Measured correlation coefficients < 0.1 in radiated measurements in multipath

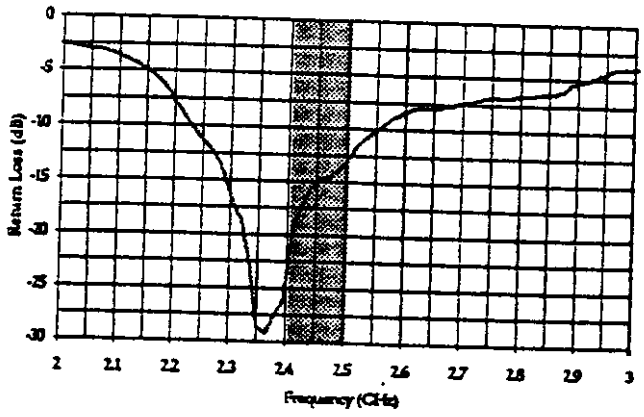
PC Card antenna
Electrical Layout, radio card



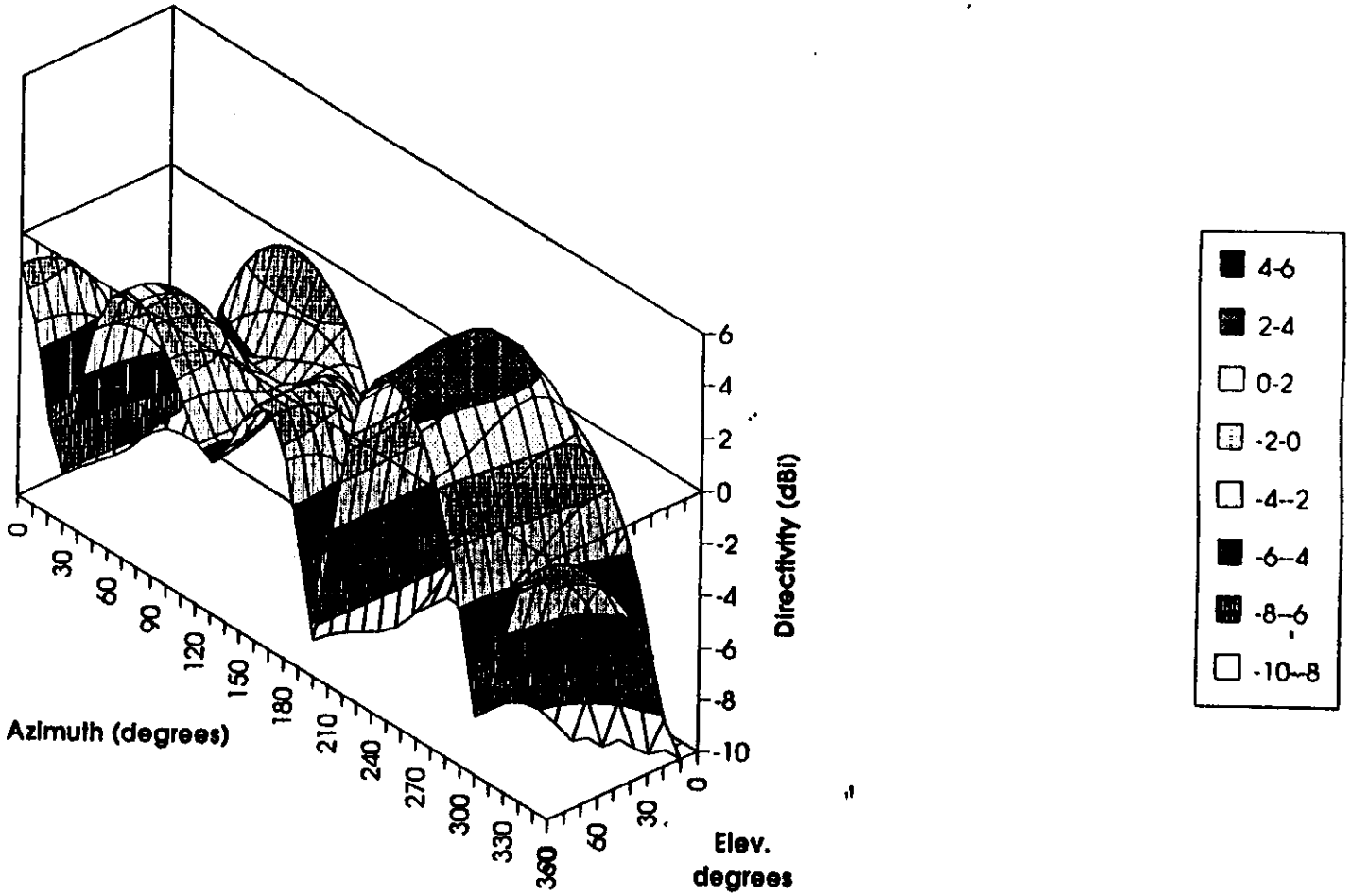
Typical Radiation Pattern Co-ordinate System



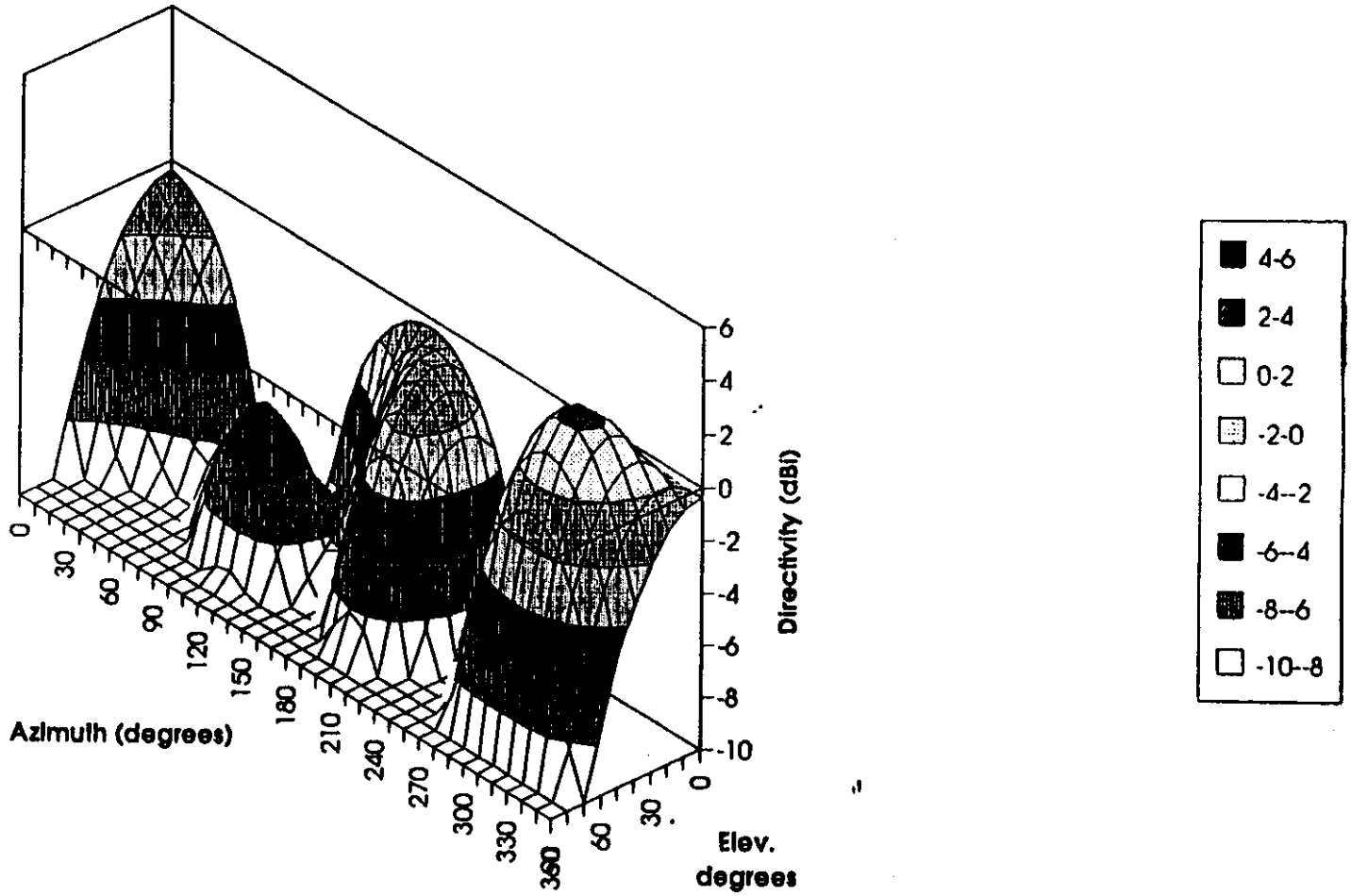
PC Card Antenna Diversity Element Return Loss



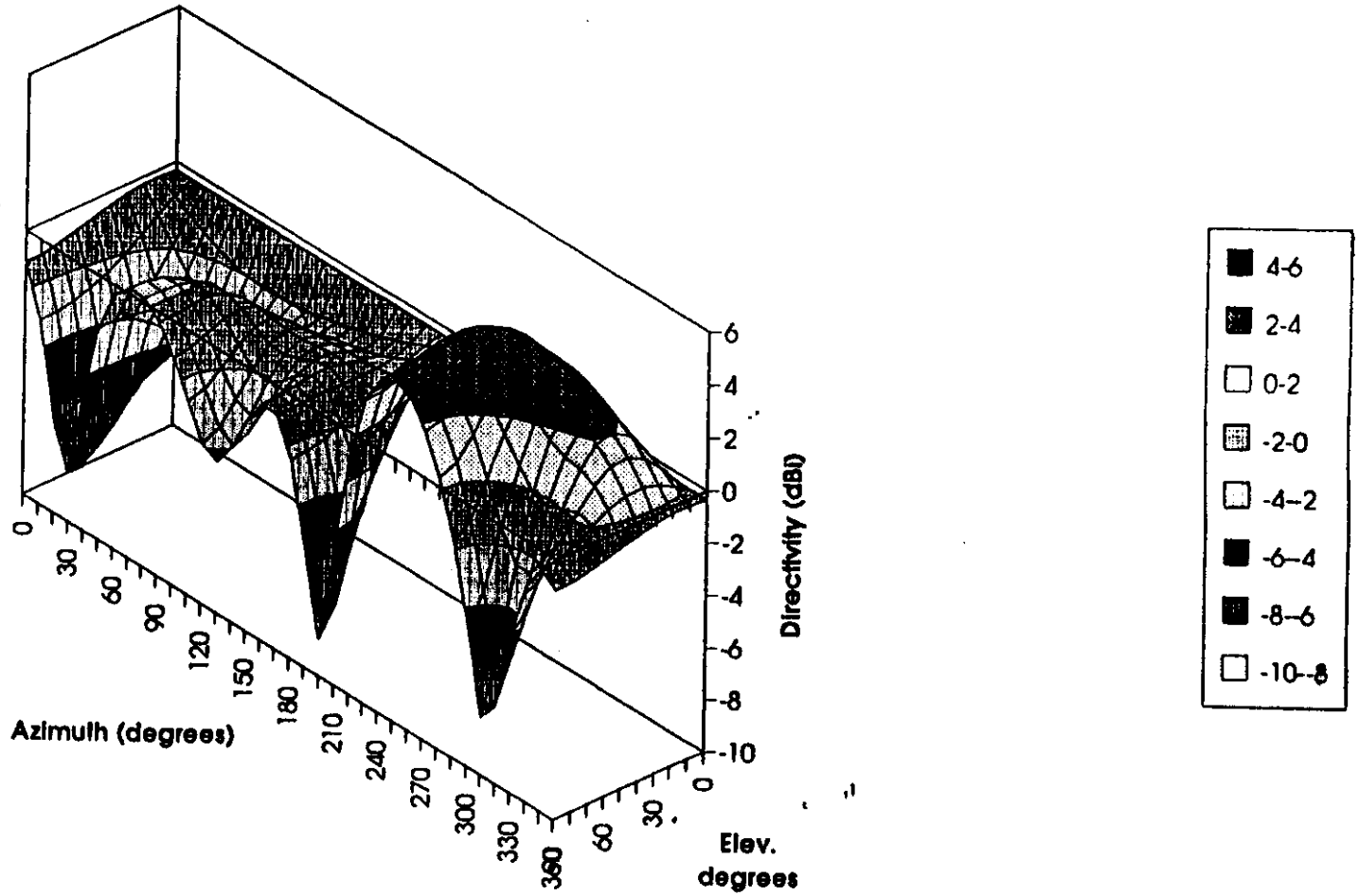
Typical Horizontal Polarisation Radiation Pattern



Typical Vertical Polarisation Radiation Pattern



Typical Elliptically Polarised Radiation Pattern



1. INTRODUCTION

This document gives an overview of the POTPOURI radio. The function of each aspect of the radio is described, with important features of the physical layout where pertinent.

2. BLOCK DESCRIPTION

For ease of reading, the radio description has been split into a number of functional blocks. The receiver is a dual conversion superhet; the transmitter uses double upconversion to final frequency. The areas covered are as follows:-

- Receiver low-noise amplifier, receiver down-conversion mixer, 1st IF filter and switches, receiver 2nd mixer, receiver limiter and demodulator, receiver video filter and data slicer.
- Transmitter modulator, transmitter IF buffer, transmitter 1st and 2nd upconversion mixer, transmitter filter PIN switches, transmitter pre-driver and driver, transmitter PA, and diversity switch.
- Low frequency synthesiser and VCO, high frequency synthesiser, VCO, buffer and frequency doubler.

Note that the Hewlett-Packard HPMX5001/HPMX5002 chipset implements most of the functionality, dramatically reducing the external component count below that required by a discrete radio solution.

Due to the restricted height available in the Type II PCMCIA card format, all the transmission line elements are in stripline form to eliminate the effect of the cover height from the design process. Where the physical constraints make it necessary to have bends in striplines, these bends have been included in the simulations of the performance of each stage. Any need to change the layout to the extent that striplines change significantly will result in the need to re-run the simulations to take account of the new layout.

3. RECEIVER

3.1. General

The receiver is a dual super heterodyne type, with nearly all the channel filtering performed by a SAW IF filter. An optional diversity PIN switch for dual antenna receive diversity is available. The overall block diagram is shown in Figure 1.

3.1.1. Diversity PIN switch

This is an optional circuit element.

At the LNA input port, a PIN switch is used to select either receive antenna. Series/shunt PIN diodes are used together with a quarter wavelength line to transform the short circuit at the shunt diode into an open circuit at the other port. A loss of approximately 1.0dB is incurred in each switch, with an off port isolation of better than 15dB.

3.1.2. Receive LNA

The receiver LNA is a single stage amplifier using a self biased OKI KGF1175 GaAsFET device at a supply current of 4mA. Input and output matching is by means of stripline impedance transforms from 50 ohms to the optimum source and load impedance for the device. The bias choke for the power supply is a surface mount wound inductor. Measured gain is >13dB, with an output 1dB compression point of +5dBm. Additional gain can be achieved by reducing the value of the external source bias resistor to increase the device current. An increase of 2-3dB can be expected at 8mA current.

3.1.3. Receive 1st Mixer

The receiver 1st mixer is integrated into the HPMX5001 Transmit/Receive chip. It is a Gilbert cell mixer that takes the LNA output after filtering and downconverts to the 240.0MHz IF frequency. The mixer output drives a nominal 750 ohm impedance, with an external matching network to transform down to 200 ohms. The mixer provides a conversion gain of 12dB and a noise figure of 9dB. The mixer input impedance is 50 ohms nominal.

3.1.4. Receive 1st IF SAW Filter

A SAW filter, with a centre frequency of 240.0MHz and a bandwidth of 1.0MHz, provides the main channel filtering. The SAW filter's matching is by means of lumped element matching networks, with a source impedance of 200 ohms and a load impedance of 200 ohms with 0.75pF parallel capacitance. This gives an insertion power loss of 11dB, together with a group delay ripple of <200ns p-p. At each end of the SAW filter circuit block, a dual diode PIN switch is used to switch the filter between the transmit and receive circuitry. As the impedance at this point is 200 ohms, the bias is supplied using a pair of 1500 ohm resistors. The parallel RF load is then 750 ohms, which has only a small effect on the impedance seen by the filter. This is preferable to the use of inductors due to the field coupling that occurs between closely spaced inductors.

3.1.5. Receive 2nd mixer

The 2nd mixer mixes down to the 24.0MHz second IF frequency at which the limiter operates, and is contained within the HPMX5002 IF chip. It provides a conversion gain of 8dB with an input impedance of 200 ohms/0.75pF parallel and an output impedance of 600 ohms. A single section LC bandpass filter follows the mixer. This filter limits the mixer output wideband noise spectrum and reduces the spurious content of the mixer output.

3.1.6. Receive limiter/discriminator

Following the post mixer filter is a limiting amplifier with >80dB gain. This has a bandwidth in excess of 30 MHz and produces a hard-limited output signal for the demodulator. The demodulator consists of a quadrature mixer with an external quadrature phase shifting circuit and produces an output signal of 100mV p-p. In addition, an RSSI signal is produced with a dynamic range of approximately 65dB which operates from 6dB below the sensitivity threshold. The RSSI output voltage level ranges from 0.8V to approximately 2.5V with a rise time of <5us into a low capacitance load..

3.1.7. Receive video filter and data slicer

Following the demodulator is a video low pass filter. This reduces the level of twice 2nd IF signal and any limiter output noise on the demodulated signal. The video signal is then fed to the data slicer that compares the instantaneous video amplitude with an averaged version of the same signal. This averaging process is applied by means of a time constant, set by an external capacitor, that can be switched to allow fast acquisition of the correct level and then slow acquisition to maintain the slicing threshold during the time slot. The slicer output drives an external fast switching transistor to provide a high current drive to the baseband circuitry.

3.2. Transmitter

To enable fast Receive to Transmit switching, the transmitter up converts a signal at the same frequency as the receive 2IF to prevent the need for switching the frequency of the 1LO or the 2LO.

3.2.1. Transmit modulator

There are two options for the generation of the modulated sub-carrier. These are:

- Modulation of the 2LO using an NRZ signal.
- Upconversion of Digitally modulated 2IF signal.

For fast Receive to Transmit switching, a carrier at 2IF is required to remove the need for switching the 1LO PLL frequency. This is best performed by a digitally generated IF. The digitally generated IF is produced by the baseband circuits, this can be modulated or unmodulated.

If a NRZ signal is used the two level FSK modulation is applied to the transmitted signal by means of a modulation varactor forming part of the low frequency local oscillator (2LO) tank circuit. The baseband circuitry generates the modulation as a square wave with logic low equal to positive frequency deviation and a logic high to negative frequency deviation. The baseband signal drives a totem pole transistor pair to ensure fast edge transitions. A potential divider network provides a bias voltage for the modulation varactor. This is set at slightly below half rail to allow for the non-linear voltage-capacitance characteristic of the modulation varactor. The deviation applied to the 2LO is determined by the value of the coupling capacitor between the tank circuit and the modulation varactor.

3.2.2. Transmit IF buffer

The output of the 2LO is fed out of the IF chip by means of a differential drive buffer. This provides a drive level of approximately -20dBm to be fed to the 1st upconversion mixer chip.

3.2.3. Transmit 1st upconversion mixer

The first upconversion mixer is used to provide a transmit 1st IF at the same frequency as the receive 1st IF, ensuring a minimum receive-transmit switching time by avoiding reprogramming of either local oscillator frequency. The 24.0MHz offset required is generated within the baseband circuitry. This is mixed with the 216MHz 2LO frequency in a Gilbert cell configuration mixer. The mixer input matching is designed to feed from the 500 ohm level into the 200 ohm mixer input impedance. The output match is designed to step down from 1000 ohms to 200 ohms which then feeds through the 1st IF SAW filter. Additional component positions are available which allow the bias conditions of the mixer to be altered. This then allows it to function at 3V supply voltages if required. An output level of -20dBm is produced which is passed through the SAW filter and its associated PIN switches, accomplishing the modulation envelope filtering required to restrict the transmitted signal's bandwidth.

3.2.4. Transmit SAW filter buffer

Following the SAW filter a bipolar transistor buffer stage is required to increase the signal level feeding the 2nd upconversion mixer. The mixer input requires -18dBm. A gain of 12dB is needed to accomplish this.

3.2.5. Transmit upconversion mixer

The upconversion mixer is contained within the HPMX5001. This takes the differential input from the 2LO buffer stage and mixes it with the high frequency local oscillator or 1LO in a

Gilbert cell mixer stage. The output from the mixer is taken in single ended mode via a matching network. This is designed to provide a 50 ohm termination to the bandpass filter following the mixer to ensure the pass band shape is not affected. The signal level at this point is a maximum of approximately -1dBm. This level is limited by the spurious output level that is acceptable from the mixer, and by the available drive from the IF chip.

3.2.6. Transmit/receive filters, PIN switches and dual use amplifier

Following the upconversion mixer, the transmit signal is filtered to remove the unwanted image and local oscillator products. This filtering consists of a pair of 3-pole ceramic stripline filters with, between them, a single stage bipolar amplifier stage with a gain of 7dB. In order to reduce the board area required and the component cost, the filter/amplifier is also used on receive by placing a series/shunt PIN diode switch at each port of the circuit block. The filter and two switches have an insertion loss of approximately 5dB, giving a total gain of approximately 2dB. This ensures that in the transmit case a signal level of approximately 0dBm is available to drive the transmit driver stage.

3.2.7. Transmit PA

This circuit comprises a Driver stage and the final power amplifier stage.

3.2.7.1. Transmit driver Stage

The transmit driver stage is nearly identical to the receive LNA, except for small differences in the matching striplines that are layout related, and the fact that the KGF1175 device is run at a higher current of 8mA. This gives a gain of >14dB, together with a 1dB output compression level of >+10dBm.

3.2.7.2. Transmit Power Amplifier Stage

The transmit PA uses a Siemens CLY2 device to provide a maximum output power of approximately +23dBm and a gain of 10-11dB. The device source and load impedances are set to those recommended in the device data sheet by means of stripline and lumped element matching networks. Since the CLY2 is not used in a self-biasing configuration, an external charge-pump voltage inverter is used to provide a negative voltage rail for gate bias. Bias is set to the correct voltage by a resistive potential divider. The current in the PA device is set to between 50 and 100mA; the final value will be determined after further development work is completed.

3.2.8. Low pass filter

The PA is followed by a 5 element low pass filter, designed to remove harmonics from the transmitter output. This consists of stripline and lumped elements and has a loss of 0.6dB approximately and a rejection of 30dB or more at both 2nd and 3rd harmonic. The filter re-enters at approximately the 4th harmonic. At this frequency the energy produced is already below the specification limit.

4. FREQUENCY SYNTHESIS

4.1. General

There are two frequency synthesisers, a fixed 2LO and a programmable 1LO. The 1LO is programmed to tune the frequency, which sets the RF channel that the radio operates on.

4.2. 2LO synthesiser

The 2LO synthesiser is contained within the HPMX5002, with the exception of the VCO tank circuit, varactor diodes and loop filter components. The only control over the synthesiser frequency is the choice of reference frequency input and a choice of one of three reference division ratios and two main divider ratios. A 16.0MHz reference is used with a reference division ratio of 16 and a main divider ratio of 216, giving a fixed frequency of 216.0MHz.

The HPMX5002 has with two control pins for the 2LO synthesiser. One of these controls the VCO alone. The other allows for the phase detector and dividers to be powered down and the VCO control voltage allowed to freewheel. This means that a high loop bandwidth can be chosen to allow a fast settling time at power up. Modulation can still be applied because when the loop is in freewheel mode the 2LO bandwidth is reduced to zero. The loop filter is arranged in the Gardner configuration since the phase detector output is a charge pump.

The current radio design modulates the 2LO by means of a second varactor diode and a modulation buffer. This can be discarded if the 24.0MHz signal to the 1st transmit upconversion mixer is digitally modulated within the baseband circuitry.

4.3. 1LO synthesiser

The 1LO synthesiser is based on an external synthesiser controller chip, the Siemens PMB2306T. The VCO is implemented inside the HPMX5001 with the exception of the tank circuit, which is external. The 1LO runs at half the final frequency, with an on-chip frequency doubler stage to produce the final output frequency that is fed to the receive and transmit mixers. The on-chip prescaler in the HPMX5001 is controlled by the PMB2306T. This synthesiser also uses a Gardner configuration loop filter.

The 1LO synthesiser currently requires to be powered up one slot in advance of the active slots. The lock-up time is <200us.

4.3.1. 1LO synthesiser programming

Using a reference frequency of 500kHz, or reference oscillator frequency/32, with the first channel at 2.401GHz centre frequency and the last at 2.482GHz, 82 channels are available at 1.0MHz spacing, for the US/Europe version. For Japanese operation the frequency tuning range is reprogrammed to go up to 2.498MHz.

For the lowest channel at 2.401GHz, the values for the synthesiser programming are:-

Ref. counter	Main counter	Swallow counter
32	67	17

For the highest channel at 2.482GHz, the values for the synthesiser programming are:-

Ref. counter	Main counter	Swallow counter
32	70	2

The swallow counter increments by 1 to increase frequency by 1 channel spacing. Once this counter reaches 31, the next increment occurs in the main counter with the swallow counter changing from 31 back to 0.

5. POWER SUPPLIES AND SWITCHING

The nominal power supply rail for the radio module is 5.0V. This is provided from the host machine in which the module is used.

An on board regulator is used to provide a clean, noise free supply rail for the more sensitive circuitry in the radio. This is switched separately, so that the radio can be shut down by removing its power supply either under software control, or in the case of ISA cards, by switching off the power to the card socket. The voltage chosen for the regulated supply, 4.0V, allows for the regulator to operate with an input voltage of 4.75V, the minimum allowed on a PC 5V supply.

The regulated power supply is fed to the frequency synthesisers, the IF circuitry and to the negative voltage inverter for the PA stage gate bias supply. All these components are rated to operate at a minimum voltage of 2.7V, so considerable headroom is available above this point with the 4.0V supply. Both the HPMX5001 and 5002 are rated to operate with power control pins at higher than supply rail voltage by at least 3V, allowing these pins to be driven when various radio supplies are shut down.

Areas of circuitry which are required to be active during both receive and transmit, such as the dual use amplifier between the RF filters, and the 1LO frequency synthesiser and buffer, are powered by a separate switching transistor to allow maximum power saving. The circuit blocks used for either receive or transmit are also separately switched, allowing for power consumption to be minimised and to give better receiver dynamic range by powering down the LNA under very strong wanted signal conditions.

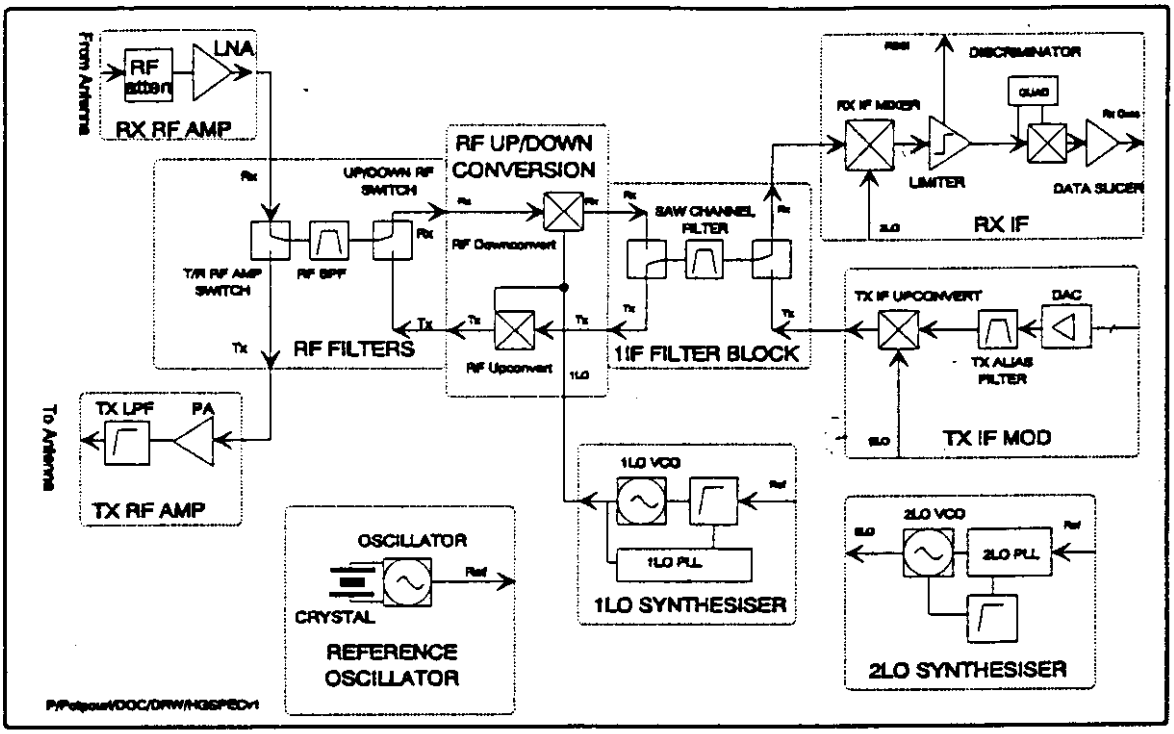


Figure 1: Block Diagram Of Radio

1 INTRODUCTION

This document provides the software programmers reference for the 802.11 Baseband Controller developed by Symbionics Networks Ltd. It details the register and memory interfaces between the host and local processors and the hardware design.

An 802.11 Wireless LAN card will typically comprise a radio, this baseband controller, a processor and a RAM. The lower layers (eg. PHY and low-level MAC functions) are performed by the baseband controller and higher layers performed by a processor.

1.1 Feature Summary

- Compatible with IEEE802.11 wireless LAN standard
- Designed for low cost Stations and Access Points
- Direct PCMCIA version 2 compliant interface supporting 16 bit data transfers
- Radio modem supporting 1Mbps FSK and 2Mbps 4FSK FH data transfers
- Radio interface to FH radio providing antena select, power control, synthesiser programming
- Processor interfaces to support 80c86 and 80c186
- Multiport memory controller on-chip for local shared memory
- Support of low cost RAMs with many size options for shared buffer memory and processor code
- EEPROM interface to download host interface configuration data and provide non-volatile card parameter storage
- Low power modes
- 144pin TQFP package for assembly in PCMCIA Type 2 cards
- 5v and 3.3v operation

1.2 Conventions

1.2.1 General

The last character in a name indicates its asserted sense. When ending with an 'N', a low is the asserted state; otherwise a high is the asserted state.

1.2.2 Addressing

Where a register occupies several address locations the low byte is in the low address and higher bytes/words are in higher addresses.

Unless specifically stated the registers are word accessible only for writes. Hence the write typically updates the odd and even bytes for the register. Memory (S/P_RAM) is designed for byte or word accesses.

The baseband controller MAC memory structures are word orientated and all diagrams show memory as left to right being msbit to lsbit and top to bottom being low address to high address. Note the baseband controller performs no big/little-endian conversions for processor types. The software must ensure the memory structure (and registers) are filled appropriately.

Address locations referenced by the local processor (eg. processor memory maps) are given as byte addresses (eg. addresses 0x00, 0x01 are successive bytes). The memory accessed by the baseband controller are 16 bit words so addresses (eg. address pointer RXINPTR) are referenced as word addresses (eg. address 0x00, 0x01 are successive words).

1.2.3 Order of Transmission

It is assumed that the bit order of transmission follows that of 802.11. The rules are:

- data is transmitted from registers and memory from lsb (left hand bit 0) to msb
- data is transmitted from low addresses to high addresses
- CRC is transmitted from msb (x^{31}) to lsb (x^{0}).
- Length, timestamp fields are transmitted low octet first, lsb first.

1.3 References

1. SN003 IEEE 802.11 Baseband Controller ES Datasheet.
2. P802.11 IEEE 802.11 MAC and PHY specification.
3. PCMCIA standard version 2.

1.4 Disclaimer

Symbionics Networks Ltd. does not guarantee that the information in this document is correct. However the information presented in this document is understood to be correct and accurate at the time of writing. Any information found to be incorrect will be communicated in revisions of this document.

2 PROCESSOR INTERFACE

The baseband controller registers occupy a 0x70 byte address space in the processor address map.

The registers are split to the following modules which are described in this programmers reference.

Addr	Module	Description
0x00	GLOBAL	Global chip register bits
0x08	HOST	Host interface registers
0x0c	EEPROM	Data, Address/control for EEPROM
0x10 - 0x2f	PHY	PHY layer
0x30 - 0x6f	MAC	MAC engine register

The baseband controller registers are designed for word accesses. If byte writes take place the undefined byte (even or odd) will result in undefined register contents for that byte.

2.1 Global Controls

Name: VER
Address: 0x0
R/W: R
Reset 0x00c1

bit 15							bit 8 0x01
0	0	0	0	0	0	0	0
bit 7							bit 0 0x01
1	1	0	0	0	0	0	1

This register contains the version number of the device. The first version is 0x00c1.

Name: GLOB_CTL
Address: 0x02
R/W: R
Reset 0x0000

bit 15							bit 8 0x03
CONF[7]	CONF[6]	CONF[5]	CONF[4]	CONF[3]	CONF[2]	CONF[1]	CONF[0]
bit 7							bit 0 0x02
0	REG	A16_EXT	PCSN_H	PCSN_E	PCK[1]	PCK[0]	MP_ENA

The baseband controller configuration modes are set by the status of the processor data lines following reset. The CONF[] register bits are read only. The following configurations are provided:

CONF[7] Reserved

CONF[6] E_CONF
This configuration bit selects the type of EEPROM used. See Section 4 EE_A_CTL[ETYPE64].

CONF[5] SCK_CONF
When asserted the SCK frequency is internally divided by two for the internal operating frequency. For example SCK is 32MHz and internal operation is 16MHz. SCK_CONF must be asserted.

CONF[4:3] H_CONF
These configuration bits select which host interface is being used. The following are currently supported:

H_CONF	Host Interface
00	PCMCIA
01 - 11	reserved

CONF[2:0] P_CONF
These configuration bits select which processor is being used. The following are currently supported:

P_CONF	Processor Type
000	reserved
001	80c86, v30 (max mode)
010	80c186
011 - 111	reserved

REG, A16_EXT, PCSN_H, PCSN_E
See section 2.2 Memory Decode

PCK[1:0] Sets the clock frequency to the processor. The following are currently supported:

PCK[1:0]	Clock rate
00	SCK / 8
01	SCK / 4
10	SCK / 2
11	SCK

The PCK value is selected according to processor type and SCK_CONF. In normal active operation the processor will run at full clock rate (of SCK or SCK / 2). The lower clock rates are where the WLAN card is not actively transmitting or receiving and the processor can operate more slowely to save power. PCLK = 11 can only be used with processors requiring a x2 clock, eg 80c186.

An example of the use of the above register bits is:

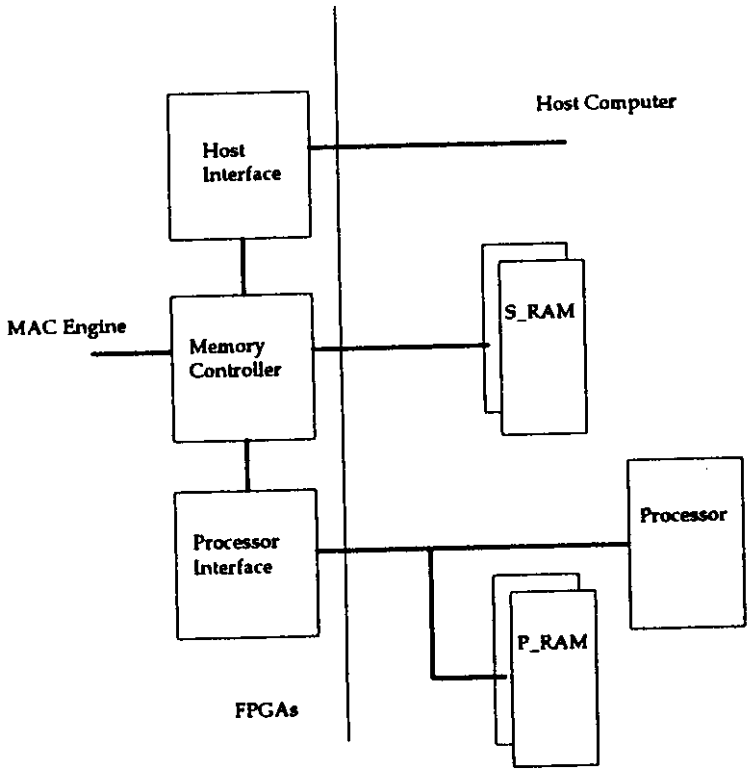
Using the 2Mbps modem, the baseband controller SCK is 32MHz so SCK_CONF is asserted to run the logic at 16MHz.

An 80c186 is used so P_CONF is "010" and PCK is "11". If a v30 processor were used P_CONF is "001" and PCK is "10".

MP_ENA When asserted the MAC and PHY modules are enabled. When not asserted the clock is stopped to the modules resulting in minimum power consumption.

2.2 Memory decode

The expected card design using the .XI baseband controller has a shared RAM (S_RAM) and, in access points local program RAM (P_RAM). RAM sizes from 32k to 128k words are allowed. S_RAM provides common data buffers between the host, the 802.11 MAC engine and the processor. The .XI baseband controller maps to the processor address space with the PCSN pin.



The host computer can only access S_RAM via the host interface and memory controller. To download program code to P_RAM the host downloads a boot loader to S_RAM which the processor runs. The processor then copies the program code from S_RAM to P_RAM and then modifies the GLOB_CTL[PCSN_H, PCSN_E] bits.

Register bits in the GLOB_CTL register control the memory map options

PCSN_E When asserted the pin PCSN is enabled. From reset the register bit is unasserted which means all processor accesses will address the .XI baseband controller. This allows boot code in S_RAM to be accessed enabling download of code/data to P_RAM before it is used. Once enabled PCSN is active high or low depending on the PCSN_H register bit.

Once PCSN_E is asserted the baseband controller uses 256k bytes of the processor memory map. If S_RAM is smaller than this size it will be aliased within this memory map.

PCSN_H When PCSN_E is asserted the .XI baseband controller responds to PCSN. PCSN can be selected to be active low (PCSN_H unasserted) or active high (PCSN_H asserted).

A16_EXT Flag is used to map all host and MAC engine accesses to area 0x20000 of the

A16_EXT Flag is used to map all host and MAC engine accesses to area 0x20000 of the S_RAM. The max address range of these modules is 64k words so this enables 128k word RAMs to be used with the low bank reserved for the processor.

REG This register bit defines whether the registers are mapped to memory (part of the SRAM) or to input/output address space.

REG	Register location
0	0x3ff80 - 0x3ffef with PCSN asserted
1	0x0000 - 0x007f i/o space

2.2.1 Memory usage from reset

From reset PCSN_E and PCSN_HI are unasserted.

The processors requires three areas of memory to be defined (ie. downloaded from the host computer) before it can be released from reset.

- The memory locations 0xffff0 - 0xfffff provide the start of program from reset
- The memory area 0x0000 to 0x03ff provide the interrupt vectors
- Some program code used from reset.

Once the above areas are initialised via the host interface the processor reset H_CTL[PRSTN] may be unasserted.

If there is external memory (RAM or ROM) PCSN_HI needs to be set depending on the address decode design of the card and PCSN_E asserted. The baseband controller will typically always be at the low 256k byte area of the processor address space.

The external memory can then be accessed. If external memory is attempted to be used before PCSN_E is asserted there will be conflict between the external memory and the .XI baseband controller.

2.3 Interrupts

Local processor interrupts are created by the MAC engine and the host interface. Registers within the respective modules provide interrupt enables, status and acknowledge. The local processor is expected to use level-based interrupts.

An interrupt vector of 32 is provided when the processors perform interrupt acknowledge cycles.

Non maskable interrupts are not used.

3 HOST INTERFACE

3.1 PCMCIA Interface

The full 16bit PCMCIA data bus is used.

Atribute memory and i/o memory are supported and common memory is not used. The interface registers are placed in i/o memory.

The PCMCIA memory usage is:

Attribute Memory	0x00 - 0xff	CIS table and configuration registers..
I/O Memory	0x00 - 0x07	Host Interface registers. Note mapping is decoded on low 3 address lines only.

3.1.1 Host Attribute memory

The attribute memory interfaces to RAM containing the CIS table and configuration registers. The RAM is loaded with the CIS table from EEPROM to boot up. Attribute memory is byte wide so the odd byte locations are not used. The following table describes the attribute memory map and registers.

0x00 - 0x0f	Start of CIS in memory. Will comprise CISTPL_DEVICE The TPL_LINK will contain 0x01f to jump to attribute memory location 0x20.
0x10 - 0x1f	Configuration Registers. (PCMCIA v2 requires 6 locations) 0x10 Configuration Option (used) 0x12 Card Configuration and Status Register (used) 0x14 Pin Replacement (not used) 0x16 Socket and Copy (not used)
0x20 - 0xff (max)	The rest of the CIS. Maximum CIS length is 256 bytes.

Two attribute memory registers are provided:

Name: CONFIGURATION OPTION
Address: 0x10
R/W (Host): R/W
Reset: 0x0000

bit 7 ... bit 0

SRESET	LIREQ	CI5	CI4	CI3	CI2	CI1	CI0

SRESET This bit is asserted to provide a reset to the card. When cleared the card is in the unconfigured state (will not respond to read/writes other than to attribute memory). Hard reset clears this bit

LIREQ Set to 1 for level mode interrupts, set to 0 for edge triggered interrupts. Not used, we always use level interrupts.

CI[5:0] Configuration Index which matches the configuration table CFTABLE_ENTRY tuple being used. This value is zero from reset. When any non-zero value is written by the host the card is deemed configured and usable (in i/o mode).

Name: CARD CONFIGURATION AND STATUS
Address: 0x12
R/W (Host): R/W
Reset: 0x0000

bit 7 ... bit 0

CHNGD	SIGCHG	IOIS8	0	AUDIO	PWRDN	INTR	0

CHNGD Signal to indicate to the host that pin replacement bit has changed. Set at 0 as pin replacement is not used.

SIGCHG Set by host to allow CHNGD bit to operate. Not used.

IOIS8 Set by host to indicate 8 bit accesses are being used. As the card is 16 bit only this bit is not used.

AUDIO Enable audio information. Not used.

PWRDN This bit is set by host to request a powerdown. When set interrupt is issued to card processor to shut down wireless link. Not used.

INTR State of the interrupt request. Used in this system to allow shared interrupts.

3.4 Host Registers

Once the card is configured the host interacts with the card processor via i/o memory space .

The following registers are provided.

Name: H_CTL
Address: 0x00
R/W (Host): R/W
Reset 0x0000

bit 15							bit 8
0	0	0	PRSTN	HA[16]	WRAP_HA	HINT_ENA	HREGINT
bit 7							**bit 0**
HINT[3]	HINT[2]	HINT[1]	HINT[0]	PINT[3]	PINT[2]	PINT[1]	PINT[0]

PRSTN When asserted (eg. from reset) the processor reset line is asserted. This allows the host to download processor code to shared RAM before processor reset is removed.

HA[16] The host address pointer H_ADDR can be offset to the upper 64k word of S_RAM (assuming a 128k word RAM size) when this register bit is asserted. Note HA[16] is not autoincremented with H_ADDR.

WRAP_HA When this bit is asserted the H_ADDR register is constrained by the receive circular buffer size. This is used when the packet data is transferred from card to host and may wrap from the end of the receive buffer to the beginning.

HREGINT Read only. When access to the baseband controller registers by the host is allowed the baseband controller interrupt is enabled to the host. This flag indicates the status of this interrupt. The enable and control registers are provided in the MAC registers address space (see section 6, MINTENA, MINTACK, MINTSTAT).

The following register bits provides status and control of interrupts to and from the local processor and host computer. There are four separate interrupts in each direction. The interrupts are provided to allow communications between the host and the local processor where the message contents are provided in Shared RAM and status with these register bits.

HINT_ENA The HINT[3:0] interrupts are enabled to the host interrupt line when this register bit is asserted. When deasserted the HINT interrupts are disabled.

HINT[3:0] These are interrupt requests from the local processor to the host computer (see local processor register P_INT). An local processor requests a host interrupt by asserting one of these HINT bits. The host computer clears the interrupt request by asserting the appropriate HINT bit.

PINT[3:0] These are interrupt requests from the host computer to the local processor (see local processor register P_INT). The host computer requests a processor interrupt by asserting one of these PINT bits. The local processor clears the interrupt request by asserting the appropriate PINT bit.

Note: Interrupts can be lost on the host computer if the host computer interrupt controller is edge sensitive. To avoid this, HINT_ENA should be deasserted and asserted around issuing an *end of interrupt* to the interrupt controller, thus generating an edge in the host computer interrupt request line.

Name: H_ADDR
Address: 0x02
R/W (Host): R/W
Reset 0x0000

bit 15							bit 8
HA[15]	HA[14]	HA[13]	HA[12]	HA[11]	HA[10]	HA[9]	HA[8]
bit 7							**bit 0**
HA[7]	HA[6]	HA[5]	HA[4]	HA[3]	HA[2]	HA[1]	HA[0]

Name: H_DATA
Address: 0x04
R/W (Host): R/W
Reset 0x0000

bit 15							bit 8
HD[15]	HD[14]	HD[13]	HD[12]	HD[11]	HD[10]	HD[9]	HD[8]
bit 7							**bit 0**
HD[7]	HD[6]	HD[5]	HD[4]	HD[3]	HD[2]	HD[1]	HD[0]

The host can read or write word data to card S_RAM through these registers. The address register H_ADDR is an autoincrementing pointer to S_RAM. The data register is read/writable. Once the address has been set up packets of data can be read from contiguous memory locations by reading the data register only. This can be from dma accesses or processor block moves.

H_ADDR can be offset to the upper 64k word of S_RAM (assuming a 128k word RAM size) when H_CTL[HA[16]] is asserted. Note HA[16] is not autoincremented with H_ADDR.

When H_CTL[WRAP_HA] is asserted the address pointer H_ADDR will be constrained by the size and base address of the receive circular buffer. This applies to the initial writing of the H_ADDR register by the host and the autoincrementing. This feature allows the host to read the data from the receive buffer without worrying about the fact that it is a circular buffer.

3.5 Processor Registers

Communications between the host and local processor are expected to be performed with message buffers in S_RAM and control flags and interrupts in the P_INT register.

Name: P_INT
Address: 0x08
R/W (Proc): R/W
Reset 0x0000

bit 15							bit 8
0	0	0	0	0	0	0	PINT_ENA
bit 7							**bit 0**
HINT[3]	HINT[2]	HINT[1]	HINT[0]	PINT[3]	PINT[2]	PINT[1]	PINT[0]

The following register bits provides status and control of interrupts to and from the local processor and host computer. There are four separate interrupts in each direction. The interrupts are provided to allow communications between the host and the local processor where the message contents are provided in Shared RAM and status with these register bits.

PINT_ENA The PINT[3:0] interrupts are enabled to the processor interrupt line when this register bit is asserted. When deasserted the PINT interrupts are disabled.

HINT[3:0] These are interrupt requests from the local processor to the host computer (see host register H_CTL). An local processor requests a host interrupt by asserting one of these HINT bits. The host computer clears the interrupt request by asserting the appropriate HINT bit.

PINT[3:0] These are interrupt requests from the host computer to the local processor (see host register H_CTL). The host computer requests a processor interrupt by asserting one of these PINT bits. The local processor clears the interrupt request by asserting the appropriate PINT bit.

4 EEPROM INTERFACE

This module provides the following functions

a/ Download of CIS table from EEPROM to RAM

b/ Read/Write of EEPROM by processor.

The module is designed for 93c46 or 35c102 EEPROM types with an 16 bit word depth. The data sheet for these devices should be read for programming opcodes and information.

The EEPROM type is detemined by post-reset configuration E_CONF. Either 64 word EEPROMs (eg. 93c46) using 6 address lines or 128/256 word EEPROM (eg. 93c56, 93c66) using 8 address lines are allowed.

4.1 CIS Download

Download is initiated following reset. An internal state machine downloads 64 or 128 words (depending on EEPROM type selected from reset) of CIS into 128 or 256 RAM even byte locations (odd locations are forced to zero). Note the PCMCIA attribute memory is only accessed as even bytes. Parameters in addition to CIS can be downloaded to RAM (eg. IEEE address, radio parameters).

The high address (0x3f or 0x7f) of the EEPROM is read first and provides the high address a[15:8] for the CIS download.

The EEPROM must be initialised with the CIS table (and high address offset).

4.2 Processor Interface

Read/Write of EEPROM is performed with a 16 bit address/status and a 16 bit data register.

For a write the data is written and cycle initiated by the address/status written. For a read the address/status is written and then polled until cycle is complete then data can be read.

Name: EE_DATA
Address: 0x0c
R/W: R/W
Reset 0x0000

bit 15							bit 8 0x11
ED[15]	ED[14]	ED[13]	ED[12]	ED[11]	ED[10]	ED[9]	ED[8]
bit 7							bit 0 0x10
ED[7]	ED[6]	ED[5]	ED[4]	ED[3]	ED[2]	ED[1]	ED[0]

Low byte contain the data to/from the EEPROM.

A read cycle will have the data in the buffer at the end of the cycle to be read by the processor. A write cycle will have the data written to this buffer prior initiating the write cycle.

Name: EE_A_CTL
Address: 0x0e
R/W: R/W
Reset 0x0000

bit 15							bit 8 0x13
BUSY	ACTIVE	DOWN	ETYPE64N	RDBUSY	ENA	CTL[1]	CTL[0]
bit 7							bit 0 0x12
EA[7]	EA[6]	EA[5]	EA[4]	EA[3]	EA[2]	EA[1]	EA[0]

Any write access will potentially start a EEPROM cycle.

Low byte contains the address to the EEPROM.

BUSY Read only. When RDBUSY is asserted the DO line from the EEPROM is provided on this register bit to monitor the busy/ready status of the EEPROM. This flag need not be used if 10msec (35C102) is allowed after a write cycle.

ACTIVE Read only. This register bit is asserted when an EEPROM cycle initiated by a write to this register) is still active. The EEPROM cycle is 116usecs long so this flag is not necessary if this time is allowed between accesses.

DOWN Read only. When asserted the CIS download state machine is active. The processor must not access the EEPROM while the download is active.

ETYPE64N Read only (identical to GLOB_CTL[E_CONF]). This flag indicates whether a 64 word or 128/256 word EEPROM has been selected by hardware configuration. When asserted (low) a 64 words EEPROM (eg. 93c46) is selected and address lines EA[5:0] are used. When deasserted (high) a 128 or 256 word EEPROM (eg. 93c56 or 93c66) is selected and address lines EA[7:0] are used. Note when a 128/256 word EEPROM is selected only 128 words are downloaded to RAM from reset.

RDBUSY When this register bit is asserted the EEPROM is selected and DO routed to the BUSY flag. EEPROM cycles are not allowed while this flag is busy.

ENA This register bit must be asserted (only when DOWN is not asserted) to allow the processor to access the EEPROM. It provides clock gating for minimal power consumption.

CTL[1:0] These two bits provides the EEPROM opcode as defined in the table below. The READ, ERASE (should not be necessary) and INSTRUCTION opcodes all use the address (the instruction opcode uses the high 2 address bits as the sub-opcode). The WRITE opcode uses the address and data registers. Once ENA has been asserted and RDBUSY is not asserted any write to this register will initiate a EEPROM cycle.

CTL[1]	CTL[0]	Cycle Type
0	0	Instruction
0	1	Write
1	0	Read
1	1	Erase

14.6.2 Regulatory Requirements

Wireless LANs implemented in accordance with this standard are subject to equipment certification and operating requirements established by regional and national regulatory administrations. The PMD specification establishes minimum technical requirements for interoperability, based upon established regulations for Europe, Japan, and the North America at the time of the draft. These regulations are subject to revision, or may be superseded. Requirements that are subject to local geographic regulations are annotated within the PMD specification. Regulatory requirements that do not affect interoperability are not addressed within this standard. Implementers are referred to the following regulatory sources for further information. Operation in countries within Europe, or other regions outside Japan or North America, may be subject to additional or alternative national regulations.

The documents listed below specify the current regulatory requirements for various geographic areas at the time the standard was developed. They are provided for information only, and are subject to change or revision at any time.

Europe:

Approval Standards: European Telecommunications Standards Institute
Documents: ETS 300-328, ETS 300-339
Approval Authority: National Type Approval Authorities

France:

Approval Standards: La Reglementation en France por les Equipements fonctionnant dans la bande de frequences 2,4 GHz LAN-Radio Local Area Network"
Documents: SP/DGPT/ATAS/23, ETS 300-328, ETS 300-339
Approval Authority: Direction Generale des Postes et Telecommunications

Japan:

Approval Standards: Association of Radio Industries and Businesses(ARIB)
Documents: RCR STD-33A
Approval Authority: Ministry of Telecommunications (MKK)

North America:

Approval Standards: Industry Canada (IC), Canada
Documents: GL36

Federal Communications Commission (FCC), USA
Documents: CFR47, Part 15, Sections 15.205, 15.209, 15.247.

Approval Authority: Industry Canada (Canada), FCC (USA)

Spain:

Approval Standards: Supplemento Del Numero 164 Del Boletin Oficial Del Estado (Published 10 July 91, Revised 25 June 93)
Documents: ETS 300-328, ETS 300-339
Approval Authority: Cuadro Nacional De Atribucion De Frecuesias

14.6.3 Operating Frequency Range

A conformant PMD implementation shall be able to select the carrier frequency (Fc) from the full geographic-specific set of available carrier frequencies. Table 36 summarizes these frequencies for a number of geographic locations:

Lower Limit	Upper Limit	Regulatory Range	Geography
2.402 GHz	2.480 GHz	2.400-2.4835 GHz	North America*
2.402 GHz	2.480 GHz	2.400-2.4835 GHz	Europe*
2.473 GHz	2.495 GHz	2.471-2.497 GHz	Japan*
2.447 GHz	2.473 GHz	2.445-2.475 GHz	Spain*
2.448 GHz	2.482 GHz	2.4465-2.4835 GHz	France*

Table 36, Operating Frequency Range

* The frequency ranges in this table are subject to the geographic specific regulatory authorities

14.6.4 Number of Operating Channels

The number of transmit and receive frequency channels used for operating the PMD entity is 79 for the US and Europe and 23 channels for Japan. This is more fully defined in Table 38 and Table 39 of 14.6.5.

Minimum*	Hopping Set	Geography
75	79	North America*
20	79	Europe*
Not Applicable	23	Japan*
20	27	Spain*
20	35	France*

Table 37, Number of Operating Channels

* The number of required hopping channels are subject to the geographic specific Regulatory Authorities

14.6.5 Operating Channel Center Frequency

The channel center frequency is defined in sequential 1.0 MHz steps beginning with the first channel, channel 2.402 GHz for the U.S.A. and Europe, as listed in Table 38. The channel centers for Japan, starting at 2.473 GHz with 1 MHz increments, is listed in Table 39.

Channel #	Value	Channel #	Value	Channel #	Value
2	2.402	28	2.428	54	2.454
3	2.403	29	2.429	55	2.455
4	2.404	30	2.430	56	2.456
5	2.405	31	2.431	57	2.457
6	2.406	32	2.432	58	2.458
7	2.407	33	2.433	59	2.459
8	2.408	34	2.434	60	2.460
9	2.409	35	2.435	61	2.461
10	2.410	36	2.436	62	2.462
11	2.411	37	2.437	63	2.463
12	2.412	38	2.438	64	2.464
13	2.413	39	2.439	65	2.465
14	2.414	40	2.440	66	2.466
15	2.415	41	2.441	67	2.467
16	2.416	42	2.442	68	2.468
17	2.417	43	2.443	69	2.469
18	2.418	44	2.444	70	2.470
19	2.419	45	2.445	71	2.471
20	2.420	46	2.446	72	2.472
21	2.421	47	2.447	73	2.473
22	2.422	48	2.448	74	2.474
23	2.423	49	2.449	75	2.475
24	2.424	50	2.450	76	2.476
25	2.425	51	2.451	77	2.477
26	2.426	52	2.452	78	2.478
27	2.427	53	2.453	79	2.479
				80	2.480

Table 38, North American and European Requirements

(Values specified in GHz)

Channel #	Value	Channel #	Value	Channel #	Value
73	2.473	81	2.481	89	2.489
74	2.474	82	2.482	90	2.490
75	2.475	83	2.483	91	2.491
76	2.476	84	2.484	92	2.492
77	2.477	85	2.485	93	2.493
78	2.478	86	2.486	94	2.494
79	2.479	87	2.487	95	2.495
80	2.480	88	2.488	-	-

Table 39, Japan Requirements

(Values specified in GHz)

Channel #	Value	Channel #	Value	Channel #	Value
47	2.447	56	2.456	65	2.465
48	2.448	57	2.457	66	2.466
49	2.449	58	2.458	67	2.467
50	2.450	59	2.459	68	2.468
51	2.451	60	2.460	69	2.469
52	2.452	61	2.461	70	2.470
53	2.453	62	2.462	71	2.471
54	2.454	63	2.463	72	2.472
55	2.455	64	2.464	73	2.473

Table 40, Spain Requirements

(Values specified in GHz)

Channel #	Value	Channel #	Value	Channel #	Value
48	2.448	60	2.460	72	2.472
49	2.449	61	2.461	73	2.473
50	2.450	62	2.462	74	2.474
51	2.451	63	2.463	75	2.475
52	2.452	64	2.464	76	2.476
53	2.453	65	2.465	77	2.477
54	2.454	66	2.466	78	2.478
55	2.455	67	2.467	79	2.479
56	2.456	68	2.468	80	2.480
57	2.457	69	2.469	81	2.481
58	2.458	70	2.470	82	2.482
59	2.459	71	2.471	-	-

Table 41, France Requirements

(Values specified in GHz)

14.6.6 Occupied Channel Bandwidth

Occupied channel bandwidth shall meet all applicable local geographic regulations for 1 MHz channel spacing. The rate at which the PMD entity will hop at is governed by the MAC. The hop rate is an attribute with a maximum dwell time subject to local geographic regulations.

14.6.7 Minimum Hop Rate

The minimum hop rate shall be governed by the regulatory authorities.

14.6.8 Hop Sequences

The hopping sequence of an individual PMD entity is used to create a pseudo-random hopping pattern utilizing uniformly the designated frequency band. Sets of hopping sequences are used to co-locate multiple PMD entities in similar networks in the same geographic area and to enhance the overall efficiency and throughput capacity of each individual network.

A frequency hopping pattern, Fx , consists of a permutation of all frequency channels defined in Table 38, and Table 39. For a given pattern number, x, the hopping sequence can be written as:

$F_X = \{f_X(1), f_X(2), \ldots f_X(p)\}$

where,

$f_X(i)$ = channel number (as defined in14.6.4) for i^{th} frequency in x^{th} hopping pattern
p = number of frequency channels in hopping pattern (79 for North America/most of Europe, 23 for Japan, 27 for France, 35 for Spain)

Given the hopping pattern number, x, and the index for the next frequency, i (in the range 1 to p), the channel number shall be defined to be:

$f_X(I) = [b(i) + x] \bmod (79) + 2$ in North America and most of Europe, with b(i) defined in Table 42

$= [(i - 1) * x] \bmod (23) + 73$ in Japan.

$= [b(i) + x] \bmod (27) + 47$ in Spain with b(i) defined in Table 43.

$= [b(i) + x] \bmod (35) + 48$ in France with b(i) defined in Table 44.

i	b(i)	i	b(i)	i	b(i)	i	b(i)	i	b(i)	i	b(i)	i	b(i)	i	b(i)
1	0	11	76	21	18	31	34	41	14	51	20	61	48	71	55
2	23	12	29	22	11	32	66	42	57	52	73	62	15	72	35
3	62	13	59	23	36	33	7	43	41	53	64	63	5	73	53
4	8	14	22	24	72	34	68	44	74	54	39	64	17	74	24
5	43	15	52	25	54	35	75	45	32	55	13	65	6	75	44
6	16	16	63	26	69	36	4	46	70	56	33	66	67	76	51
7	71	17	26	27	21	37	60	47	9	57	65	67	49	77	38
8	47	18	77	28	3	38	27	48	58	58	50	68	40	78	30
9	19	19	31	29	37	39	12	49	78	59	56	69	1	79	46
10	61	20	2	30	10	40	25	50	45	60	42	70	28		

Table 42, Base Hopping Sequence b(i) for North America and Most of Europe

i	b(i)	i	b(i)	i	b(i)
1	13	10	19	19	14
2	4	11	8	20	1
3	24	12	23	21	20
4	18	13	15	22	7
5	5	14	22	23	16
6	12	15	9	24	2
7	3	16	21	25	11
8	10	17	0	26	17
9	25	18	6	27	26

Table 43, Base Hopping Sequence b(i) for Spain

i	b(i)	i	b(i)	i	b(i)
1	17	13	31	25	15
2	5	14	20	26	3
3	18	15	29	27	11

4	32	16	22	28	30
5	23	17	12	29	24
6	7	18	6	30	9
7	16	19	28	31	27
8	4	20	14	32	19
9	13	21	25	33	2
10	33	22	0	34	21
11	26	23	8	35	34
12	10	24	1		

Table 44, Base Hopping Sequence b(i) for France

The sequences are designed to ensure some minimum distance in frequency between contiguous hops. The minimum hop size is 6 MHz for North America and Europe, including Spain and France, and 5 MHz for Japan.

The hopping pattern numbers x are divided into three sets. The sets are designed to avoid prolonged collision periods between different hopping sequences in a set. Hopping sequence sets contain 26 sequences for North America/Europe and 4 sequences per set for Japan:

For North America/most of Europe:
x = {0,3,6,9,12,15,18,21,24,27,30,33,36,39,42,45,48,51,54,57,60,63,66,69,72,75} Set 1
x = {1,4,7,10,13,16,19,22,25,28,31,34,37,40,43,46,49,52,55,58,61,64,67,70,73,76} Set 2
x = {2,5,8,11,14,17,20,23,26,29,32,35,38,41,44,47,50,53,56,59,62,65,68,72,74,77} Set 3

For Japan:
x = {6,9,12,15} Set 1
x = {7,10,13,16} Set 2
x = {8,11,14,17} Set 3

For Spain:
x = {0,3,6,9,12,15,18,21,24} Set 1
x = {1,4,7,10,13,16,19,22,25} Set 2
x = {2,5,8,11,14,17,20,23,26} Set 3

For France:
x = {0,3,6,9,12,15,18,21,24,27,30} Set 1
x = {1,4,7,10,13,16,19,22,25,28,31} Set 2
x = {2,5,8,11,14,17,20,23,26,29,32} Set 3

The three sets of hopping sequences for North America and most of Europe, of 26 patterns each, are listed Tables A, B, and C in Annex B. Similarly, the three sets for Japan, of four patterns each, are listed in Table D in Annex B. The three sets for Spain has nine patterns each. The three sets for France has 11 patterns each. The channel numbers listed under each pattern refer to the actual frequency values listed in Table 38 and Table 39.

B. Annex - Hopping Sequences (informative)

The following tables pertain to the hopping sequences for North America and ETSI.

Table B-1, Hopping Sequence Set 1

index	0	3	6	9	12	15	18	21	24	27	30	33	36
1	2	5	8	11	14	17	20	23	26	29	32	35	38
2	25	28	31	34	37	40	43	46	49	52	55	58	61
3	64	67	70	73	76	79	3	6	9	12	15	18	21
4	10	13	16	19	22	25	28	31	34	37	40	43	46
5	45	48	51	54	57	60	63	66	69	72	75	78	2
6	18	21	24	27	30	33	36	39	42	45	48	51	54
7	73	76	79	3	6	9	12	15	18	21	24	27	30
8	49	52	55	58	61	64	67	70	73	76	79	3	6
9	21	24	27	30	33	36	39	42	45	48	51	54	57
10	63	66	69	72	75	78	2	5	8	11	14	17	20
11	78	2	5	8	11	14	17	20	23	26	29	32	35
12	31	34	37	40	43	46	49	52	55	58	61	64	67
13	61	64	67	70	73	76	79	3	6	9	12	15	18
14	24	27	30	33	36	39	42	45	48	51	54	57	60
15	54	57	60	63	66	69	72	75	78	2	5	8	11
16	65	68	71	74	77	80	4	7	10	13	16	19	22
17	28	31	34	37	40	43	46	49	52	55	58	61	64
18	79	3	6	9	12	15	18	21	24	27	30	33	36
19	33	36	39	42	45	48	51	54	57	60	63	66	69
20	4	7	10	13	16	19	22	25	28	31	34	37	40
21	20	23	26	29	32	35	38	41	44	47	50	53	56
22	13	16	19	22	25	28	31	34	37	40	43	46	49
23	38	41	44	47	50	53	56	59	62	65	68	71	74
24	74	77	80	4	7	10	13	16	19	22	25	28	31
25	56	59	62	65	68	71	74	77	80	4	7	10	13
26	71	74	77	80	4	7	10	13	16	19	22	25	28
27	23	26	29	32	35	38	41	44	47	50	53	56	59
28	5	8	11	14	17	20	23	26	29	32	35	38	41
29	39	42	45	48	51	54	57	60	63	66	69	72	75
30	12	15	18	21	24	27	30	33	36	39	42	45	48
31	36	39	42	45	48	51	54	57	60	63	66	69	72
32	68	71	74	77	80	4	7	10	13	16	19	22	25
33	9	12	15	18	21	24	27	30	33	36	39	42	45
34	70	73	76	79	3	6	9	12	15	18	21	24	27
35	77	80	4	7	10	13	16	19	22	25	28	31	34
36	6	9	12	15	18	21	24	27	30	33	36	39	42
37	62	65	68	71	74	77	80	4	7	10	13	16	19
38	29	32	35	38	41	44	47	50	53	56	59	62	65
39	14	17	20	23	26	29	32	35	38	41	44	47	50

index	0	3	6	9	12	15	18	21	24	27	30	33	36
40	27	30	33	36	39	42	45	48	51	54	57	60	63
41	16	19	22	25	28	31	34	37	40	43	46	49	52
42	59	62	65	68	71	74	77	80	4	7	10	13	16
43	43	46	49	52	55	58	61	64	67	70	73	76	79
44	76	79	3	6	9	12	15	18	21	24	27	30	33
45	34	37	40	43	46	49	52	55	58	61	64	67	70
46	72	75	78	2	5	8	11	14	17	20	23	26	29
47	11	14	17	20	23	26	29	32	35	38	41	44	47
48	60	63	66	69	72	75	78	2	5	8	11	14	17
49	80	4	7	10	13	16	19	22	25	28	31	34	37
50	47	50	53	56	59	62	65	68	71	74	77	80	4
51	22	25	28	31	34	37	40	43	46	49	52	55	58
52	75	78	2	5	8	11	14	17	20	23	26	29	32
53	66	69	72	75	78	2	5	8	11	14	17	20	23
54	41	44	47	50	53	56	59	62	65	68	71	74	77
55	15	18	21	24	27	30	33	36	39	42	45	48	51
56	35	38	41	44	47	50	53	56	59	62	65	68	71
57	67	70	73	76	79	3	6	9	12	15	18	21	24
58	52	55	58	61	64	67	70	73	76	79	3	6	9
59	58	61	64	67	70	73	76	79	3	6	9	12	15
60	44	47	50	53	56	59	62	65	68	71	74	77	80
61	50	53	56	59	62	65	68	71	74	77	80	4	7
62	17	20	23	26	29	32	35	38	41	44	47	50	53
63	7	10	13	16	19	22	25	28	31	34	37	40	43
64	19	22	25	28	31	34	37	40	43	46	49	52	55
65	8	11	14	17	20	23	26	29	32	35	38	41	44
66	69	72	75	78	2	5	8	11	14	17	20	23	26
67	51	54	57	60	63	66	69	72	75	78	2	5	8
68	42	45	48	51	54	57	60	63	66	69	72	75	78
69	3	6	9	12	15	18	21	24	27	30	33	36	39
70	30	33	36	39	42	45	48	51	54	57	60	63	66
71	57	60	63	66	69	72	75	78	2	5	8	11	14
72	37	40	43	46	49	52	55	58	61	64	67	70	73
73	55	58	61	64	67	70	73	76	79	3	6	9	12
74	26	29	32	35	38	41	44	47	50	53	56	59	62
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76	53	56	59	62	65	68	71	74	77	80	4	7	10
77	40	43	46	49	52	55	58	61	64	67	70	73	76
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79	48	51	54	57	60	63	66	69	72	75	78	2	5

index	39	42	45	48	51	54	57	60	63	66	69	72	75
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