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TUNEUP PROCEDURE

At full power level of 2 watts, the resistive voltage divider formed by R154, R166, R182, R190 and R165 determines the reference voltage, VSET, that is applied to the logarithmic detector/controller, U23. U23 provides the power control voltage, VCONTROL, that is applied to the transmit power amplifier, U26. This is a closed loop power control system that does not require external adjustments.

The Processor can also select a power of less than 2 watts, via the RF ATTEN signal, in power reduction steps of about 1 dB down to -10 dB.

FREQUENCY STABILIZING CIRCUITRY

The frequency source is shown on page two of the RF Module schematic 10405. U2 is a frequency synthesizer chip, which in conjunction with the voltage controlled oscillator (VCO), U9, provides a frequency output of 912.5 to 919.0 MHz in steps of 500 kHz, resulting in 14 channels. The reference oscillator, G1, provides a stable 16 MHz signal to the synthesizer chip at U2 pin 8. The 16 Mhz reference signal is divided down by a factor of 32 to 500 kHz internally within U2. This sets the frequency spacing between channels to 500 kHz. The 16 Mhz reference oscillator, G1, has a frequency stability of + or – 200 ppm, which determines the basic frequency stability of the transmitter.

SPURIOUS SUPPRESSION, MODULATION LIMITING AND POWER LIMITING

Spurious products and harmonics in the transmitter are attenuated by the filter F1 on page 3 of RF Module schematic 10405 and the filter on page 5 formed by Z28 through Z33and C39, C40, C65, C73, C72, C67, C46, C30 and C8. A plot of the measured frequency response of the filter is shown in the attached Figure 1.

The data modulator is on page 3 of schematic 10405. This modulator, formed by U32, U33, U27 and the lowpass filter following U27, achieves 100% amplitude modulation with an ON/OFF ratio of more than 40 dB. The filter following U27 provides shaping of the incoming data in order to limit the bandwidth of the modulated signal to less than 5 Mhz, typically 3 MHz, at 58 dB down.

Full power limiting is accomplished using a logarithmic detector/controller IC, U23, on page 4. U23 produces an output voltage proportional to the difference of the logarithm of the incoming signal, RF POWER, on pins 2 and 3 and the DC power set level, VSET, applied to pin 7 of U23. The signal on pin 3, RF POWER, is a sample of the transmitted signal obtained from the directional coupler, U24, and suitably attenuated by R150, R151, and R153 and R196, R198 and R199. The output of the logarithmic detector/controller on pin 8 of U23 is buffered and filtered by U31 and U30 and applied to the power control terminal, pin 2 of U26, of the power amp (PA) on page 3 of the schematic. Nominally, 2.5 volts DC at pin 2 results in a full power of two watts to the antenna. The resistive voltage divider network formed by R154, R166, R182, R190 and R165 results in a precise adjustment of VSET, for 2 watts output at full power.

DESCRIPTION OF DIGITAL MODULATOR

The digital data modulator is shown on page 3 of the RF Module schematic 10405 and is formed by U32, U33, U27 and the lowpass filter at the output of U27. This is an amplitude modulator which achieves an ON/OFF ratio in excess of 40 dB. The response for the filter realized with L13 through L15, C225 through C227 and C198 is attached as Figure 2. This filter achieves a rejection of about 58 dB at the 1.5MHz point resulting in a modulated bandwidth of about 3 MHz at 58 dBc when excited with 30 KB/s data modulation.

The modulation is at 30 KB/s and consists of 22 synchronization bits followed by a 1 ms. pause and then approximately 216 more bits. The pattern is retransmitted approximately every 11 ms. with a pause of about 6 ms. between 5 ms. bursts. During all pauses, the carrier is on continuously without modulation. During the 6ms. pause, the PARC Reader receives reflected modulated carrier back from the target RF tag(s).