MODULATION SOURCE DESCRIPTION:

RULE PART NUMBER: 2.1047, 90.535

The G3+ modem generates digitized multi-level frequency shift keying modulating signal. This digital modulation scheme is produced by the main CPU in conjunction with the DSP processor as follows:

The main CPU processes incoming binary data to comply with data layer requirements, and then this binary stream is fed to the DSP processor which runs the functions of applying Forward Error Correction (FEC), interleaving and scrambling in binary and, from it, generates an NRZ for encoding and pulse shaping. The digital processing computes the binary differential and maps the binary stream into a symbol stream. The binary stream is processed as stream of clusters of multiple-bits as required by multiple level FSK modulation type. The number of levels of the digital symbol stream corresponds to the numbers of levels of NFSK modulation.

The digital symbol signal has further applied a pulse shaping filter through the DSP. The pulse-shaping filter is in Raised Cosine family and the appropriate equation designs the filter characteristic together with the 3dB cutoff frequency. The equation trim factor, which for RC family is the cosine weight "α", is set according to the bit rate selected and channel bandwidth as follows:

Bit rate	levels FSK	Symbol rate	Pulse shape and modulation type	Acronyms/ factor / 3dB cutoff frequency	Deviation	Occupied Bandwidth
128000 bps	16	32000 bauds	Raised Cosine 16 Levels Frequency Shift Keying	RC16FSK α=0.4 16000Hz	± 8.3 KHz	27666Hz

The pulse-shaped signal has further applied a amplification constant which adjusts the transmitter deviation level and then is fed to the CODEC for digital to analog conversion.

The resulting waveshape applied to the FM modulator will then produce a compact RF spectrum such that, when using proper frequency deviation, to fit inside the restrictive limits inherent to the intended channel bandwidth.

The same processes but backwards happen to demodulate the modulated symbols into data stream

TX Data Test Pattern:

The transmit "test data pattern" command produces a 2047 bit pseudo-random pattern. This pattern is generated by the internal software using the polynomial $X^{11}+X^{9}+1$ form and a 12-bit shift register. Initial value of the register is 111111111110 (FFE hex). The 2047 bit sequence is repeated thereafter as long is necessary to complete the test duration (55 sec). This pattern is applied to the DSP processor data input for encoding and pulse shaping as described above.