7. CIRCUIT EXPLANATION

HOW EACH SECTION WORKS

We will explain operations of each section based on block diagrams.

(1) MICROPHONE (Block diagram No. 1)
An internal microphone is of unidirectional dynamic type.
Impedance: 600 Ω
Sensitivity: -56 dB (1k Hz, 0 dB = 1 V/1 pa)

(2) MICROPHONE AMPLIFIER (2)
The microphone amplifier uses an OP amp (M1) and amplifies the signal from the microphone capsule to the level necessary for the compressor circuit. By changing the feedback amount, this microphone amplifier permits gain control of 15 dB.

(3) COMPRESSOR (3)
The compander IC is SA575DK (M2), and has a compressor circuitry and 2 OP amps. The compression ratio is 1/2 (logarithmic compression).

(4) PRE-EMPHASIS (4)
Pre-emphasis is carried out to improve the system's S/N ratio. Amplifier (M1) is used as an OP amp. A time constant if 50 µsec.

(5) LPF (5)
The third Butterworth type low-pass filter is constructed using the OP amp built in M2 to attenuate the audio signal components of over 15 kHz. Also, the harmonic components of the tone signal to be superimposed in the LPF circuit are attenuated by the-pass filter..

(6) MUTE SW (6)
Using the analog switch (M101), this circuit mutes both the audio and tone signals during the periods of from the power switch-on to the commencement of signal transmission and from power switch-off to transmission termination to operate the receiver tone squelch.

(7) TONE OSC(7, 8)
Consists of a quarts oscillator (X1) and an inverter (M3) and oscillates a signal for tone squelch (tone signal). The oscillation frequency is 32.768 kHz, and the output signal is taken out through a buffer (M4).

(8) PLL FREQUENCY SYNTHESIZER (9, 10, 11)
VCO (M7), PLL IC (M8) and LOOP FILTER make up a phase locked loop. The VCO oscillates the transmission frequency directly and divides the output. It then compares the frequency phase by means of the 25 kHz comparison frequency, and outputs a pulse corresponding to the phase difference. The pulse is applied to the VCO as a control voltage after integrated at a loop filter, and then is locked to the set transmission frequency. Both the audio and tone signals are input from the VCO's modulation terminal, and then are frequency-modulated. The modulation method is a reactance modulation system using a variable capacitance diode.

(9) RF AMP, RF POWER AMP (12,13, 14)
By amplifying the VCO's oscillation output with a transistor, these amplifiers not only make up for losses in a pad or RF LPF, but also gain the antenna power. The two-stage construction method is employed for the amplifiers to obtain sufficient buffer effects for the VCO, and a 6 dB pad is installed in the amplifier input. The output is less than 50 mW, and is adjusted by changing Q8's bias current using VR4 to change operation points.

(10) BIAS REGULATOR, BIAS SWITCH (15, 16)
By compensating for the temperature by means of a diode (D4), the bias circuit suppresses the changes of operation points due to temperature variations. When the VCO's transmission frequency becomes stable after PLL lockup completion, the switch (Q6) turns on and the bias is applied for radio signal transmission.

(11) RF LPF (17)

A 3-stage π type low-pass filter is used for the RF section's band limiting filter to suppress the spurious-radiated signals with frequencies much different from the transmission frequency.

(12) CPU and its peripheral parts (18, 19, 20, 21, 22)
This section is comprised of the CPU (M9), voltage detector (M10) and crystal-controlled reference oscillator (X2). The reference oscillator is 6.0 MHz in frequency, and is oscillated by the CPU's internal inverter to operate the CUP as a clock. At the same time, the 6 MHz signal is supplied to the PLL IC via the buffer (M12) as the PLL reference oscillation frequency. The oscillation frequency is adjusted by TCI so that its deviation stays within ±1 kHz. After its power switch is set to the ON position, the CPU controls the transmission frequency setting, the start of transmission, actions till voice transmission, and actions when the system is switched off. The operating procedures are stored in the CPU's mask ROM, and the control contents are as follows:

(A) The CPU reads transmission frequency setting data from both the Bank and Channel setting switches, and transmits data to PLL IC for the division ratio setting.

(B) The CPU controls the bias circuitry and Q6 so that the radio signal is not transmitted until the transmission frequency becomes stable.

(C) The CPU controls MUTE SW, VCO SW, BIAS SW, and BATT.CHECKER.

When the circuit voltage drops below 4.2 V, the voltage detector transmits a reset signal to the CPU to stop the CPU's operation so that no radio signal is transmitted.

(13) REG.CONT/SW OFF DETECT (23, 24, 29)
Setting the power switch to the ON position turns on Q3, and adds the control voltage to a regulator (M5) for its operation. As a result, the voltage of 5 VDC is supplied to each circuit all circuits begin to operate.

If the power switch is set to the OFF position, both Q1 and Q4 transmit the SW OFF DETECT signal to the CPU and the tone signal is muted (M101) to enable the receiver's tone squelch. Both Q5 and Q6 then turn off, and the radio signal transmission stops. During this process, M5 continues to operate according to time constants of both C30 and R31. One second after the signal transmission stops, when R31's terminal voltage becomes lower than M5's operating voltage, M5 and all other circuits stop their operations.

(14) BATT.CHECKER (25, 26, 27)
Informs the battery consumption by means of a lamp (D2). Although the lamp lights bright when the battery is new, it becomes darker as the battery voltage drops. When the voltage drops below 6 V, M102 transmits a signal to the CPU and causes the lamp to flash bright, indicating the battery needs to be replaced.

(15) Frequency registration (28)
Transmission frequencies and their banks and channels are written in the EEPROM (M11), and the contents can be changed as required.